A 1.25GHz 0.219pJ 4-bit Absolute-Value Detector for use in Neural Spike Sorting

Khoa Quach, Nate Atkinson, Josh Futterman

Design Summary

Circuit topology & style

CMOS Ripple carry adder and Inverter with PTL mux

- Adder input < 4 bits, so ripple will perform slightly better than select/bypass
- PTL allows for low transistor count in mux
- Ignore sum in adder design, just use carry chain since we only care about > 0

Schematic	Layout Size	Energy	Verification
$t_{p\_X(1)\rightarrow OUT}$ = 647 ps	X=42.045µm, Y=45.34µm	Sch E = 0.219pJ	Func: Y
$t_{p\_X(2)\rightarrow OUT}$ = 531 ps	A=1906µm^2	Layout E = 0.308pJ	DRC: Y
$t_{p\_X(3)\rightarrow OUT}$ = 608 ps	Aspect Ratio = 1.04	VDDs = 0.667V VDDl = 0.736V	LVS: Y

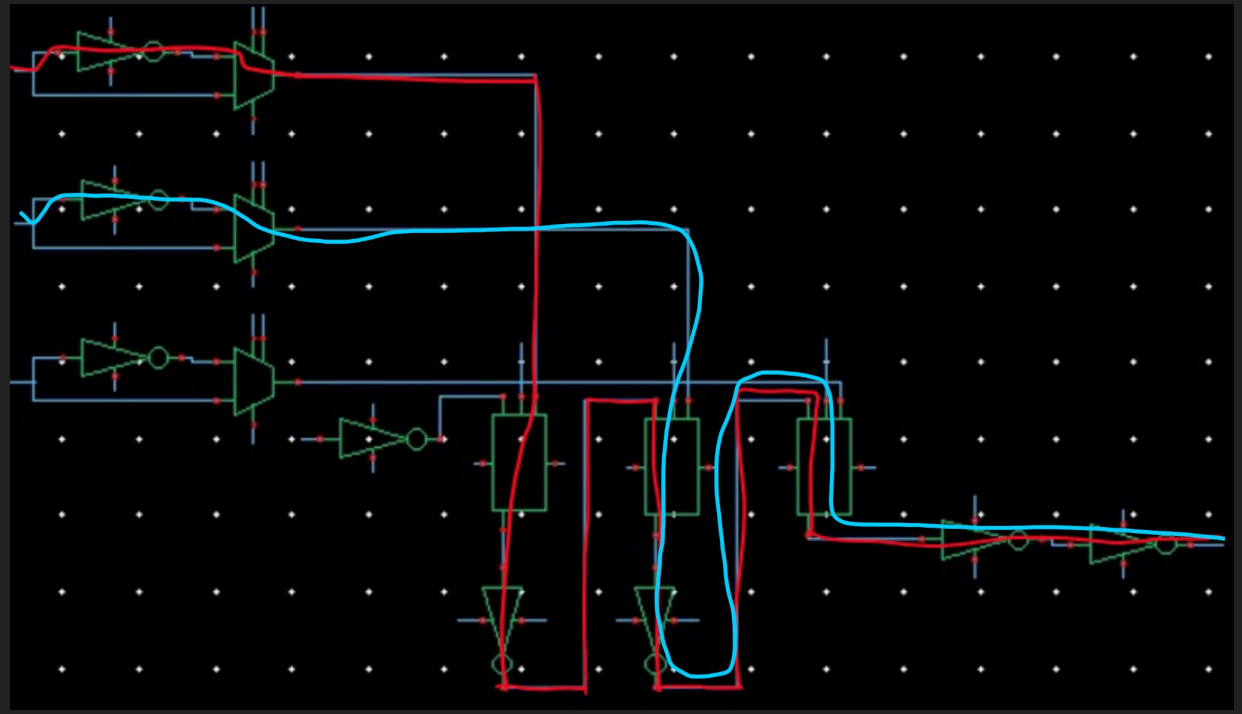
Critical Path Analysis

Worst-case

tcritical = 5tinv + tmux + 3tcarry

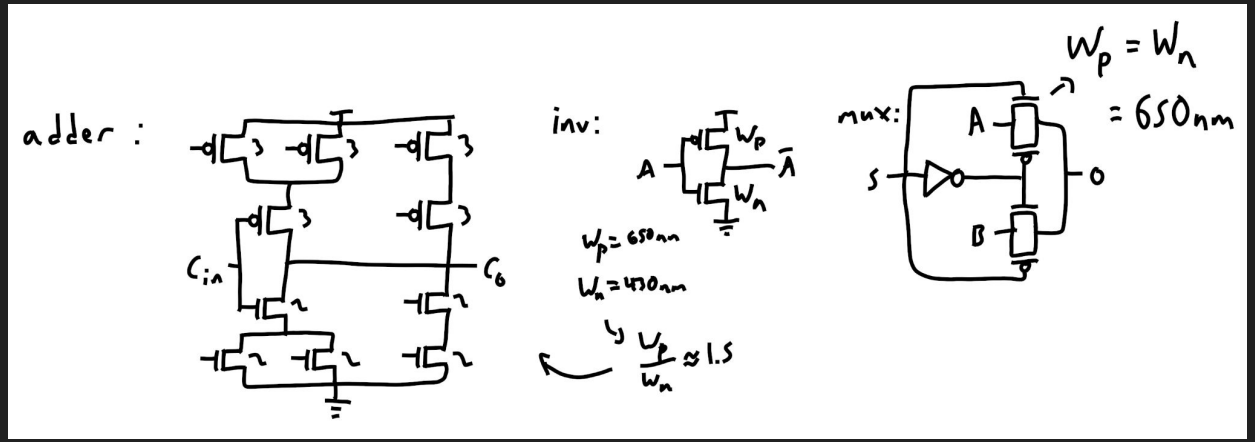
Second-worst-case

tcritical = 4tinv + tmux + 2tcarry



Gate Sizing

- G=25.6
- F=16
- Stage effort = 1.95



- Adders in carry chain sized equally as above (wrt unit inverter)
- Unit inverter of ratio 1.5:1 for all inverters in schematic
- Mux transmission gates equal-width for NMOS/PMOS

Design Optimization (VDD)

Pre Layout: VDD at 1v

8	tplh_X0_OUT	404.996p	✓	✓
9	tphl_X0_OUT	339.345p	✓	✓
10	tplh_X1_OUT	380.516p	✓	✓
11	tphl_X1_OUT	301.794p	✓	✓
12	tplh_X2_OUT	337.839p	✓	✓
13	tphl_X2_OUT	247.706p	✓	✓
14	tplh_X3_OUT	338.895p	✓	✓
15	tphl_X3_OUT	302.938p	✓	✓
16	Delay_X3_OUT	320.917p	✓	✓
17	Delay_X2_OUT	292.772p	✓	✓
18	Delay_X1_OUT	341.155p	✓	✓
19	Delay_X0_OUT	372.17p	✓	✓
20	Energy	505.864f	✓	✓

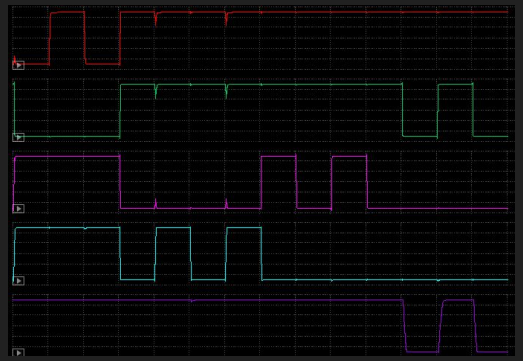
Pre Layout: VDD at 0.665v

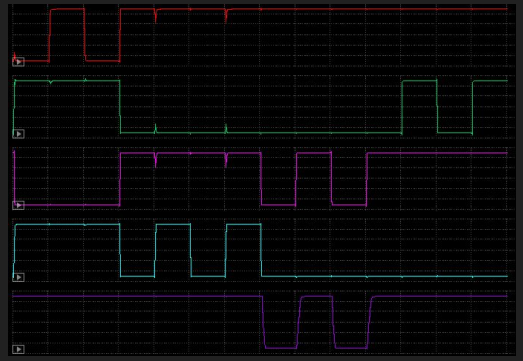
8	tplh_X0_OUT	652.853p	✓	✓
9	tphl_X0_OUT	653.048p	✓	✓
10	tplh_X1_OUT	604.063p	✓	✓
11	tphl_X1_OUT	694.199p	✓	✓
12	tplh_X2_OUT	518.385p	✓	✓
13	tphl_X2_OUT	586.956p	✓	✓
14	tplh_X3_OUT	503.315p	✓	✓
15	tphl_X3_OUT	699.756p	✓	✓
16	Delay_X3_OUT	601.536p	✓	✓
17	Delay_X2_OUT	552.67p	✓	✓
18	Delay_X1_OUT	649.131p	✓	✓
19	Delay_X0_OUT	652.951p	✓	✓
20	Energy	219.37f	✓	✓

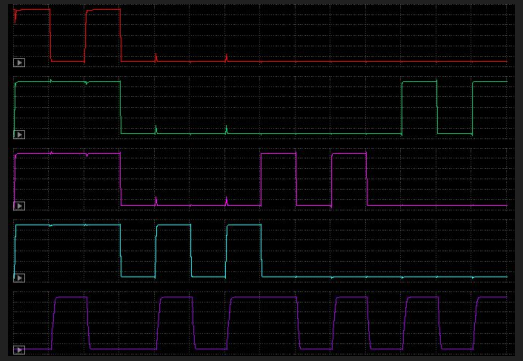
Post Layout: VDD at 0.736v

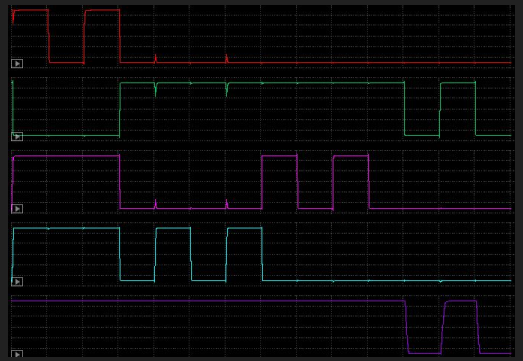
8	tplh_X0_OUT	687....	✓	✓
9	tphl_X0_OUT	678....	✓	✓
10	tplh_X1_OUT	616....	✓	✓
11	tphl_X1_OUT	678....	✓	✓
12	tplh_X2_OUT	511....	✓	✓
13	tphl_X2_OUT	551....	✓	✓
14	tplh_X3_OUT	517....	✓	✓
15	tphl_X3_OUT	698....	✓	✓
16	Delay_X3_OUT	608....	✓	✓
17	Delay_X2_OUT	531....	✓	✓
18	Delay_X1_OUT	647....	✓	✓
19	Delay_X0_OUT	683....	✓	✓
20	Energy	308....	✓	✓

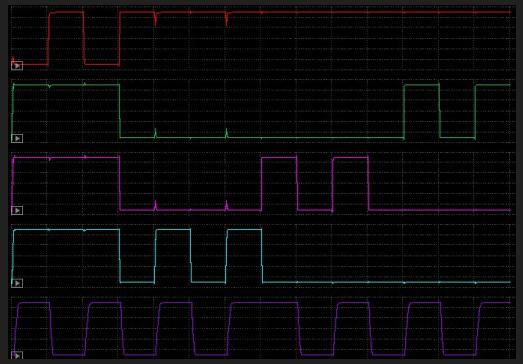
Functionality Check











X0 (MSB)
X1
X2
X3
OUT

Absolute Value Detector Layout

Critical Path in Light Blue

Size: Y = 45.34µm, X = 42.045µm

Aspect Ratio: 1.07

Area: 1906µm^2