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# Title

FPGA based CNN Implementation

# Problem Statement

Convolutional Neural Networks (CNNs) have become a fundamental tool in the field of computer vision and deep learning. However, their computational requirements can be demanding, especially for large-scale models or real-time applications. To achieve high detection accuracy, the large and complex CNN models are used but this leads to expensive computational cost, which is hard to process in real-time in resource-constrained devices with strict latency and energy requirements. CPUs, and GPUs may not provide the necessary real-time or energy efficiency required for these tasks. Secondly, the physical size and energy efficiency of GPUs is not feasible for a CNN to be implemented in many such scenarios. High computation, physical size, energy efficiency, and other constraints cause to CPU and GPU based CNNs be unusable or not being fully utilized in real-time applications involving resource-constraint devices.

# Introduction

This project introduces a Hardware Accelerator for a Convolutional Neural Network. It will run on a custom-made RISC-V processor and will incorporate the inherit parallelism present in CNNs to make them run much faster, and thus being usable in resource constraint as well as real-time applications such as surveillance and object detection in autonomous vehicles. The RISC-V processor will have an improved Instruction Set Architecture (ISA) which will contain instructions regarding the processing of machine/deep learning algorithms – specifically those used inside the CNNs. All this circuity, the RISC-V processor and the CNN, will be implemented on Field Programmable Gate Array (FPGA).

# Expertise/Tools

The expertise required in this project includes the understanding of Deep Learning, specifically Convolution Neural Networks; also, the Hardware Description Language (Verilog); as well as RISC-V processor, its assembly language, and its ISA.

# Comments

We are looking forward for mentorship so that we can be properly guided in pursuing this project of this large size; and to get expert guidance in the challenges we might face in the development of the processor and customizing the instruction set architecture, as well as industry-level understanding of how accelerators are designed.