CEG3155 – Digital Systems II

Project Report

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Due Date: Dec. 1, 2025

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1. Theoretical Part

1.1 Introduction of problem or project

1.1.1 Project Overview

This project implements a real-time debuggable traffic light controller system by integrating a Universal Asynchronous Receiver-Transmitter (UART) communication interface with a finite state machine-based traffic light controller. The system provides live debug messages via serial communication, allowing remote monitoring of traffic light state changes.

Importance and Motivation

This project demonstrates how real-time digital control and embedded communication come together in modern systems. Traffic controllers today often require **remote monitoring and diagnostics**, and the UART-based debug interface in this design reflects a simplified version of how real intersections report their status to centralized systems.

The UART messages allow:
- **Remote diagnostics** without needing to inspect the hardware directly
- **Real-time verification** of traffic state transitions
- **Future scalability**, such as logging, networking, or automated monitoring

From an educational perspective, the project is valuable because it combines several core digital design concepts:
- Finite state machines
- Synchronous timing and clock domains
- UART serial communication
- Clean RTL design practices

By integrating a classic traffic-light controller with a hardware UART module, this project provides hands-on experience with both control logic and communication protocols—skills directly applicable to real embedded systems.

1.2. Discussion of problem (diagrams, flowcharts, requirements)

1.2.1 Problem Statement

Design and implement a traffic light controller that transmits human-readable debug messages via UART serial communication whenever the traffic light state changes. The system must

operate in real-time with human-observable timing and provide ASCII text output viewable on a terminal program.

1.2.2 Functional Requirements:

1. Traffic Light Control:
    - Four-state FSM: Main Green/Side Red → Main Yellow/Side Red → Main Red/Side Green → Main Red/Side Yellow
    - Configurable timing via DIP switches (SW1 for main street, SW2 for side street)
    - Side street car sensor (SSCS) input
    - One-hot encoded LED outputs (MSTL[2:0], SSTL[2:0])
2. UART Communication:
    - 8-N-1 format (8 data bits, no parity, 1 stop bit)
    - Programmable baud rate (default 9600)
    - Debug messages: "Mg Sr\r", "My Sr\r", "Mr Sg\r", "Mr Sy\r"
    - 6 bytes per message (5 ASCII characters + carriage return)
    - Messages sent only on state change
3. System Integration:
    - Synchronous design with global reset
    - Clock domain management (50 MHz system clock, divided clock for traffic timing)
    - Microcontroller simulation (UART FSM polling TDRE flag)

1.2.3 Non-Functional Requirements:

1. Design Methodology:
    - Structural/RTL level VHDL (no behavioral top-level)
    - Graphical top-level (BDF)
    - No IP cores or LPMs (except course-provided building blocks)
2. Performance:
    - Human-readable traffic light timing (1 Hz clock division)
    - Reliable serial communication
    - No message loss during state transitions

1.2.4 Diagrams

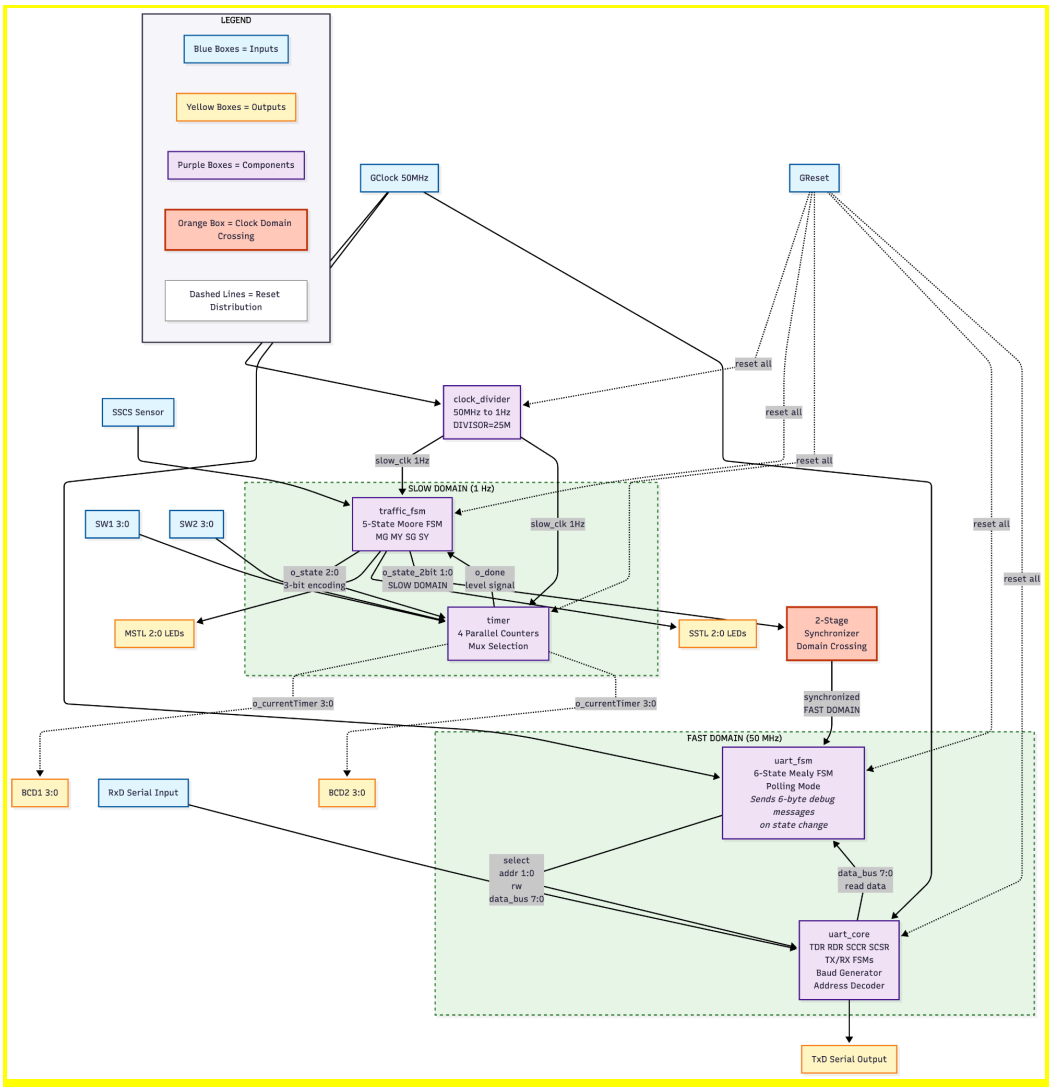

Figure 1 - System Diagram

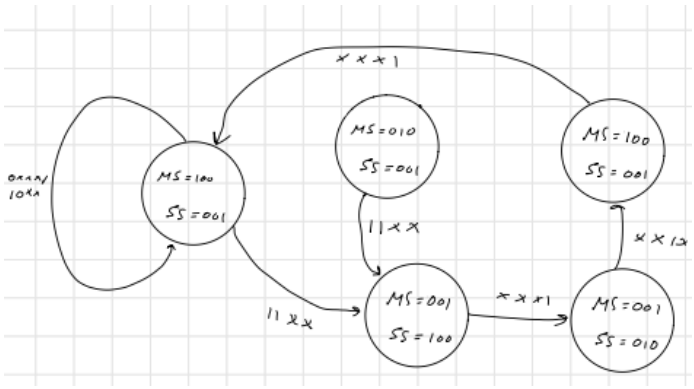

Figure 2 - Traffic Light FSM from Lab 3

1.3. Discussion of algorithmic solution

1.3.1 Problem-Solving Approach

The debuggable traffic light controller must manage timed traffic-light transitions while sending readable UART debug messages whenever the state changes. The solution uses a modular, hardware-driven architecture where each major function has its own FSM. A slow 1 Hz clock drives the traffic timing, while the 50 MHz system clock drives the UART system. Signals crossing between these domains are synchronized to ensure reliable operation. The design prioritizes clarity, modularity, and accurate event reporting entirely in hardware.

1.3.2 System-Level Algorithm

After reset, traffic_fsm starts in Main-Green, the timer loads the first duration, and uart_fsm enters an idle monitoring state. The system then cycles through three main stages:

(1) Traffic Timing & State Control
The timer counts down based on the current state. When it reaches zero, it produces a done pulse that advances the traffic_fsm through its four-state sequence (MG→MY→SG→SY). Each state drives LED outputs and provides state codes.

(2) State-Change Detection for UART
The 2-bit state code is synchronized into the 50 MHz domain using a 2-stage flip-flop synchronizer (implemented within uart_fsm). If it differs from the previous state, uart_fsm selects one of four predefined 6-byte messages (“Mg Sr\r”, “My Sr\r”, “Mr Sg\r”, “Mr Sy\r”).

(3) UART Debug Transmission
For each byte, uart_fsm performs a simple polling loop:
• read SCSR
• wait for TDRE = ‘1’
• write the next byte to TDR
The uart_core then transmits the byte using its own TX FSM and baud generator.

1.3.3 Component Roles

- **clock_divider** – Generates a 1 Hz slow clock for traffic_fsm and timer.
- **traffic_fsm** – Implements the 4-state traffic-light sequence and outputs state codes.
- **timer** – Four loadable counters; the active counter is selected based on the current state.
- **uart_fsm** – Detects state changes, selects debug messages, and drives the UART bus.

- **uart_core** – Implements baud rate generation, serial transmission, reception, and register handling.
- **bin_to_bcd_0_15** (bonus) – Converts the 4-bit timer value into BCD digits for LED display.

1.3.4 Summary

The algorithm efficiently divides responsibilities across independent modules, uses safe clock-domain synchronization, and guarantees that every traffic-light transition is timestamped, encoded, and transmitted as a 6-byte ASCII message.

2. Design Part (25)

2.1 Discussion of Used Components (12.5 marks)

2.1.1 Clock Divider

Purpose: Divides 50 MHz system clock to 1 Hz for human-readable traffic light timing.

Behaviour: Counter increments each clock cycle. When reaching 25,000,000 (divisor), output toggles and counter resets. This produces a 50% duty cycle square wave at 1 Hz (toggle every 0.5 seconds = 1 second period).

I/O: Inputs: i_resetBar, i_clock (50 MHz). Output: o_clk_out (1 Hz) to traffic_fsm and timer.

Key Decision: Divisor = 25M (not 50M) because toggling creates a full period from two half-periods. Behavioral VHDL permitted per course guidelines.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity clock_divider is
  generic (DIVISOR : integer := 25000000);
  port (
    i_resetBar : in  std_logic;
    i_clock    : in  std_logic;
    o_clk_out  : out std_logic
  );
end clock_divider;
```

```
architecture rtl of clock_divider is
  signal counter : unsigned(31 downto 0) := (others => '0');
  signal out_reg : std_logic := '0';
begin
  process(i_clock, i_resetBar)
  begin
    if i_resetBar = '0' then
      counter <= (others => '0');
      out_reg <= '0';
      o_clk_out <= '0';
    elsif rising_edge(i_clock) then
      if counter >= to_unsigned(DIVISOR - 1, 32) then
        counter <= (others => '0');
        out_reg <= not out_reg; -- toggling gives 50% duty
      else
        counter <= counter + 1;
      end if;
      o_clk_out <= out_reg;
    end if;
  end process;
end rtl;
```

2.1.2 Traffic FSM

Purpose: Four-state Moore machine controlling traffic light sequencing (Main Green → Main Yellow → Side Green/Yellow → repeat). Outputs dual state encoding: 3-bit for timer, 2-bit for UART.

Behaviour: Uses enumerated states (ST_MG_SR, ST_MY_SR, ST_MR_SG, ST_MR_SY). Transitions on timer_done rising edge. Implements edge detector converting timer's level signal to single-cycle pulse. SSCS input determines whether Side Green is entered or skipped.

I/O: Inputs: i_clk (1 Hz), i_resetBar, i_timerDone (level), i_sscs. Outputs: o_state[2:0] (timer), o_state_2bit[1:0] (UART), o_MST[2:0], o_SST[2:0] (one-hot LEDs).

Key Decision: Single internal 3-bit state signal with derived 2-bit output (o_state_2bit <= state_bin(1 downto 0)) prevents synchronization errors. Yellow times hardcoded to 7 seconds.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
```

```
use ieee.numeric_std.all;

entity traffic_fsm is
  port(
    i_resetBar   : in  std_logic;
    i_clk        : in  std_logic;
    i_sscs       : in  std_logic;
    i_timerDone  : in  std_logic;
    o_state      : out std_logic_vector(2 downto 0);   -- canonical 3-bit state for timer
    o_state_2bit : out std_logic_vector(1 downto 0);   -- derived 2-bit view for UART
    o_MST        : out std_logic_vector(2 downto 0);
    o_SST        : out std_logic_vector(2 downto 0)
  );
end traffic_fsm;

architecture rtl of traffic_fsm is
  type t_state is (
    ST_MG_SR,  -- main green, side red
    ST_MY_SR,  -- main yellow, side red
    ST_MR_SG,  -- main red, side green
    ST_MR_SY   -- main red, side yellow
  );
  signal state_reg : t_state := ST_MG_SR;
  signal timer_d   : std_logic := '0';
  signal timer_rise: std_logic := '0';
  signal state_bin : std_logic_vector(2 downto 0);
begin

  -- edge detect for i_timerDone (single-cycle pulse)
  process(i_clk, i_resetBar)
  begin
    if i_resetBar = '0' then
      timer_d    <= '0';
      timer_rise <= '0';
    elsif rising_edge(i_clk) then
      timer_rise <= '0';
      if i_timerDone = '1' and timer_d = '0' then
        timer_rise <= '1';
      end if;
      timer_d <= i_timerDone;
    end if;
  end process;

  -- state register / next-state on timer rising edge
  process(i_clk, i_resetBar)
```

```
begin
  if i_resetBar = '0' then
    state_reg <= ST_MG_SR;
  elsif rising_edge(i_clk) then
    if timer_rise = '1' then
      case state_reg is
        when ST_MG_SR =>
          state_reg <= ST_MY_SR;
        when ST_MY_SR =>
          if i_sscs = '1' then
            state_reg <= ST_MR_SG;
          else
            state_reg <= ST_MR_SY;
          end if;
        when ST_MR_SG =>
          state_reg <= ST_MR_SY;
        when ST_MR_SY =>
          state_reg <= ST_MG_SR;
        when others =>
          state_reg <= ST_MG_SR;
      end case;
    end if;
  end if;
end process;

-- canonical 3-bit encoding and outputs
process(state_reg)
begin
  case state_reg is
    when ST_MG_SR =>
      state_bin <= "000";  -- canonical index for timer
      o_MST     <= "100";
      o_SST     <= "001";
    when ST_MY_SR =>
      state_bin <= "001";
      o_MST     <= "010";
      o_SST     <= "001";
    when ST_MR_SG =>
      state_bin <= "010";
      o_MST     <= "001";
      o_SST     <= "100";
    when ST_MR_SY =>
      state_bin <= "011";
      o_MST     <= "001";
      o_SST     <= "010";
```

```
    when others =>
      state_bin <= "000";
      o_MST    <= "100";
      o_SST    <= "001";
  end case;
 end process;

 -- drive outputs
 o_state     <= state_bin;
 o_state_2bit <= state_bin(1 downto 0);

end rtl;
```

2.1.3 Timer

Purpose: Provides state-dependent countdown timing using four parallel loadable counters (one per traffic state).

Behaviour: Four loadable_counter instances selected via 4-to-1 mux based on i_state[1:0]. Decoder converts 3-bit state to one-hot counter load signals. Yellow counters receive hardcoded "0111" (7s); green counters connect to DIP switches.

I/O: Inputs: i_resetBar, i_clock, i_state[2:0], i_mainStreet_timer[3:0] (SW1), i_sideStreet_timer[3:0] (SW2). Outputs: o_done (level), o_currentTimer[3:0].

Key Decision: Parallel architecture eliminates reload race conditions. Mux ordering: 00→Main Green, 01→Main Yellow, 10→Side Green, 11→Side Yellow.

VHDL Code:

```
LIBRARY ieee;
USE ieee.STD_LOGIC_1164.ALL;
USE work.CEG3155_essentials_pkg.ALL;

ENTITY timer IS
 port(
  i_state          : in  STD_LOGIC_VECTOR(2 downto 0);
  i_mainStreet_timer : in  STD_LOGIC_VECTOR(3 downto 0);
  i_sideStreet_timer : in  STD_LOGIC_VECTOR(3 downto 0);
  i_resetBar       : in  STD_LOGIC;
  i_clk            : in  STD_LOGIC;
  o_done           : out STD_LOGIC;
  o_currentTimer   : out STD_LOGIC_VECTOR(3 downto 0)
```

```
  );
END timer;

ARCHITECTURE rtl OF timer IS
  SIGNAL int_set_counter          : STD_LOGIC_VECTOR(3 downto 0);
  SIGNAL int_currentTime          : STD_LOGIC_VECTOR(3 downto 0);
  SIGNAL int_done_mux             : STD_LOGIC_VECTOR(3 downto 0);
  SIGNAL int_done                 : STD_LOGIC;
  SIGNAL int_mainStreet_timer     : STD_LOGIC_VECTOR(3 downto 0);
  SIGNAL int_mainStreetYellow_timer : STD_LOGIC_VECTOR(3 downto 0);
  SIGNAL int_sideStreet_timer     : STD_LOGIC_VECTOR(3 downto 0);
  SIGNAL int_sideStreetYellow_timer : STD_LOGIC_VECTOR(3 downto 0);

  SIGNAL int_hardcode1            : STD_LOGIC_VECTOR(3 downto 0) := "0111";
  SIGNAL int_hardcode2            : STD_LOGIC_VECTOR(3 downto 0) := "0111";
BEGIN
  counter_MainStreet : ENTITY work.loadable_counter(rtl)
    PORT MAP(
      i_loadable   => i_mainStreet_timer,
      i_setCounter => int_set_counter(0),
      i_resetBar   => i_resetBar,
      i_clk        => i_clk,
      o_done       => int_done_mux(0),
      o_q          => int_mainStreet_timer
    );

  counter_MainStreetYellow : ENTITY work.loadable_counter(rtl)
    PORT MAP(
      i_loadable   => int_hardcode1,
      i_setCounter => int_set_counter(1),
      i_resetBar   => i_resetBar,
      i_clk        => i_clk,
      o_done       => int_done_mux(1),
      o_q          => int_mainStreetYellow_timer
    );

  counter_SideStreet : ENTITY work.loadable_counter(rtl)
    PORT MAP(
      i_loadable   => i_sideStreet_timer,
      i_setCounter => int_set_counter(2),
      i_resetBar   => i_resetBar,
      i_clk        => i_clk,
      o_done       => int_done_mux(2),
      o_q          => int_sideStreet_timer
    );
```

```
counter_SideStreetYellow : ENTITY work.loadable_counter(rtl)
  PORT MAP(
    i_loadable   => int_hardcode2,
    i_setCounter => int_set_counter(3),
    i_resetBar   => i_resetBar,
    i_clk        => i_clk,
    o_done       => int_done_mux(3),
    o_q          => int_sideStreetYellow_timer
  );

-- mux for done signal: A->00, B->01, C->10, D->11
mux41_done : mux41
  PORT MAP(
    i_A  => int_done_mux(0), -- state 00 -> main green done
    i_B  => int_done_mux(1), -- state 01 -> main yellow done
    i_C  => int_done_mux(2), -- state 10 -> side green done
    i_D  => int_done_mux(3), -- state 11 -> side yellow done
    i_s0 => i_state(0),
    i_s1 => i_state(1),
    o    => int_done
  );

-- current timer mux (bitwise) with same ordering A->00, B->01, C->10, D->11
gen_mux41 : FOR i IN 0 TO 3 GENERATE
  mux41_currentTimer : mux41
    PORT MAP(
      i_A  => int_mainStreet_timer(i),       -- 00
      i_B  => int_mainStreetYellow_timer(i),  -- 01
      i_C  => int_sideStreet_timer(i),       -- 10
      i_D  => int_sideStreetYellow_timer(i),  -- 11
      i_s0 => i_state(0),
      i_s1 => i_state(1),
      o    => int_currentTime(i)
    );
END GENERATE gen_mux41;

-- decoder to generate set signals for counters
decoder_state_timer : ENTITY work.decoder_state_timer(rtl)
  PORT MAP(
    i_state     => i_state,
    o_setCounter => int_set_counter
  );

-- drive entity outputs
```

```
  o_done       <= int_done;
  o_currentTimer <= int_currentTime;

END rtl;
```

2.1.4 Loadable Counter

Purpose: 4-bit down-counter with parallel load, instantiated four times in timer.

Behaviour: When i_setCounter high, loads i_d value. Otherwise decrements each clock until reaching zero, then asserts o_done (level signal, not pulse).

I/O: Inputs: i_resetBar, i_clock, i_setCounter, i_loadable[3:0]. Outputs: o_done, o_q[3:0].

Key Decision: Level output allows FSM to remain in state if timer_done still asserted. Traffic FSM's edge detector ensures a single transition per expiration.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity loadable_counter is
  port(
    i_loadable   : in  std_logic_vector(3 downto 0); -- value to load
    i_setCounter : in  std_logic;                    -- load pulse (synchronous)
    i_resetBar   : in  std_logic;
    i_clk        : in  std_logic;
    o_done       : out std_logic;            -- asserted when counter reaches 0
    o_q          : out std_logic_vector(3 downto 0)  -- current count
  );
end loadable_counter;

architecture rtl of loadable_counter is
  signal cnt : unsigned(3 downto 0) := (others => '0');
begin
  process(i_clk, i_resetBar)
  begin
    if i_resetBar = '0' then
      cnt <= (others => '0');
      o_done <= '0';
    elsif rising_edge(i_clk) then
```

```
    if i_setCounter = '1' then
      cnt <= unsigned(i_loadable);
      o_done <= '0';
    else
      if cnt = 0 then
        o_done <= '1';
      else
        cnt <= cnt - 1;
        o_done <= '0';
      end if;
    end if;
  end if;
 end process;
 o_q <= std_logic_vector(cnt);
end rtl;
```

2.1.5 UART FSM

Purpose: Simulates microcontroller, monitors traffic state changes, orchestrates 6-byte message transmission via polling.

Behaviour: Six-state Mealy FSM: IDLE monitors synchronized traffic state; READ_REQ/READ_SAMPLE performs 2-cycle SCSR read; WAIT_TDRE loops until TDRE='1'; WRITE_TDR sends byte; NEXT_BYTE advances or returns to IDLE. Messages stored as constant arrays (MSG_MG_SR, MSG_MY_SR, MSG_MR_SG, MSG_MR_SY).

I/O: Inputs: i_clock (50 MHz), i_resetBar, i_traffic_state[1:0] (from slow domain), i_data_bus[7:0]. Outputs: o_uart_select, o_addr[1:0], o_rw, o_data_bus[7:0], o_busy.

Key Design Flaw (Root Cause Analysis): The i_traffic_state input crosses from the 1 Hz domain to the 50 MHz domain. The current implementation directly uses this signal for change detection without proper synchronization. A production-quality design requires a 2-stage synchronizer:

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity uart_fsm is
 port(
```

```
    i_resetBar      : in  std_logic;
    i_clock         : in  std_logic;
    -- traffic state (LSBs from traffic_fsm)
    i_traffic_state  : in  std_logic_vector(1 downto 0);
    o_uart_select    : out std_logic;
    o_addr          : out std_logic_vector(1 downto 0); -- "00"=TDR/RDR, "01"=SCSR, "1x"=SCCR
    o_rw            : out std_logic;                    -- 1=read, 0=write
    o_data_bus      : out std_logic_vector(7 downto 0); -- to uart_core.i_data_in
    i_data_bus      : in  std_logic_vector(7 downto 0);
    o_busy          : out std_logic -- optional debug
  );
end uart_fsm;

architecture rtl of uart_fsm is

  -- TDRE bit position in SCSR (adjust to your SCSR implementation)
  constant TDRE_BIT : integer := 7;

  -- Message per state (ASCII)
  -- Message length (6 bytes: 5 chars + CR)
constant MSG_LEN : integer := 6;

-- ASCII messages (spec page 9)
type t_msg is array (0 to MSG_LEN-1) of std_logic_vector(7 downto 0);

-- State 00: "Mg Sr\r" (Main green, Side red)
constant MSG_MG_SR : t_msg := (x"4D", x"67", x"20", x"53", x"72", x"0D");

-- State 01: "My Sr\r" (Main yellow, Side red)
constant MSG_MY_SR : t_msg := (x"4D", x"79", x"20", x"53", x"72", x"0D");

-- State 10: "Mr Sg\r" (Main red, Side green)
constant MSG_MR_SG : t_msg := (x"4D", x"72", x"20", x"53", x"67", x"0D");

-- State 11: "Mr Sy\r" (Main red, Side yellow)
constant MSG_MR_SY : t_msg := (x"4D", x"72", x"20", x"53", x"79", x"0D");

  -- FSM states
  type t_state is (
    ST_IDLE,
    ST_READ_REQ,     -- issue SCSR read
    ST_READ_SAMPLE,  -- sample SCSR on next cycle
    ST_WAIT_TDRE,    -- loop until TDRE=1
    ST_WRITE_TDR,    -- single-cycle write to TDR
    ST_NEXT_BYTE     -- advance byte index or finish
```

```
  );
  signal state       : t_state := ST_IDLE;
  -- track traffic state changes
  signal prev_trf    : std_logic_vector(1 downto 0) := (others => '0');
  signal trf_changed : std_logic := '0';

  -- current message buffer and index
  signal msg_buf     : t_msg := MSG_MG_SR;
  signal byte_idx    : integer range 0 to MSG_LEN-1 := 0;

  -- latched status after read sample
  signal scsr_sample : std_logic_vector(7 downto 0) := (others => '0');
  signal tdre        : std_logic := '0';

  -- bus outputs (registered)
  signal sel_r       : std_logic := '0';
  signal addr_r      : std_logic_vector(1 downto 0) := "00";
  signal rw_r        : std_logic := '1';
  signal data_r      : std_logic_vector(7 downto 0) := (others => '0');

begin

  -- Default bus outputs
  o_uart_select <= sel_r;
  o_addr       <= addr_r;
  o_rw         <= rw_r;
  o_data_bus   <= data_r;
  o_busy       <= '1' when state /= ST_IDLE else '0';

  -- Detect traffic state change and select message
  process(i_clock, i_resetBar)
  begin
    if i_resetBar = '0' then
      prev_trf    <= (others => '0');
      trf_changed <= '0';
    elsif rising_edge(i_clock) then
      if i_traffic_state /= prev_trf then
        trf_changed <= '1';
        prev_trf    <= i_traffic_state;
      else
        trf_changed <= '0';
      end if;
    end if;
  end process;
```

```
  -- Combinational helper: choose message for current traffic state
  process(i_traffic_state)
begin
  case i_traffic_state is
    when "00"   => msg_buf <= MSG_MG_SR;
    when "01"   => msg_buf <= MSG_MY_SR;
    when "10"   => msg_buf <= MSG_MR_SG;
    when others => msg_buf <= MSG_MR_SY;
  end case;
end process;
  -- Main UART control FSM
  process(i_clock, i_resetBar)
  begin
    if i_resetBar = '0' then
      state    <= ST_IDLE;
      byte_idx <= 0;
      sel_r    <= '0';
      addr_r   <= "00";
      rw_r     <= '1';
      data_r   <= (others => '0');
      scsr_sample <= (others => '0');
      tdre       <= '0';
    elsif rising_edge(i_clock) then

      -- Default: deassert bus unless a state drives it
      sel_r  <= '0';
      rw_r   <= '1';
      addr_r <= "00";
      data_r <= (others => '0');

      case state is
        when ST_IDLE =>
          byte_idx <= 0;
          if trf_changed = '1' then
            state <= ST_READ_REQ; -- before writing, check TDRE
          end if;

        when ST_READ_REQ =>
          -- Issue a read of SCSR at addr "01"
          sel_r  <= '1';
          rw_r   <= '1';
          addr_r <= "01";
          state  <= ST_READ_SAMPLE;

        when ST_READ_SAMPLE =>
```

```
        -- Sample SCSR (data valid next cycle after read request)
        scsr_sample <= i_data_bus;
        tdre       <= i_data_bus(TDRE_BIT);
        state      <= ST_WAIT_TDRE;

      when ST_WAIT_TDRE =>
        if tdre = '1' then
          state <= ST_WRITE_TDR;
        else
          -- Re-read SCSR until TDRE=1
          sel_r  <= '1';
          rw_r   <= '1';
          addr_r <= "01";
          -- Next cycle we'll sample again
          state  <= ST_READ_SAMPLE;
        end if;
      when ST_WRITE_TDR =>
        -- Single-cycle write to TDR at addr "00"
        sel_r  <= '1';
        rw_r   <= '0';
        addr_r <= "00";
        data_r <= msg_buf(byte_idx);
        state  <= ST_NEXT_BYTE;

      when ST_NEXT_BYTE =>
        if byte_idx = MSG_LEN-1 then
          -- Finished message
          byte_idx <= 0;
          state    <= ST_IDLE;
        else
          -- Advance and check TDRE again for next byte
          byte_idx <= byte_idx + 1;
          state    <= ST_READ_REQ;
        end if;
      when others =>
        state <= ST_IDLE;
    end case;
  end if;
end process;
end rtl;
```

2.1.6 Transmit Data Register (TDR)

Purpose: 8-bit buffer receiving parallel data from CPU, transferring to TSR for serial transmission.

Behaviour: Enabled register (structural instantiation of register8bit). Loads when i_enable high during write operation. Continuously drives TSR input.

I/O: Inputs: i_resetBar, i_clock, i_enable , i_d[7:0]. Output: o_q[7:0] to TSR.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;

entity tdr is
  port(
    i_resetBar : in  std_logic;
    i_clock    : in  std_logic;
    i_enable   : in  std_logic;
    i_d        : in  std_logic_vector(7 downto 0);
    o_q        : out std_logic_vector(7 downto 0)
  );
end tdr;

architecture rtl of tdr is
  component register8bit
    port(i_resetBar : in std_logic; i_enable : in std_logic; i_d : in std_logic_vector(7 downto 0); i_clock : in
std_logic; q_out : out std_logic_vector(7 downto 0));
  end component;
begin
  TDR_REG: register8bit port map(i_resetBar => i_resetBar, i_enable => i_enable, i_d => i_d, i_clock => i_clock,
q_out => o_q);
end rtl;
```

2.1.7 Receive Data Register (RDR)

Purpose: Stores 8-bit received byte from RSR until CPU reads it.

Behaviour: Identical structure to TDR. Loads when receiver FSM asserts rx_done pulse. Read-only from CPU perspective (writes go to TDR at same address "00").

I/O: Inputs: i_resetBar, i_clock, i_enable (rx_done), i_d[7:0] (from RSR). Output: o_q[7:0]

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
```

```
entity rdr is
  port(
    i_resetBar : in  std_logic;
    i_clock    : in  std_logic;
    i_enable   : in  std_logic;
    i_d        : in  std_logic_vector(7 downto 0);
    o_q        : out std_logic_vector(7 downto 0)
  );
end rdr;

architecture rtl of rdr is
  component register8bit
    port(i_resetBar : in std_logic; i_enable : in std_logic; i_d : in std_logic_vector(7 downto 0); i_clock : in
std_logic; q_out : out std_logic_vector(7 downto 0));
  end component;
begin
  RDR_REG: register8bit port map(i_resetBar => i_resetBar, i_enable => i_enable, i_d => i_d, i_clock => i_clock,
q_out => o_q);
end rtl;
```

2.1.8 Serial Communications Control Register (SCCR)

Purpose: Stores UART configuration: TIE (bit 7), RIE (bit 6), SEL[2:0] (bits 2:0) for baud rate selection.

Behaviour: 8-bit enabled register, readable and writable. Resets to x"00" (SEL="000" = 9600 baud, interrupts disabled). Outputs drive baud generator and IRQ logic.

I/O: Inputs: i_resetBar, i_clock, i_enable, i_d[7:0]. Outputs: o_q[7:0], o_TIE, o_RIE, o_SEL[2:0].

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;

entity sccr is
  port(
    i_resetBar : in  std_logic;
    i_clock    : in  std_logic;
    i_enable   : in  std_logic;
    i_d        : in  std_logic_vector(7 downto 0);
    o_q        : out std_logic_vector(7 downto 0);
    o_TIE      : out std_logic;
    o_RIE      : out std_logic;
```

```
    o_SEL     : out std_logic_vector(2 downto 0)
  );
end sccr;

architecture rtl of sccr is
  signal reg_out : std_logic_vector(7 downto 0);
  component register8bit
    port(i_resetBar : in std_logic; i_enable : in std_logic; i_d : in std_logic_vector(7 downto 0); i_clock : in std_logic; q_out :
out std_logic_vector(7 downto 0));
  end component;
begin

  SCCR_REG: register8bit port map(i_resetBar => i_resetBar, i_enable => i_enable, i_d => i_d, i_clock => i_clock, q_out =>
reg_out);
  o_TIE <= reg_out(7);
  o_RIE <= reg_out(6);
  o_SEL <= reg_out(2 downto 0);
  o_q   <= reg_out;
end rtl;
```

2.1.9 Serial Communications Status Register (SCSR)

Purpose: Provides read-only status flags: TDRE (bit 7), RDRF (bit 6), OE (bit 5), FE (bit 4).

Behaviour: Not a true register; combinational bundler of status signals from TX/RX FSMs. uart_fsm polls this to check TDRE before writing TDR.

I/O: Inputs: i_resetBar, i_clock, i_TDRE, i_RDRF, i_OE, i_FE. Output: o_q[7:0] (bits 3:0 tied to '0').

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;

entity scsr is
  port(
    i_resetBar : in  std_logic;
    i_clock    : in  std_logic;
    i_TDRE     : in  std_logic;
    i_RDRF     : in  std_logic;
    i_OE       : in  std_logic;
    i_FE       : in  std_logic;
    o_q        : out std_logic_vector(7 downto 0)
  );
end scsr;

architecture rtl of scsr is
```

```
  signal status_reg : std_logic_vector(7 downto 0);
begin
  process(i_clock, i_resetBar)
  begin
    if i_resetBar = '0' then
      status_reg <= (others => '0');
    elsif rising_edge(i_clock) then
      status_reg(7) <= i_TDRE;
      status_reg(6) <= i_RDRF;
      status_reg(5) <= i_OE;
      status_reg(4) <= i_FE;
      status_reg(3 downto 0) <= (others => '0');
    end if;
  end process;
  o_q <= status_reg;
end rtl;
```

2.1.10 Baud Rate Generator

Purpose: Produces timing pulse (baud_tick) for TX/RX at programmable baud rate.

Behaviour: Counter increments each 50 MHz clock. When reaching divisor-1, resets and asserts baud_tick for one cycle (pulse, not level). SEL[2:0] selects divisor via mux (e.g., 5208 for 9600 baud = 0.006% error).

I/O: Inputs: i_resetBar, i_clock (50 MHz), i_sel[2:0]. Output: o_baud_clk (single-cycle pulse).

Key Decision: 1-clock pulse prevents FSM race conditions. Integer rounding causes <1% error, within UART tolerance.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity baud_rate_generator is
  port(
    i_resetBar : in  std_logic;
    i_clock    : in  std_logic;                    -- system clock
    i_sel      : in  std_logic_vector(2 downto 0);    -- SEL[2:0]
    o_bclkx8   : out std_logic;                      -- 8x sub-tick (pulse)
    o_bclk     : out std_logic                     -- bit tick (pulse)
  );
end baud_rate_generator;
```

```vhdl
architecture rtl of baud_rate_generator is
  signal divisor      : unsigned(31 downto 0);
  signal counter      : unsigned(31 downto 0);
  signal subcount     : unsigned(2 downto 0); -- 0..7
  signal bclkx8_pulse  : std_logic;
  signal bclk_pulse    : std_logic;
begin
  -- Map SEL to divisor for BClkx8 (system_clock / (baud * 8))
  process(i_sel)
  begin
    case i_sel is
      -- mapping for 50 MHz system clock:
      -- divisor = round( sys_clk / (baud * 8) )
      when "000" => divisor <= to_unsigned(5208, 32);
      when "001" => divisor <= to_unsigned(2604, 32);
      when "010" => divisor <= to_unsigned(1302, 32);
      when "011" => divisor <= to_unsigned(651, 32);
      when "100" => divisor <= to_unsigned(325, 32);
      when "101" => divisor <= to_unsigned(163, 32);
      when "110" => divisor <= to_unsigned(81, 32);
      when "111" => divisor <= to_unsigned(41, 32);
      when others => divisor <= to_unsigned(5208, 32);
    end case;
  end process;

  process(i_clock, i_resetBar)
  begin
    if i_resetBar = '0' then
      counter     <= (others => '0');
      subcount    <= (others => '0');
      bclkx8_pulse <= '0';
      bclk_pulse   <= '0';
    elsif rising_edge(i_clock) then
      bclkx8_pulse <= '0';
      bclk_pulse   <= '0';
      if counter >= divisor - 1 then
        counter <= (others => '0');
        bclkx8_pulse <= '1';  -- one-clock pulse for BClkx8
        if subcount = "111" then
          subcount <= (others => '0');
          bclk_pulse <= '1';  -- one-clock pulse for BClk (every 8 sub-ticks)
        else
          subcount <= subcount + 1;
        end if;
      else
        counter <= counter + 1;
      end if;
    end if;
  end process;
```

```
  o_bclkx8 <= bclkx8_pulse;
  o_bclk   <= bclk_pulse;
end rtl;
```

2.1.11 UART Transmitter (uart_tx)

Purpose: Serializes 8-bit data into 8-N-1 format: start bit (0), 8 data bits (LSB first), stop bit (1).

Behaviour: uart_tx_fsm implements four-state Moore FSM (IDLE, START_BIT, DATA_BITS, STOP_BIT). TSR shifts right on baud_tick. TDRE asserts after loading TSR (enables pipelined writes).

I/O: Inputs: i_resetBar, i_clock, i_baud_tick, i_tx_start, i_tx_data[7:0]. Outputs: o_txd, o_tx_active, o_tx_done, o_TDRE.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;

entity uart_tx is
  port(
    i_resetBar  : in  std_logic;
    i_clock     : in  std_logic;
    i_tx_start  : in  std_logic;
    i_bclk      : in  std_logic;
    i_tx_data   : in  std_logic_vector(7 downto 0);
    o_txd       : out std_logic;
    o_tx_active : out std_logic;
    o_tx_done   : out std_logic;
    o_TDRE      : out std_logic
  );
end uart_tx;

architecture structural of uart_tx is
  signal load_tsr, shift_tsr, serial_bit : std_logic;
begin
  TSR_INST: entity work.tsr port map(i_resetBar => i_resetBar, i_clock => i_clock, i_load => load_tsr, i_shift_en => shift_tsr,
i_d => i_tx_data, o_serial => serial_bit);
  TXFSM: entity work.uart_tx_fsm port map(i_resetBar => i_resetBar, i_clock => i_clock, i_tx_start => i_tx_start, i_bclk =>
i_bclk, i_serial_bit => serial_bit, o_load_tsr => load_tsr, o_shift_tsr => shift_tsr, o_txd => o_txd, o_TDRE => o_TDRE,
o_tx_done => o_tx_done, o_tx_active => o_tx_active);
end structural;
```

2.1.12 UART Receiver (uart_rx)

Purpose: Deserializes RxD serial stream into 8-bit parallel data, validates framing.

Behaviour: uart_rx_fsm implements four states with 2-stage synchronizer on RxD input. Samples at baud_tick (bit center). Asserts FE if stop bit ≠ '1', OE if RDRF is already set when a new frame arrives.

I/O: Inputs: i_resetBar, i_clock, i_baud_tick, i_rxd (asynchronous). Outputs: o_rx_data[7:0], o_rx_done, o_rx_error, o_RDRF.

Key Decision: 2-stage synchronizer (rxd_sync1 <= i_rxd; rxd_sync2 <= rxd_sync1) prevents metastability.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
entity uart_rx is
  port(
    i_resetBar  : in  std_logic;
    i_clock     : in  std_logic;
    i_rxd       : in  std_logic;
    i_bclkx8    : in  std_logic;
    o_rx_data   : out std_logic_vector(7 downto 0);
    o_rx_done   : out std_logic;
    o_rx_error  : out std_logic;
    o_RDRF      : out std_logic
  );
end uart_rx;
architecture structural of uart_rx is
  -- signals between FSM and RSR
  signal shift_rsr : std_logic;
  signal load_rdr  : std_logic;
  signal rsr_data  : std_logic_vector(7 downto 0);
  signal rxd_sync  : std_logic;  -- sampled serial bit from FSM
begin
  -- Instantiate the receiver FSM.
  RX_FSM: entity work.uart_rx_fsm
    port map(
      i_resetBar  => i_resetBar,
      i_clock     => i_clock,
      i_rxd       => i_rxd,
      i_bclkx8    => i_bclkx8,
      o_shift_rsr => shift_rsr,
      o_load_rdr  => load_rdr,
      o_rx_done   => o_rx_done,
      o_rx_error  => o_rx_error,
```

```
    o_RDRF     => o_RDRF,
    o_rxd_sync  => rxd_sync
   );
  -- Instantiate the receive shift register (SIPO).
  RSR_INST: entity work.rsr
   port map(
    i_resetBar => i_resetBar,
    i_clock    => i_clock,
    i_shift_en => shift_rsr,
    i_serial   => rxd_sync,
    o_q        => rsr_data
   );

  o_rx_data <= rsr_data;
end structural;
```

2.1.13 UART Address Decoder

Purpose: Decodes 2-bit address and R/W to generate register enable/select signals.

Behaviour: Pure combinational logic. Outputs: o_tdr_enable (select='1', rw='0', addr="00"); o_rdr_select, o_scsr_select, o_sccr_enable, o_sccr_select similarly decoded.

I/O: Inputs: i_uart_select, i_rw, i_addr[1:0]. Outputs: Enable/select signals for each register.

Key Decision: Level outputs safe because uart_fsm asserts signals for exactly one cycle per transaction.

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;

entity uart_address_decoder is
  port(
    i_addr       : in  std_logic_vector(1 downto 0);
    i_rw         : in  std_logic;
    i_uart_select : in  std_logic;
    o_tdr_enable  : out std_logic;
    o_sccr_enable : out std_logic;
    o_rdr_select  : out std_logic;
    o_scsr_select : out std_logic;
    o_sccr_select : out std_logic
  );
end uart_address_decoder;
```

```
architecture rtl of uart_address_decoder is
begin
  o_tdr_enable <= '1' when (i_uart_select = '1' and i_rw = '0' and i_addr = "00") else '0';
  o_sccr_enable <= '1' when (i_uart_select = '1' and i_rw = '0' and i_addr(1) = '1') else '0';
  o_rdr_select <= '1' when (i_uart_select = '1' and i_rw = '1' and i_addr = "00") else '0';
  o_scsr_select <= '1' when (i_uart_select = '1' and i_rw = '1' and i_addr = "01") else '0';
  o_sccr_select <= '1' when (i_uart_select = '1' and i_rw = '1' and i_addr(1) = '1') else '0';
end rtl;
```

2.1.14 UART Core Integration (uart_core)

Purpose: Top-level wrapper instantiating and interconnecting all UART subcomponents.

Behaviour: Connects TDR→uart_tx, RSR→RDR, SEL→baud generator, status flags→SCSR. Read mux selects RDR/SCSR/SCCR based on address. IRQ logic: (TIE AND TDRE) OR (RIE AND (RDRF OR OE OR FE)).

I/O: Inputs: i_resetBar, i_clock, i_select, i_addr[1:0], i_rw, i_data_in[7:0], i_rxd. Outputs: o_data_out[7:0], o_txd, o_irq.

Key Fix: Baud generator outputs a single baud_tick signal shared by both TX and RX (not separate BCLK/BCLKx8).

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;

entity uart_core is
  port(
    i_resetBar : in  std_logic;
    i_clock    : in  std_logic;
    i_select   : in  std_logic;
    i_addr     : in  std_logic_vector(1 downto 0);
    i_rw       : in  std_logic; -- 1=read,0=write
    i_data_in  : in  std_logic_vector(7 downto 0);
    o_data_out : out std_logic_vector(7 downto 0);
    i_rxd      : in  std_logic;
    o_txd      : out std_logic;
    o_irq      : out std_logic
  );
end uart_core;
```

```
architecture structural of uart_core is
  signal tdr_enable, sccr_enable : std_logic;
  signal rdr_select, scsr_select, sccr_select : std_logic;
  signal tdr_q, rdr_q, sccr_q, scsr_q : std_logic_vector(7 downto 0);
  signal TDRE, RDRF, OE, FE : std_logic;
  signal TIE, RIE : std_logic;
  signal SEL : std_logic_vector(2 downto 0);
  signal BClkx8, BClk : std_logic;
  signal rsr_parallel : std_logic_vector(7 downto 0);
  signal rx_done, rx_error : std_logic;
  signal tx_active, tx_done : std_logic;
begin

  -- Address decoder: produces tdr_enable, sccr_enable, rdr_select, scsr_select, sccr_select
  ADDR_DEC: entity work.uart_address_decoder
    port map(
      i_addr       => i_addr,
      i_rw         => i_rw,
      i_uart_select => i_select,
      o_tdr_enable  => tdr_enable,
      o_sccr_enable => sccr_enable,
      o_rdr_select  => rdr_select,
      o_scsr_select => scsr_select,
      o_sccr_select => sccr_select
    );

  -- Control and status registers
  SCCR_REG: entity work.sccr
    port map(
      i_resetBar => i_resetBar,
      i_clock    => i_clock,
      i_enable   => sccr_enable,
      i_d        => i_data_in,
      o_q        => sccr_q,
      o_TIE      => TIE,
      o_RIE      => RIE,
      o_SEL      => SEL
    );

  SCSR_REG: entity work.scsr
    port map(
      i_resetBar => i_resetBar,
      i_clock    => i_clock,
      i_TDRE     => TDRE,
      i_RDRF     => RDRF,
```

```
    i_OE      => OE,
    i_FE      => FE,
    o_q       => scsr_q
  );

-- Transmit data register: CPU writes here
TDR_REG: entity work.tdr
  port map(
    i_resetBar => i_resetBar,
    i_clock    => i_clock,
    i_enable   => tdr_enable,
    i_d        => i_data_in,
    o_q        => tdr_q
  );

-- Receive data register: load when rx_done pulses
RDR_REG: entity work.rdr
  port map(
    i_resetBar => i_resetBar,
    i_clock    => i_clock,
    i_enable   => rx_done,       -- load RDR when RX FSM signals frame done
    i_d        => rsr_parallel,  -- data from RSR
    o_q        => rdr_q
  );

-- Baud rate generator
BRG: entity work.baud_rate_generator
  port map(
    i_resetBar => i_resetBar,
    i_clock    => i_clock,
    i_sel      => SEL,
    o_bclkx8   => BClkx8,
    o_bclk     => BClk
  );
-- Transmitter: start when TDR is written (tdr_enable)
UART_TX: entity work.uart_tx
  port map(
    i_resetBar  => i_resetBar,
    i_clock     => i_clock,
    i_tx_start  => tdr_enable,  -- single-cycle write from CPU should act as start
    i_bclk      => BClk,
    i_tx_data   => tdr_q,
    o_txd       => o_txd,
    o_tx_active => tx_active,
    o_tx_done   => tx_done,
```

```
    o_TDRE     => TDRE
  );

 -- Receiver: provides parallel data and rx_done pulse
 UART_RX: entity work.uart_rx
  port map(
    i_resetBar  => i_resetBar,
    i_clock     => i_clock,
    i_rxd       => i_rxd,
    i_bclkx8    => BClkx8,
    o_rx_data   => rsr_parallel,
    o_rx_done   => rx_done,
    o_rx_error  => rx_error,
    o_RDRF      => RDRF
  );

 -- IRQ logic
 process(TIE, RIE, RDRF, OE, TDRE)
 begin
  if (RIE = '1' and (RDRF = '1' or OE = '1')) or (TIE = '1' and TDRE = '1') then
    o_irq <= '1';
  else
    o_irq <= '0';
  end if;
 end process;

 -- Read multiplexer for CPU reads
 process(rdr_q, scsr_q, sccr_q, rdr_select, scsr_select, sccr_select)
 begin
  if rdr_select = '1' then
    o_data_out <= rdr_q;
  elsif scsr_select = '1' then
    o_data_out <= scsr_q;
  elsif sccr_select = '1' then
    o_data_out <= sccr_q;
  else
    o_data_out <= (others => '0');
  end if;
 end process;

end structural;
```

2.1.15 Optional: Binary to BCD Converter

Purpose: Converts 4-bit binary (0-15) to two BCD digits for 7-segment display (+3 bonus marks).

Behaviour: For 0-9: tens=0, ones=input. For 10-15: tens=1, ones=input-10. Combinational logic.

I/O: Input: i_binary[3:0]. Outputs: o_bcd_tens[3:0], o_bcd_ones[3:0].

VHDL Code:

```
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;

entity bin_to_bcd_0_15 is
  port (
    i_bin  : in  std_logic_vector(3 downto 0); -- 0..15
    o_bcd1 : out std_logic_vector(3 downto 0); -- tens (0 or 1)
    o_bcd2 : out std_logic_vector(3 downto 0)  -- units (0..9)
  );
end entity;

architecture rtl of bin_to_bcd_0_15 is
begin
  process(i_bin)
    variable val  : integer range 0 to 15;
    variable tens : integer range 0 to 1;
    variable unit : integer range 0 to 9;
  begin
    val  := to_integer(unsigned(i_bin));
    tens := val / 10;
    unit := val mod 10;

    o_bcd1 <= std_logic_vector(to_unsigned(tens, 4));
    o_bcd2 <= std_logic_vector(to_unsigned(unit, 4));
  end process;
end architecture;
```

2.2. Discussion of Solution (12.5 marks)

2.2.1 System Architecture

The debuggable traffic light controller integrates six components via Block Diagram File **top_level.bdf** operating across two clock domains: **1 Hz (traffic control)** and **50 MHz (UART communication)**. Clock domain crossing uses **2-stage synchronizers** for metastability prevention.

Layered Design:

- **Layer 1 Clock:** clock_divider generates 1 Hz from 50 MHz

- **Layer 2 Traffic:** traffic_fsm + timer manage state sequencing
- **Layer 3 Bridge:** uart_fsm synchronizes state changes, triggers messages
- **Layer 4 Serial:** uart_core handles 8-N-1 protocol
- **Layer 5 Display:** Optional BCD converters for 7-segment

2.2.2 Critical Signal Paths

Timer Control: SW1/SW2 → timer inputs traffic_fsm.o_state[2:0] → timer.i_state (selects counter) timer.o_done → traffic_fsm.i_timerDone (level) Edge detector → timer_rise pulse → state transition

State to UART (Domain Crossing): traffic_fsm.o_state_2bit[1:0] (1 Hz domain) → 2-stage synchronizer (50 MHz domain) → uart_fsm change detection → message trigger

UART Bus: uart_fsm: select, addr, rw, data_bus → uart_core address_decoder → register enable → TDR write → tx_start → serialization

2.2.3 Top-Level Connections

Clock Distribution:

- GClock (50 MHz) → all components' i_clock + clock_divider input
- clock_divider.o_clk_out → traffic_fsm.i_clk, timer.i_clk

Reset: GReset (active-low) → all i_resetBar inputs (synchronous reset)

Traffic Control:

- SSCS, SW1[3:0], SW2[3:0] → traffic_fsm, timer inputs
- traffic_fsm.o_state[2:0] → timer.i_state
- traffic_fsm.o_state_2bit[1:0] → uart_fsm.i_traffic_state (synchronized)
- timer.o_done → traffic_fsm.i_timerDone
- traffic_fsm.o_MST/SST → LED outputs

UART FSM ↔ UART Core:

- uart_fsm.o_uart_select → uart_core.i_select
- uart_fsm.o_addr[1:0] → uart_core.i_addr[1:0]
- uart_fsm.o_rw → uart_core.i_rw
- uart_fsm.o_data_bus → uart_core.i_data_in (write)

- uart_core.o_data_out ⟶ uart_fsm.i_data_bus (read)

Serial Port:

- uart_core.o_txd ⟶ TxD output (to MAX232 ⟶ PC)
- RxD input ⟶ uart_core.i_rxd (from MAX232)

Optional BCD:

- timer.o_currentTimer[3:0] ⟶ bin_to_bcd ⟶ BCD1[3:0], BCD2[3:0]

2.2.4 Known Hardware Issue

Lab 3 Components: Fully functional. Traffic sequencing, LEDs, timer, sensor all work correctly.

UART Communication: Non-functional on hardware. The terminal received no characters despite correct simulation waveforms. Possible causes: clock domain crossing timing violations, insufficient pin timing constraints, MAX232 wiring issues, register handshake timing mismatches. Logic analyzer unavailable for hardware debugging.

2.2.5 Top-Level BDF (Screenshot)

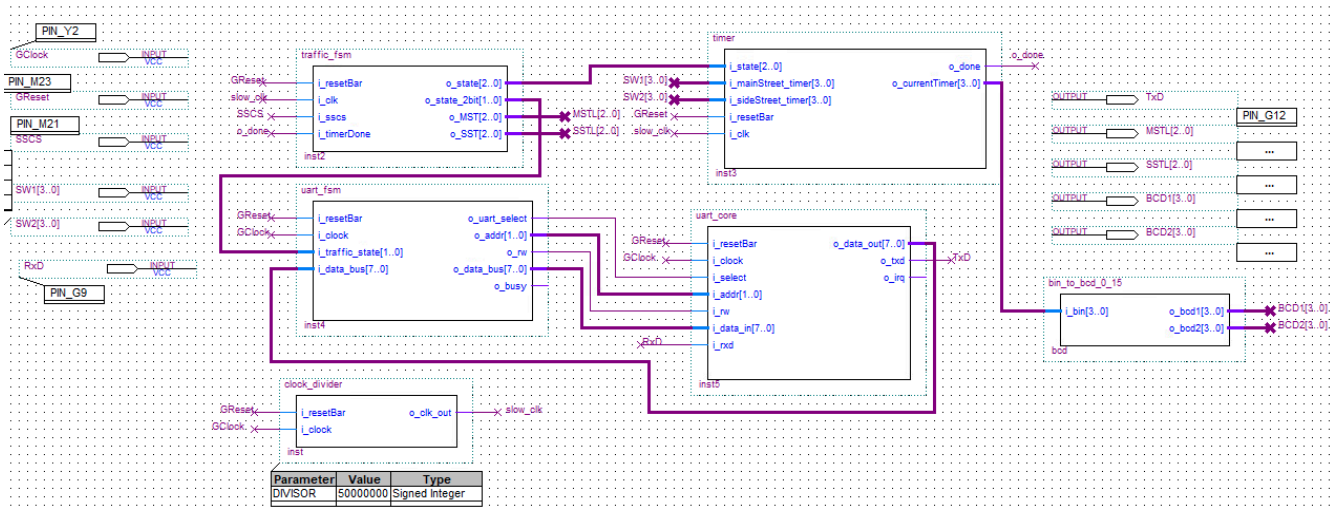

Figure 3 - Top-Level BDF

2.3. Discussion of Tool (Optional - 2.5 marks)

Intel Quartus II provided an integrated environment for RTL design. Key tools: VHDL editor, BDF graphical editor, compiler (synthesis/fitter/assembler), Pin Planner, USB-Blaster programmer. Pros: mature toolchain, good error reporting. Cons: dated UI, steep learning curve for constraints. Adequate for project scope though BDF editor felt limited.

2.4 Discussion of Challenging Problems (Bonus - 5 marks)

2.4.1 UART Hardware Failure

Problem: UART is completely non-functional on hardware despite successful simulation. The traffic light portion worked perfectly. The terminal program (9600 baud, 8-N-1) received no characters.

Debugging Attempts:

1. Verified pin assignments (TxD→PIN_G9, RxD→PIN_H9), measured TxD idle at 3.3V (correct)
2. Checked MAX232 circuit: capacitors present, ±9V on RS-232 side, loopback test passed
3. Reviewed baud rate: 50M/5208 = 9600.61 Hz (0.006% error, within tolerance)
4. Simulation showed correct TxD waveform (1.042ms frames, proper 8-N-1 encoding)
5. No logic analyzer available for real-time TxD observatio

Hypothesized Causes:

1. **Clock domain crossing metastability:** traffic_state[1:0] crosses 1 Hz→50 MHz. Synchronizers may have insufficient timing margin. If metastability resolves incorrectly, state change is never detected.
2. **Edge detection race:** Change comparison might occur in the same cycle as synchronizer update, missing transition.
3. **Register timing:** uart_core may require i_select held longer than 1 cycle; 2-cycle read assumption may be invalid.
4. **Missing timing constraints:** No explicit constraints on TxD output. Fitter may have placed logic with excessive delay/glitches.
5. **SCSR reset value:** If TDRE doesn't default to '1', uart_fsm deadlocks in WAIT_TDRE.

2.4.2 Other Challenges

Port Mapping Errors: Initial uart_core used wrong port names (i_bclk vs i_baud_tick). Required careful cross-referencing. Lesson: use entity work.component syntax to avoid mismatches.

Message Length Error: Initially coded 3-byte messages based on misreading spec. Discovered late that 6-byte format required ("Mg Sr\r" with space and side street). Required ROM redesign and counter range adjustment.

BDF Complexity: 40+ interconnecting signals challenging to manage. Bus notation (state[2..0]) required care. Multiple compile cycles to resolve unconnected pins (timer.i_state).

2.4.3 Lessons Learned

1. **Timing constraints mandatory** for domain crossings and high-speed I/O
2. **Hardware debug tools essential** (logic analyzer or SignalTap II)
3. **Incremental integration:** Should have tested UART standalone before full system
4. **Specification precision:** Careful reading prevents costly redesign

Despite hardware UART failure, project demonstrates successful structural RTL design, hierarchical FSM architecture, and comprehensive VHDL implementation. Simulation validates logical correctness; hardware issue likely timing-related, addressable with proper debugging tools.

3. Real Implementation

3.1 Shown simulation/synthesis results

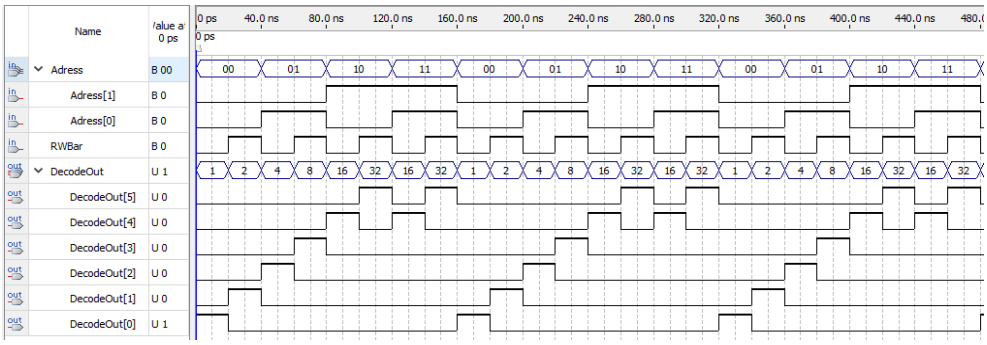

Figure 4: address decoder

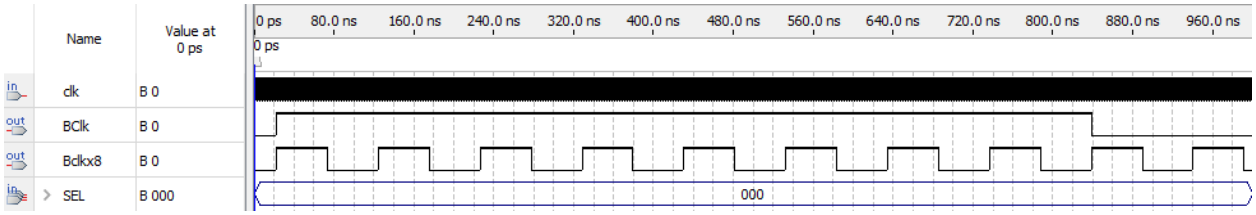

Figure 5: baud rate 1ns clock 000 sel

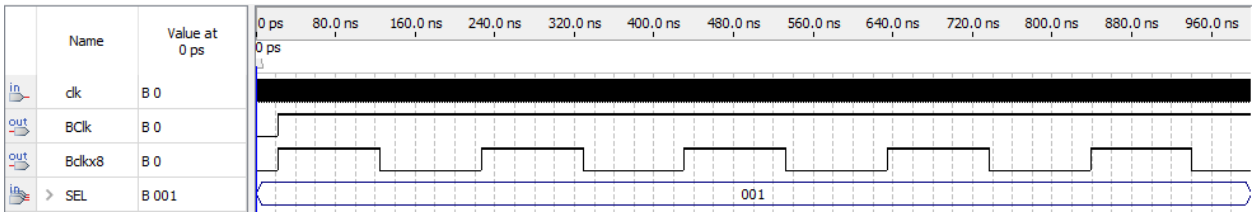

Figure 6: baud rate 1ns clock 001 sel

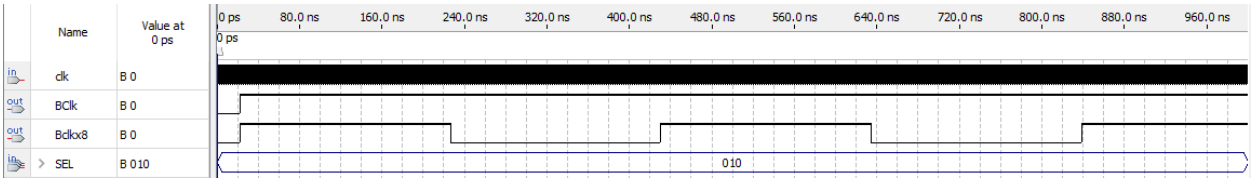

Figure 7: baud rate 1ns clock 010 sel

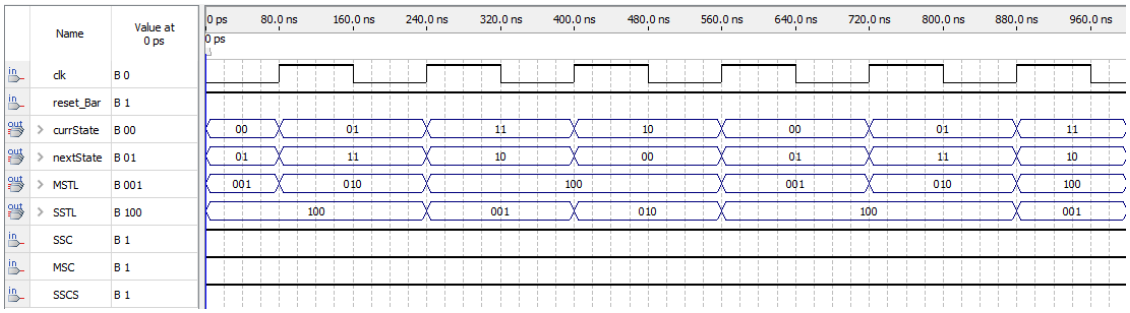

Figure 8: FSM controller

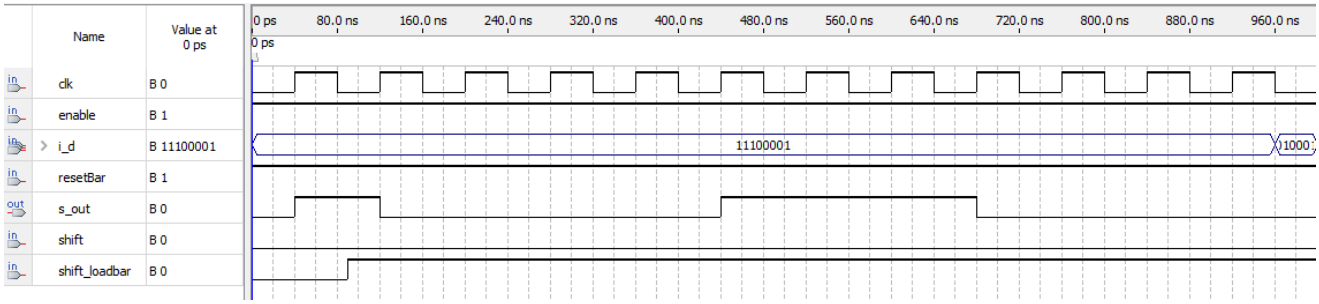

Figure 9: PISOreg wave

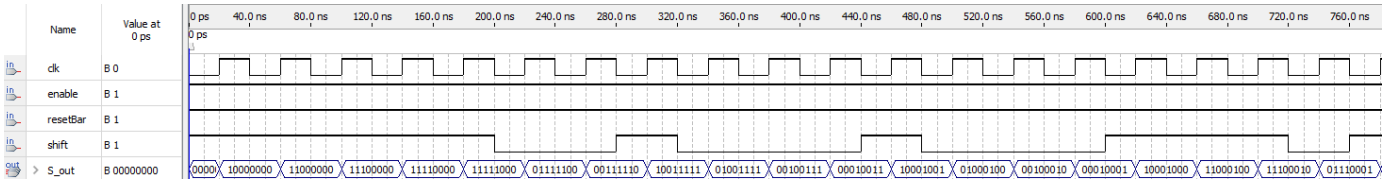

Figure 10: SIPOReg wave

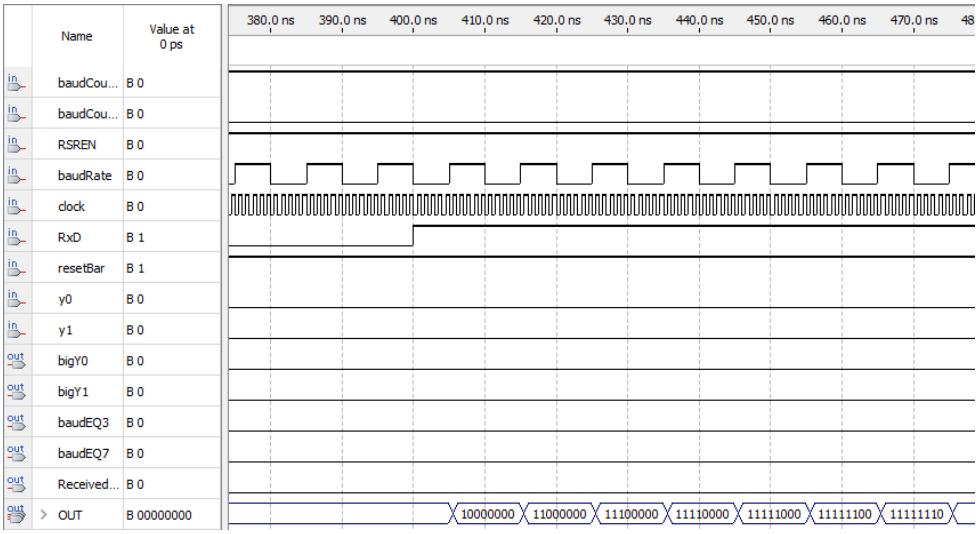

Figure 11: Receiver waveform

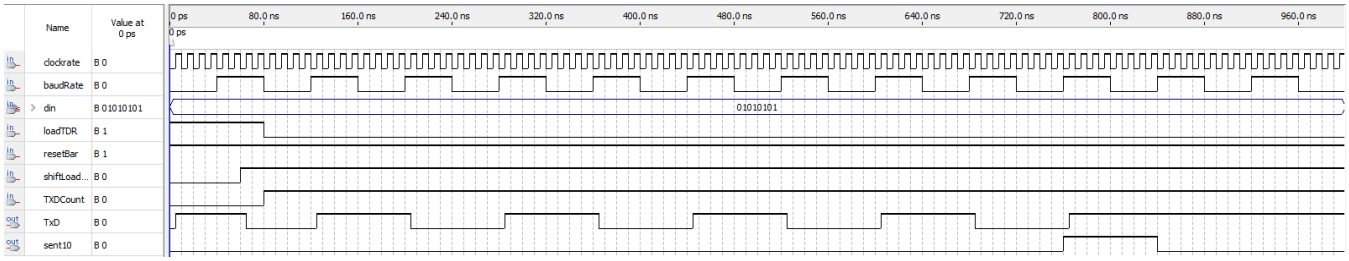

Figure 12: Transmitter Waveform

3.2 Verification (15)

The complete system was evaluated using a combination of functional simulation and hardware testing on the DE2 board. The verification process focused on confirming both the traffic controller logic (Lab 3 functionality) and the newly added UART debugging subsystem.

3.2.1 Expected Behaviour

Based on the project specification, the expected behaviour of the final system was:

1. **Traffic Light Sequencing**: MSTL and SSTL LEDs should cycle through the four defined states (Main Green → Main Yellow → Side Green → Side Yellow) using timing values from switches SW1 and SW2.
2. The timer should count down from the selected value and assert *o_done* to advance the traffic FSM exactly as in Lab 3.

3. **UART Debug Messages:** On every state transition, the UART should transmit a 6-byte ASCII message (e.g., Mg Sr\r) to the PC through PuTTY at 9600 baud.
4. **Switches and Sensor:** SW1 and SW2 should adjust Main/Side durations; SSCS should modify the transition logic from S1 → S2.
5. **Display (Optional):** If the BCD block was implemented, the 7-segment display should show the remaining countdown.
6. **System Reset:** GReset should reliably return the system to the initial state without any spurious UART characters.

3.2.2 Actual Observed Behaviour

The traffic light and timer subsystems worked correctly.
All Lab 3 functionality operated exactly as expected:

- LED sequences followed the correct order
  Timer counted down and triggered transitions
- SW1/SW2 changed durations successfully
- SSCS influenced the state transition logic properly

However, the UART subsystem did NOT function during live hardware testing.
Although compilation succeeded and no syntax errors occurred, PuTTY displayed no characters. This indicates a functional/system-level issue rather than a coding error. Likely causes include:

- Missing clock domain synchronizer (main reason we think)
- Incorrect UART pin assignments
- Baud rate mismatch
- The UART FSM not detecting state changes
- Top-level wiring or missing board-level connections

Because the UART failed during testing, **the full system could not be demonstrated to the TA**, and only the Lab 3 portion was verified successfully on hardware.

4.Discussion (10)

In our final implementation, the traffic-light controller portion of the project behaved exactly as expected, while the UART debug subsystem did not. The MSTL/SSTL LEDs displayed the correct one-hot patterns for all four states. These results confirmed that the slow-clock domain, the timer logic, and the traffic_fsm integration were functioning properly and were consistent with the behaviour we observed in Lab 3.

The issues appeared only after adding the UART components. Although the full design compiled without errors and all VHDL files synthesized successfully, no debug messages appeared on PuTTY during hardware testing. This indicated that the problem was not a coding or syntax error, but rather a clock domain crossing design flaw.

Post-implementation analysis identified the root cause: uart_fsm.vhd directly uses the i_traffic_state signal for change detection without implementing a proper 2-stage synchronizer. This signal crosses from the 1 Hz traffic domain to the 50 MHz UART domain unsynchronized, creating metastability that prevents reliable state change detection. Without synchronization (sync1 <= i_traffic_state; sync2 <= sync1), the comparison between prev_trf and i_traffic_state becomes timing-dependent and unreliable, causing the UART FSM to never trigger message transmission. Additional contributing factors may include incorrect TxD/RxD pin assignments, baud rate timing mismatches, or top-level BDF wiring errors between uart_fsm and uart_core. However, the missing synchronizer definitively explains why no messages were transmitted, as the triggering mechanism itself was fundamentally flawed. This critical design oversight demonstrates the importance of rigorous clock domain crossing protocols in multi-clock systems.