Tutorial for Chapter 9 - MSI

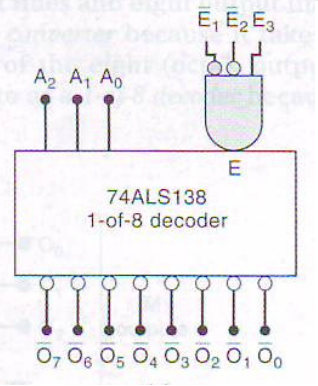
→ 9-1. Refer to Figure 9-3. Determine the levels at each decoder output for the following sets of input conditions.

(a) All inputs LOW

(b) All inputs LOW except E_3 = HIGH

(c) All inputs HIGH except $\overline{E}_1 = \overline{E}_2$ = LOW

(d) All inputs HIGH



→ 9-2. What is the number of inputs and outputs of a decoder that accepts 64 different input combinations?

→ 9-3. For a 74ALS138, what input conditions will produce the following outputs:

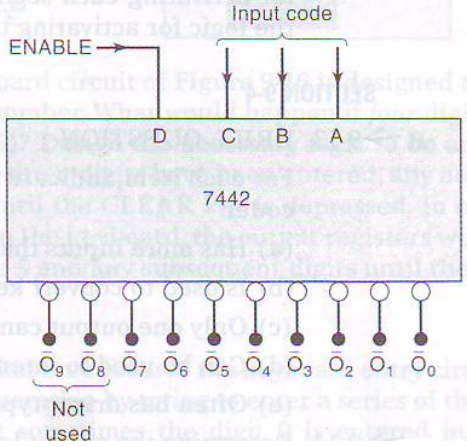
(a) LOW at $\overline{O}_6$

(b) LOW at $\overline{O}_3$

(c) LOW at $\overline{O}_5$

(d) LOW at $\overline{O}_0$ and $\overline{O}_7$, simultaneously

→ 9-7. The 7442 decoder of Figure 9-5 does not have an ENABLE input. However, we can operate it as a 1-of-8 decoder by not using outputs $\overline{O}_8$ and $\overline{O}_9$ and by using the D input as an ENABLE. This is illustrated in Figure 9-71. Describe how this arrangement works as an enabled 1-of-8 decoder, and state how the level on D either enables or disables the outputs.



CHAPTER 9

→ 9-1. (a) All HIGH (b) $\overline{O}_0$ = LOW (c) $\overline{O}_7$ = LOW (d) All HIGH

→ 9-2. Six inputs, 64 outputs

→ 9-3. (a) $E_3E_2E_1 = 100$; $[A] = 110$ (b) $E_3E_2E_1 = 100$; $[A] = 011$ (c) $E_3E_2E_1 = 100$; $[A] = 101$ (d) No input conditions

→ 9-7. Enabled when $D = 0$

→9-13. DRILL QUESTION

For each item, indicate whether it is referring to a decoder or an encoder.

(a) Has more inputs than outputs.

(b) Is used to convert key actuations to a binary code.

(c) Only one output can be activated at one time.

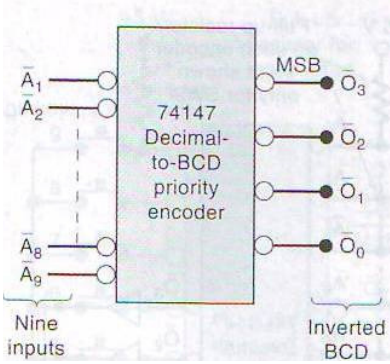
(d) Can be used to interface a BCD input to an LED display.

(e) Often has driver-type outputs to handle large I and V.

→9-13. (a), (b) Encoder (c), (d), (e) Decoder

→9-14. Determine the output levels for the 74147 encoder when $\overline{A}_8 = \overline{A}_4 = 0$ and all other inputs are HIGH.

→9-14. 0111



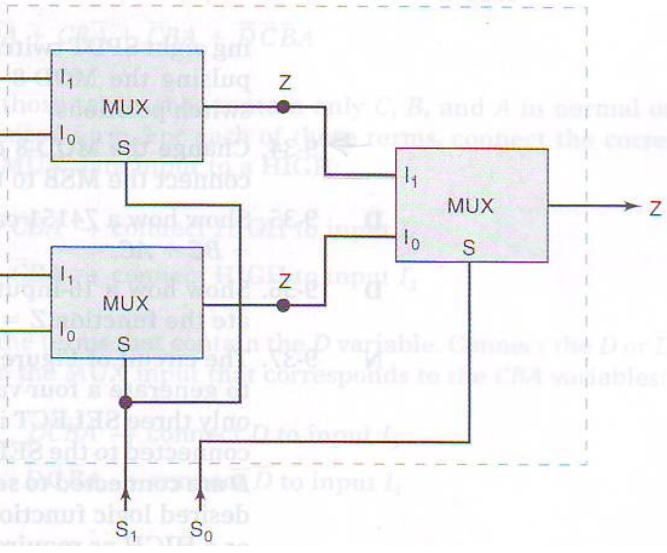
$\overline{A}_1$	$\overline{A}_2$	$\overline{A}_3$	$\overline{A}_4$	$\overline{A}_5$	$\overline{A}_6$	$\overline{A}_7$	$\overline{A}_8$	$\overline{A}_9$	$\overline{O}_3$	$\overline{O}_2$	$\overline{O}_1$	$\overline{O}_0$
1	1	1	1	1	1	1	1	1	1	1	1	1
X	X	X	X	X	X	X	X	0	0	1	1	0
X	X	X	X	X	X	X	0	1	0	1	1	1
X	X	X	X	X	X	0	1	1	1	0	0	0
X	X	X	X	X	0	1	1	1	1	0	0	1
X	X	X	X	0	1	1	1	1	1	0	1	0
X	X	X	0	1	1	1	1	1	1	0	1	1
X	X	0	1	1	1	1	1	1	1	1	0	0
X	0	1	1	1	1	1	1	1	1	1	0	1
0	1	1	1	1	1	1	1	1	1	1	1	0

X = either 0 or 1

clock.

9-29. The circuit in Figure 9-75 uses three two-input multiplexers (Figure 9-19). Determine the function performed by this circuit.

FIGURE 9-75 Problem 9-29.



→9-29. A 4-to-1 MUX

→9-33. Figure 9-76 shows how a multiplexer can be used to generate logic waveforms with any desirable pattern. The pattern is programmed us-

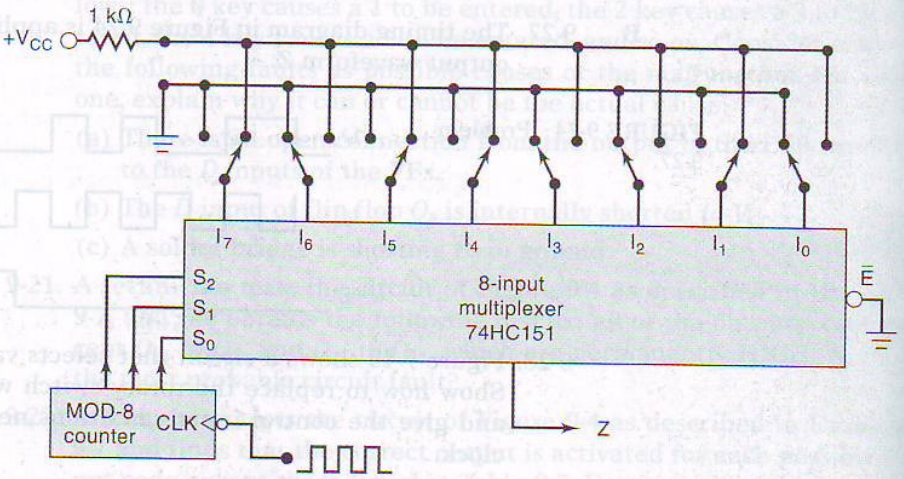


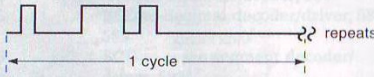
FIGURE 9-76 Problems 9-33 and 9-34.

ing eight SPDT switches, and the waveform is repetitively produced by pulsing the MOD-8 counter. Draw the waveform at Z for the given switch positions.

→9-33.

→9-34. Change the MOD-8 counter in Figure 9-76 to a MOD-16 counter, and connect the MSB to the multiplexer $\overline{E}$ input. Draw the Z waveform.

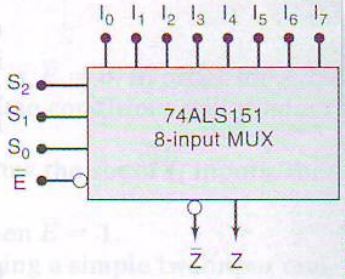
→9-34.



D→9-35. Show how a 74151 can be used to generate the logic function $Z = AB + BC + AC$.

→9-35.

Inputs				Outputs	
$\overline{E}$	S_2	S_1	S_0	$\overline{Z}$	Z
H	X	X	X	H	L
L	L	L	L	$\overline{I}_0$	I_0
L	L	L	H	$\overline{I}_1$	I_1
L	L	H	L	$\overline{I}_2$	I_2
L	L	H	H	$\overline{I}_3$	I_3
L	H	L	L	$\overline{I}_4$	I_4
L	H	L	H	$\overline{I}_5$	I_5
L	H	H	L	$\overline{I}_6$	I_6
L	H	H	H	$\overline{I}_7$	I_7



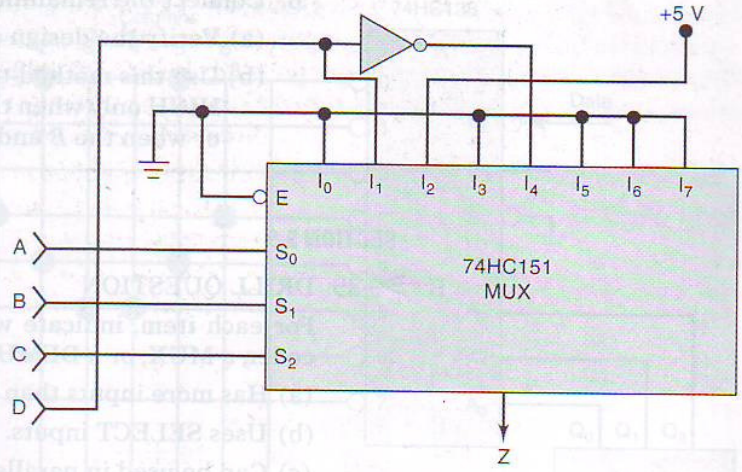
(c)

A	B	C	
0	0	0	$0 \Rightarrow I_0$
0	0	1	$0 \Rightarrow I_1$
0	1	0	$0 \Rightarrow I_2$
0	1	1	$1 \Rightarrow I_3$
1	0	0	$0 \Rightarrow I_4$
1	0	1	$1 \Rightarrow I_5$
1	1	0	$1 \Rightarrow I_6$
1	1	1	$1 \Rightarrow I_7$

N →9-37. The circuit of Figure 9-77 shows how an eight-input MUX can be used to generate a four-variable logic function, even though the MUX has only three SELECT inputs. Three of the logic variables A, B, and C are connected to the SELECT inputs. The fourth variable D and its inverse $\overline{D}$ are connected to selected data inputs of the MUX as required by the desired logic function. The other MUX data inputs are tied to a LOW or a HIGH as required by the function.

(a) Set up a truth table showing the output Z for the 16 possible combinations of input variables.

oblems



(b) Write the sum-of-products expression for Z and simplify it to verify that

$$Z = \overline{C}B\overline{A} + D\overline{C}B\overline{A} + \overline{D}C\overline{B}\overline{A}$$

→9-37. Z = HIGH for $DCBA$ = 0010, 0100, 1001, 1010.

→9-39. DRILL QUESTION

For each item, indicate whether it is referring to a decoder, an encoder, a MUX, or a DEMUX.

(a) Has more inputs than outputs.

(b) Uses SELECT inputs.

(c) Can be used in parallel-to-serial conversion.

(d) Produces a binary code at its output.

(e) Only one of its outputs can be active at one time.

(f) Can be used to route an input signal to one of several possible outputs.

(g) Can be used to generate arbitrary logic functions.

→9-39. (a) Encoder, MUX (b) MUX, DEMUX
(c) MUX (d) Encoder (e) Decoder, DEMUX
(f) DEMUX (g) MUX