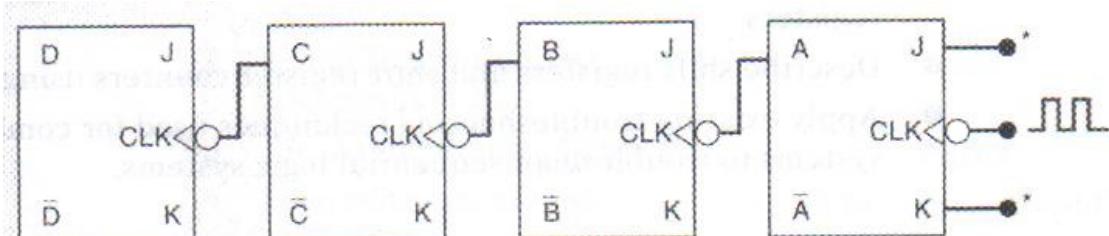


SECTIONS 7-1 AND 7-2

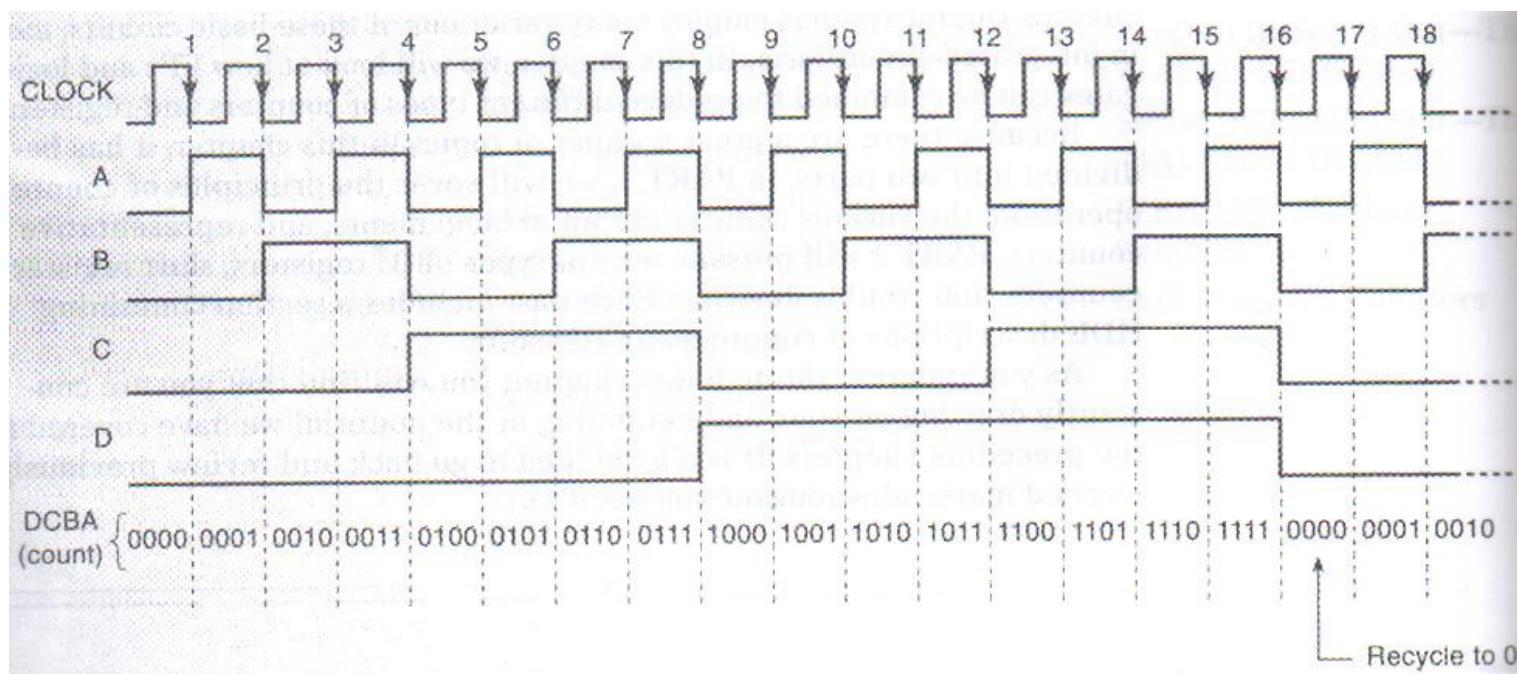
p.300

>7-1. Add another flip-flop, E, to the counter of Figure 7-1. The clock signal is an 8-MHz square wave.

- What will be the frequency at the *E* output? What will be the duty cycle of this signal?
- Repeat (a) if the clock signal has a 20 percent duty cycle.
- What will be the frequency at the *C* output?
- What is the MOD number of this counter?



*All J and K inputs assumed to be 1.



7-2. Construct a binary counter that will convert a 64-kHz pulse signal into a 2-kHz square wave.

7-3. Assume that a five-bit binary counter starts in the 00000 state. What will be the count after 144 input pulses?

7-4. Use J-K flip-flops and any other necessary logic to construct a MOD-24 asynchronous counter.

- 7-7. Change the inputs to the NAND gate of Figure 7-7 so that the counter divides the frequency by 50. Repeat for a frequency division of 100.

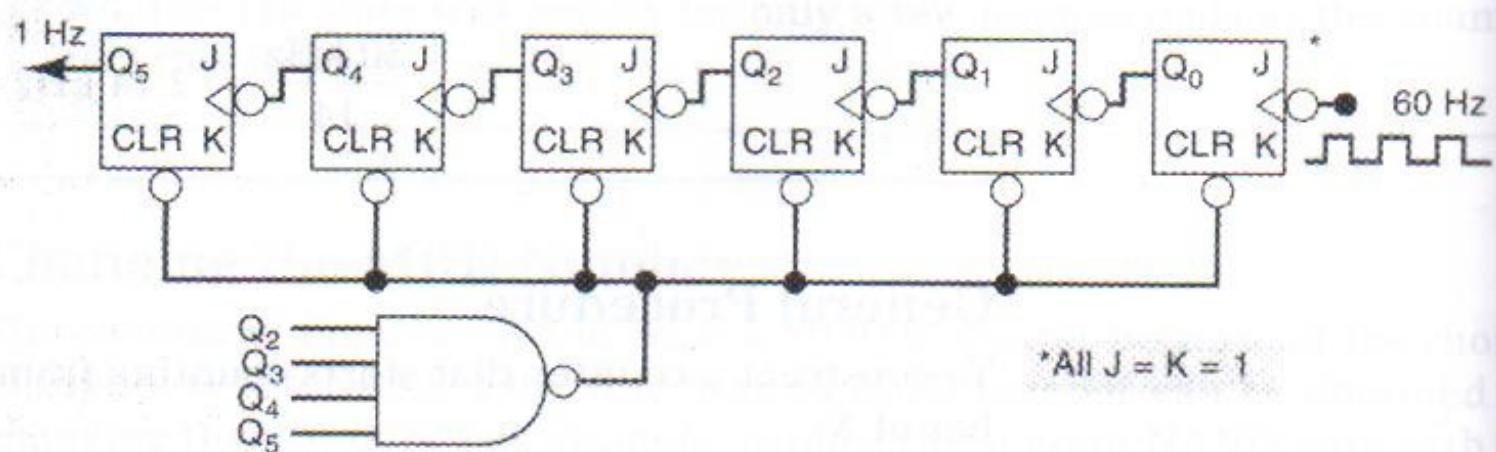


FIGURE 7-7 MOD-60 counter.

- 7-9. In Figure 7-8, connect Q_0 to \overline{CP}_1 and MR_1 , and connect Q_3 to MR_2 . If 180-kHz pulses are applied to \overline{CP}_0 , determine the following: (a) the count sequence; (b) MOD number; (c) frequency at Q_3 .

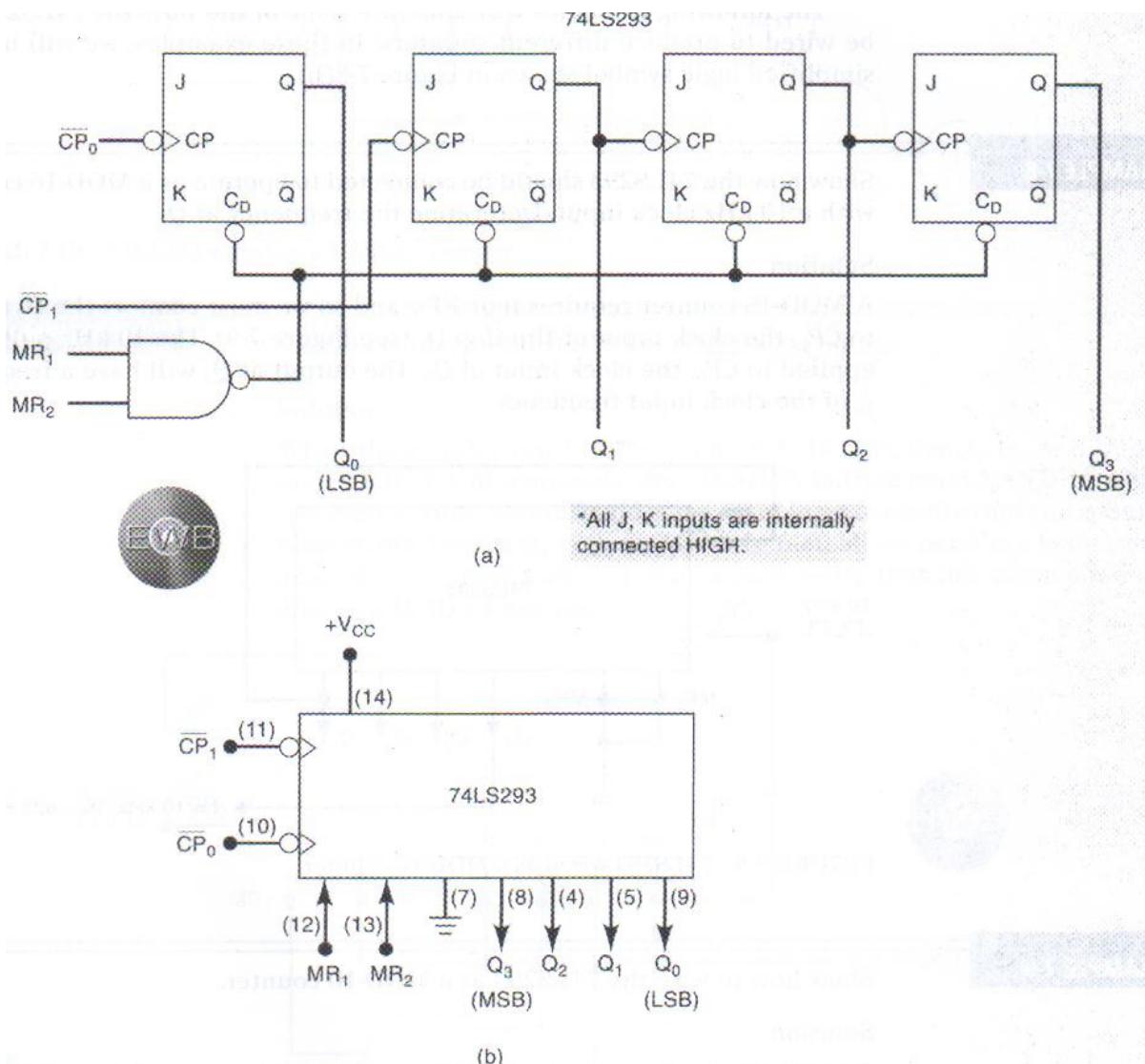
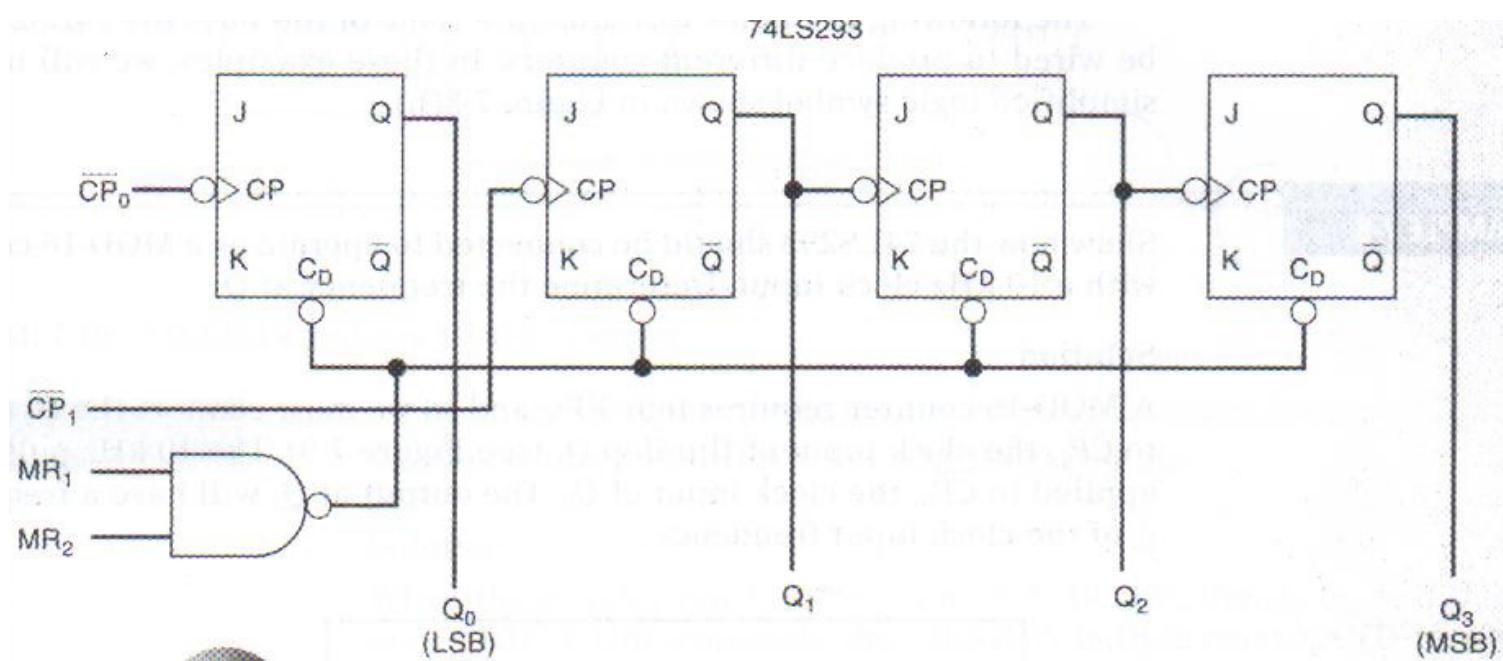


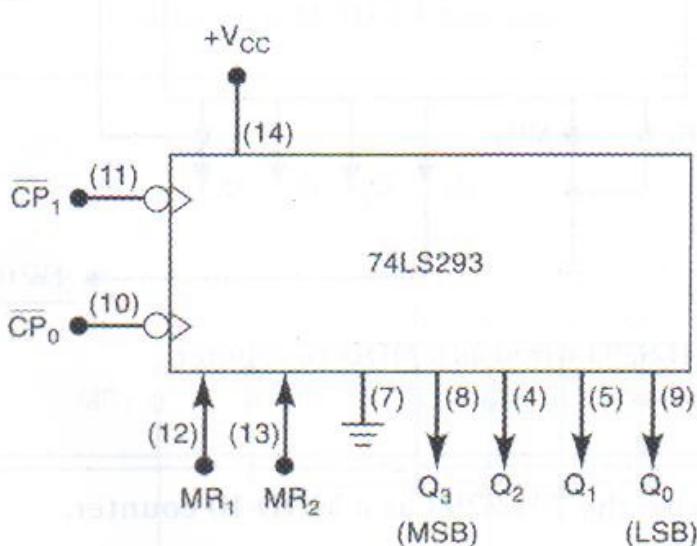
FIGURE 7-8 (a) Logic diagram for 74LS293 asynchronous counter IC; (b) block symbol, with pin numbers in parentheses.

7-10. Show how a 74LS293 counter can be used to produce a 1.2-kpps output from an 18-kpps input.



(a)

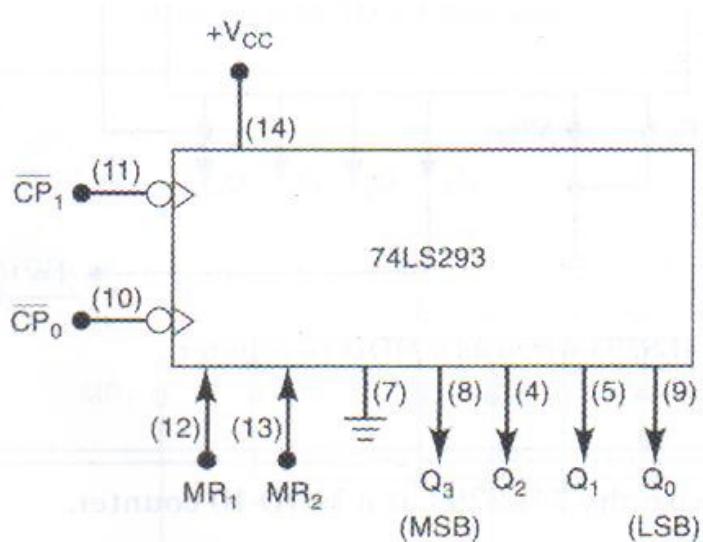
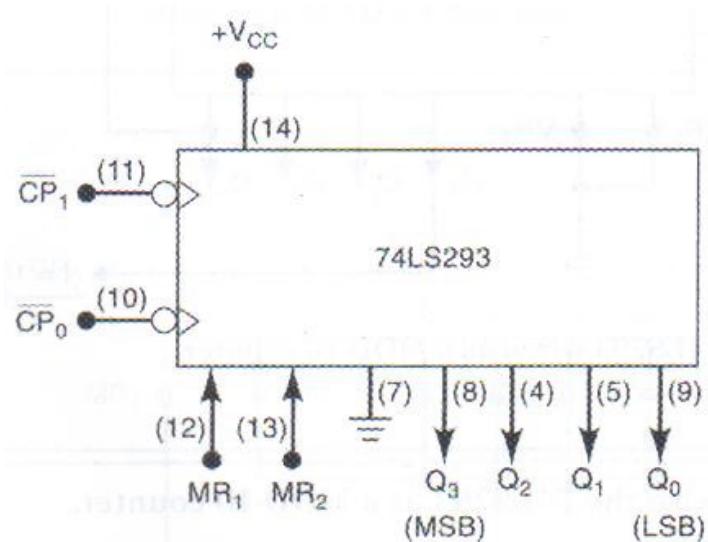
*All J, K inputs are internally connected HIGH.



(b)

FIGURE 7-8 (a) Logic diagram for 74LS293 asynchronous counter IC; (b) block symbol, with pin numbers in parentheses.

7-11. Show how two 74LS293s can be connected to divide an input frequency by 60 while producing a symmetrical square-wave output.



C \rightarrow 7-12. Determine the frequency at output X in Figure 7-81.

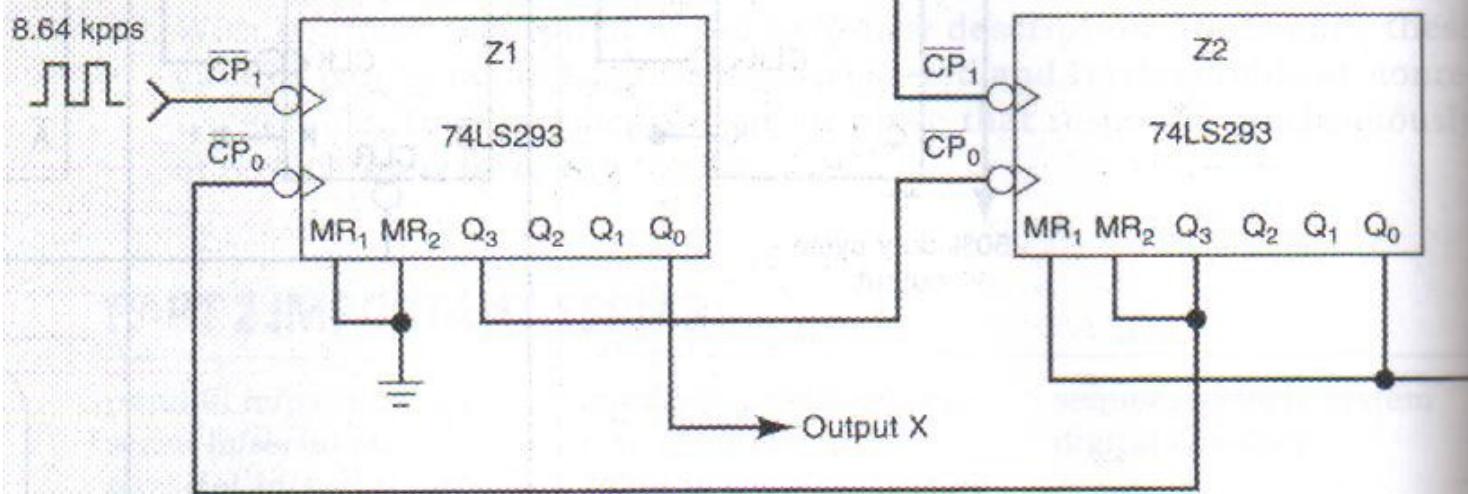


FIGURE 7-81 Problems 7-12 and 7-69.

- >7-14. (a) Draw the diagram for a MOD-16 *down* counter.
(b) Construct the state transition diagram.
(c) If the counter is initially in the 0110 state, what state will it be in after 37 clock pulses?

7-30. Draw the AND gates necessary to decode the 10 states of the BCD counter of Figure 7-6(b).

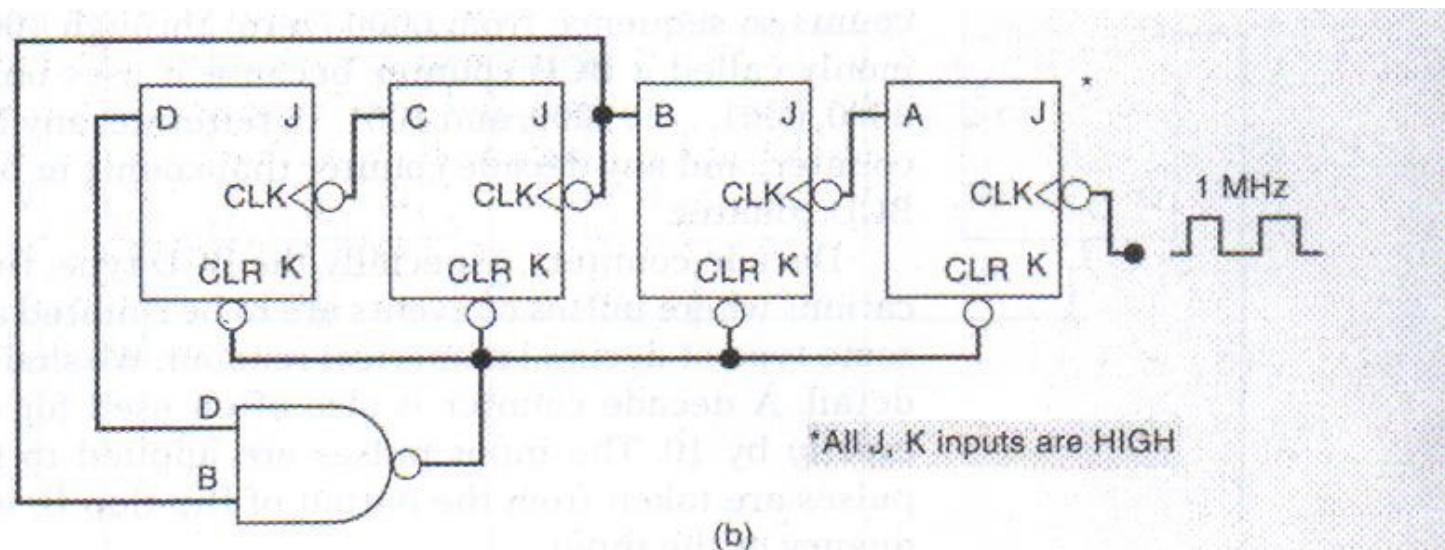
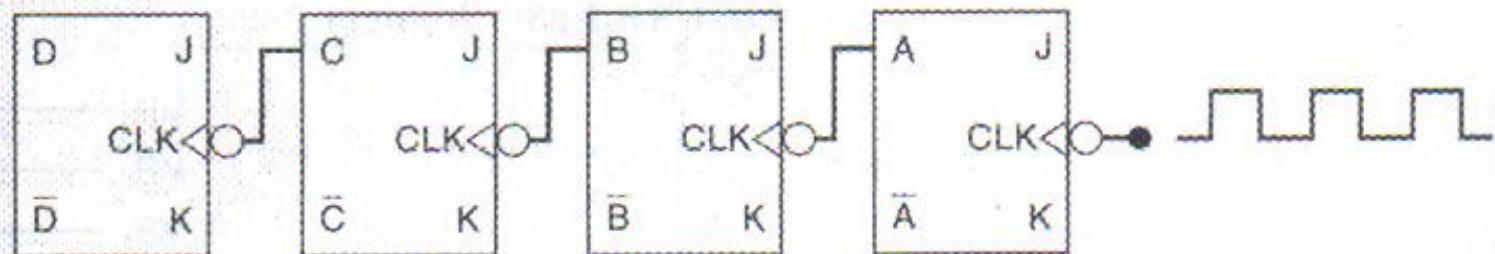


FIGURE 7-6 (a) MOD-14 ripple counter; (b) MOD-10 (decade) ripple counter.

7-31. Figure 7-86 shows a ripple counter being used to help generate control waveforms. Control waveforms 1 and 2 can be used for many purposes, including control of motors, solenoids, valves, and heaters. Determine the control waveforms, assuming that all FFs are initially LOW. Ignore decoding glitches. Assume that clock frequency = 1 kpps.



All J, K
inputs = 1

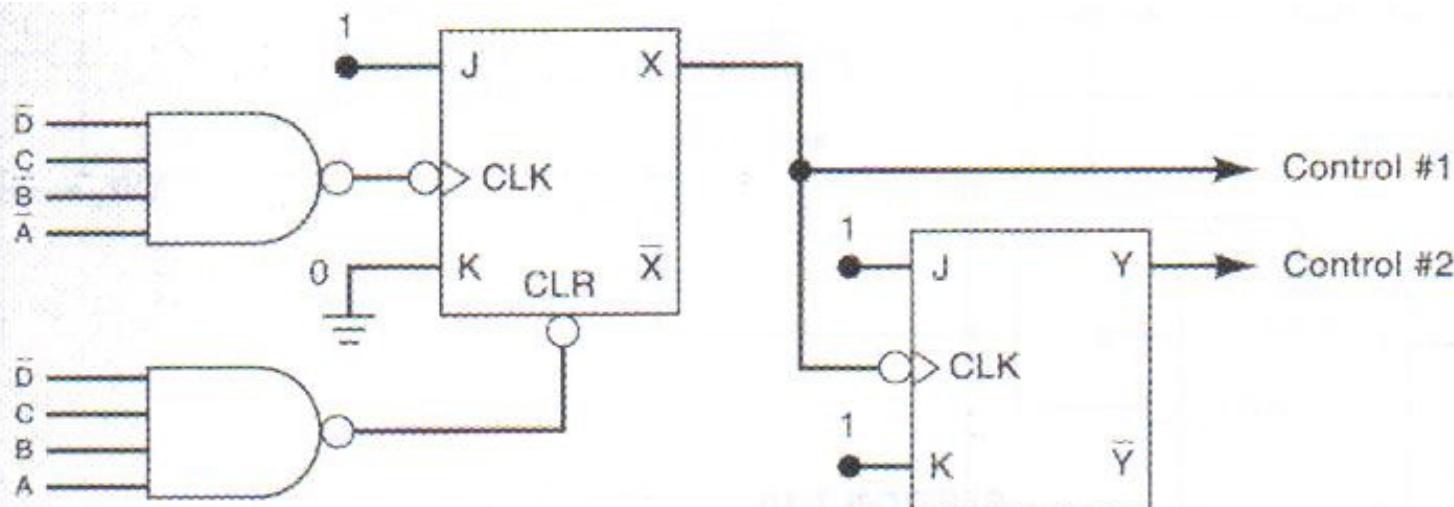


FIGURE 7-86 Problem 7-31.

7-35. How many cascaded BCD counters are needed to be able to count up to 8000? How many FFs does this operation require? Compare this with the number of FFs required for a normal binary counter to count up to 8000. Even though it uses more FFs, why is the cascaded BCD method used?

7-55. Suppose a 74ALS174 is connected as follows:

$$\overline{MR} = \text{HIGH}; Q_5 \rightarrow D_2; Q_4 \rightarrow D_1; Q_3 \rightarrow D_0$$

$$D_5 = D_3 = \text{HIGH}; D_4 = \text{LOW}$$

Assume all FFs have a zero hold-time and are initially LOW.

- Determine the states of each FF after a single pulse is applied to CP .
- Repeat for a second clock pulse.

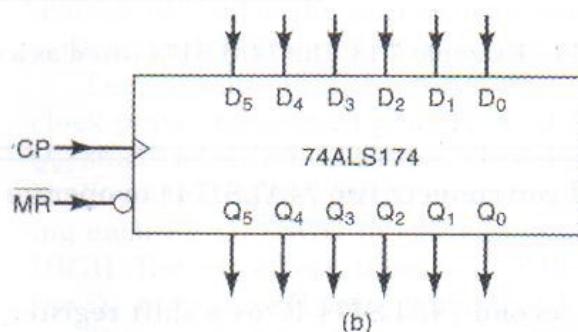
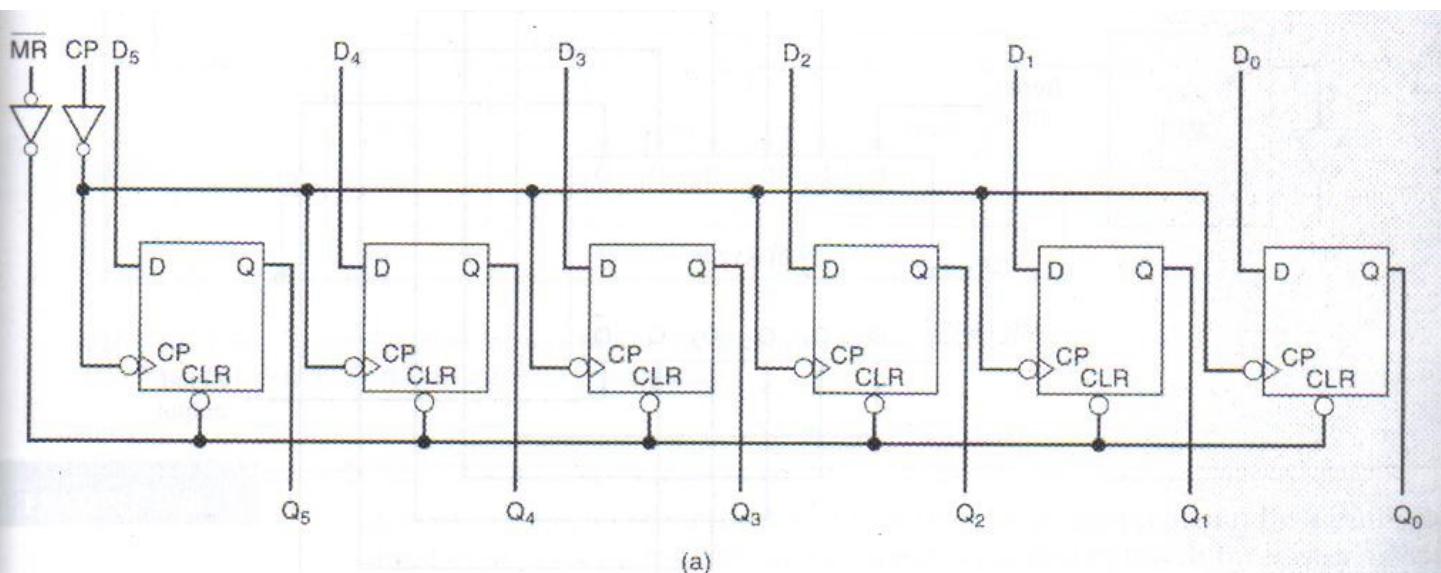


FIGURE 7-52 (a) Circuit diagram of the 74ALS174; (b) logic symbol. (Courtesy of Fairchild, a Schlumberger company)

7-57. Show how the 4731B chip can be connected as a 256-bit shift register.

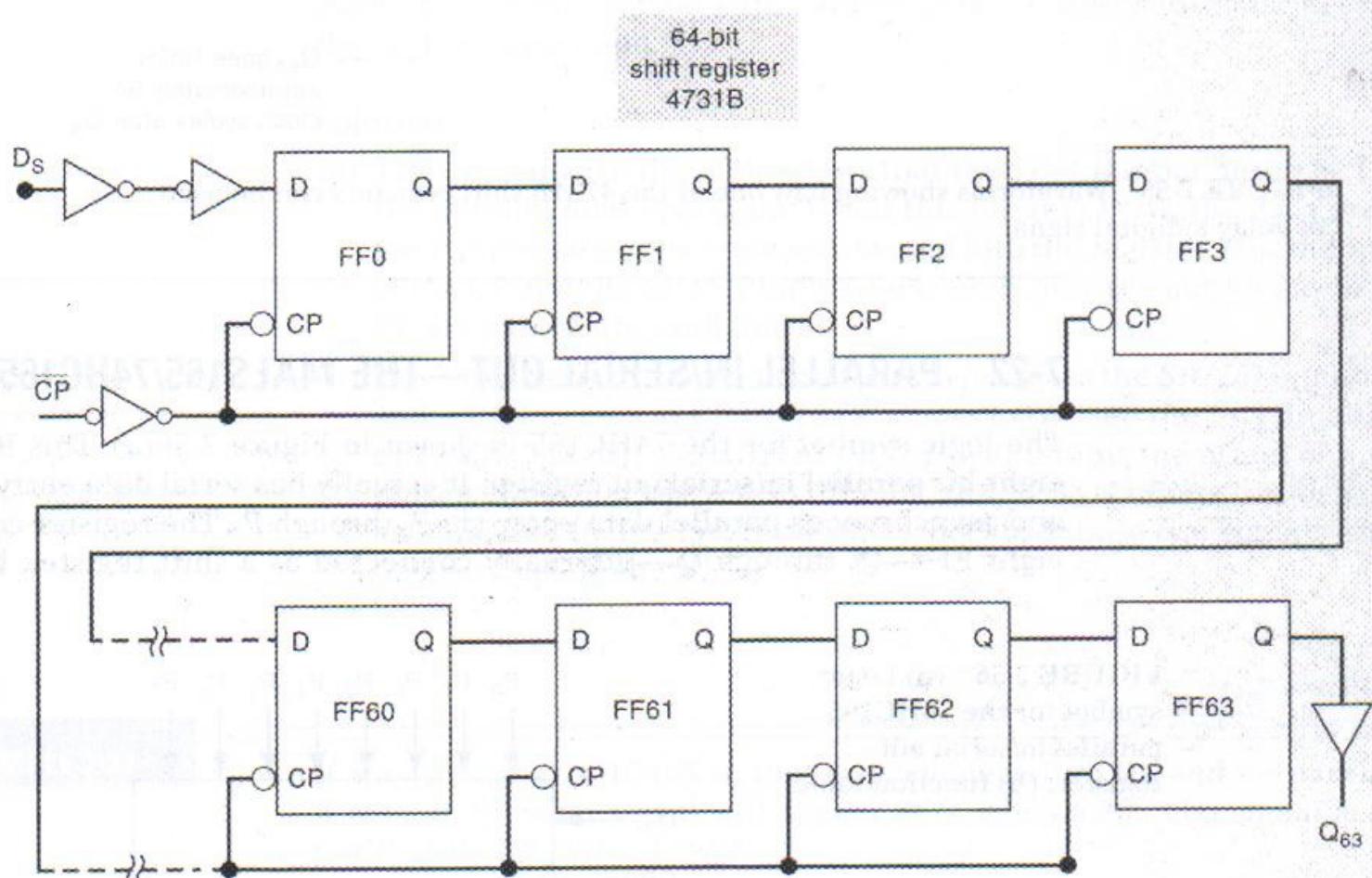
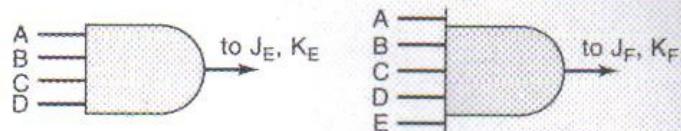


FIGURE 7-54 Logic diagram for one of four 64-bit shift registers on a 4731B.
(Courtesy of Fairchild, a Schlumberger company)

7-18. (a) Add two FFs (E and F) to Figure 7-17. Connect AND gates below to appropriate FF inputs.
 (b) 33 MHz



CHAPTER 7

7-1. (a) 250 kHz; 50% (b) Same as (a)

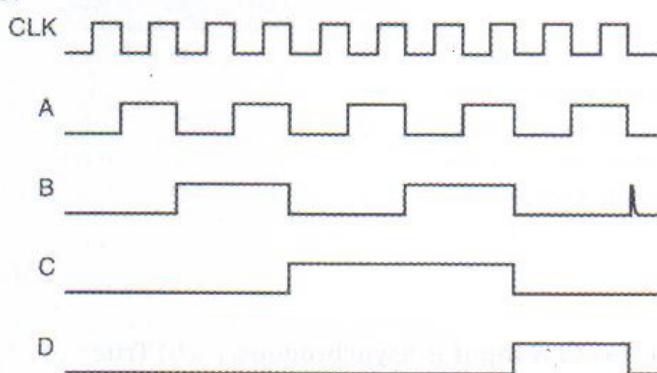
(c) Frequency at $C = 1$ MHz (d) 32

7-2. 2 kHz

7-3. 10000_2

7-4. Five FFs are required: Q_0-Q_4 with Q_4 as the MSB. Connect Q_3 and Q_4 outputs to a NAND gate whose output is connected to all CLRs.

7-5.

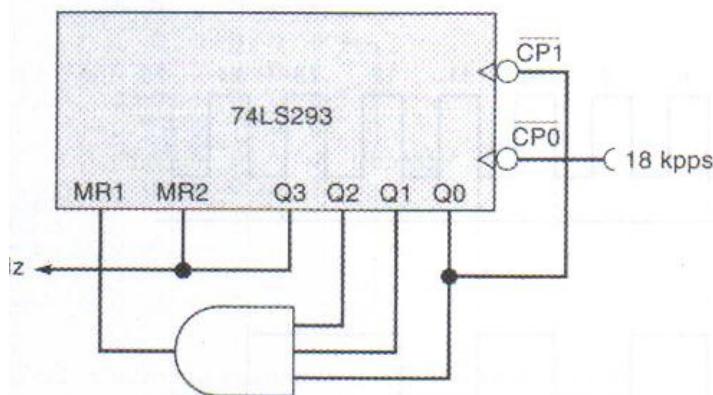


7-6. Glitch at B output on fourteenth NGT of the clock

7-7. Connect Q_5 , Q_4 , and Q_1 for MOD-50. A MOD-100 cannot be constructed without more logic.

7-8. (b) 000, 001, 010, 100, 101, 110, and repeats

7-10.



7-11. A MOD-15 (from Problem 7-10) driving a MOD-4

7-12. 60 Hz

7-14. (c) 0001

7-15. 100, 011, 010, 001, 000, and repeats

7-16. 1000 and 0000 states never occur.

7-17. (a) 12.5 MHz (b) 8.33 MHz

7-19. 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001, and repeats

7-21. The counter FFs will switch between the 000 and 111 states on each clock pulse.

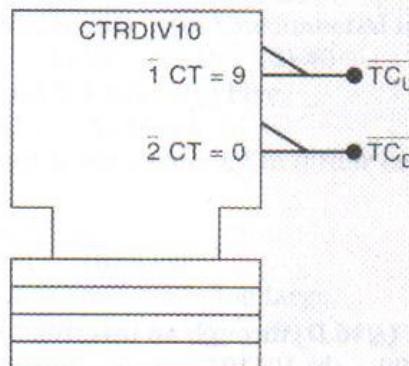
7-23. (d) Z will not be cleared and the timer cannot be restarted.

7-24. Change the parallel data input to 1010.

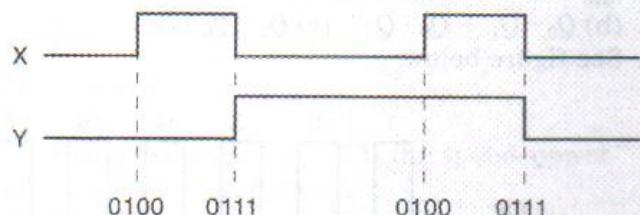
7-25. Nine

7-27. (a) Ten (b) Clears counter to 0000 (c) Sets counter to 1001 (d) Up (e) Connect Q_0 to CP_1 and clock signal to CP_0 ; ground MR_1 , MR_2 , MS_1 , and MS_2 . (f) Connect clock signal to CP_1 ; connect Q_3 to CP_0 ; ground all MR and MS inputs.

7-28.



7-31.



7-33. (a) When the counter goes from 0111 to 1000

7-34. 12 FFs

7-35. Four; sixteen; thirteen

7-36. (a) $J_A = BC$, $K_A = 1$, $J_B = CA + \bar{C}A$, $K_B = 1$, $J_C = \bar{A}B$, $K_C = B + \bar{A}$

(b) $J_A = BC$, $K_A = 1$, $J_B = K_B = 1$, $J_C = K_C = B$

7-37. $J_A = K_A = 1$, $J_B = K_B = \bar{A}$, $J_C = K_C = \bar{A}B$, $J_D = K_D = \bar{A}BC$

7-38. $J_A = K_A = 1$; $J_B = K_B = AD + \bar{A}\bar{D}$; $J_C = K_C = ABD + \bar{A}\bar{B}\bar{D}$