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2020/2021 SEMESTER 1 EXAMINATION

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| Diploma in Electrical & Electronic Engineering DEEE 1st Year FT  Diploma in Computer Engineering DCPE 1st Year FT  Diploma in Aerospace Electronics DASE 1st Year FT |
| **DIGITAL ELECTRONICS II** Time Allowed : 2 hours |

**Instructions to Candidates**

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of **THREE** sections:

Section A - 10 Multiple Choice Questions, 2 marks each.

Section B - 6 Short Questions, 10 marks each.

Section C - 1 Long Question of 20 marks.

3. Answer **ALL** questions in the accompanying Answer Booklet. Start each question in Sections B and C on a new page.

4. This Examination Paper consists of 9 pages

5. Your admission number and module class must be entered in the box provided on the cover page of your Answer Booklet.

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

###### **Section A** Multiple Choice Questions (20 Marks)

**A1.** Refer to Figure A1**,** what is the output frequency at Flip-Flop (F/F) H if the CLK input to F/F A is 128 kHz and the counter is a naturally resetting type?

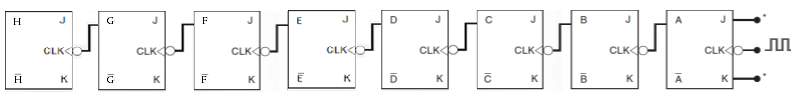
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Figure A1

All J and K inputs are tied to Vcc and PRESET inputs are disabled.

(a) 250 Hz

(b) 500 Hz

(c) 1000 Hz

(d) 2000 Hz

**A2.** Refer to the Figure A2, what are the outputs at DCBA of the counter after 60 clock pulses if the counter starts from 0000?

Figure A2



All J and K inputs are tied to Vcc and PRESET and CLEAR inputs are disabled.

(a) 1001

(b) 1010

(c) 1011

(d) 1100

**A3.** A shift register circuit with **one** data input and **many** data output is a \_\_\_\_\_\_\_\_\_.

(a) serial-in, serial-out shift register

(b) parallel-in, serial-out shift register

(c) serial-in, parallel-out shift register

(d) parallel-in, parallel-out shift register

**A4.** What is the range of decimal values that can be represented by a **16-bit** (including the sign bit) 2’s-complement system?

(a) -3276810 to +3276710

(b) -3276710 to +3276810

(c) -3276810 to +3276810

(d) -3276710 to +3276710

**A5.** How many 7483 (4-bit) parallel adder ICs are required to construct a parallel adder that can add two sets of 16-bit numbers?

(a) 110

(b) 210

(c) 310

(d) 410

**A6.** The parameter that defines how much electrical noise a digital IC can tolerate is:

1. Fan-out
2. Noise Margin

(c) Speed-power product

(d) Standard unit load

**A7.** What is the correct mathematical expression to calculate the average power consumed by a TTL digital IC?

(a) (ICCH + ICCL)**/**2 \* VCC

(b) (IOL + IOH)**/**2 \* VCC

(c) (IOH + ICCH)**/**2 \* VCC

(d) (IOL + ICCL)**/**2 \* VCC

**A8.**  A Multiplexer accepts data from

1. many input lines and transfers it to one of the SELECT lines.
2. many input lines and transfers it to multiple SELECT lines.
3. many input lines and transfers it to many different output lines.
4. many input lines and transfers it to one output line.

**A9.** A 74147 BCD priority encoder is connected as shown in Figure A9. What decimal digit value will be represented at Z3 to Z0?

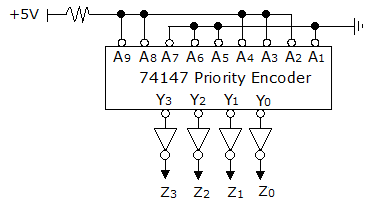


Figure A9

(a) 710 (b) 810 (c) 910 (d) 1010

**A10.** How many SELECT lines are there in a 1-to-64 demultiplexer?

(a) 1

(b) 6

(c) 8

(d) 64

**Section B** Short Questions (60 marks)

**B1** (a) Use the 8 bits (including the sign bit) 2’s-complement system to perform the

following addition:

Add +6910 to -3810 (5 marks)

1. Express the following numbers in BCD format and hence, perform the addition

of the numbers using BCD arithmetic.

Add +7910 to +2110 (5 marks)

NB: **All workings** for question B1 must be **shown or marks** will **not** be awarded.

**B2.** Figure B2 shows is a cascade of 4 Full Adder units.



Figure B2

1. If A3 A2 A1 A0 = 0 0 1 1 and, B3 B2 B1 B0 = 0 1 0 0, respectively,

what will be the binary value of the outputs Cout, S3 S2 S1 S0 if Cin = 0? (4 marks)

1. If A3 A2 A1 A0 = 0 1 1 1 and, B3 B2 B1 B0 = 1 1 0 1, respectively,

what will be the binary value of the outputs Cout, S3 S2 S1 S0 if Cin = 1?

(4 marks)

(c) How many magnitude bits (without counting the sign bit) are there in a parallel Adder that is built with twenty (20) Full Adder units for 2’s-complement system addition?

(2 marks)

**B3.** The 74LS93 is a 4 bit Asynchronous Counter IC that permits flexible configuration.

The symbol and internal circuitry for the 74LS93 is shown in the Figure B3.

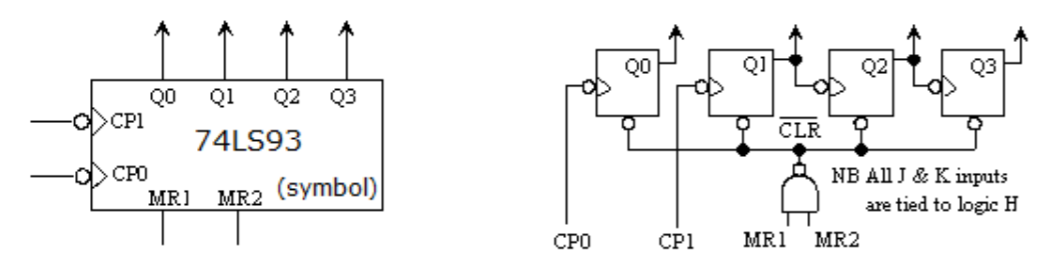


Figure B3

(a) Show how you would configure the 74LS93 IC to count upward as a Mod-12 counter. Draw the circuit in your answer booklet using the 74LS93 symbol, ensuring that all inputs and outputs are clearly labelled. (5 marks)

1. The Mod-12 counter starts from the binary state 0101 and 1322 clock cycles are applied to its clock input. At the end of which, what will be the state of the counter in binary? (5 marks)

**B4.** The 74151 is an 8-to-1 multiplexer. Figure B4.1 shows the symbol of this multiplexer.

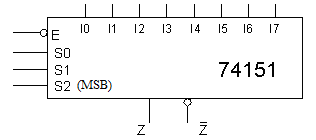


Figure B4.1

(a) Show how a 74151 IC can be connected as a 4-to-1 multiplexer. In your diagram, label the data inputs as D0 D1 D2 D3 and the select inputs as A1 A0, where A0 is the LSB. Unused inputs should be labelled as N.C. (5 marks)

(b) Refer to the circuit in Figure B4.2.

Draw a truth table with B, A as inputs and  as outputs.

Hence, determine the boolean expressions at the outputs.

What generic logic functions are the above outputs representing?

(5 marks)

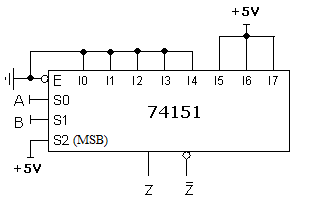
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Figure B4.2

**B5** (a) The 74138 is a **3-to-8** decoder device and has a symbol as shown in Figure B5.1.

What logic levels are required at the E3, E2 and E1 inputs to enable the decoder?

Hence, show how you would connect the 74138 to function as a 2-to-4 decoder.

Any unconnected inputs/outputs should be labelled as N.C.

(5 marks)

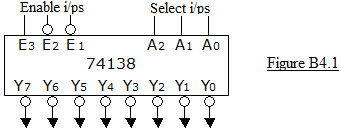


Figure B5.1

1. Refer to the circuit in Figure B5.2.

What values (‘1’, ‘0’ or ‘X’) should be applied to A9 to A1 in order to produce the given outputs at the inverters?

(5 marks)

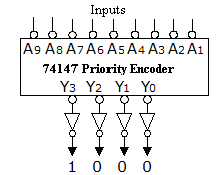


Figure B5.2

**B6** Table B6 lists the typical values of the AC and DC parameters (characteristics) for three different logic families of the 7408 Quad 2-input AND IC.

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| **Parameter** | **Unit** | **Device A** | **Device B** | **Device C** |
| Vcc | V | 5 | 5 | 5 |
| VIH (min) | V | 2 | 2 | 2 |
| VIL (max) | V | 0**.**8 | 0**.**7 | 0**.**8 |
| VOH (min) | V | 2**.**4 | 2**.**7 | 2**.**5 |
| VOL (max) | V | 0**.**4 | 0**.**5 | 0**.**5 |
| IccH | mA | 12 | 2**.**4 | 10 |
| IccL | mA | 36 | 6**.**6 | 22 |
| tpLH | ns | 16 | 10 | 2 |
| tpHL | ns | 14 | 9 | 2 |

Table B6

(a) Calculate the average power consumption **per gate** for Device **A**.

(4 marks)

(b) Which device can operate at the highest operating frequency?

(2 marks)

(c) Which device has the highest value of output voltage for logic High and what is the value of this voltage?

(2 marks)

(d) Calculate the High-state noise margin VNH for Device B.

(2 marks)

**Section C** Long Question (20 marks)

**C1** Refer to the circuit in Figure C1.1.

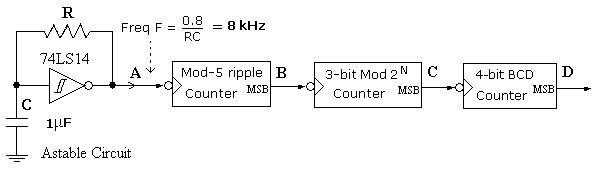


Figure C1.1

1. Calculate the value of R in the astable multivibrator circuit in order to produce an

8 kHz frequency, given the value of C as indicated.

(3 marks)

(b) Which counter has the highest MOD number? What is the overall MOD number of the three cascaded counters?

(3 marks)

1. What are the frequencies at the counter outputs B, C and D?

(3 marks)

1. Figure C1.2 shows the symbol and internal circuit of the 7493 counter. Draw a diagram with the 7493 symbol to indicate how a BCD counter can be constructed. Any unconnected inputs/outputs should be marked as N.C.

(5 marks)

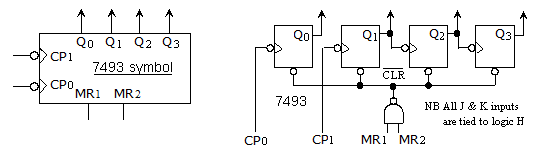


Figure C1.2

(e) Determine the duty cycle of the signal at output D. (3 marks)

(f) Show how you can rearrange the three counters to obtain a 50% duty cycle at D.

(3 marks)

**------------- End of Paper ------------**