| **No** | **SOLUTION** | **MARKS** | **TOTAL MARKS** |
| --- | --- | --- | --- |
|  | **SECTION – A (10 MCQ, 2 marks each)** A1 (b)  A2 (d)  A3 (c)  A4 (a)  A5 (d)  A6 (b)  A7 (a)  A8 (d)  A9 (a)  A10 (b) |  | 20 |

| **No** | **SOLUTION** | **MARKS** | **TOTAL MARKS** |
| --- | --- | --- | --- |
| **B1**  (a)  (b) | **SECTION – B (10 marks each)** ADD +6910 to -3810  sign 64 32 16 8 4 2 1  **+38 = 0 0 1 0 0 1 1 0**  **- 38 = 1 1 0 1 1 0 1 0**  **+69 = 0 1 0 0 0 1 0 1**  +31 **=  ~~1~~ 0 0 0 1 1 1 1 1**  ADD +7910 to +2110  12 11 10 9 8 7 6 5 4 3 2 1  **+ 79 = 0 0 0 0 0 1 1 1 1 0 0 1**  **+ 21 = 0 0 0 0 0 0 1 0 0 0 0 1**  **0 0 0 0 1 0 0 1 1 0 1 0**  **1 1 0**  **= 0 0 0 0 1 0 1 0 0 0 0 0**  **= 1 1 0 \_\_\_\_\_**  **+**100 **= 0 0 0 1 0 0 0 0 0 0 0 0 (BCD)** | 2  1  2    1  1  1  1  1 | 10 |

| **No** | **SOLUTION** | **MARKS** | **TOTAL MARKS** |
| --- | --- | --- | --- |
| **B2**  (a)  (b)  (c) | Cout S3 S2 S1 S0 = 0 0 1 1 12  Cout S3 S2 S1 S0 = 1 0 1 0 12    19 | 4  4  2 | 10 |

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **No** | **SOLUTION** | **MARKS** | | **TOTAL MARKS** | |
| **B3**  (a)  (b) | Indicating correct clock input Indicating correct LSB and MSB outputs – (2 marks)  Connection of Q0 to CP1 – (1 mark)  Correct feedback (MR1 MR2) connections to outputs – (2 marks)  Number of rounds for MOD-12 Counter after 1322 clock cycles  = 1322/12 = 110.167 rounds  After 110 rounds, the number of clock cycles more  =0.167 x 12 = 2 clock pulses  So ,the output values will be 0101 + 0010 = 0111 | 5  2  1  2 | | 10 | |
|  | **SOLUTION** | | **MARKS** | | **TOTAL MARKS** | |
| **B4**  (a)  (b) | NB: Marks distribution as shown.  Enabled E can be shown grounded (1 mark).  Accept other possible solutions on how the select inputs are utilized.  For example, if S2 is tied to +5V instead, then I4 I5 I6 I7 will be used instead and I0 to I3 will be N.C. instead.    Generic names of function is **OR** for function **Z**  And for **Not\_Z** it is **NOR** | | 5  1  1  1  1  1 | | 10 | |

1

1

| **No** | **SOLUTION** | | **MARKS** | | **TOTAL MARKS** | |
| --- | --- | --- | --- | --- | --- | --- |
| **B5**  (a)  (b) | To enable the decoder, enable inputs must be:  E1 = 0 E2 = 0 and E3 = 1    Marks Distribution  1 mark for grounding A2  1 mark for indicating N.C. to 4 o/ps  1 mark for correct labelling of select i/ps and o/ps  Accept other possible solutions for 1-to-4 decoder  For BCD code of 1000, input A8 must be activated  Being a priority encoder, this means A9 must be High.  But A7 to A1 being lower than 7 are don’t cares or Xs.  Thus A8 = 0  A9 = 1  A7 to A1 = X (don’t care) | | 2  3  2  2  1 | | 10 | |
| **o** | **SOLUTION** | **MARKS** | | **TOTAL MARKS** | |
| **B6**  (a)  (b)  (c)  (d) | Power consumption for Device A  = Vcc \* (ICCH + ICCL)/2  = 5 \* ( 12 + 36) / 2 mW  = 120 mW  Power dissipation per gate = 120/4 = 30 mW  Device C has the highest operating frequency as it has the lowest values of propagation delay.  Parameter VOH is required.  Device B has the highest VOH of 2.7V  VNH for device B = VOH -VIH  = 2.7 – 2.0  = 0.7V | 2  2  2  2  1  1 | | 10 | |

| **No** | **SOLUTION** | **MARKS** | **TOTAL MARKS** |
| --- | --- | --- | --- |
| **C1**  (a)  (b)  (c)  (d) | **SECTION – C (20 marks)**  = 8 kHz  Therefore R = 0.8/( 8000 \* 10-6) = 100 Ohms  The 4-bit BCD counter has the highest MOD number of 10.  Overall MOD number = 5 \* 8 \* 10 = 400  Frequency at B = 8000/5 = 1600 Hz  Frequency at C = 1600/8 = 200 Hz  Frequency at D = 200/10 = 20 Hz  BCD Counter:    Marks distribution  Use of 4 flip-flops = 1 mark  Correct CLK input = 1 mark  LSB and MSB = 1 mark,  Feedback from outputs to MR1 & MR2 = 2marks | 3  1  2  1  1  1  5 |  |
| **o** | **SOLUTION** | **MARKS** | **TOTAL MARKS** |
| (e)  (f) | The sequence of the mod-10 counter is as follows:   |  |  |  |  | | --- | --- | --- | --- | | **Q3** | Q2 | Q1 | Q0 | | **0** | 0 | 0 | 0 | | **0** | 0 | 0 | 1 | | **0** | 0 | 1 | 0 | | **0** | 0 | 1 | 1 | | **0** | 1 | 0 | 0 | | **0** | 1 | 0 | 1 | | **0** | 1 | 1 | 0 | | **0** | 1 | 1 | 1 | | **1** | 0 | 0 | 0 | | **1** | 0 | 0 | 1 |   Looking at the MSB output Q3, it can be seen that in 1 cycle of the counter, there are 8 periods of Low and two periods of High.  Hence,  Duty cycle of signal at Q3 (MSB) = 2/10 \* 100%  = 20 %  In order to obtain 50% duty cycle at the last MSB output, the cascade of counters should be rearranged such that the MSB counter unit should be the mod 8 counter, i.e. as shown: | 3  3  1  1  1  3 | 20 |