SINGAPORE POLYTECHNIC

2017/2018 S2 MID-SEMESTER TEST

MODULE: DIGITAL ELECTRONICS   MOD. CODE: ET1004

COURSE/YEAR: DASE/DCEP/DESM/DCPE/ DEEE 1FT

No	SOLUTION
	SECTION – A A1 (b) A2 (c) A3 (d) A4 (d) A5 (b) A6 (a) A7 (c) A8 (b) A9 (a) A10 (c)

	A	B	C	D
A1		✓		
A2			✓	
A3				✓
A4				✓
A5		✓		
A6	✓			
A7			✓	
A8		✓		
A9	✓			
10			✓	

SOLUTIONS

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SAS code:
MST

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	SOLUTION
	SECTION – B
B1 a)	Add $+54_{10}$ to $+61_{10}$

$$\text{sign } 64\ 32\ 16\ 8\ 4\ 2\ 1$$

+54 =   **0   0   1   1   0   1   1   0**

+61 =   **0   0   1   1   1   1   0   1**

+115 =   **0   1   1   1   0   0   1   1** ◄---------------- +ve sum result

Subtract $+36_{10}$ from $+53_{10}$ = Add -36 to +53

$$\text{sign } 64\ 32\ 16\ 8\ 4\ 2\ 1$$

+36 =   **0   0   1   0   0   1   0   0** ◄------ start with +ve equivalent

 -36 =   **1   1   0   1   1   1   0   0** ◄------ 2's complement of +36

+53 =   **0   0   1   1   0   1   0   1**

+17 = ~~1~~ **0   0   0   1   0   0   0   1** ◄------- discard 9th bit for 8 bit system

b)

ADD $+137_{10}$ to $+25_{10}$ in BCD format

+ 137 = 0 0 0 1   0 0 1 1   0 1 1 1 ◄------ BCD for 137

+ 25 =   0 0 1 0   0 1 0 1 ◄------ BCD for 25

        = 0 0 0 1   0 1 0 1^1 1 1 0 0

                                + 1 1 0 ◄---- Adjust by adding 6

+ 162 = 0 0 0 1   0 1 1 0   0 0 1 0

SOLUTIONS
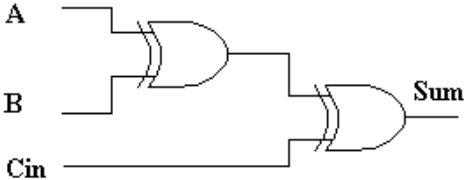
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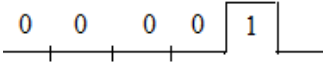
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No	SOLUTION

B2 (a)

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

(b)

$$Sum = \overline{A}\,\overline{B}\,Cin \;+\; \overline{A}\,B\,\overline{Cin} \;+\; A\,\overline{B}\,\overline{Cin} \;+\; A\,B\,Cin$$

$$Cout = \overline{A}\,B\,Cin \;+\; A\,\overline{B}\,Cin \;+\; A\,B\,\overline{Cin} \;+\; A\,B\,Cin$$

(c)

$$Sum = \overline{A}\,\overline{B}\,Cin \;+\; \overline{A}\,B\,\overline{Cin} \;+\; A\,\overline{B}\,\overline{Cin} \;+\; A\,B\,Cin$$

$$= \overline{A}\,(\,\overline{B}\,Cin \;+\; B\,\overline{Cin}\,) \;+\; A\,(\,\overline{B}\,\overline{Cin} + B\,Cin\,)$$

$$= \overline{A}\,(\,B \oplus Cin\,) \;+\; A\,\overline{(\,B \oplus Cin\,)}$$

$$= A \oplus (\,B \oplus Cin\,)$$

$$= A \oplus B \oplus Cin$$

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No	SOLUTION
B3	
(a)	(i) Period = 20 + 60 = 80uS (ii) Frequency = 1/80uS = 12500 Hz or 12.5 kHz (iii) Duty cycle = 20/80 * 100% = 25%
(b)	Mod-Number of counter = 5. Given that the Clock frequency applied is 1000Hz, Signal Freq at MSB output = 1000/5 = 200 Hz To determine duty cycle of mod-5, examine the bit sequence at the MSB output for I cycle of counter, which is: 0 0 0 0 1 $\quad$ 0 $\quad$ 0 $\quad$ 0 $\quad$ 0 $\boxed{1}$ Hence duty cycle at MSB = 1/5 * 100 = 20%
(c)	Given initial state = 010_2 and 62_{10} clock cycles are continuously applied, 62 Clk cycles is = 12 complete cycles (12* 5 =60) plus remainder of 2 Clock cycles Thus final output state = 010 + 10 = 100_2

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No	SOLUTION
C1 (a)	4 possible configurations for cascaded divide-by-18 counter:
(b)	Configuration that provides 50% duty cycle at divide-by-18 output is Mod-9, followed by Mod-2
(c)	<u>Important points to note</u> Use of 4 FF for mod 9 & Q0 connected to CP1 Feedback to MR1 MR2 Correct connection between mod-9 & Mod-2 Correct connection for mod-2
(d)	State diagram for 1st counter in cascade:

SOLUTIONS