SAMPLE DE1 EXAM Solution

: DIGITAL MODULE ELECTRONICS 1 MOD. CODE: ET1003

No	SOLUTION
A	**SECTION – A (2 marks each)** 1) (c) 2) (b) 3) (c) 4) (c) 5) (d) 6) (a) 7) (a) 8) (c) 9) (c) 10) (a)
	SECTION – B (10 marks each)
B1 a)	Decimal 7788_{10} to Binary and Hexadecimal. As number is quite large, it is better to convert to hex first & then to binary.

16	7788	Remainder
16	486	C
	30	6
	1	E

Thus $7788_{10} = 1\ E\ 6\ C_H = 1\ 1110\ 0110\ 1100_2$

(b) Binary 10110011_2 to Decimal or base 10.

$10110011_2 = (1*128) + 0 + (1*32) + 1*16 + 0 + 0 + (1*2) + 1$

$= 128 + 32 + 16 + 2 + 1 = \mathbf{179_{10}}$

Octal 56271 to decimal

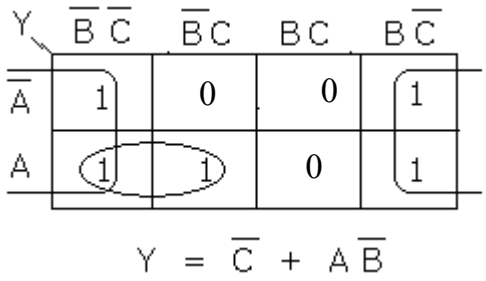
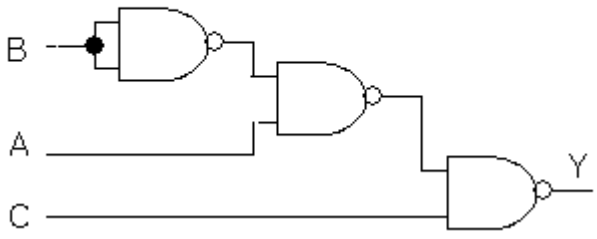
$= 5*8^4 + 6*8^3 + 2*8^2 + 7*8^1 + 1$

$= 23737_{10}$

Hex 3FAD to decimal

$= 3*16^3 + 15*16^2 + 10*16 + 13$

$= 16301_{10}$

No	SOLUTION
B2	Boolean Equation from truth table is
(a)	$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C + A\,B\,\overline{C}$
(b)	$Y = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}\,B\,\overline{C} + A\,\overline{B}\,\overline{C} + A\,\overline{B}\,C + A\,B\,\overline{C}$ $= \overline{C}(\overline{A}\,\overline{B} + \underline{A}\,B + A\,\overline{B} + A\,B) + A\,\overline{B}\,C$ $= \overline{C} + A\,\overline{B}\,C$ $= \overline{C} + A\,\overline{B}$ ***Or***  $Y = \overline{C} + A\,\overline{B}$
(C)	$Y = \overline{\overline{C} + A\,\overline{B}} = \overline{\overline{C}}\;\overline{A\,\overline{B}} = \overline{C\;A\,\overline{B}}$ 

No	SOLUTION

B3

CLK	J	K	Q1	Q2
L	L	L	H	H
↓	L	L	H	H
↑	L	H	L	H
↑	H	L	H	H
↓	H	H	H	H
↑	H	H	L	H

B4

(a) Boolean Equation is

$$Z = \overline{(\overline{A+B}).C}.C\overline{D}$$

Simplifying

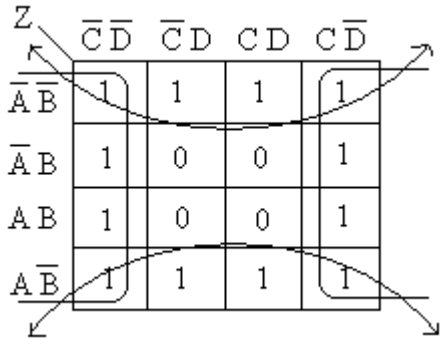
$$Z = (\overline{\overline{A+B}} + \overline{C}).C\overline{D}$$

$$Z = (A+B+\overline{C}).C\overline{D}$$

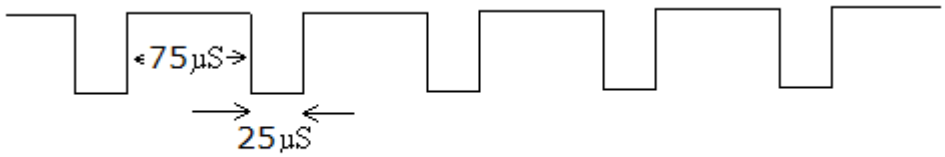
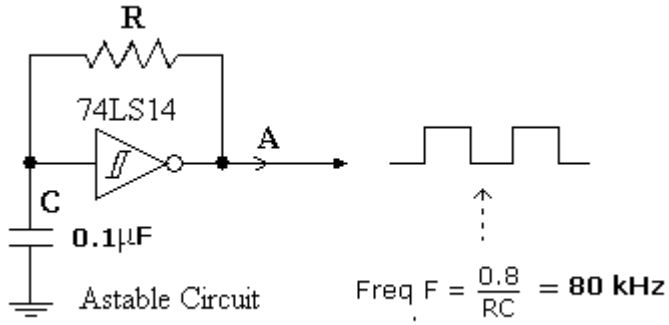
$$Z = AC\overline{D} + BC\overline{D} + \overline{C}CD$$

$$Z = AC\overline{D} + BC\overline{D}$$

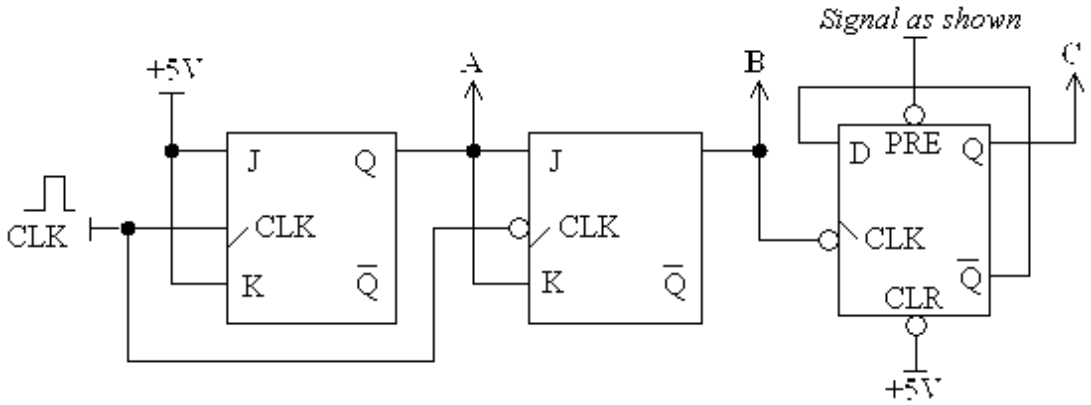
(b)

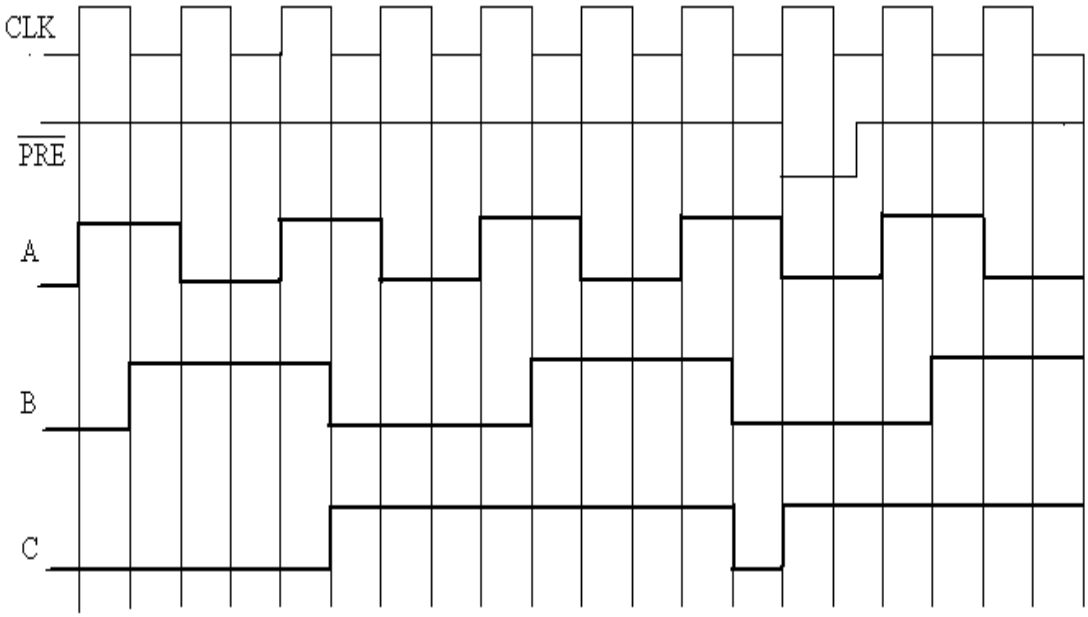


$$Z = \overline{B} + \overline{D}$$

No	SOLUTION
B5 a)	Given:  Figure B5.1 Frequency = 1/(period) = 1/(75+25) µS = 10,000 Hz or 10kHz. Duty Cycle = 75/(25+75) * 100 = 75% To change the duty cycle without changing the CLK frequency a monostable or one-shot can be used for this purpose.
b)	 $F = \frac{0.8}{R\,C}$ = 80000 Hz Therefore R = 0.8/(80000 * 10^{-7}) = 100 Ohms

B6


Signal as shown
+5V
A
B
C
J
Q
CLK
K
$\overline{Q}$
D
PRE
CLR
+5V


CLK
$\overline{PRE}$
A
B
C

No	SOLUTION
C1 (a)	Required Truth-table is as shown:

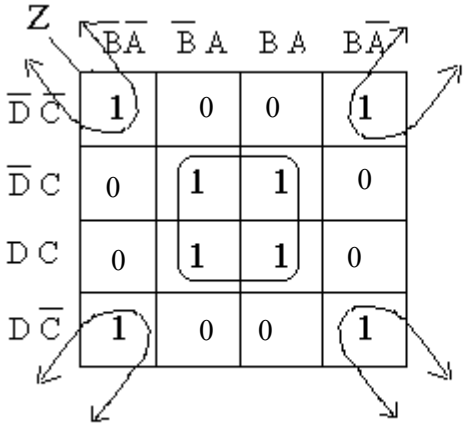
Inputs				Output
D	C	B	A	Z
0	0	0	0	1
0	0	0	1	0
0	0	1	0	1
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	1
1	0	0	0	1
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	1
1	1	1	0	0
1	1	1	1	1

Table C1

Boolean expression for output is therefore:

$$Z = \overline{D}\,\overline{C}\,\overline{B}\,\overline{A} + \overline{D}\,\overline{C}\,B\,\overline{A} + \overline{D}\,C\,\overline{B}\,A + D\,\overline{C}\,\overline{B}\,\overline{A} + D\,\overline{C}\,B\,\overline{A} + D\,C\,\overline{B}\,A + D\,C\,B\,A + \overline{D}\,C\,B\,A$$

No	SOLUTION
C1 (b)	Using the K-Map,



Marks Distribution
4 marks for the K-map
2 marks for correct equation

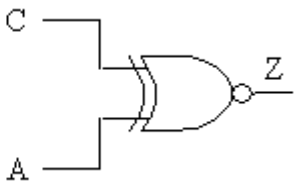
$$Z = A\,C + \overline{A}\,\overline{C}$$

Or, if Boolean theorems are used instead, then the solution is:

$$Z = \overline{D}\,\overline{C}\,\overline{B}\,\overline{A} + \overline{D}\,\overline{C}\,B\,\overline{A} + \overline{D}\,C\,\overline{B}\,A + \overline{D}\,C\,B\,A +$$
$$D\,\overline{C}\,\overline{B}\,\overline{A} + D\,\overline{C}\,B\,\overline{A} + D\,C\,\overline{B}\,A + D\,C\,B\,A$$
$$Z = \overline{C}\,\overline{A}(\overline{D}\,\overline{B} + \overline{D}\,B + D\,\overline{B} + D\,B) +$$
$$C\,A(\overline{D}\,\overline{B} + \overline{D}\,B + D\,\overline{B} + D\,B)$$
$$= \overline{C}\,\overline{A} + C\,A$$

Implementing with the least possible number of gates,
the simplified equation is the Boolean expression of an XOR gate.
Thus:

$$Z = \overline{C}\,\overline{A} + C\,A$$
$$= \overline{C \oplus A}$$



No	SOLUTION
	Double complementing the expression and applying DeMorgan's theorems, the NAND gate implementation is: $Z = \overline{\overline{\overline{C}\,\overline{A} + CA.}}$ $= \overline{\overline{\overline{C}\,\overline{A}}\ \overline{CA.}}$ Hence the circuit is as shown: