pulse per sec.

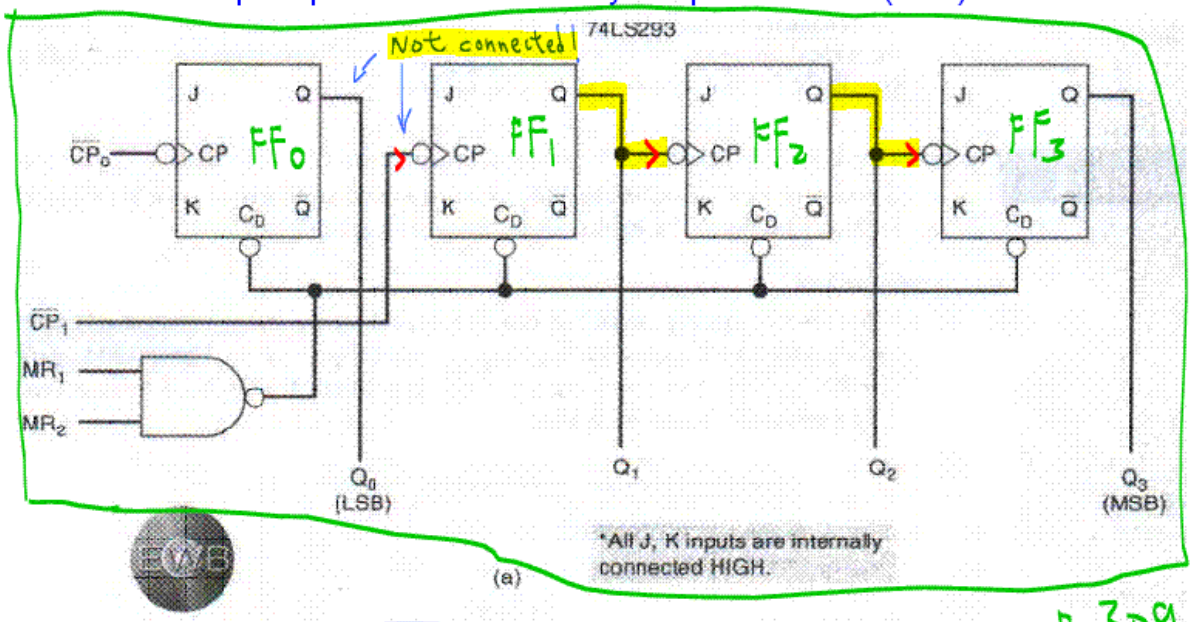
7-10. Show how a 74LS293 counter can be used to produce a 1.2-kpps output from an 18-kpps input.

18 Kpps → MOD-? → 1.2 Kpps

ie KHz

$\frac{18}{1.2} = 15$ → MOD-15

Reset all flip-flops when the binary output is 1111 (=15).



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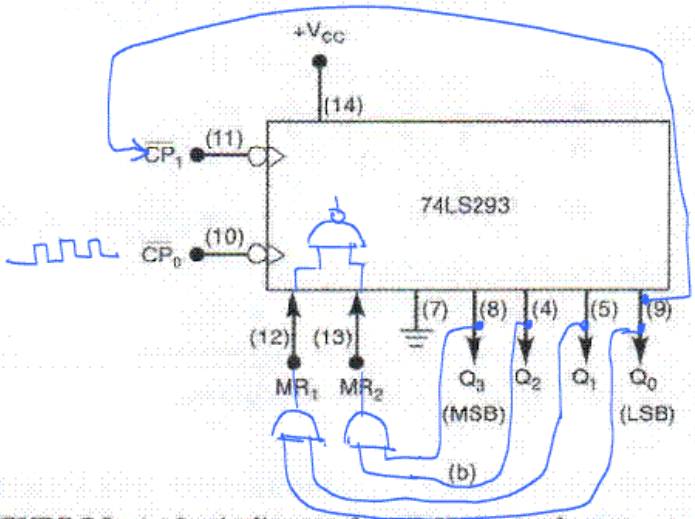


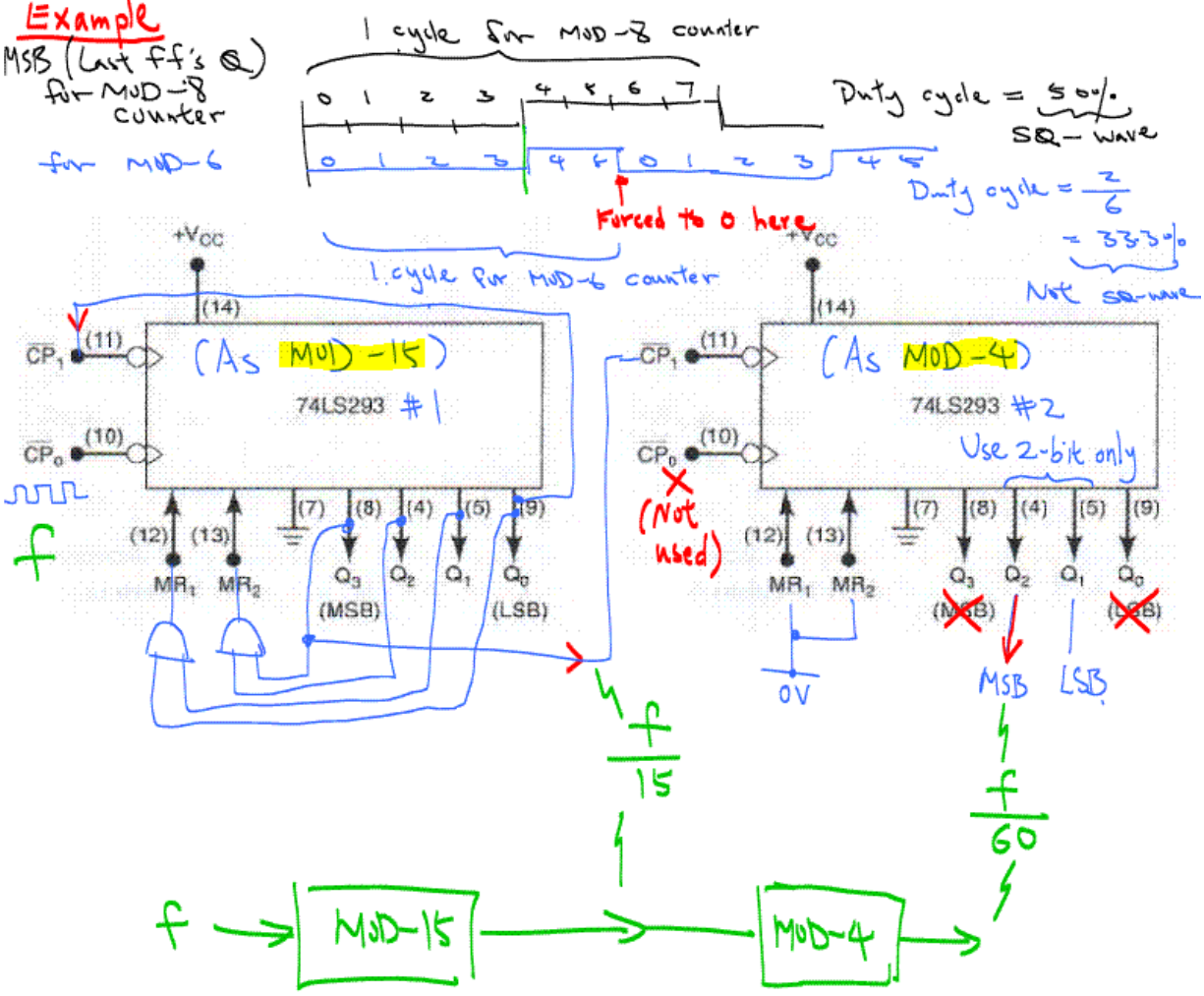
The NAND gate inside 74LS293 will output 0 to reset all flip-flops when the binary output is 1111 (=15).

FIGURE 7-8 (a) Logic diagram for 74LS293 asynchronous counter IC; (b) block symbol, with pin numbers in parentheses.

7-11. Show how two 74LS293s can be connected to divide an input frequency by 60 while producing a symmetrical square-wave output.

The 2nd counter must be MOD-2^N

Note - the output waveform at the final stage (i.e. MSB) of the counter will be square-wave (i.e. 50% duty-cycle) **only if** the counter has MOD = 2, 4, 8,



C→7-12. Determine the frequency at output X in Figure 7-81.

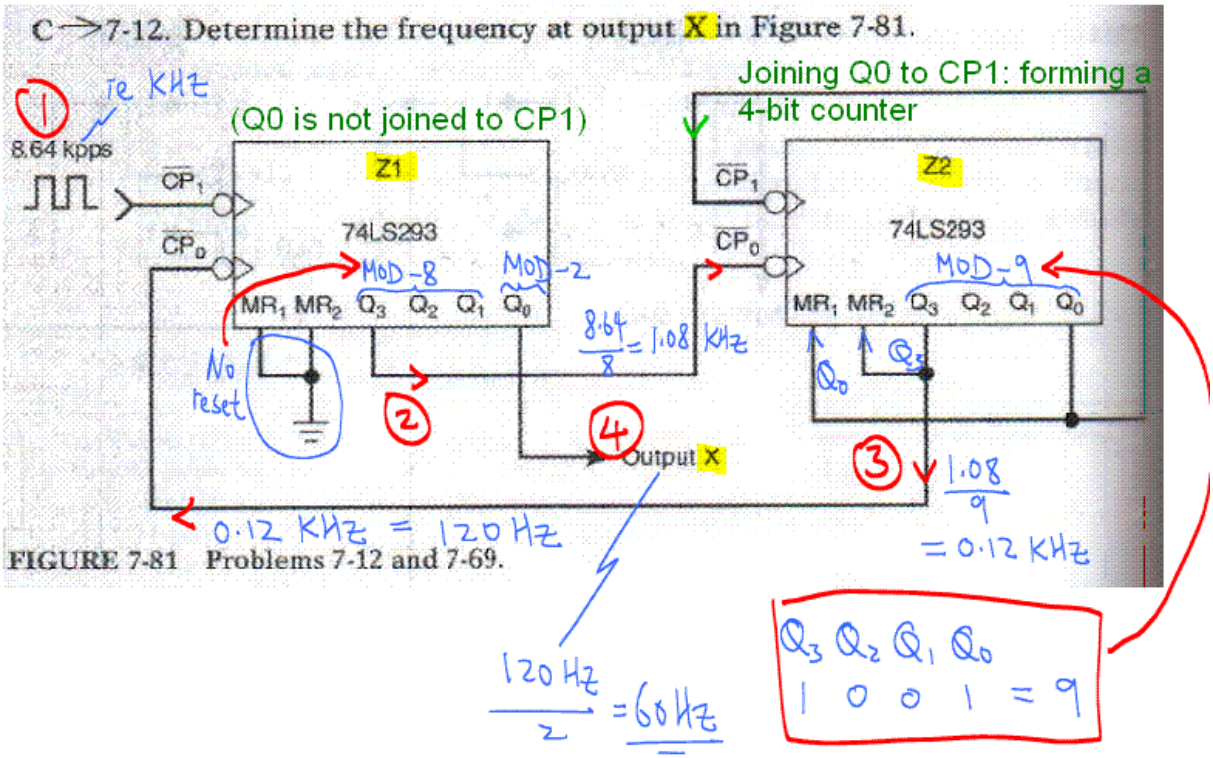
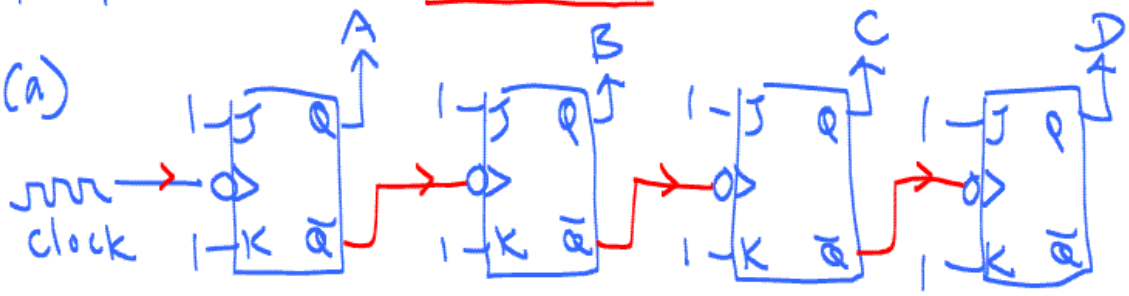


FIGURE 7-81 Problems 7-12 and 7-69.

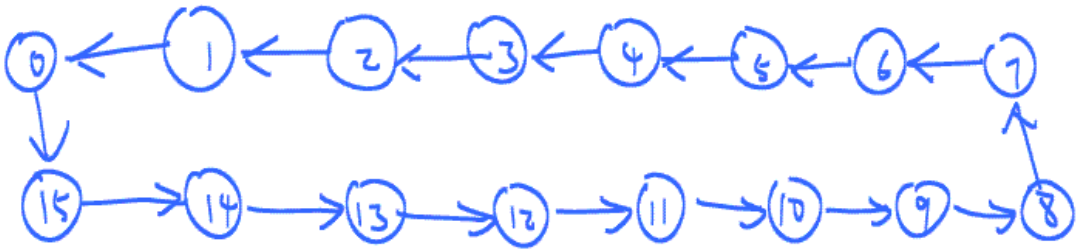
7-14. (a) Draw the diagram for a MOD-16 *down* counter.
(b) Construct the state transition diagram.
(c) If the counter is initially in the 0110 state, what state will it be in after 37 clock pulses?

7-14 MOD-16 Down Counter

(a)



(b) State Diagram:



(c) Initial state = 6, what is final state after 37 pulses?

The state returns to 6 after every 16 pulses.

After 32 pulses, the state = 6,

After 5 pulses more, the state = 6 - 5 = 1.

7-30. Draw the AND gates necessary to decode the 10 states of the BCD counter of Figure 7-6(b).

ie outputs '1' only during that state

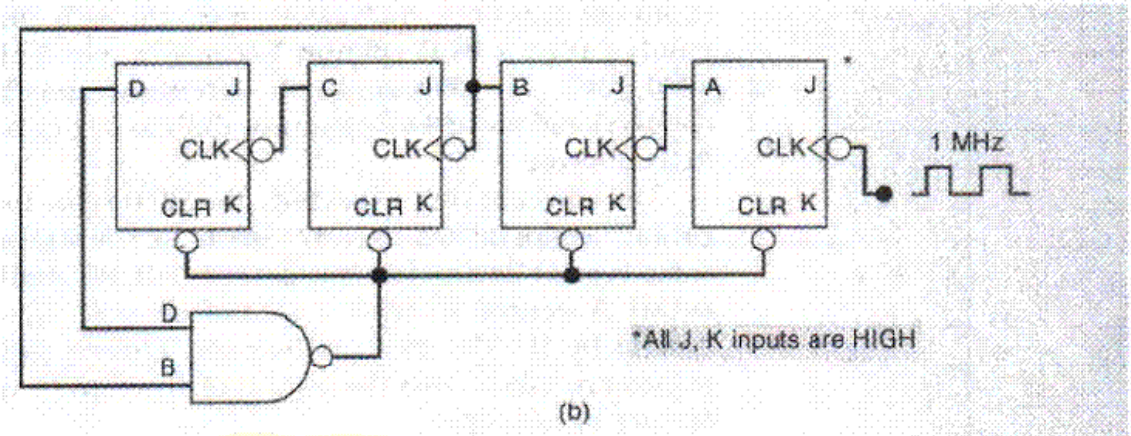


FIGURE 7-6 (b) MOD-10 (decade) ripple counter.

DCBA = 0000 → $\bar{D}\,\bar{C}\,\bar{B}\,\bar{A}$ → X_0 = '1' only when state = 0

DCBA = 0001 → $\bar{D}\,\bar{C}\,\bar{B}\,A$ → X_1 = '1' only when state = 1

etc. etc.

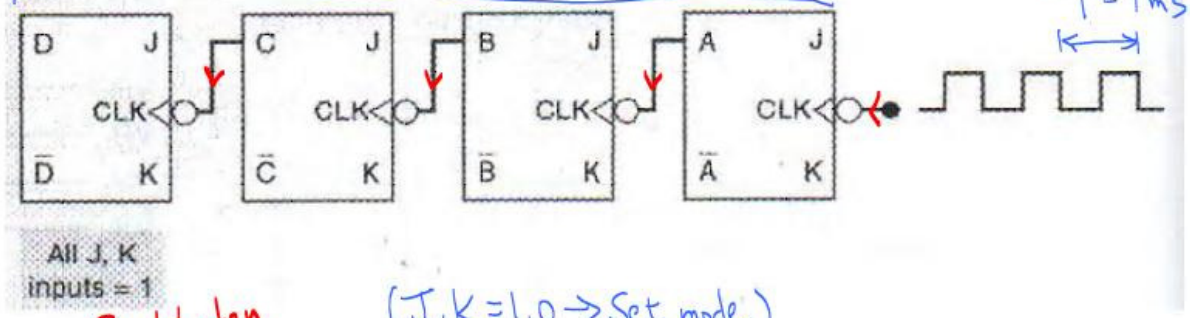
DCBA = 1001 → $D\,\bar{C}\,\bar{B}\,A$ → X_9 = '1' only when state = 9

7-31. Figure 7-86 shows a ripple counter being used to help generate control waveforms. Control waveforms 1 and 2 can be used for many purposes, including control of motors, solenoids, valves, and heaters. Determine the control waveforms, assuming that all FFs are initially LOW. Ignore decoding glitches. Assume that clock frequency = 1 kpps. ($T = \frac{1}{f}$)

kHz

MOD-16 counter

$T = 1$ ms



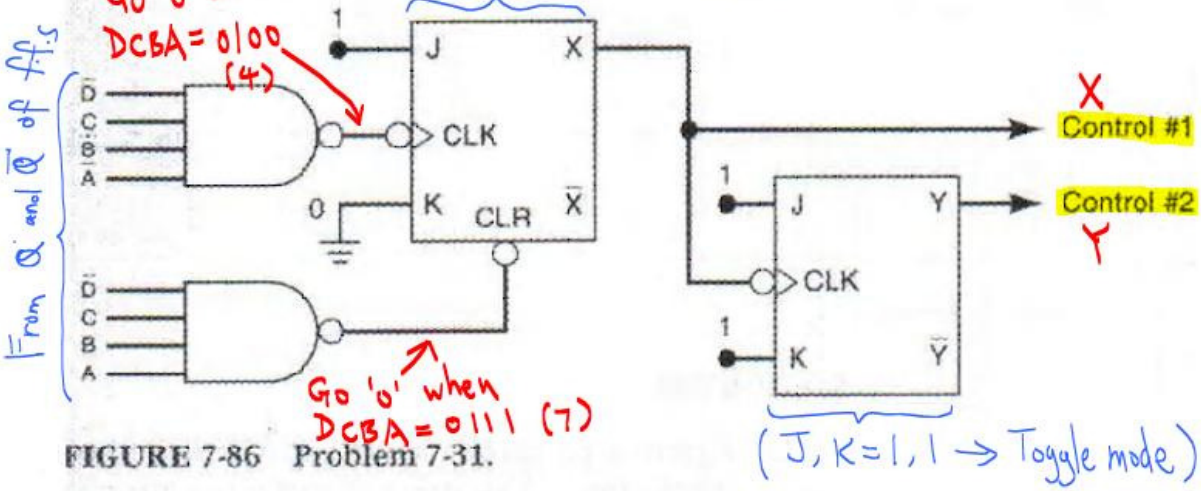
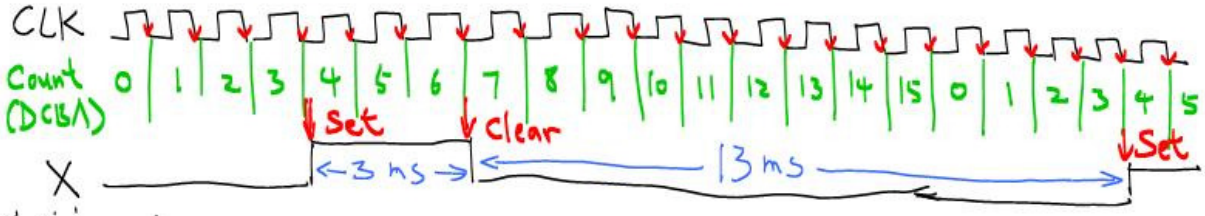


FIGURE 7-86 Problem 7-31.



Sketch with larger time-scale to show X and Y only: