SECTIONS 7-1 AND 7-2

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→ 7-1. Add another flip-flop, *E*, to the counter of Figure 7-1. The clock signal is an 8-MHz square wave.

(a) What will be the frequency at the *E* output? What will be the duty cycle of this signal? Duty cycle : $\frac{\text{High Time}}{\text{Clock cycle}} \times 100\%$

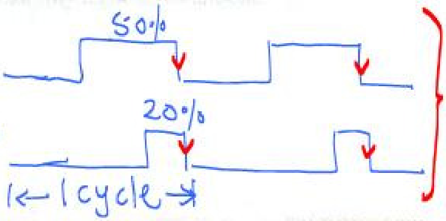
(b) Repeat (a) if the clock signal has a 20 percent duty cycle.

(c) What will be the frequency at the *C* output?

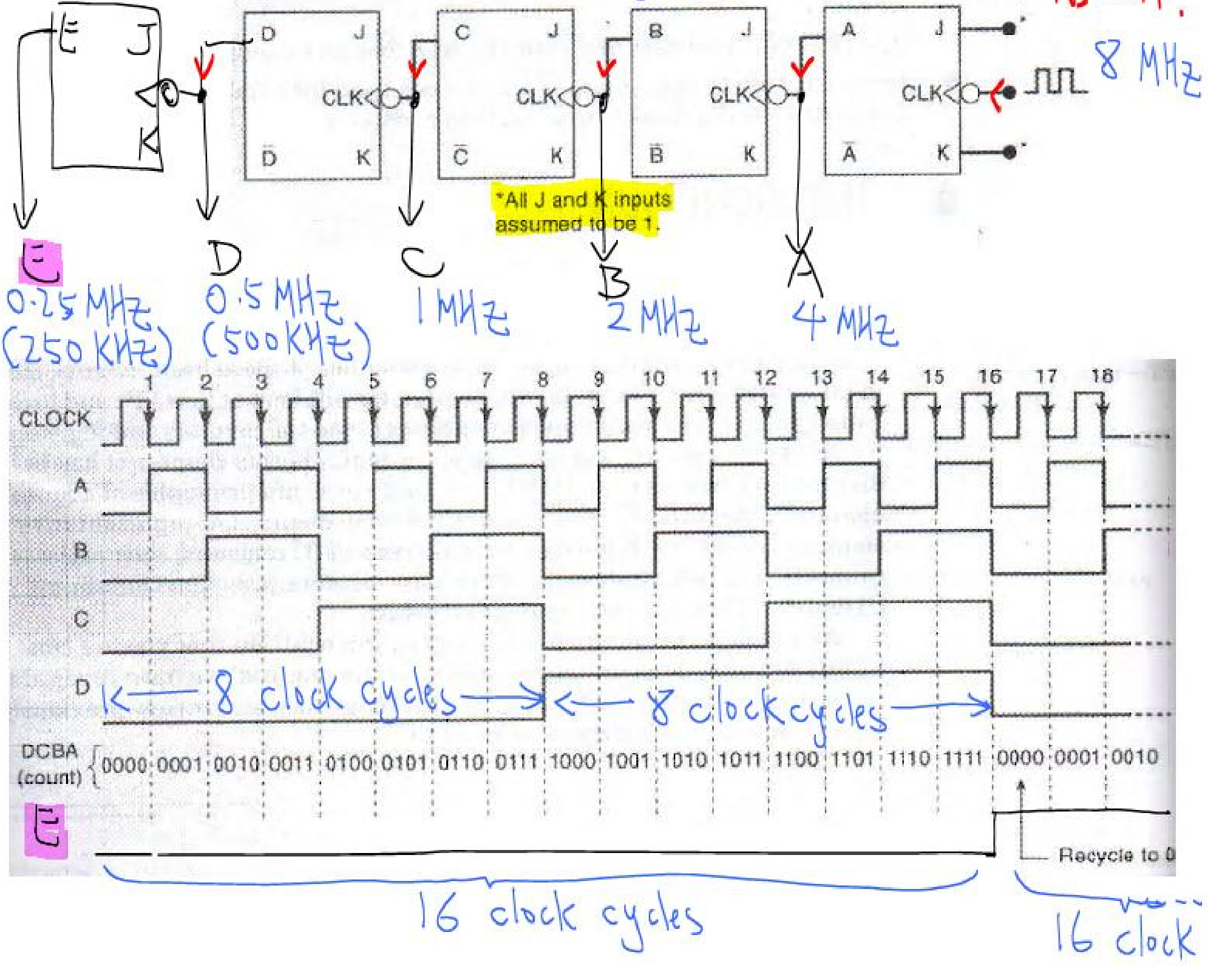
(d) What is the MOD number of this counter?

e.g. 50% duty cycle :

20% " " :



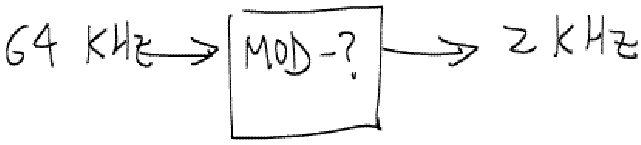
The duty cycle of the clock has no effect on its NGT.



(d) 5 ff.s → $2^5 = 32$ states → MOD-32

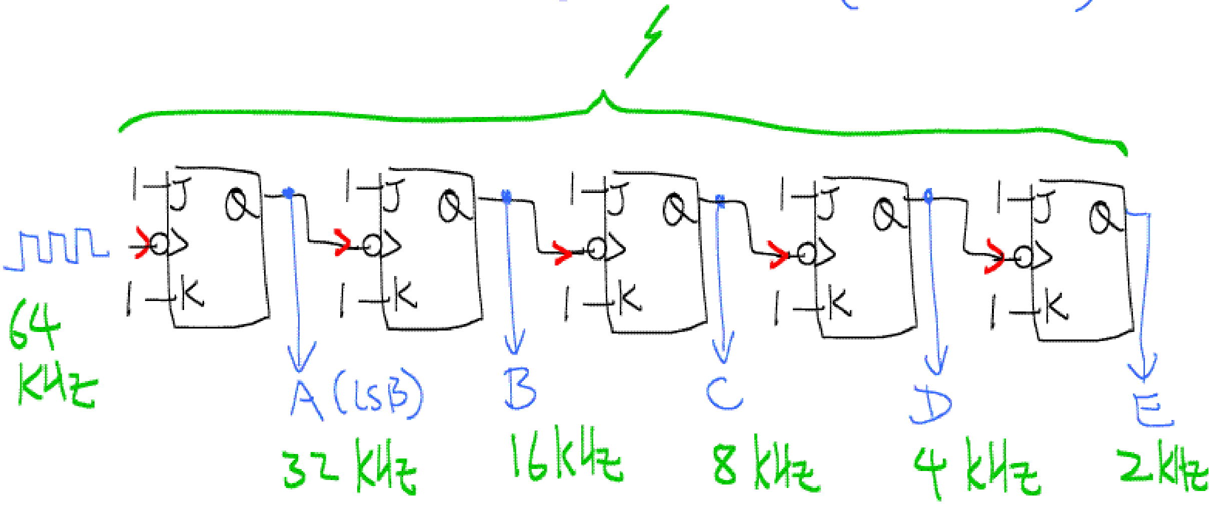
ie count in binary sequence

7-2. Construct a $\underbrace{\text{binary counter}}$ that will convert a 64-kHz pulse signal in a 2-kHz square wave.

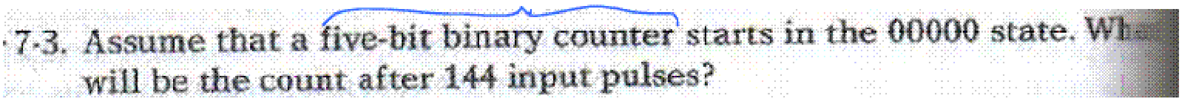


$\frac{64}{2} = 32 \rightarrow$ MOD-32

MOD-32 needs 5 ff's ($2^5 = 32$)



5 ff.s → MOD-32

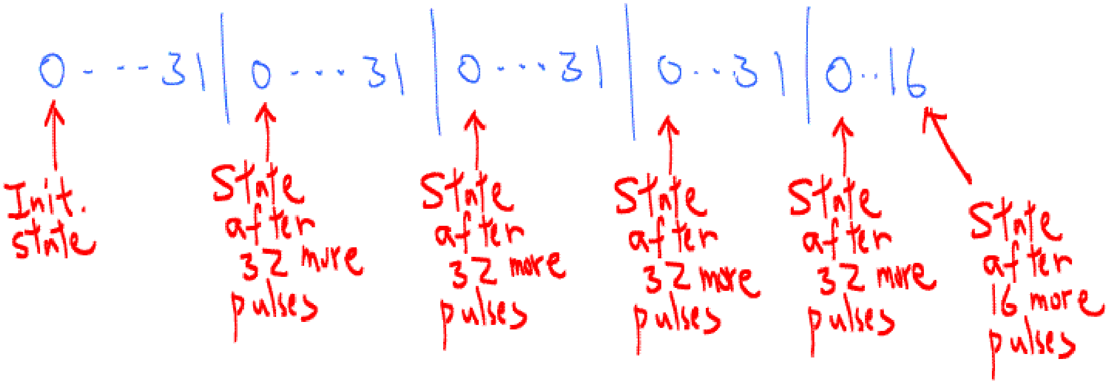


7-3. Assume that a five-bit binary counter starts in the 00000 state. Wh will be the count after 144 input pulses?

(Hint: It will return to the same state after every 32 clock pulses.)

$$144 \div 32 = 4 \text{ remainder } 16$$

Hence the final count is $16 = \underline{\underline{10000_2}}$


0 ··· 31
0 ··· 31
0 ··· 31
0 ·· 31
0 ·· 16
Init. state
State after 32 more pulses
State after 32 more pulses
State after 32 more pulses
State after 32 more pulses
State after 16 more pulses

What will be the final state after 144 pulses if the initial state is

What will be the final state after 144 pulses if the initial state is 20?

$$\frac{20+144}{32} = 5 \text{ remainder } \underline{\underline{4}}$$

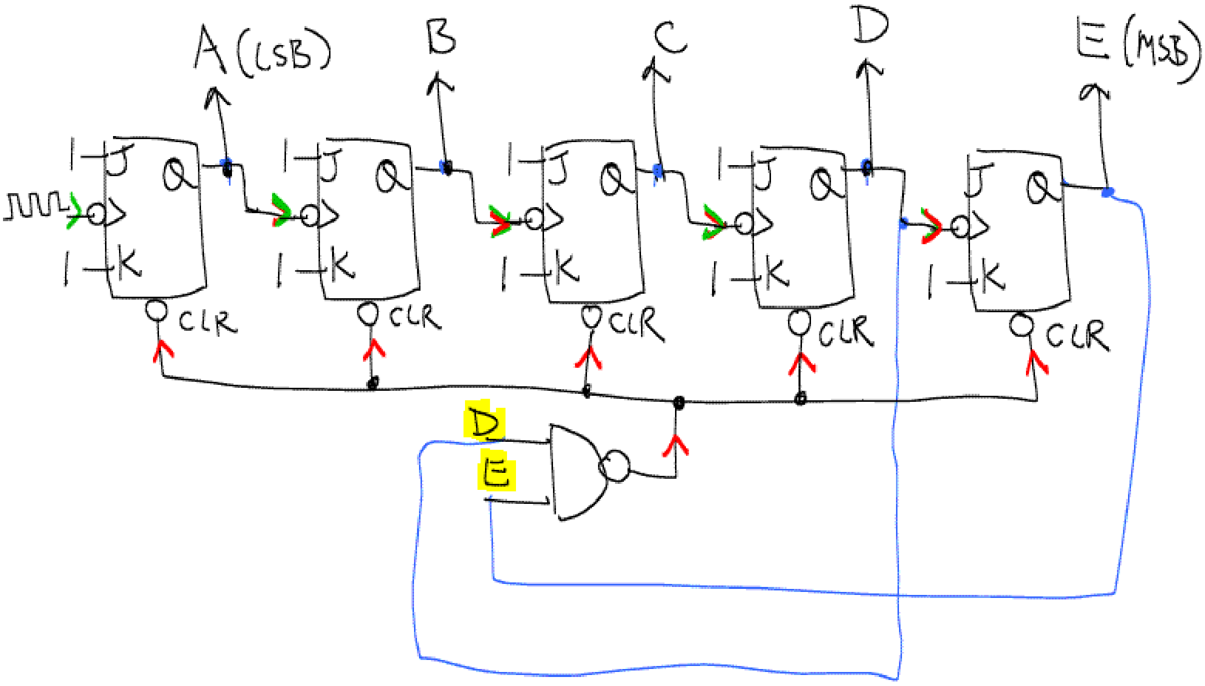
ie $\dfrac{\text{Init. State + No. of Pulses}}{\text{MOD}}$

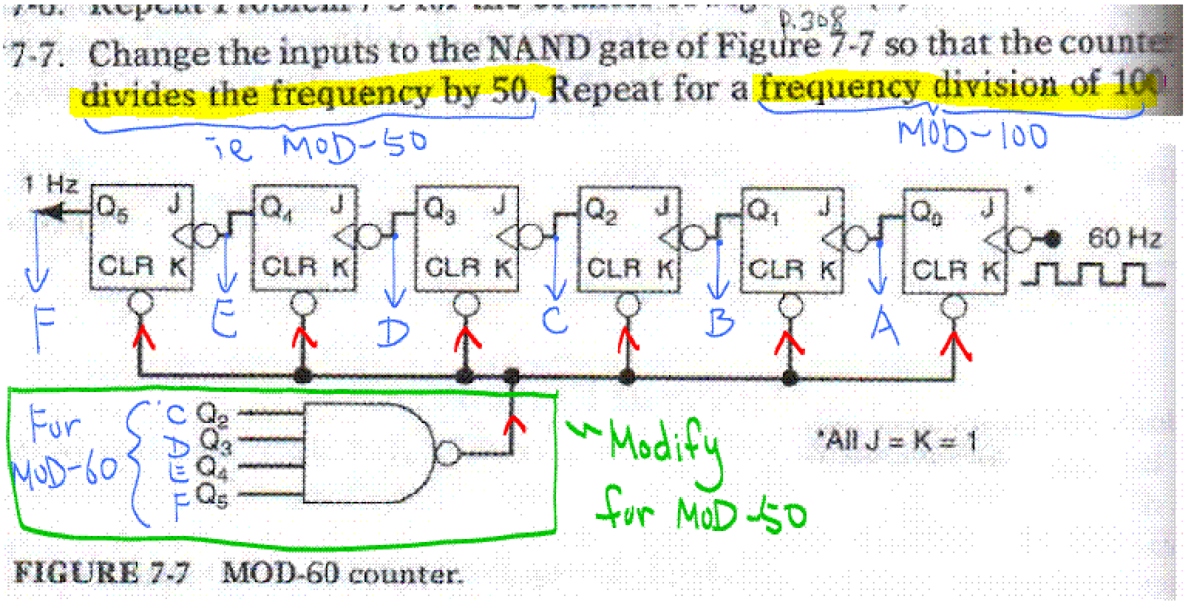
*7-4. Use J-K flip-flops and any other necessary logic to construct a MOD-24 asynchronous counter.

$$\text{MOD-24} \rightarrow \text{Modified from } \underbrace{\text{MOD-32}}_{5 \text{ ff.s}}$$

$$24 = \overset{E}{1}\overset{D}{1}\overset{C}{0}\overset{B}{0}\overset{A}{0}{}_2$$

Resets all ff.s when E=1 and D=1





7-7. Change the inputs to the NAND gate of Figure 7-7 so that the counter divides the frequency by 50. Repeat for a frequency division of 100.

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ie MOD-50

MOD-100

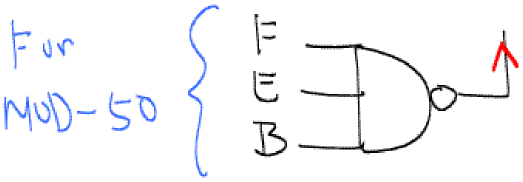
1 Hz
Q_5
Q_4
Q_3
Q_2
Q_1
Q_0
J
K
CLR
60 Hz
F
E
D
C
B
A
For MOD-60
C Q_2
D Q_3
E Q_4
F Q_5
Modify for MOD-50
*All J = K = 1

FIGURE 7-7 MOD-60 counter.

For MOD-50:

$$\begin{array}{cccccccc} & F & E & D & C & B & A & \\ 50_{10} = & 1 & 1 & 0 & 0 & 1 & 0 & _2 \end{array}$$

Reset all ff.s when F=1 and E=1 and B=1



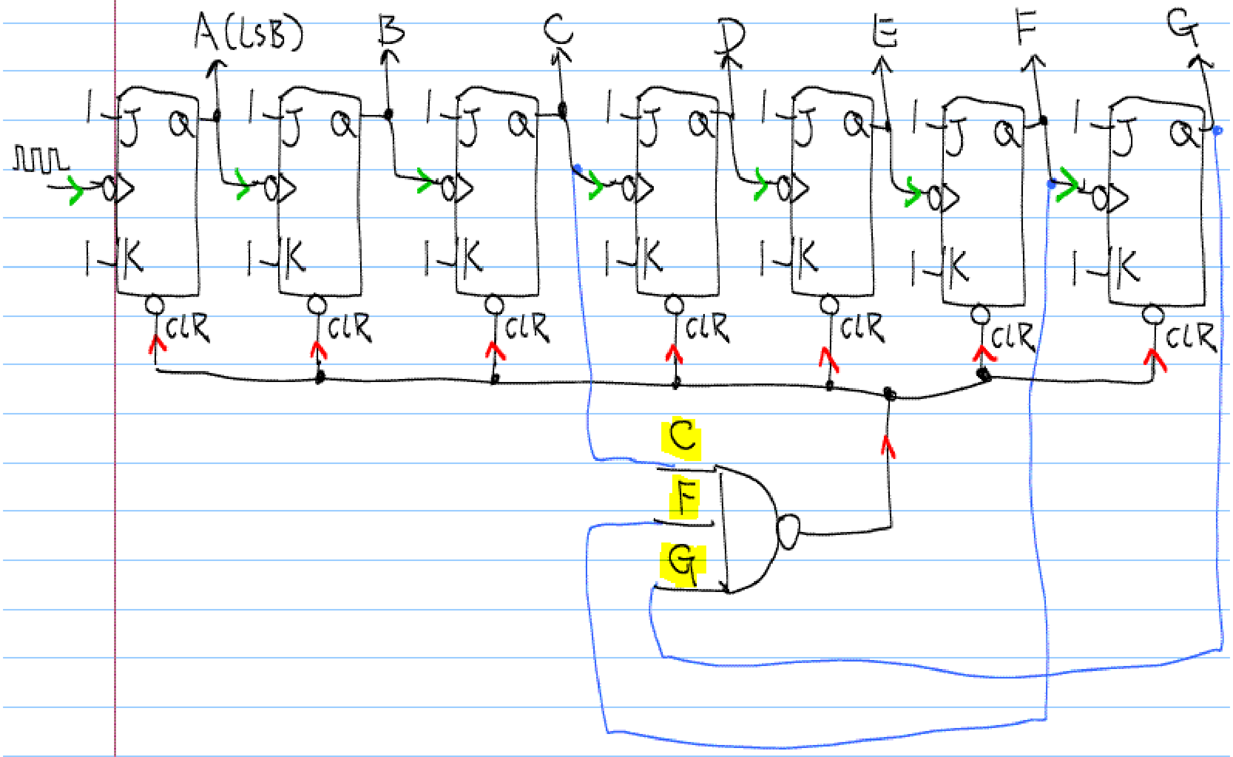
Q7.7

For MOD-100 :

$$100_{10} = \overbrace{1\,1\,0\,0\,1\,0\,0_2}^{\text{7-bit (7 ff.s)}}$$

G F E D C B A

Reset all ff.s when G, F, C are all '1'.


A(LSB)
B
C
D
E
F
G
1 J Q
1 K
CLR
C
F
G