Laboratory Experiment on Basic & Universal Gates

Introduction to basic logic gates and the use of NI Multisim for schematic capture and logic circuit simulation.

Objective :	To familiarise oneself with the operation of the basic logic gates using TTL devices.
Equipment required :	Logic probe Digital Trainer NI Multisim Simulation Software
ICs required :	74LS04 - NOT gate 74LS32 - OR gate 74LS08 - AND gate 74LS00 - NAND gate 74LS02 - NOR gate

Experiment A - Device identification

Identify any 4 of the devices to be used in this experiment and write down the markings printed on the IC chips. Indicate the type of package used.

SN74LS04NSR-74LS04, DM74LS32-74LS04, DM74LS06-74LS08 DM74LS00-74LS00

All 4 IC chip uses through hole packages.

Experiment B

Using the device chart (pin diagrams) provided, view how the logic gates are connected internally to the pins of the IC. Take note of the pins use for providing power to the IC.

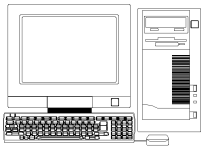
Question?

How many logic gates are there in the 74LS04 and 74LS86 ICs?

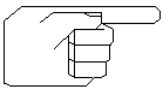
Answer 74LS04 : 14

Answer 74LS86 : 14

Experiment C - Introduction to NI Multisim



Starting the Tutorial - To start your NI Multisim training, you'll need to make sure that the simulation software has been installed on your Notebook and know the procedure of obtaining the network licence. If it is not please approach your Lecturer for assistance.



Before you start your first experiment on simulation, it is advisable for you to go through "Introduction to NI Multisim Software" handout in the Lab Experiments Folder of DE-Blackboard.

1. To launch the Multisim software, click on ***Start*** » then select ***Programs*** » ***National Instruments*** » ***Circuit Design Suite*** » and lastly ***Multisim.***

   After some startup delay, a blank file opens on the workspace with a default name of "Circuit1". You are now ready to start schematic capture and simulation with NI Multisim™ software.

2. In this first experiment using NI Multisim™, sufficient instructions will be given to get you started. As you progress, you can then use more of the software features for subsequent exercises.

   If you are still in doubt as to how to perform a certain task, you can always ask your lecturer or refer to the on-screen help menu.

3. The 'Circuit' window is your viewpoint to the circuit diagram and will be manipulated by you using the mouse. To resize the circuit window or drawing page, click on the ***View*** menu and use the ***Zoom_in/Zoom_out*** function to select an appropriate drawing page size. Alternatively, you can place the mouse cursor anywhere on the drawing page and rotate the wheel on your mouse to achieve the same effect. To change other properties of the drawing page, such as sheet size or turning off the drawing grid, place the cursor within the drawing page and right click on the mouse to open up the properties menu. Changing sheet properties does not change the content of your schematic capture, but only the appearance of your circuit. In your exercises on simulation, it is advisable to hide all unnecessary information which might appear as 'clutter' on your drawing page. To do this, select "**Hide All**" for the Net Names property and uncheck all Component properties except for Reference Designator or "**RefDes**".

4. To draw your circuit, which is technically known as "schematic capture", you need to first **place** all the required components and then connect them together. To **Place a Device** on the drawing page you have to access the database library and select the correct component**.** To do this, click on the **Place** menu and select the first item on the list which is **Component**. This will open up the component dialog box to allow you to select all the required components. All the components in the database library are sorted into groups for easy access. You will have to select the group first in order to select the required component in that group. Try and explore what are the various type of components listed under each groups. You may not know what each of these components is at this point in time but you need not worry. You will learn about some of these components in due course.

5. For this first simulation exercise, you will simulate the Inverter or **NOT** gate, which is the simplest 'building block' digital device. The components/items required will be as follows:

   - Supply voltage **Vcc**
   - Digital Ground **DGND**
   - Single pole double throw switch **SPDT**
   - Inverter or **NOT gate**
   - A display indicator which is a **Probe**

   Vcc and **DGND** are obtained from the **Sources/Power Sources** group.

   Switch **SPDT** is obtained from the **Basic/Switch** group.

   The NOT gate may be obtained **Misc Digital/TTL** group or from an actual device which is the 74LS04N found in the **TTL/74LS** group.

   The display indicator or probe is found in the **Indicators/Probe** group. You may select any colour such as red or green, depending on your preference.

6. Having placed each of the required components (see figure 2.1), you may have to move and/or re-orientate the position of each component. To move a component, Left click on the required component and drag it to the desired position. For the **SPDT** switch, you will probably have to change the default orientation of the switch to as shown in figure 2.1. Right click on the **SPDT** switch and select **Flip Horizontal**. This will re-orientate switch to what is as shown in the diagram.

   Note: *More devices of the same type could be placed by 'Left clicking' on the component and doing a copy and paste operation. Similarly to delete an unwanted component, left click on the component and press the Del button on the keyboard to delete or remove the component from the drawing page* or *alternatively, 'Right click' on the component and then selecting delete operation from resultant menu list.*

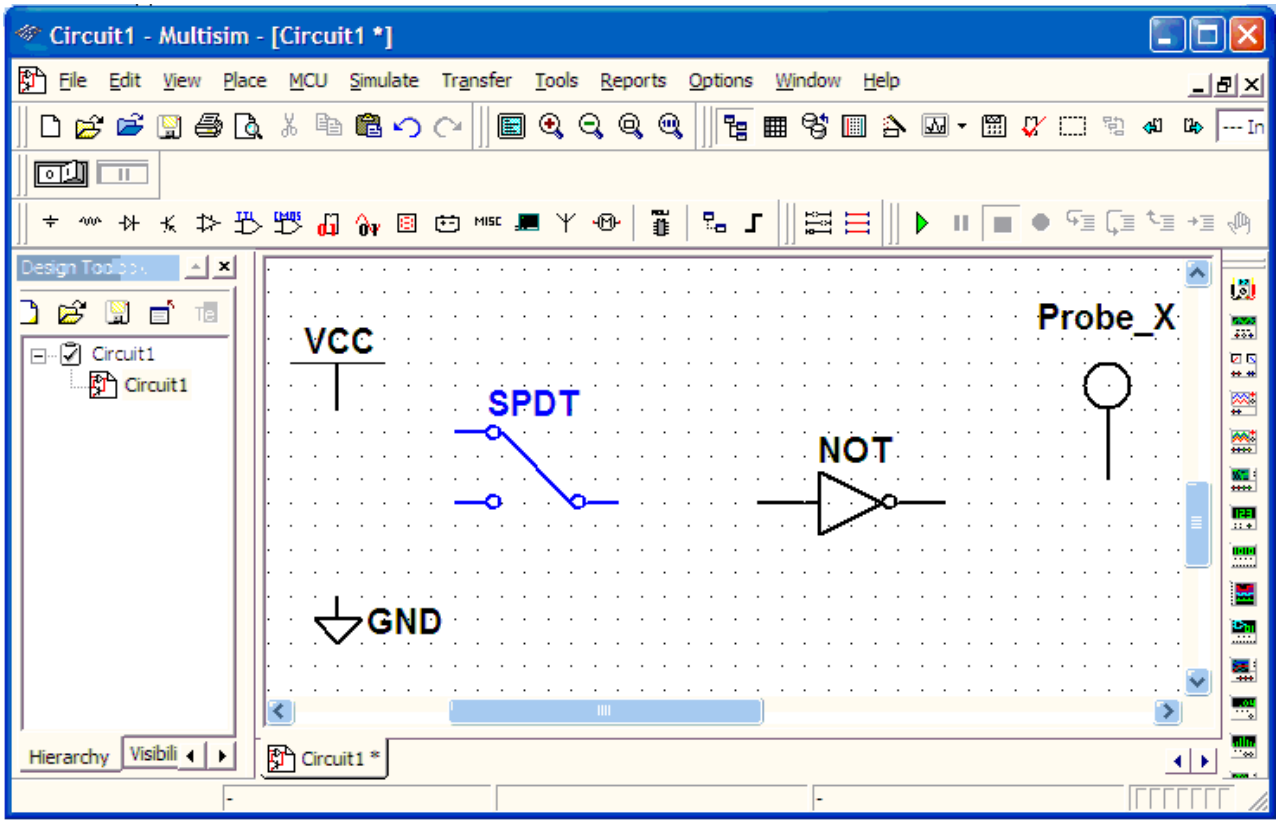


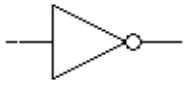
Figure 2.1

7. **Drawing Signal Connections -** To attach the Switch output to the input of the NOT gate, position the pointer (cursor) at the end point of the switch, click and drag (remember to keep mouse key depressed) it to the input of the NOT gate. Repeat the process for the connection of the Probe to the NOT gate output. Do the same by completing the connections from the 2 poles of the switch to Vcc and DGND. You may also place a probe (preferably of a different colour) at the input to the NOT gate to allow you to display the status of the switch during your simulation.

8. To **simulate** your completed circuit, click on the **Simulate** menu, and select **Run**. This will start the simulation process in real time. Click on the **SPDT** switch using your mouse button and observe what happen to the Probe connected to the output of the **NOT** gate. The probe will show the output status of the NOT gate, either ON (logic H) or OFF (logic L). Record your results in a truth table. To stop the simulation process, select **Stop** from the same simulation menu.

You have now completed the basic NI Multisim tutorial. The software is capable of many more functions and these you will learn with use and experience. As you progress through the experiments, you will be expected to design and simulate your circuit on your notebook before you build it on the trainer. You are also encouraged to experiment with you own designed circuits, or those taken from the text book. You may even solve some of your tutorial problems using NI Multisim™.

Experiment D - NOT logic gate



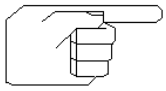
The NOT logic gate - has only one input and one output. Its output is always the logical inverse of the state of the input.

The standard logic symbol for an inverter has a triangle with a bubble at the apex or output. However, the bubble may be drawn at the input, but the function remains the same. The truth table states that when the input A is 0, the output is 1, and when the input is 1, the output is 0. The Boolean expression is $F(A) = \overline{A}$. The bar over the A represents "NOT," or the complement of A.

1. Insert the 74LS04 Inverter IC onto the breadboard of the logic trainer.

2. Connect the power supply to the 74LS04 IC. Refer to the pin diagram or chip layout as found in the appendix of this manual for the pin connections to the IC.

3. Connect a wire from one of the toggle switches to an input of a NOT gate. Connect a wire from the output of the NOT gate to one of the LED's.



Check carefully that your IC is wired correctly before applying any power.

Make sure the power supply is switched off whenever you want make any circuit changes

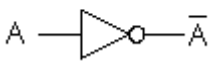
4. Toggle the switch and record the results in the form of a truth table.

5. Compare this truth table with the truth table obtained from your simulation experiment. They should match exactly.

Truth Table

Input (A)	Output (A)
0	1
1	0

Symbol of NOT gate



If the input to an inverter is 1, the output will be ___

The Boolean expression for an inverter is $Z = 0$

Double click on the object to complete the Boolean Eqn.

Experiment E - OR logic gate

The OR logic gate has two inputs and the output will be a logical 1 if either one or both the inputs are equal to one. (In future you will meet OR gates with more than 2 inputs).

1. Simulate the OR gate. Repeat the steps shown in Experiment D and this time select the OR-2 instead of the NOT gate. Connect in two switches and a probe. Change the logic level of the switches and observe the probe status. Record the simulated behaviour of this 2-input OR gate in a truth table.

2. Insert the 74LS32 IC onto the trainer and connect the power supply to it. Refer to the chip layout as given in the appendix for the pin connections.

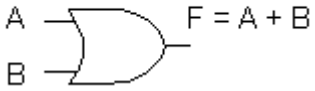
3. Connect two wires from two of the toggle switches to the two inputs of an OR gate and a wire from the output of the OR gate to one of the LEDs.

4. Toggle the switches and record the results in the truth table shown below:

Truth Table for OR gate

Input (A)	Input (B)	Output F
0	0	0
0	1	1
1	0	1
1	1	1

Symbol of OR gate



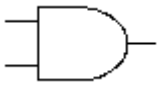
5. Compare the results in this truth table with those obtained in the truth table completed for step 1. Are they the same?

The OR gate turns on when _any_ input is 1.

If one input is a 1 and the other input is a 0, the output for the OR gate will be _1_.

The Boolean expression for the OR gate is _Y = A+B_.

Experiment F - AND logic gate



The 2-input AND logic gate has two inputs and the output will be a logical 1 only if both inputs are equal to one. (In future you will meet AND gates with more than 2 inputs).

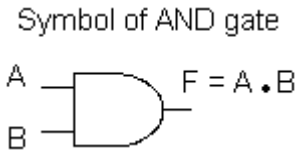
1. Simulate the AND gate. Repeat the steps shown in Experiment E and this time select the AND-2 instead of the OR-2 gate. As in the case of the OR gate, connect in two switches and a probe. Change the logic level of the switches and observe the probe status. Record the simulated behaviour of this 2-input AND gate in a truth table.

2. Repeat steps 2 to 4 of the OR gate experiment on the trainer but this time using the 74LS08 AND gate IC instead.

3. Record the results of your experiment in the truth table given below.

Truth Table for AND gate

Input (A)	Input (B)	Output F
0	0	0
0	1	0
1	0	0
1	1	1



4. Compare the results in this truth table with those obtained from your circuit simulation, i.e. results of step 1. Are they the same?

The AND gate turns on when _all_ inputs are 1.

If one input is a 1 and the other input is a 0, the output for the AND gate will be _0_.

The Boolean expression for the AND gate is _F = A*B_.

Experiment G - NOR logic gate

The NOR function states that when all inputs are 0, the output will produce a 1. The Boolean expression for NOR gate can be stated as A or B, NOT or it can be read as NOT (A or B).

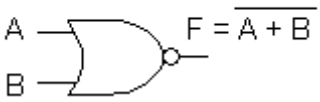
1. Using NI Multisim™, simulate the NOR gate and record the simulated behaviour of this 2-input NOR gate in a truth table.

2. Connect a 2-input NOR gate from the 74LS02 IC on the Logic Trainer and as in the previous cases, verify the functionality of the 2-input NOR gate by applying all the input combinations and recording the output responses or results in the truth table below.

Truth Table for NOR gate

Input (A)	Input (B)	Output F
0	0	1
0	1	0
1	0	0
1	1	0

Symbol of NOR gate



3. Compare the results obtained from your simulation to those that you obtained from the physical circuit. They should be the same.

The NOR gate turns on when all inputs are 0.

If one input is a 1 and the other input is a 0, the output for the NOR gate will be 0.

The Boolean expression for the NOR gate is Y = NOT(A+B)

Double click on the object to complete the Boolean Equation.

Experiment H - NAND logic gate

The NAND function states that when any or all inputs are 0, the output will produce a 1. The Boolean expression for NAND gate can be stated as A and B, NOT or it can be read as NOT (A and B).

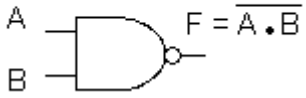
1. Simulate a 2-input NAND gate using NI Multisim™ and then record the simulated behaviour of the device in a truth table.

2. Connect a 2-input NAND gate from the 74LS00 IC on the logic trainer and hence, verify its functional behaviour by applying all the possible input combinations and recording its output responses in the truth table shown below.

Truth Table for NAND gate

Input (A)	Input (B)	Output F
0	0	1
0	1	1
1	0	1
1	1	0

Symbol of NAND gate



3. As in the previous cases, the results obtained from circuit simulation should be the same as those obtained from the physical circuit.

The NAND gate turns on when any input is a __1__.

If one input is a 1 and the other input is a 0, the output for the NAND gate will be __1__.

The Boolean expression for the NAND gate is Z = NOT(A*B)

Double click on the object to complete the Boolean Equation.

Instant Review An easy way to learn the operation of the various logic gates is to remember the input condition which turns on each gate (i.e. the combinations that produce a High or 1 at the output). Any other condition will not turn it on. Using this approach, the operation of digital logic gates can be summarized as follows:

1. The AND gate will have a **High** (or logic 1) at its output when **all** the inputs are **High**.

2. The OR gate will have **a High** at its output when **any** or all of its inputs are **High**.

3. The inverter's output will be the opposite or complement of its input.

4. The NAND gate will have a High at its output when any of its inputs are Low (or logic 0).

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5. The NOR gate will have a High at its output when all inputs are Low.

As a further reinforcement of your understanding of the devices covered in this experiment, you may want to think of similar statements to describe the input conditions required to produce a logic Low (or logic 0) at the output of each of the above gates.