SINGAPORE POLYTECHNIC ET1004

2019/2020 SEMESTER 2 EXAMINATION

Diploma in Electrical & Electronic Engineering DEEE 1st Year FT
Diploma in Computer Engineering DCPE 1st Year FT
Diploma in Aerospace Electronics DASE 1st Year FT
Diploma in Energy Systems and Management DESM 1st Year FT
Common Engineering Programme DCEP 1st Year FT

DIGITAL ELECTRONICS II

Time Allowed : 2 hours

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of **THREE** sections:

   Section A - 10 Multiple Choice Questions, 2 marks each.

   Section B - 6 Short Questions, 10 marks each.

   Section C - 1 Long Question of 20 marks.

3. Answer **ALL** questions in the accompanying Answer Booklet. Start each question in Sections B and C on a new page.

4. This Examination Paper consists of 9 pages

5. Your admission number and module class must be entered in the box provided on the cover page of your Answer Booklet.

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Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

A1. Refer to Figure A1**,** what is the clock frequency at the CLK input to Flip-Flop (F/F) A if the frequency of CLK signal at F/F H is 220 Hz and the counter is a naturally resetting type?

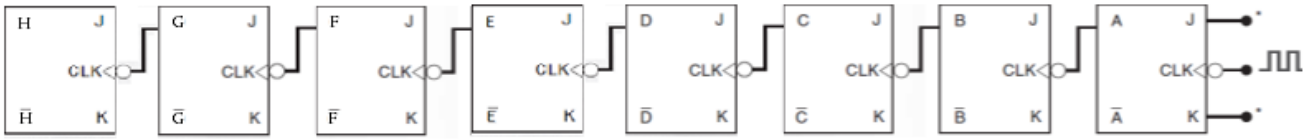

Figure A1

All J and K inputs are tied to Vcc and PRESET inputs are disabled.

(a) 14.08 kHz
(b) 28.16 kHz
(c) 56.32 kHz
(d) 112.64 kHz

A2. Refer to Figure A2**,** what is the new Modulus (Mod-number) that can be attained by the counter of Figure A1 if both of the F/F outputs, H and D, are connected to a two-input NAND gate which output is used to activate all the F/F active-low asynchronous CLEAR (CLR) inputs of the counter?

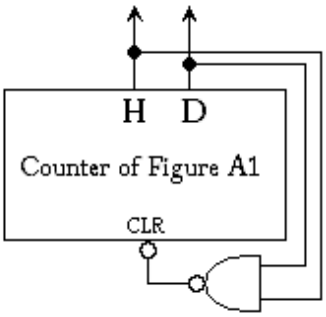

Figure A2

(a) Mod-120
(b) Mod-128
(c) Mod-136
(d) Mod-256

A3. A shift register circuit with **one** data input and **one** data output is a _____.

(a) serial-in, serial-out shift register
(b) parallel-in, serial-out shift register
(c) serial-in, parallel-out shift register
(d) parallel-in, parallel-out shift register

A4. In the 8-bits two's complement system, what does $1001\ 1001_2$ convert to in decimal?

(a) -25_{10}
(b) -101_{10}
(c) -103_{10}
(d) -153_{10}

A5. A parallel adder which can add signed binary numbers using the 2's complements signed numbering system has a range from -32768_{10} to $+32767_{10}$, is to be constructed using the 74LS83 IC, a 4-bit parallel adder IC. How many of these 74LS83 ICs are required to build this parallel adder circuit?

(a) 1
(b) 2
(c) 3
(d) 4

A6. The Figure A6 illustrates the current flow conditions between two logic gates. The current flowing at gate-2 I_B is best described by the symbol _____.

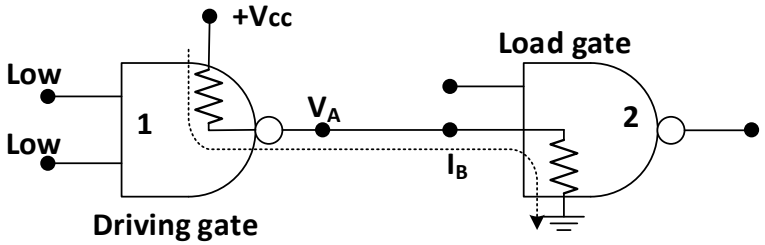

Figure A6

(a) I_{IL}
(b) I_{IH}
(c) I_{OL}
(d) I_{OH}

A7. A common means for comparing and measuring the performance of IC family is the _____.

(a) power consumption

(b) propagation delays
(c) speed-power product
(d) noise immunity

A8. What is the maximum possible number of data inputs for a multiplexer with 4 select inputs?

(a) 4 inputs
(b) 16 inputs
(c) 32 inputs
(d) 64 inputs

A9. A 7442 BCD decoder is connected as shown in Figure A9. Which one of its outputs has a level of low(0) if the select inputs of DCBA are 1010?

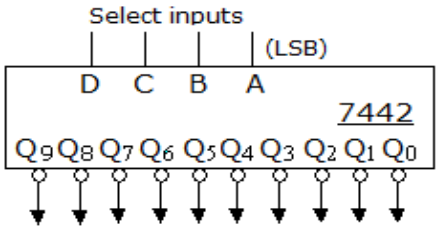

Figure A9

(a) Q_0
(b) Q_7
(c) Q_9
(d) none

A10. Which one of the following digital devices can be used to implement any logic function?

(a) Multiplexer
(b) Demultiplexer
(c) Encoder
(d) Decoder

Section B Short Questions (60 marks)

B1.(a) Determine the range, and the number of different values (in decimal) for the two following numbering systems. (6 marks)

(i) 18 bit (including sign bit) signed magnitude signed numbering system

(ii) 18 bit (including sign bit) 2's complement signed numbering system

(b) Use the 8 bits (including the sign bit) 2's complement system to perform the following addition:

Add -68_{10} to $+39_{10}$ (4 marks)

NB: **All workings** for question B1 must be **shown or marks** will **not** be awarded.

B2. The 74LS283 as shown in Figure B2 is a 4-bit parallel adder IC, i.e., a device that adds two sets of 4-bit numbers simultaneously.

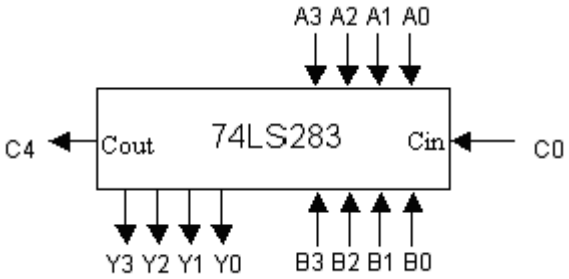

Figure B2

(a) If $A_3\ A_2\ A_1\ A_0 = 1\ 0\ 1\ 1$ and $B_3\ B_2\ B_1\ B_0 = 1\ 1\ 0\ 1$, what will be the binary value of the outputs C_4, $Y_3\ Y_2\ Y_1\ Y_0$ if $C_0 = 1$? (3 marks)

(b) How many magnitude bits (without counting the signed bit) are there in a parallel Adder that is built with ten (10) pieces of 74LS283 ICs for 2's complement numbering system addition? (2 marks)

(c) Express the following numbers in BCD format and hence, perform the addition of the numbers using BCD arithmetic.

Add $+81_{10}$ to $+29_{10}$ (5 marks)

B3. Each one of the following five statements comprising this question describes MSI devices, namely: **Encoder**, **Decoder**, **Multiplexer** and **De-multiplexer**. You are required to state in your answer booklet, the type of MSI device(s) being described by each statement. Ensure that your answers are labelled exactly according to each of the statements, i.e. [(a), (b)....(e)] or marks will not be awarded. (10 marks)

(a) This device converts a decimal key input to binary code.

(b) A logic circuit that has a single output with 16 data inputs and 4 select input lines.

(c) It has a single input which can be switched to one of the 8 outputs and it is also known to be a data distributor.

(d) This logic circuit is using a 4 binary input code to activate one of the 16 output lines.

(e) This device can be used for handling numbered key buttons and determines the BCD code generated.

B4. Figure B4 shows a Three-line-to-Eight-line decoder.

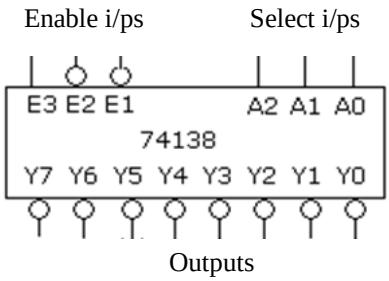

Figure B4

(a) Briefly describe what a Three-line-to-Eight-line decoder is. (2 marks)

(b) What should the logic levels to apply to the inputs, E3, E2 and E1, to enable the device? (2 marks)

(c) If the data at the inputs, A2 A1 A0 is 101_2 when the decoder is enabled, what will be the output logic states at each output Y_0 to Y_7? (2 marks)

(d) Assuming the decoder is enabled, what must be the combination applied to the inputs A2 A1 A0 (in this order) to select output Y_3? And what happens to the output Y_3 when it is selected? (1 mark)

(e) Using two 74138 ICs, show how these ICs can be connected as a 1-of-16 decoder. Ensure you label your circuit clearly or marks will not be awarded. (3 marks)

B5. Figure B5.1 shows a Mod-15 counter.

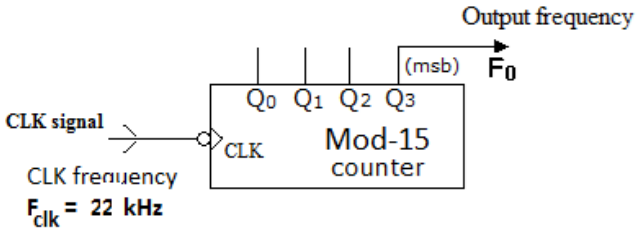

Figure B5.1

(a) What should be the output frequency at the Q3 of the Mod-15 counter if the frequency at its clock input is **22 kHz**? (3 marks)

(b) Using one 7493 IC, the symbol and internal circuit of which is given in Figure B5.2, show how you would connect the IC to function as the **Mod-15** counter. Draw your circuit in your answer booklet using only the 7493 symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will not be awarded. (5 marks)

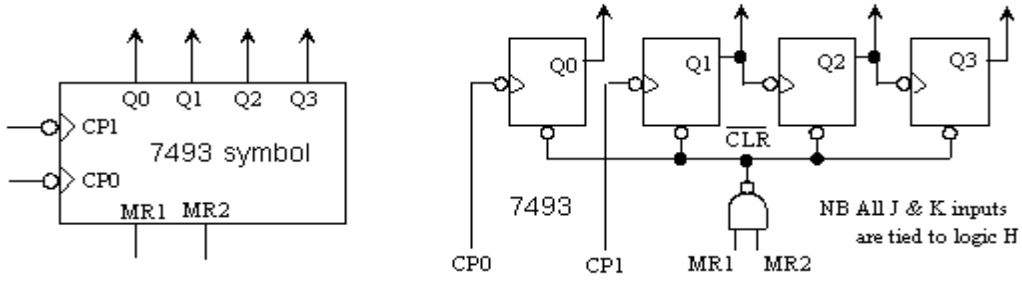

Figure B5.2

(c) Determine the duty cycle of the signal at the LSB output of the Mod-15 counter. (2 marks)

B6. Table B6 lists some of the electrical parameters of the **74ALS08 IC,** Quad 2-input AND gate Integrated Circuit.

Symbol	Parameters	Nominal	Min
V_{CC}	Supply voltage (V)	5	
V_{IH}	High level input voltage (V)		2
V_{IL}	Low level input voltage (V)	0.8	
V_{OH}	High level output voltage (V)		3
V_{OL}	Low level output voltage (V)	0.4	
$I_{CC(H)}$	Supply current (mA), outputs High	0.92	
$I_{CC(L)}$	Supply current (mA), outputs Low	3.1	
tp_{LH}	Propagation delay (nS)	11	
tp_{HL}	Propagation delay (nS)	8	

Table B6

(a) What does the description "Quad 2-input AND gate" mean? (2 marks)

(b) What is the parameter for maximum output voltage when the output is at logic High, and what is the value of this voltage? (2 marks)

(c) What is the expression for calculating the power dissipation of an IC? Hence, calculate the power dissipation of the 74ALS08 IC on a per gate basis. (3 marks)

(d) Calculate the High and Low level noise margins for the IC. What is the overall noise margin? (3 marks)

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Section C Long Question (20 marks)

C1. The following Boolean expression is to be implemented with an 8-input multiplexer:

$$Z = CBA + CB\overline{A} + \overline{C}BA + \overline{C}B\overline{A} + \overline{C}\,\overline{B}A$$

(a) From the given Boolean expression, determine the truth table for output Z with the input variable C is the MSB and A is the LSB. (4 marks)

(b) Using one 74151 multiplexer IC, show how you would implement the output Z using the truth-table derived in part (a). The 74151 symbol given in Figure C1.1 is to be used and input C should be assigned to the multiplexer SELECT input S2. Your completed circuit must be clearly labelled or marks will be deducted. (6 marks)

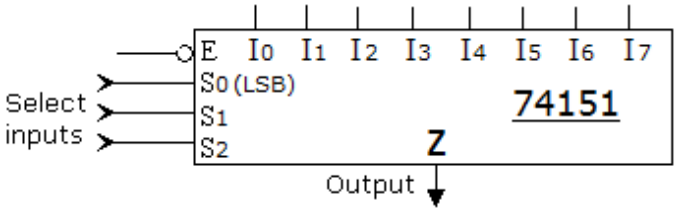

Figure C1.1

(c) Show how you would connect one 74151 IC (Figure C1.1) to function as a 5-to-1 multiplexer. In your completed diagram, label the data inputs as D0 D1 D2 D3 D4 and the SELECT inputs as A_2 A1 A0, where the subscript of 0 denotes the LSB. Unused inputs should be indicated as N.C. (i.e. No Connection). (4 marks)

(d) Given the 74151 multiplexer connected as shown in Figure C1.2, determine the logic function (i.e. Boolean expression) implemented at the output X. From the resultant expression obtained, implement the output function with only one logic gate.
Hint: Create a truth table with C, B and A as input variables, X as output.
(6 marks)

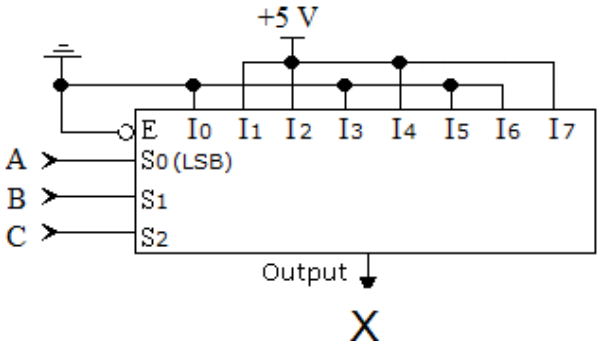

Figure C1.2

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