B2. Figure 1 shows the excitation table for an FSM. The FSM has an input P, and two output Y and Z. Both flip-flops response to a PGT clock signal.

Present state		Input	Output		Next state	
Q_A	Q_B	P	Y	Z	D_A	D_B
0	0	0	0	0	0	0
		1	0	0	1	1
0	1	0	0	1	0	1
		1	0	0	1	1
1	0	0	0	1	0	0
		1	0	0	1	1
1	1	0	1	1	0	1
		1	1	0	1	1

(a) Derive the minimized Boolean equations for Y, Z, D_A and D_B.

(b) Draw the schematic diagram for the FSM using the minimum number of logic gates.

$Y = Q_A Q_B$

Z	P=0	P=1
Q_AQ_B = 00	0	0
01	1	0
11	1	0
10	1	0

$Z = P'Q_A + P'Q_B = P'(Q_A + Q_B)$

$Z = \overline{P} \cdot (Q_A + Q_B)$

$Z = \overline{P + (\overline{Q_A + Q_B})}$

D_A	P=0	P=1
Q_AQ_B = 00	0	1
01	0	1
11	0	1
10	0	1

$D_A = P$

D_B	P=0	P=1
Q_AQ_B = 00	0	1
01	1	1
11	1	1
10	0	1

$D_B = Q_B + P$