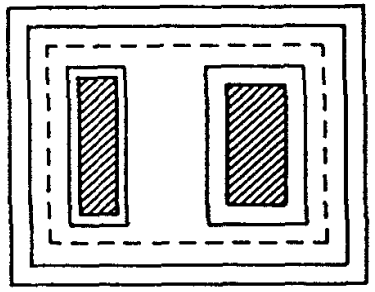
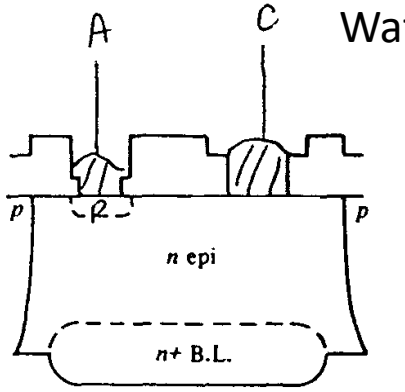
pn Junction Diode

IC Designer



(a)



(b)

Wafer Fab Engineer

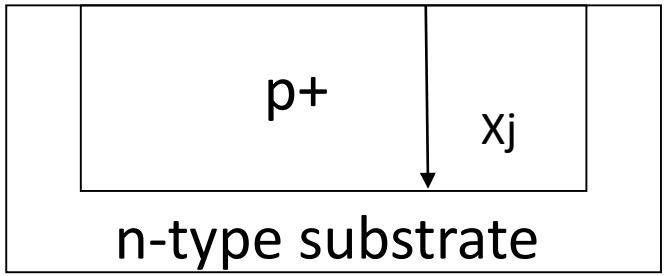
All Electrical & Electronics Engineer know the circuit symbol of the diode

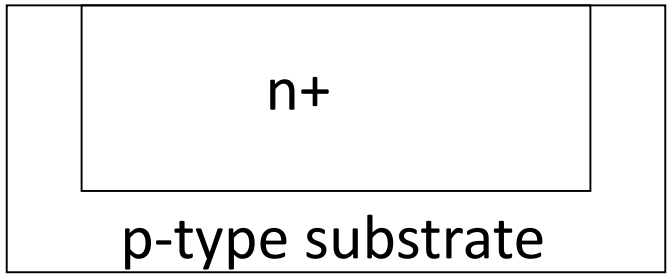
a) top view b) side view

2 Possibilities:

- p^+n diode: p+ region on n-type substrate or n epi with Buried Layer (BL)
- n^+p diode: n+ region on p-type substrate or p epi with Buried Layer (BL)

pn Junction Diode- Simplified





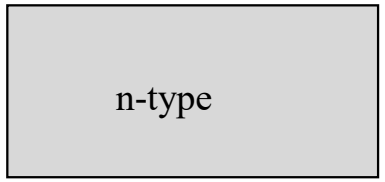
- p-type: majority carriers are holes doped with acceptors, group III elements.
- n-type: majority carriers are free electrons doped with donors, group V elements.
- p^+n diode means it has more holes in the region than there are free electrons in the substrate
- n^+p diode means it has more free electrons in the region than there are holes in the substrate.
- The junction depth Xj is the concern of wafer fabrication engineers as it will affect the characteristics of the diode, for example the Breakdown Voltage of the diode.
  (Characteristics of diode in relation to fabrication to be covered in Advanced Wafer Fabrication Technology)

Mask Step versus Process

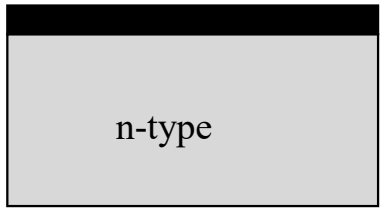
- A mask step is when the mask generated from IC Design is required. It is used in conjunction with the process of photolithography.
- A mask step defines the pattern on the surface of the wafer based on the pattern of the mask, which is the placement & dimensions of the components of the IC.
- A mask step consists of a series of processes, including photolithography, to achieve a particular cross section structure of the component at the correct place & dimension define by the mask.
- A series of mask steps are required to complete the component with the final cross section structure of the component at the correct place & dimension.
- The lesser the masks required the cheaper is the fabrication cost therefore this must be considered during chip design.

pn Junction Diode Process Steps

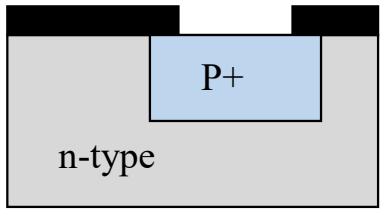
The fabrication of the pn junction diode is considered to illustrate the processes & mask steps required.



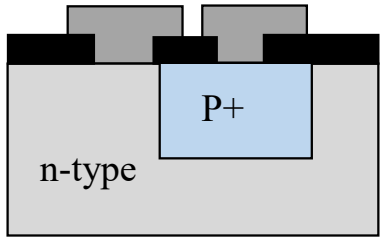
Starting material: n-type silicon substrate.



Oxidation process to grow a layer of silicon dioxide thickness.



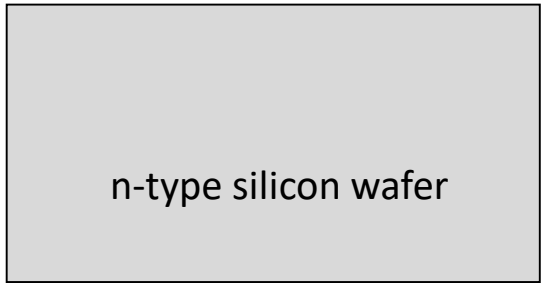
Mask Step 1: Diffused p+ region.

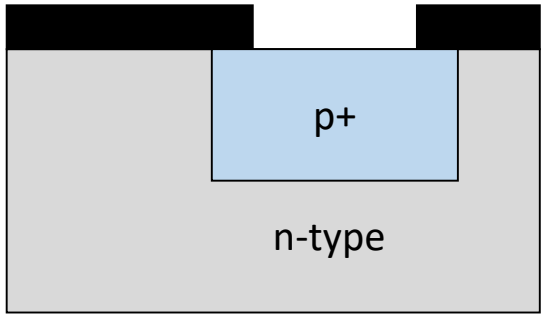


Mask Step 2: Contact Opening for anode & cathode.

Mask Step 3: Aluminium metallization & components interconnection patterning.

pn Junction Diode Process Steps





Mask Step 1 (Diffused p+ Region):

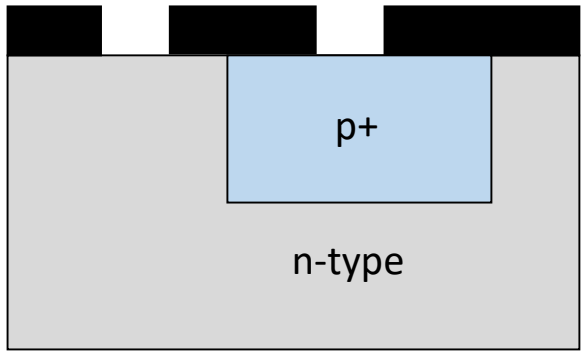
Oxidation Process:
A layer of silicon dioxide is grown all over the wafer surface to help block dopants during diffusion.

Photolithograpy:
To transfer the mask pattern to the photoresist. The mask is required to define the location & dimension (pattern) of the p region with the help of photoresist & UV light.

Etching:
To remove the silicon dioxide not protected by the photoresist & reveal the silicon for diffusion followed by photoresist removal which is now no longer needed.

Diffusion:
To introduce dopants into the defined region not protected by the silicon dioxide.

pn Junction Diode Process Steps



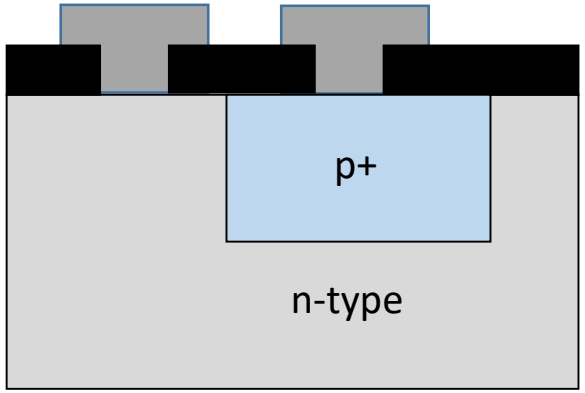
Mask Step 2 (Contact Opening):

Re-Oxidation Process:
Oxide removal by etching & a new layer of silicon dioxide thickness is grown all over the wafer surface for the purpose of contact opening & insulation.

Photolithograpy:
To transfer the mask pattern to the photoresist. The mask is required to define the location & dimension (pattern) of the contact opening with the help of photoresist & UV light.

Etching:
To remove the silicon dioxide not protected by the photoresist & reveal the openings to p+ region & substrate for contact by metal followed by photoresist removal, which is now no longer needed.

pn Junction Diode Process Steps



Mask Step 3 (Metallization & Interconnection):

Metal Deposition Process (Any PVD technique):
Aluminium is deposited all over the wafer surface to make contact with the p+ region (anode) & substrate (cathode) of the diode.

Photolithograpy:
To transfer the mask pattern to the photoresist. The mask is required to define the interconnection pattern of the conducting connecting lines of all the components of the IC with the help of photoresist & UV light.

Etching:
To remove the aluminium not protected by the photoresist followed by photoresist removal, which is now no longer needed.