SINGAPORE POLYTECHNIC

2014/2015/S2 – MST

SAS code: **TST1**

MODULE: DIGITAL ELECTRONICS 2 MODULE CODE: ET1004

COURSE/YEAR: DASE/DEEE/DCPE/DESM/DCEP/1FT

No	SOLUTION

SECTION – A

A) 1. (b) 2. (c) 3. (a) 4. (c) 5. (d) 6. (b) 7. (a)
8. (c) 9. (d) 10. (c)

SECTION – B

B1) **Add -53_{10} to $+88_{10}$**

(a)

	sign	64	32	16	8	4	2	1	
+53 =	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	← +ve Equvalent
-53 =	**1**	**1**	**0**	**0**	**1**	**0**	**1**	**1**	← 2's complement
+88 =	**0**	**1**	**0**	**1**	**1**	**0**	**0**	**0**	←
+35 = 1	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**	←

(b) **Add $+57_{10}$ to $+35_{10}$ in BCD**

+57 =	0	1	0	1	0	1	1	1	← BCD of 57
+35 =	**0**	**0**	**1**	**1**	**0**	**1**	**0**	**1**	← BCD of 35
	1	**0**	**0**	**1 0**	**1**	**1**	**0**	**0**	←
					+1	**1**	**0**		← Adjust by +6
92 =	**1**	**0**	**0**	**1**	**0**	**0**	**1**	**0**	← **correct Result**

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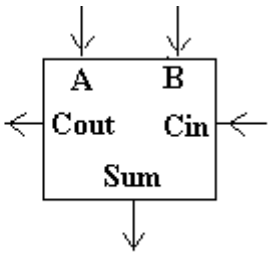
No	SOLUTION

B2

(a)

Symbol of Full Adder



(b)

A	B	Cin	Cout	Sum
0	0	0	0	0
0	0	1	0	1
0	1	0	0	1
0	1	1	1	0
1	0	0	0	1
1	0	1	1	0
1	1	0	1	0
1	1	1	1	1

NB

Output combinations obtained by adding A + B + Cin

$$\text{Sum} = \overline{A}\,\overline{B}\,Cin + \overline{A}\,B\,\overline{Cin} + A\,\overline{B}\,\overline{Cin} + A\,B\,Cin$$

$$\text{Cout} = \overline{A}\,B\,Cin + A\,\overline{B}\,Cin + A\,B\,\overline{Cin} + A\,B\,Cin$$

(c)

$$\begin{aligned}\text{Sum} &= \overline{A}\,\overline{B}\,Cin + \overline{A}\,B\,\overline{Cin} + A\,\overline{B}\,\overline{Cin} + A\,B\,Cin \\ &= \overline{A}\,(B\,\overline{Cin} + \overline{B}\,Cin) + A\,(\overline{B}\,\overline{Cin} + B\,Cin) \\ &= \overline{A}\,(B \oplus Cin) + A\,\overline{(B \oplus Cin)} \\ &= A \oplus (B \oplus Cin) \\ &= A \oplus B \oplus Cin\end{aligned}$$

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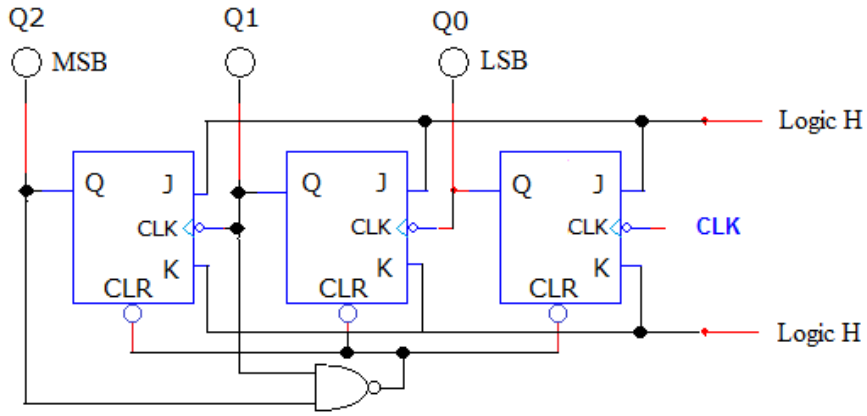
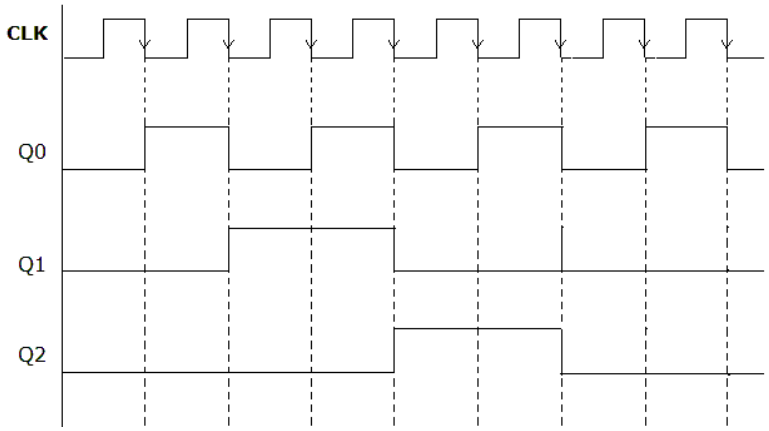
No	SOLUTION
B3 (a)	 Important points to note Correct Connections between the three flip-flops. Logic H to the J and K inputs of each JK flip-flop for toggle mode.
(b)	
(c)	Given the clock frequency is 3000 Hz Frequency at Q2 (MSB) = 3000/6 = 500 Hz Duty cycle at Q2 (MSB) = 2/6 *100 % = 33.3%

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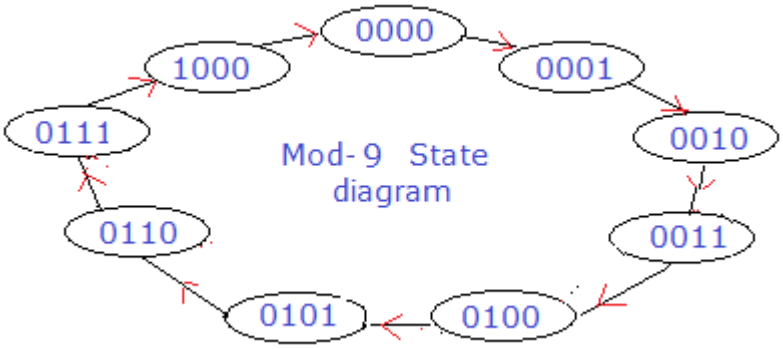
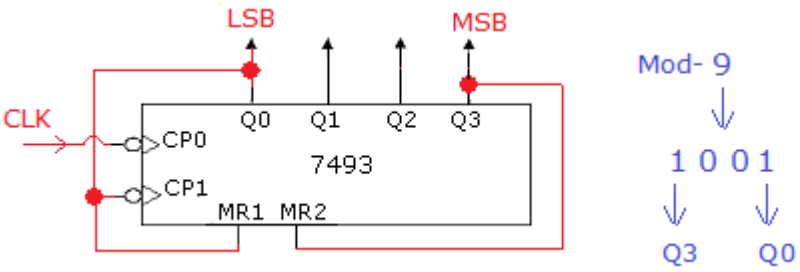
	SOLUTION
C1 (a)	**Section C (25 marks)** Counter with table given is a Mod-9 counter
(b)	
(c)	
	NB: Important points to note: Use of 4 flip-flops & connection between flip-flops Indicate correct MSB & LSB outputs. Correct CLK input used . Correct feedback from outputs to MR1 and MR2.

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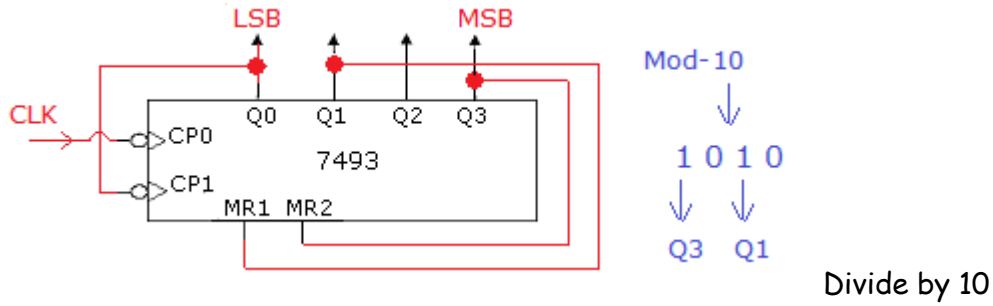
No	SOLUTION
(d)	If the signal frequency at the Mod-9 MSB output is 10kHz, then the clock frequency applied is 9* 10 kHz = 90 kHz
(e)	To obtain a 1 kHz signal from 10 kHz, a mod-10 counter is required. Using one 7493, the connections is as follows:  Divide by 10 Important points to note Q0 to CP1 connection for 4 Flip-flops connection. CLK to CP0. MSB and LSB indication. Correct Feedback from outputs to MR1/MR2.

SOLUTIONS