2015/2016 S2 MID-SEMESTER TEST

SAS code: **MST**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Energy Systems Management DESM 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet, unless indicated otherwise.

4. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

5. There are 6 pages in this paper.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

1. What is the range of decimal values that can be represented by a 16-bit (including sign bit) 2's complement signed numbering system?

(a) $+15_{10}$ to -16_{10} (b) $+63_{10}$ to -64_{10}

(c) $+127_{10}$ to -128_{10} (d) $+32767_{10}$ to -32768_{10}

2. The two's complement of 00001111_2 is _____.

(a) 11110000_2 (b) 11110010_2

(c) 11100001_2 (d) 11110001_2

3. In the two's complement signed numbering system, if the addition of two positive numbers gives a sign bit of 1 for the resultant Sum, how should this result be interpreted?

(a) The resultant Sum is a positive number.

(b) An arithmetic overflow has occurred.

(c) The sign bit must be discarded to interpret the result.

(d) The resultant Sum is a negative number.

4. If the logic inputs to a 7483, 4-bit parallel adder IC, are as shown in figure A4 what would be the logic levels at the outputs C4 S3 S2 S1 S0?

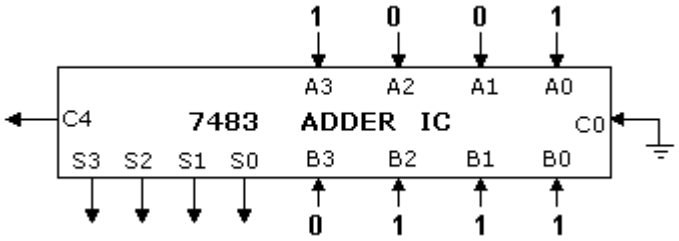

Figure A4

(a) 00000_2 (b) 01111_2

(c) 10000_2 (d) Invalid due to overflow

5. What is the Mod-number of a binary counter that counts from 0000_2 to 1101_2?

(a) Mod 11_{10} (b) Mod 12_{10} (c) Mod 13_{10} (d) Mod 14_{10}

6. The signal frequency at the MSB output of a Mod-12_{10} counter is 600 Hz, what is the frequency of the input clock signal frequency applied to the counter?

(a) 720_{10} Hz (b) 7200_{10} Hz (c) 50_{10} Hz (d) 600_{10} Hz

7. _____ are often used whenever clock pulses are to be counted and the results displayed in decimal using the 7 segment LED display.

(a) BCD counters (b) Mod 2^N parallel counters with N > 4

(c) Mod 2^N ripple counters with N > 4 (d) serial-in, serial-out shift registers

8. The number of JK flip-flops required to build a 16-bit serial-in, serial-out shift register is _____.

(a) 4_{10} (b) 8_{10} (c) 16_{10} (d) 64_{10}

9. The circuit shown in Figure A9 is a _____.

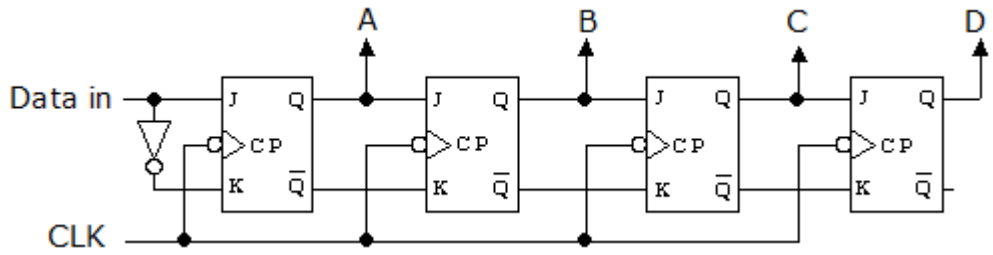

Figure A9

(a) parallel-in, parallel-out shift register

(b) Mod-16_{10} parallel counter.

(c) serial-in, parallel-out shift register

(d) Mod-16_{10} ripple counter.

10. Which one of the following statements pertaining to Counters is False?

(a) In a binary up-counter, the count increases by 1 for every clock pulse applied.

(b) In ripple-counters, the number of flip-flops required increases when the mod-number decreases.

(c) In asynchronous counters, the overall propagation delay increases with the number of flip-flops used.

(d) A decade counter divides its clock frequency by a factor of 10_{10} at its MSB output.

Section B (45 marks)

B1(a) Use BCD arithmetic to add the following decimal numbers.

(i) $+23_{10}$ to $+66_{10}$

(ii) $+76_{10}$ to $+37_{10}$

(7 marks)

(b) Use the 8 bits (including the sign bit) 2's complement system to perform the following addition.

Add -48_{10} to $+67_{10}$

(8 marks)

NB: All steps and **workings** for this question **must be shown** or marks will be deducted.

B2 Two 74LS283 ICs (each a 4-bit parallel Adder IC) are connected as shown in figure B2.

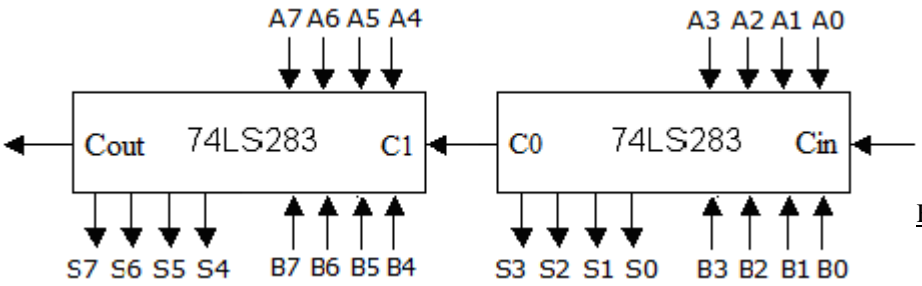

Figure B2

(a) Given: $A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0 = 0\ 1\ 0\ 0\ 0\ 1\ 1\ 1_2$ and,

$B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0 = 1\ 1\ 0\ 1\ 1\ 1\ 1\ 0_2$ respectively,

What will be the binary value at the outputs: $C_{out}\ S_7\ S_6\ S_5\ S_4\ S_3\ S_2\ S_1\ S_0$ for **Cin = 1**?

(4 marks)

(b) If 8 bits (including the sign bit) 2's complement signed arithmetic is used in part (a), what are the equivalent decimal numbers being added (i.e. the decimal equivalent at the A inputs & the decimal equivalent at the B inputs) and the decimal Sum result?

(7 marks)

(c) If a 32-bit parallel adder is to be constructed using the 74LS283 IC, how many 74LS283 ICs are required?

(4 marks)

B3. For the circuit shown in figure B3.1, determine the following:

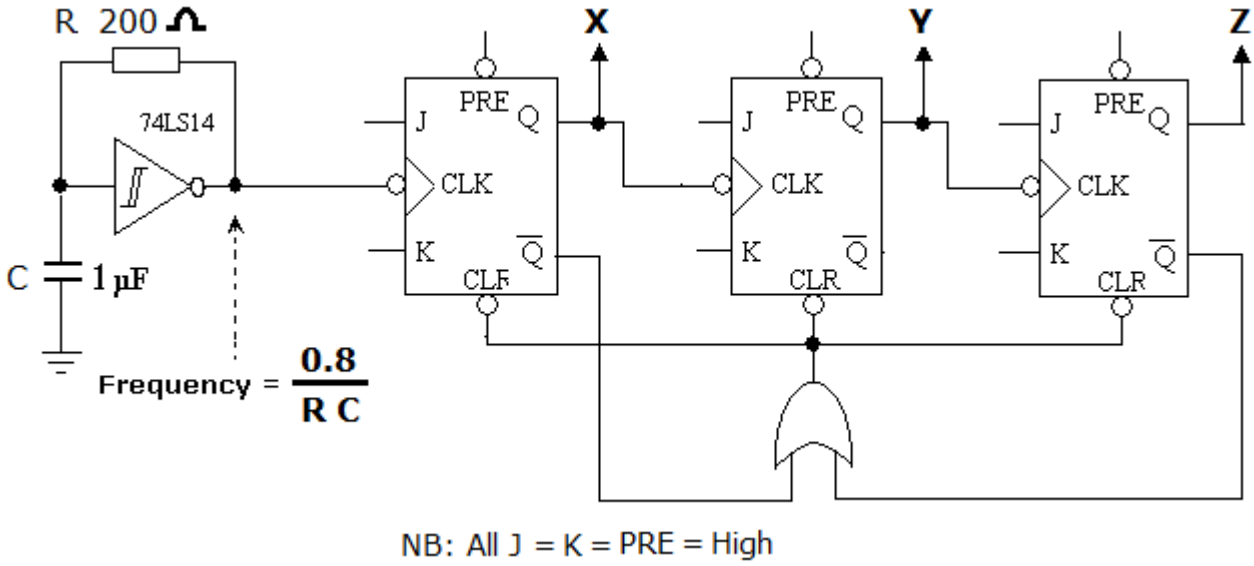

Figure B3.1

(a) Calculate the CLK (clock) frequency generated by the Astable circuit connected to the CLK input of the 3-bit counter in figure B3.1, given that frequency = (0.8)/RC.

(4 marks)

(b) In figure B3.1, which flip-flop output is the LSB and which flip-flop output is the MSB?

(2 marks)

(c) Analyze the counter circuit carefully and determine its modulus (i.e. mod-number). Take note that the feedback to clear the counter is from the complementary outputs of flip-flops X and Z and an OR gate is used instead of the usual NAND gate.
Hint: use alternate logic symbol or DeMorgan's theorems to analyze the feedback circuit.

(4 marks)

(d) Calculate the signal frequency and duty cycle at the counter MSB output.

(4 marks)

Section C (25 marks)

C1. Figure C1.1 is a block diagram showing three counters connected in cascade, a Mod-8 counter, a 4-bit BCD counter and a counter with a Mod-number that is not stated.

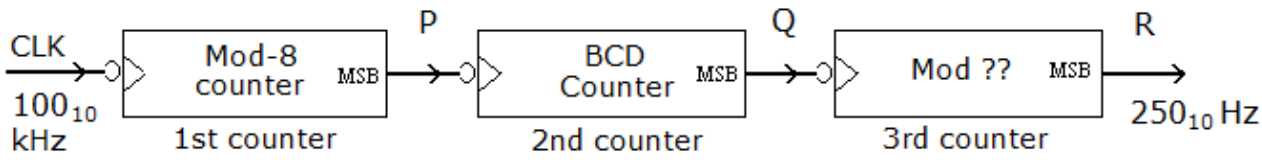

Figure C1.1

(a) What is the modulus (i.e. mod number) of the 4-bit BCD counter?

(3 marks)

(b) If the CLK signal frequency to the Mod-8 counter is 100_{10} kHz, what are the signal frequencies at nodes P and Q in the cascade of three counters? Take note that P and Q are the MSB outputs of each respective counter.

(6 marks)

(c) If the signal frequency at output R is 250_{10} Hz, what is the modulus of the third counter in the cascade? Hence, determine the overall modulus of the cascade of three counters.

(6 marks)

(d) Using one 7493 counter IC, symbol and internal circuit as shown in Figure C1.2, construct the 4-bit BCD counter. Ensure that all inputs and outputs are clearly labelled.

(7 marks)

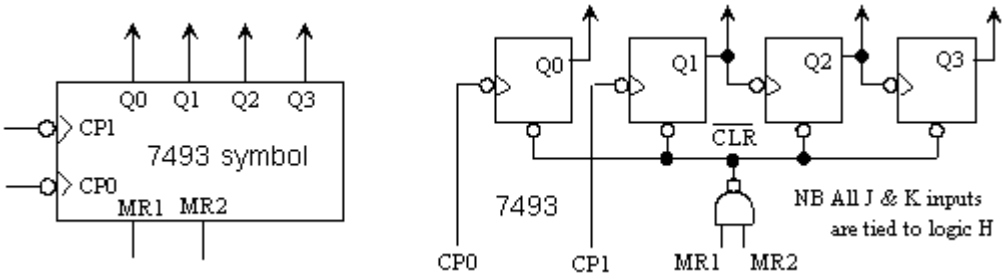

Figure C1.2

(e) If a 50% duty cycle signal (perfect square wave) is required at node R (250_{10}Hz signal), how should the cascade of three counters be re-arranged so that this can be achieved? Note that no additional components or counters are required to achieve this.

(3 marks)

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