2012/2013 S2

SINGAPORE POLYTECHNIC ET1004

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

16-bit gives 2^{16} numbers; half being +ve and half being -ve.

1. What is the range of decimal values that can be represented by a 16-bit (including sign bit) 2's complement signed numbering system?

(a) $+15_{10}$ to -16_{10} (b) $+63_{10}$ to -64_{10}

(c) $+127_{10}$ to -128_{10} (d) $+32767_{10}$ to -32768_{10}

Ans: (d)

2. How many 74LS93 (4-bit) counter ICs are required to construct a BCD counter that counts to a maximum of 999_{10}?

BCD counter: 0000 to 1001 (i.e. 0-9)

(a) 2_{10} (b) 3_{10}

(c) 4_{10} (d) 6_{10}

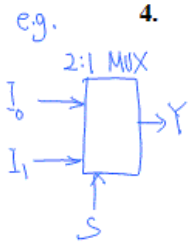
(Each BCD counter will increment the next one when it rolls over from 9 back to 0.) **Ans: (b)**

3. A mod-16 down counter is clocked by a signal of 256 kHz, at 30% duty cycle. The signal frequency and duty cycle at its MSB output will be: *MSB freq. = Clock freq. / MOD = 256 kHz / 16*

(a) 64 kHz, 30% duty cycle (b) 64 kHz, 50 % duty cycle

(c) 16 kHz, 30% duty cycle (d) 16 kHz, 50% duty cycle

If MOD = 2^N, the MSB is always a square-wave, i.e. at 50 % duty cycle. (The duty cycle of the clock has no effect to the outputs.) **Ans: (d)**



4. A Multiplexer accepts data from one of -

(a) many input lines and transfers it to one of the select lines.

(b) many input lines and transfers it to one output line.

(c) many input lines and transfers it to several output lines.

(d) many input lines and transfers it to multiple select lines.

Ans: (b)

5. How many Select inputs are required for a Decoder with 1 enable input and 64 data outputs?

(a) 1_{10} (b) 3_{10}

(c) 6_{10} (d) 64_{10}

Ans: (c)

6. What is the correct mathematical expression to calculate the average power consumed by a TTL digital IC?

P = Vcc x Icc

Average P = Vcc x Average Icc

(a) $(I_{OH} + I_{CCH})/2 * V_{OH}$

(b) $(I_{CCL} + I_{OL})/2 * V_{CC}$

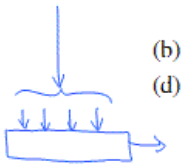
(c) $(I_{OL} + I_{OH})/2 * V_{OL}$

(d) $(I_{CCH} + I_{CCL})/2 * V_{CC}$

Icc when all outputs are High / Low

Ans: (d)

7. A shift register which inputs multiple data bits simultaneously but transfer out data one bit at a time is a:



(a) parallel-in, serial-out register (b) parallel-in, parallel-out register

(c) serial-in, parallel-out register (d) serial-in, serial-out register

Ans: (a)

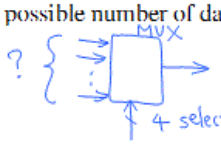
8. In the **8-bit** (including the sign bit) two's complement signed numbering system, what does the binary number 10000000 equates to when converted to decimal?

(a) -128_{10} *1000 0000 - Biggest -ve number* (b) -1_{10} *1111 1111*

(c) $+127_{10}$ *0111 1111 - Biggest +ve number* (d) Zero *0000 0000*

Ans: (a)

9. What is the maximum possible number of data inputs for a multiplexer with 4 select inputs?



(a) 4_{10} inputs (b) 16_{10} inputs

(c) 32_{10} inputs (d) 64_{10} inputs

Ans: (b)

10. A 74147 Decimal-to-BCD priority encoder circuit is connected as shown in Figure A10. What is the binary code generated at its outputs? *It encodes the highest input at its output.*

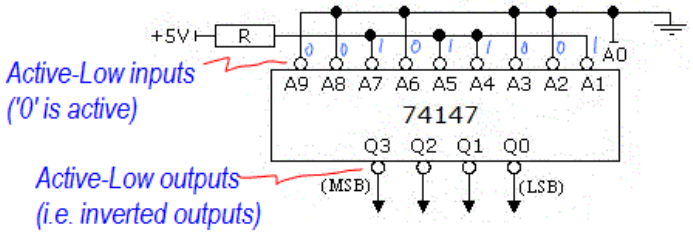


Figure A10

(a) $Q_3 Q_2 Q_1 Q_0 = 1001$ *Inversion of 0110 (6)* (b) $Q_3 Q_2 Q_1 Q_0 = 1000$ *Inv. of 0111 (7)*

(c) $Q_3 Q_2 Q_1 Q_0 = 0111$ *Inversion of 1000 (8)* (d) $Q_3 Q_2 Q_1 Q_0 = 0110$ *Inv. of 1001 (9)*

Ans: (d)

B1 (a)
+38 = 0010 0110
+53 = 0011 0101
0101 1011

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Section B Short Questions (60 marks)

B1. Perform the following operation using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit.

(a) Add $+38_{10}$ to $+53_{10}$ (4 marks)

(b) Add -32_{10} to $+77_{10}$ (6 marks)

B1 (b)
+32 = 0010 0000
Inv. : 1101 1111
+1 : 1
1110 0000 = -32

-32 = 1110 0000
+77 = 0100 1101
1 0010 1101
+45 (8-bit)
Discard

NB: All workings in question B1 must be shown or marks will not be awarded.

B2(a) The 74LS138 is a **1-of-8** decoder device and has a symbol as shown in figure B2.1. What is another name for this decoder? If output **Y7** of the 74LS138 decoder is to be selected, what logic levels are required at both the **Enable** and **Select** inputs? (5 marks)

1-of-8 decoder
(Only 1 of the 8 outputs can be ON)

Also known as 3-to-8 decoder.
(3 select inputs to 8 outputs)

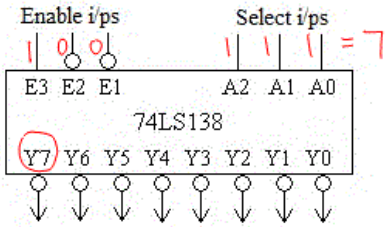


Figure B2.1

(b) Figure B2.2 shows a partially completed circuit diagram of two 74LS138 decoder ICs being connected as a 1-of-16 decoder. Copy figure B2.2 and complete in your answer booklet, the circuit diagram of this 1-of-16 decoder. Ensure that you label all inputs and outputs as according to the labels used in figure B2.2.
Hint: Output O0 is selected when select inputs S3 S2 S1 S0 = 0 0 0 0 and Output O15 is selected when S3 S2 S1 S0 = 1 1 1 1.
(5 marks)

S3 = 1 : Left decoder enabled, right decoder disabled.
S3 = 0 : Left decoder disabled, right decoder enabled.

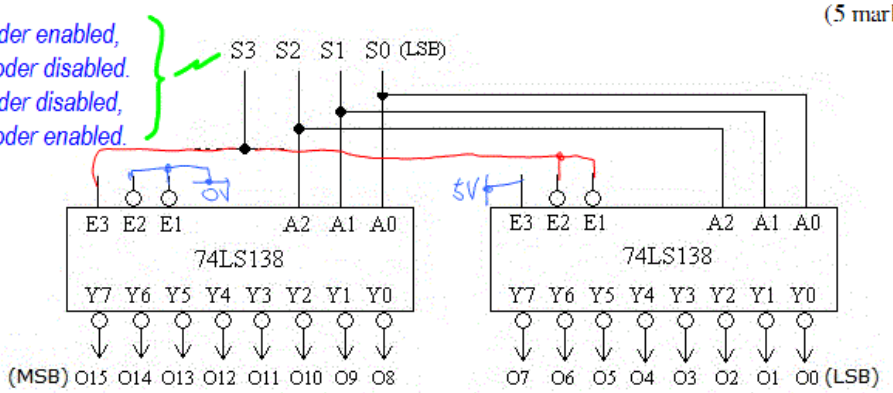


Figure B2.2

Note:
When a decoder is **enabled**, one of its outputs (the selected one) will be on.
When a decoder is **disabled**, all of its outputs will be off.

B3 The 74LS283 as shown in figure B3, is a 4-bit parallel adder IC, i.e. a device that adds two sets of 4-bit numbers simultaneously.

4-bit adder operation: ***B3 (a)***

A3 A2 A1 A0	*0101*
B3 B2 B1 B0	*1101*
+ Cin	*+ 1*
Cout Y3 Y2 Y1 Y0	***1 0011***

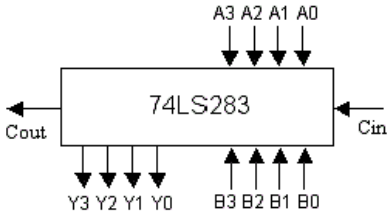


Figure B3

(a) If A3 A2 A1 A0 = 0 1 0 1 and B3 B2 B1 B0 = 1 1 0 1, respectively, what will be the binary value of the outputs Cout, Y3 Y2 Y1 Y0 with Cin = 1? (4 marks)

Cout, Y3 Y2 Y1 Y0 = ***1, 0011***

(b) If 4 bits (including the sign bit) 2's complement signed arithmetic is used in part (a) above, what are the equivalent decimal numbers being added and the decimal sum result? (4 marks)

A = 0101 = ***+5****, B = 1101 =* ***-3****, Y = 0011 =* ***+3***

(c) How many 74LS283 ICs are needed to build a **16 bit** parallel Adder? (2 marks)

Four*. (Each IC will take care 4 of the 16-bit.)*

Working:
Let 1101 = -x
Invert: 0010 +1 = 0011 = +3 = +x
Hence -x = ***1101 = -3***

B4 Each of the 5 statements comprising this question describes a particular type of counter or shift register. You are required to state in your answer booklet, the type of counter or shift register being described by each statement. Ensure that your answers are labelled exactly according to each of the statements i.e. **[(a), (b)....(e)]** or marks will not be awarded. (10 marks)

(a) This counter allows its outputs to be displayed as decimal digits through the use of the seven-segment LED display and appropriate decoder.

BCD counter *(i.e. MOD-10)*

(b) Each flip-flop of this asynchronous counter functions as a divide-by 2 circuit.

Ripple counter *- the output freq. of each flip-flop is half of the freq. at its clock.*

(c) This shift register circuit can be used to delay a signal by a fix number of clock cycles that correspond to the number of flip-flops used.

Serial-In Serial-Out *Shift Register*

(d) This shift register circuit has only one data input and several data outputs.

Serial-In Parallel-Out *Shift Register*

(e) This counter divides its input clock signal frequency by its mod-number.

Divide-by-N *counter (i.e. mod-N counter)*

B5 The 74151 is described as an 8- to-1 multiplexer. Figure B5.1 shows the symbol of this multiplexer.

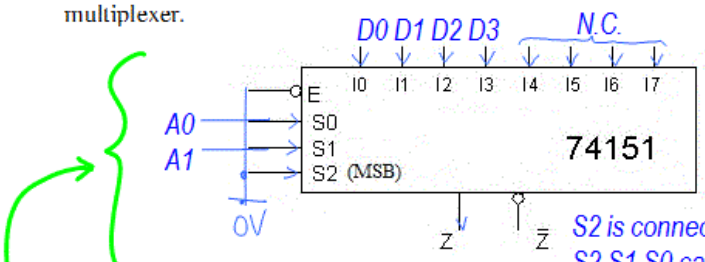


Figure B5.1

S2 is connected to '0' so that S2,S1,S0 can only be 000 (0) to 011 (3), selecting one of D0 to D3.

(a) Using one 74151 8-input multiplexer IC, show how the 74151 can be connected as a 4-to-1 multiplexer. In your completed diagram, label the required data inputs as D_0 D_1 D_2 D_3 and the select inputs as A_1 A_0, where the subscript of 0 denotes the LSB. Unused inputs should be indicated as N.C.

(4 marks)

(b) Given the 74151 multiplexer connected as shown in figure B5.2, determine the logic function (i.e. Boolean expression) implemented at both outputs: Z and $\overline{Z}$. From the resultant expressions obtained, what are the generic names of these two output functions?

Hint: Create a truth table with B and A as input variables and Z, $\overline{Z}$ as outputs.

(6 marks)

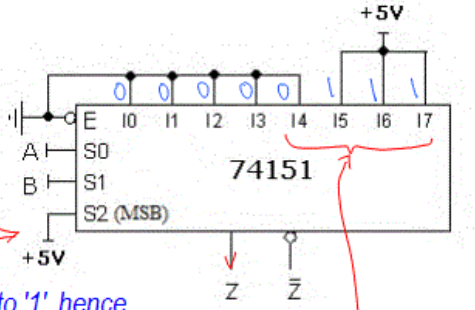


Figure B5.2

S2 is connected to '1', hence S2,S1,S0 can only be 100 (4) to 111 (7), selecting one of I4 to I7.

B A	Z
0 0	I4 = 0
0 1	I5 = 1
1 0	I6 = 1
1 1	I7 = 1

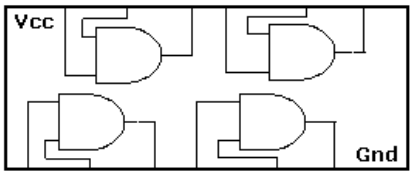
0 1 1 0 1 1

$Z = B'.A + B.A' + B.A$
$= B'.A + B.(A' + A)$
$= B'.A + B$
$Z = B + A$

Recall:
$x + x'.y$
$= x + y$

Z is the OR function of A and B while **Z' is the NOR** function.

B6. Table B6 lists the typical values of the AC and DC **parameters** (characteristics) for three different logic families of the 7408 Quad 2-input AND gate **Integrated Circuit**.



7408

Parameter	Unit	Device A	Device B	Device C
Vcc	V	5	5	5
$V_{IH\ (min)}$	V	2	2	2
$V_{IL\ (max)}$	V	0.8	0.7	0.8
$V_{OH\ (min)}$	V	2.4	2.7	2.5
$V_{OL\ (max)}$	V	0.4	0.5	0.5
Icc_H	mA	16	2.4	10
Icc_L	mA	32	6.6	22
tp_{LH}	nS	15	10	2
tp_{HL}	nS	14	9	2

Table B6

(a) Calculate the average power consumption **per gate** for device **A**. (4 marks)

(Note that there are 4 gates on the device.)

Average P = Vcc x average Icc = 5V x (16 mA + 32 mA) / 2

*= 120 mW for device A --> i.e. 120 / 4 = **30 mW per gate***

(b) By comparing the values of the relevant parameters given in Table B6, which device has the **lowest** power dissipation? Note that **you are not required** to calculate the actual power dissipation for the devices. (2 marks)

A**: 5V x (16 mA + 32 mA) / 2 = **120 mW

B**: 5V x (2.4 mA + 6.6 mA) / 2 = **22.5 mW

C**: 5V x (10 mA + 22 mA) / 2 = **80 mW

(B is the lowest.)

(c) Which device has the lowest value of output voltage for logic High and what is the value of this voltage? (2 marks)

V_{OH}

A has the lowest, at 2.4V

(d) By comparing the values of the relevant parameters given in Table B6, which device can operate at the **highest** frequency? As in part (b), numerical calculations are not required. (2 marks)

*The one with **smallest delay** can operate at highest frequency - **Device C***

t_{PHL}, t_{PLH}

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Section C Long Question (20 marks)

C1 An Astable circuit is connected to the CLK input of a frequency divider circuit as shown in figure C1.1.

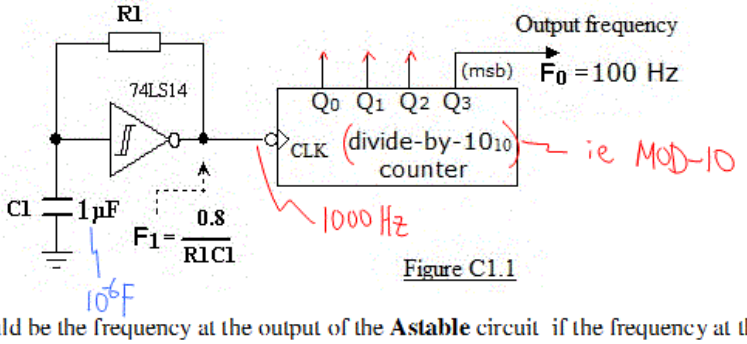


Figure C1.1

(a). What should be the frequency at the output of the **Astable** circuit if the frequency at the MSB output of the **counter** is **100 Hz**?

(3 marks)

*At the CLK, freq = **1000 Hz** (in order to produce 100 Hz at the MSB of the MOD-10 counter)*

(b) Calculate the resistance **R1** of the Astable circuit, given that its frequency $F_1 = \frac{0.8}{R_1 C_1}$ Hz.

$1000\text{Hz} = \frac{0.8}{R_1 \times 10^{-6}} \rightarrow R_1 = \frac{0.8}{1000 \times 10^{-6}} = 800\,\Omega$ (4 marks)

(c) Using one 7493 IC, the symbol and internal circuit of which is given in figure C1.2, show how you would connect the IC to function as the **divide-by-10$_{10}$** counter. Draw your circuit in your answer booklet using only the 7493 symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will be deducted.

(7 marks)

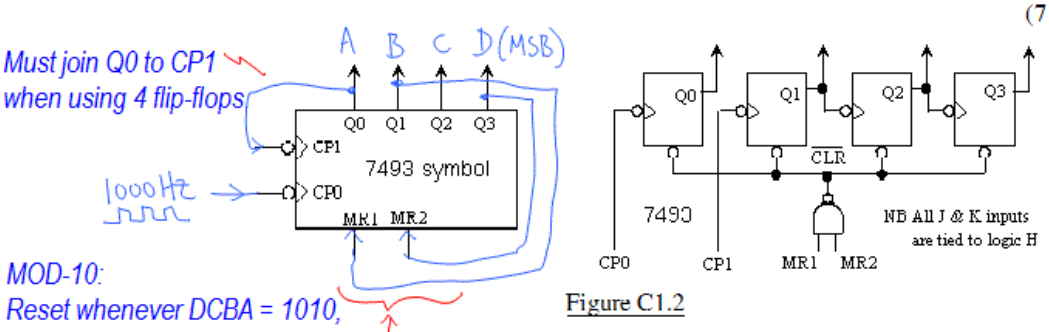
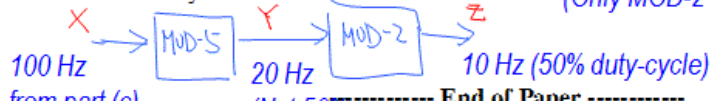


Figure C1.2

(d) If the frequency at the output of the divide-by-10$_{10}$ counter is to be further divided to **10 Hz** at **50% duty cycle**, what other counter circuits must be connected to the MSB output of the divide-by-10$_{10}$ counter? You may use as many 7493 ICs to implement these circuits which must be clearly labelled or marks will be deducted. *(Only MOD-2^N will produce 50% duty-cycle.)*

(6 marks)



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