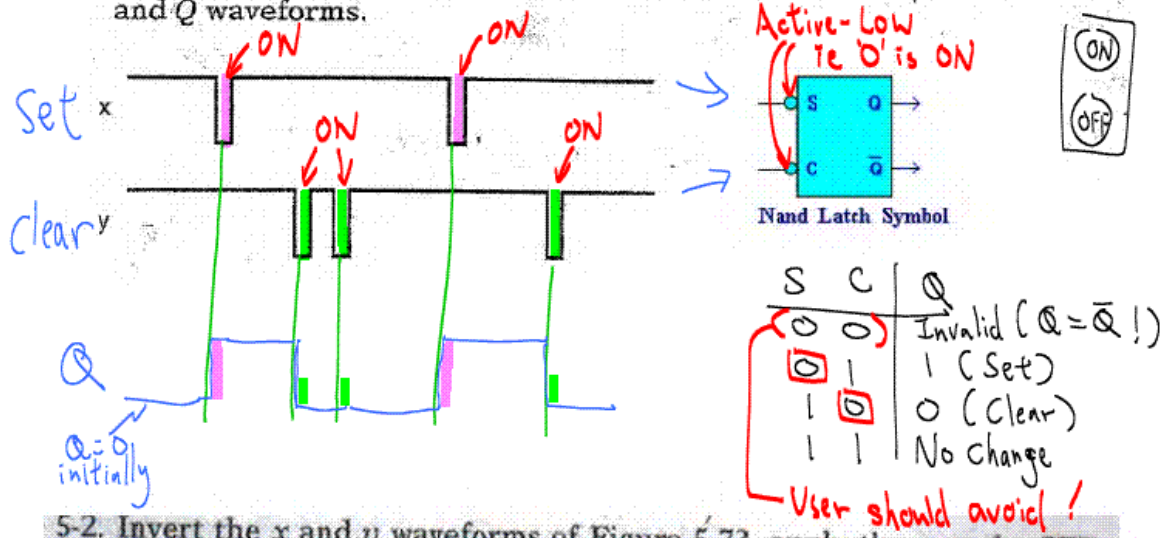
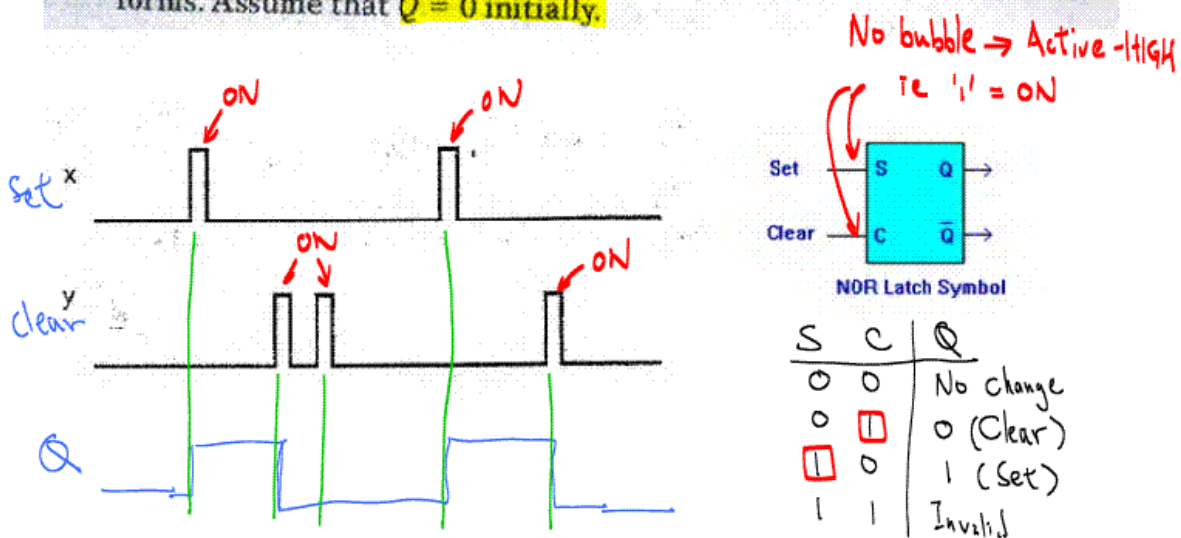


5-1. Assuming that  $Q = 0$  initially, apply the  $x$  and  $y$  waveforms of Figure 5-73 to the SET and CLEAR inputs of a **NAND latch**, and determine the  $Q$  and  $\bar{Q}$  waveforms.

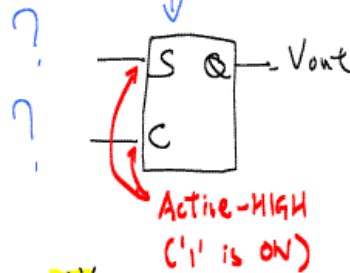
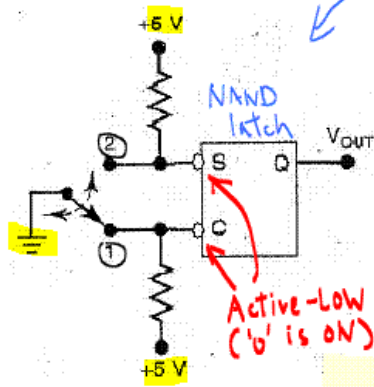


5-2. Invert the  $x$  and  $y$  waveforms of Figure 5-73, apply them to the SET and CLEAR inputs of a **NOR latch**, and determine the  $Q$  and  $\bar{Q}$  waveforms. Assume that  $Q = 0$  initially.

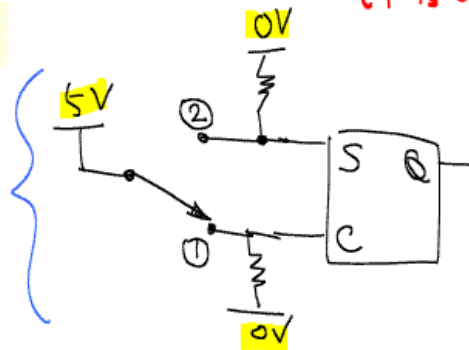


P.182: Debounced switch using NAND latch

→ 5.4. Modify the circuit of Figure 5-9 to use a NOR gate latch.



Ans.



Comparison

	At ①	Between ① & ②	At ②
<u>NAND latch</u> (Active-Low i/p's ie 0 is ON)	S = 1 (5V) = OFF C = 0 (0V) = ON Hence Q → 0 (Cleared)	S = 1 (5V) = OFF C = 1 (5V) = OFF Hence Q → No Change	S = 0 (0V) = ON C = 1 (5V) = OFF Hence Q → 1 (Set)
<u>NOR latch</u> (Active-High i/p's ie 1 is ON)	S = 0 (0V) = OFF C = 1 (5V) = ON Hence Q → 0 (Cleared)	S = 0 (0V) = OFF C = 0 (0V) = OFF Hence Q → No Change	S = 1 (5V) = ON C = 0 (0V) = OFF Hence Q → 1 (Set)

5-9. Apply the waveforms of Figure 5-76 to the FF of Figure 5-17 and determine the waveform at Q. Assume  $Q = 0$  initially.

Figure 5-76

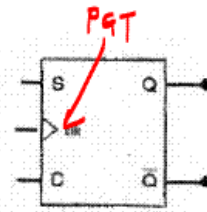
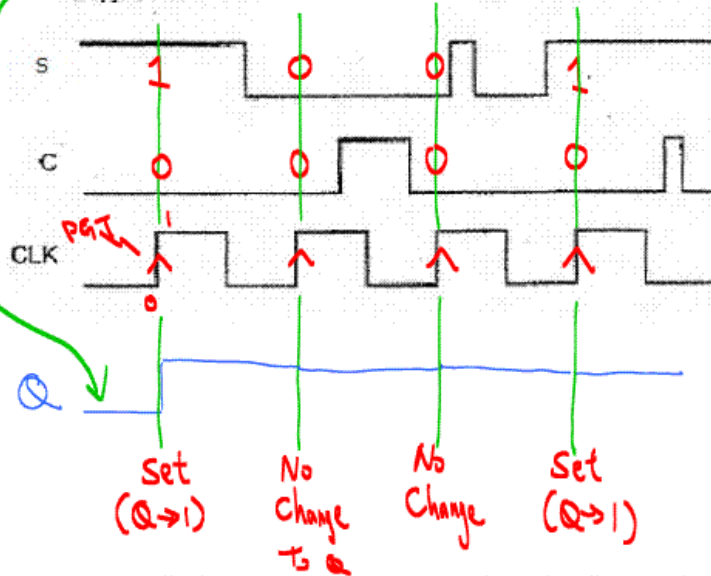


Fig. 5.17

S-C ff.

S	C	CLK	Q
0	0	↑	No Change
0	1	↑	0 (Clear)
1	0	↑	1 (Set)
1	1	↑	Invalid

Repeat for the FF of Figure 5-18. Assume  $Q = 0$  initially.

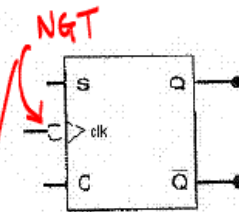
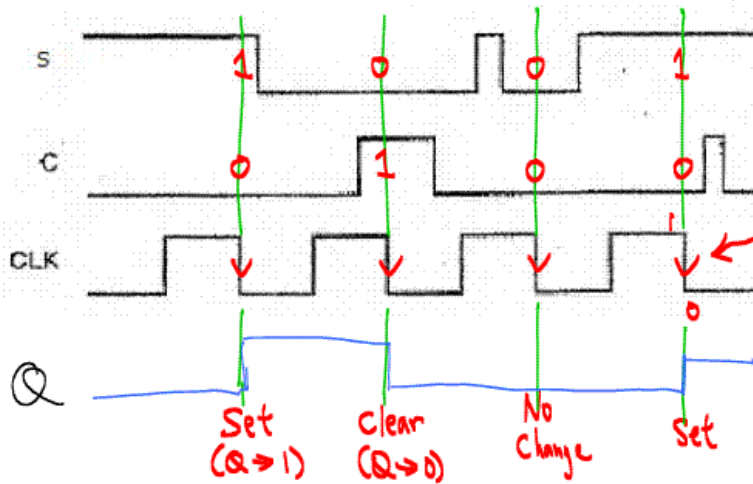


Fig. 5.13

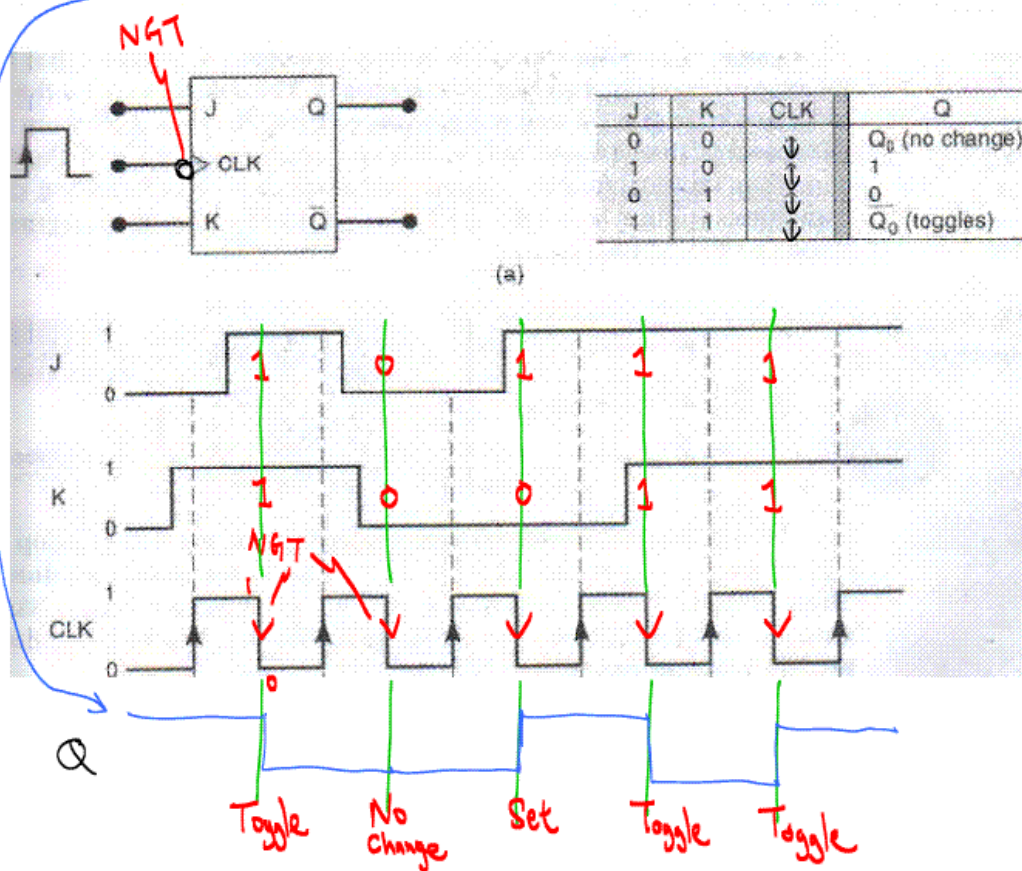
SECTION 5-8

→ 5-10. Apply the  $J$ ,  $K$ , and  $CLK$  waveforms of Figure 5-21 to the FF of Figure 5-22. Assume that  $Q = 1$  initially, and determine the  $Q$  waveform.

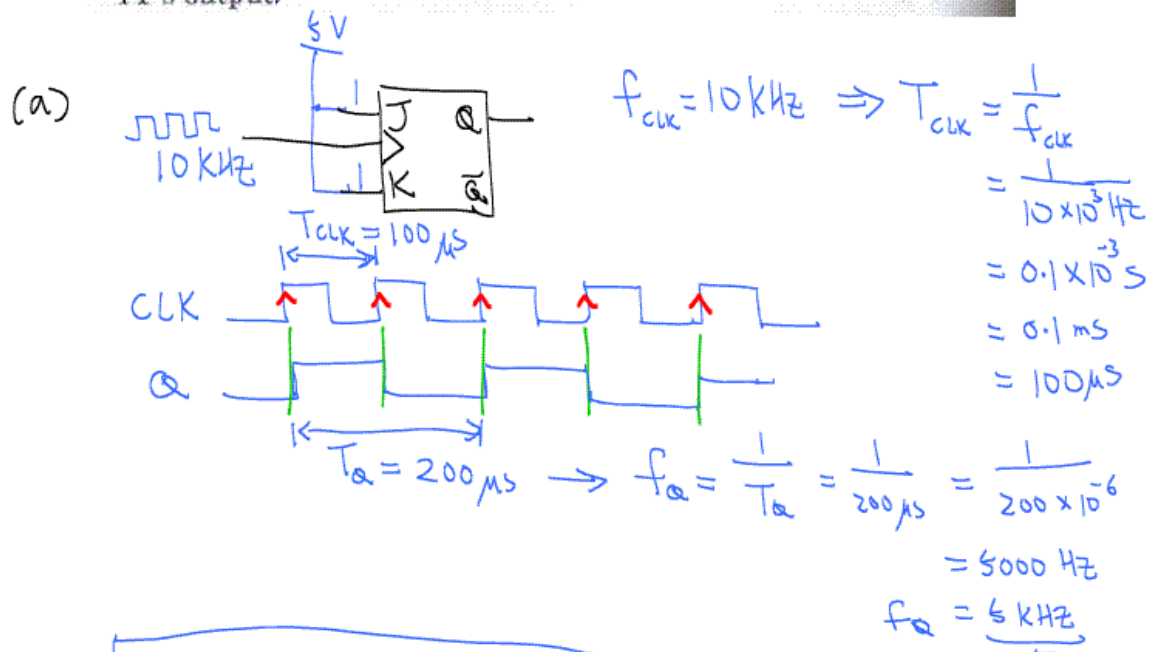
p. 193

J-K (N&T)

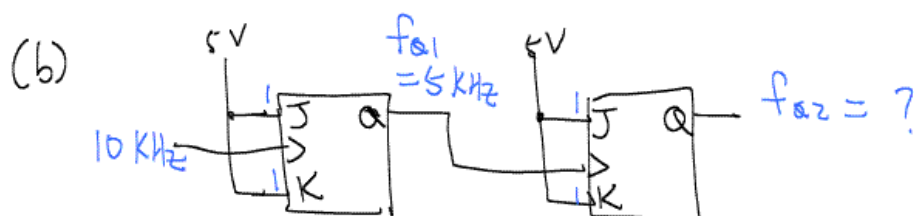
p. 194



- 5-11. (a) Show how a J-K flip-flop can operate as a *toggle FF* (changes states on each clock pulse). Then apply a 10-kHz clock signal to its *CLK* input and determine the waveform at *Q*.
- (b) Connect *Q* from this FF to the *CLK* input of a second J-K FF that also has  $J = K = 1$ . Determine the frequency of the signal at this FF's output.



$$f_Q = \frac{1}{2} f_{clk} \text{ — ie freq. has been divided by 2}$$



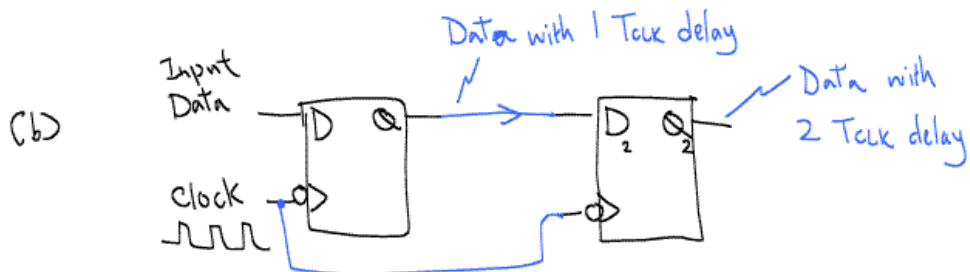
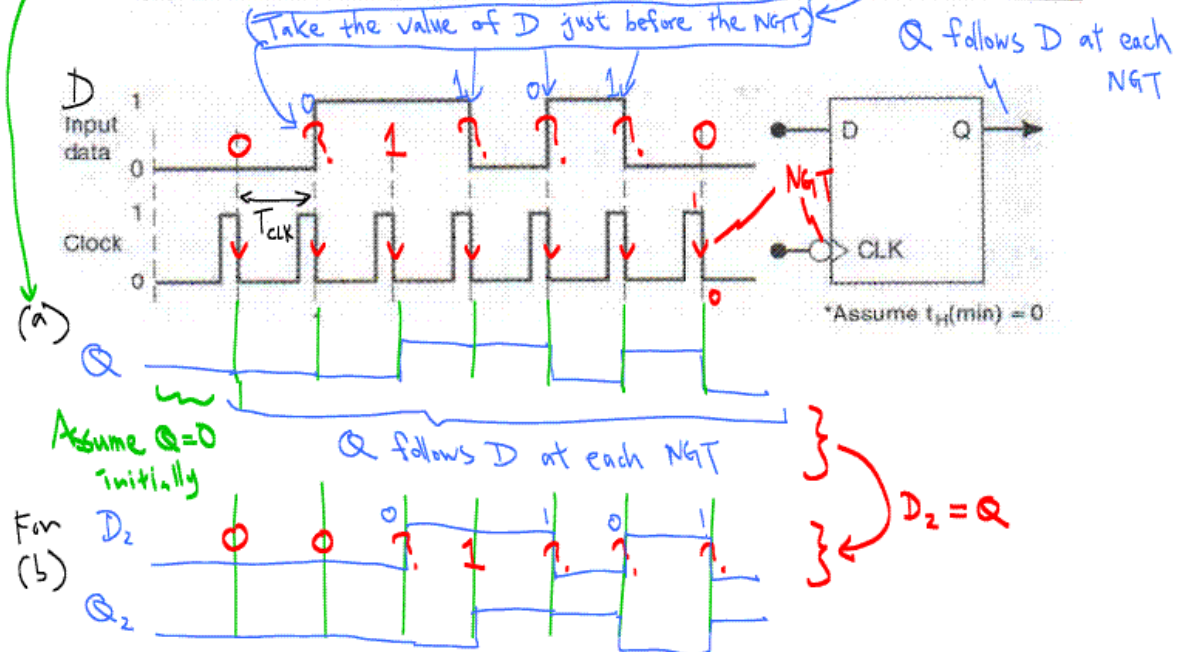
$$f_{Q1} = \frac{10 \text{ kHz}}{2} = 5 \text{ kHz}$$

$$f_{Q2} = \frac{5 \text{ kHz}}{2} = 2.5 \text{ kHz}$$

5-13. A D FF is sometimes used to *delay* a binary waveform so that the binary information appears at the output a certain amount of time after it appears at the *D* input.

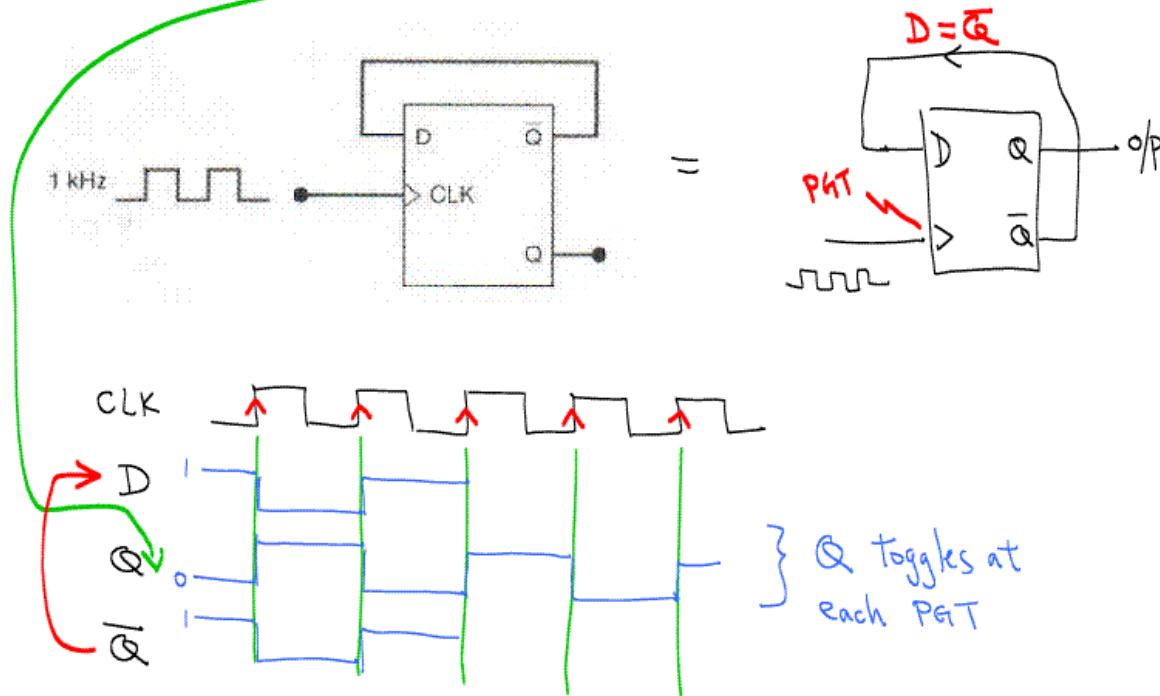
(a) Determine the *Q* waveform in Figure 5-78, and compare it with the input waveform. Note that it is delayed from the input by one clock period. ( $T_{clk}$ )

(b) How can a delay of two clock periods be obtained?





5-15. An edge-triggered D flip-flop (can be made to operate in the toggle mode) by connecting it as shown in Figure 5-79. Assume that  $Q = 0$  initially, and determine the  $Q$  waveform. (below)

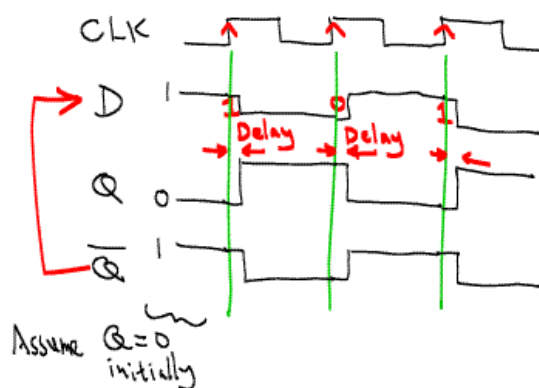


Initially  $Q = 0 \rightarrow \bar{Q} = 1 = D$

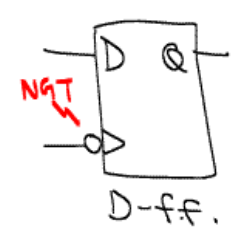
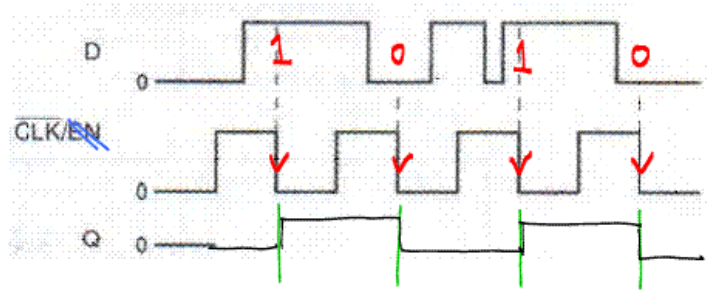
At the 1st PHT,  $Q$  follows  $D \rightarrow$  After PHT  $Q = 1$  (Hence  $\bar{Q} \rightarrow 0, \bar{D} \rightarrow 0$ )

At the 2nd PHT,  $Q = \bar{D} \rightarrow Q = 0$  ( "  $\bar{Q} \rightarrow 1, \bar{D} \rightarrow 1$ )

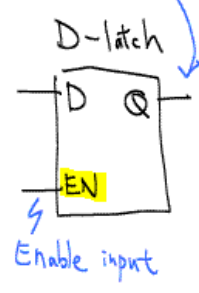
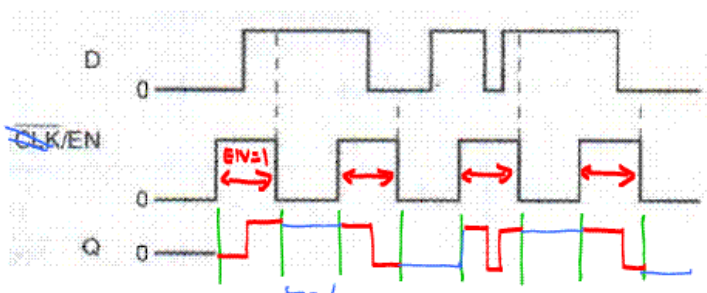
Alternative explanation — using propagation delay :



→ 5-18. Compare the operation of the *D* latch with a negative-edge-triggered *D* flip-flop by applying the waveforms of Figure 5-80 to each and determining the *Q* waveforms. (below)



$Q = D$  when  $EN = 1$   
 $Q$  has no change when  $EN = 0$



$Q = D$  (when  $EN = 1$ )  
 $Q$  has no change (when  $EN = 0$ )