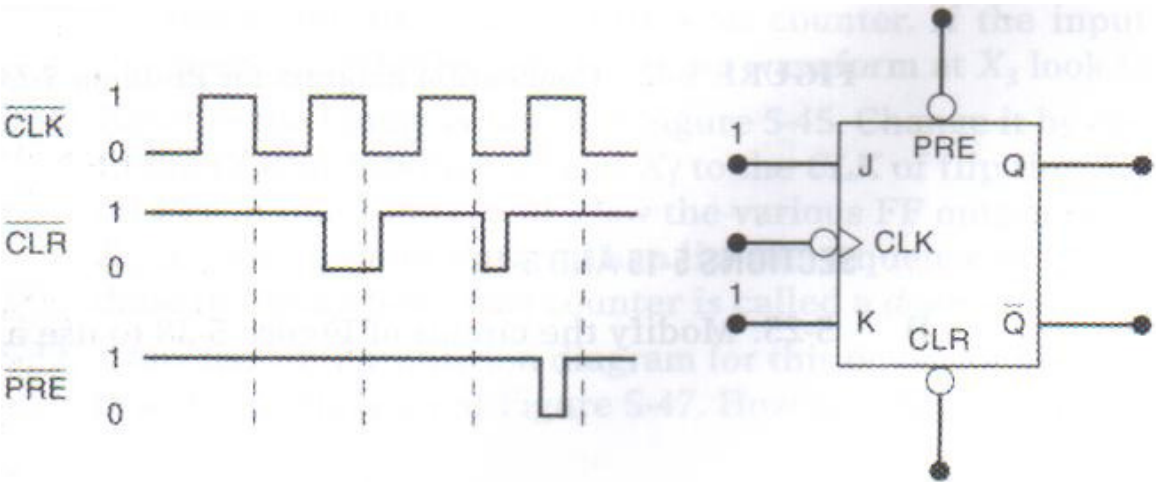
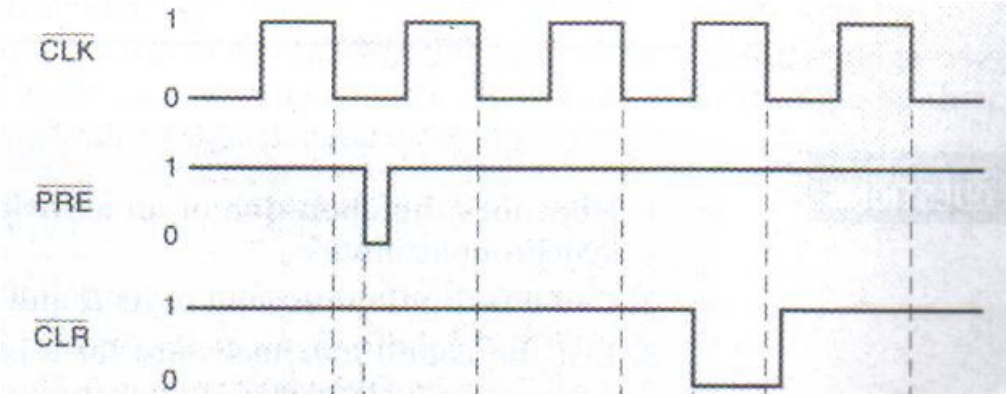
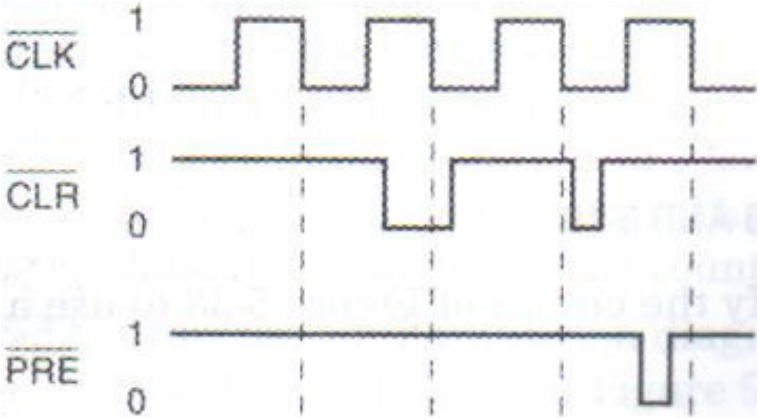
5-20. Determine the Q waveform for the FF in Figure 5-81. Assume that $Q = 0$ initially, and remember that the asynchronous inputs override all other inputs.



5-21. Apply the $\overline{CLK}$, $\overline{PRE}$, and $\overline{CLR}$ waveforms of Figure 5-30 to a positive-edge-triggered D flip-flop with active-LOW asynchronous inputs. Assume that D is kept HIGH and Q is initially LOW. Determine the Q waveform.



5-22. Apply the waveforms of Figure 5-81 to a D flip-flop that triggers on NGTs and has active-LOW asynchronous inputs. Assume that D is kept LOW and that Q is initially HIGH. Draw the resulting Q waveform.



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5-23. Use Table 5-2 in Section 5-11 to determine the following.

(a) How long can it take for the *Q* output of a 74C74 to switch from 0 to 1 in response to an active *CLK* transition?

(b) Which FF in Table 5-2 requires its control inputs to remain stable for the longest time *after* the active *CLK* transition? *Before* the transition?

(c) What is the narrowest pulse that can be applied to the $\overline{PRE}$ of a 7474 FF?

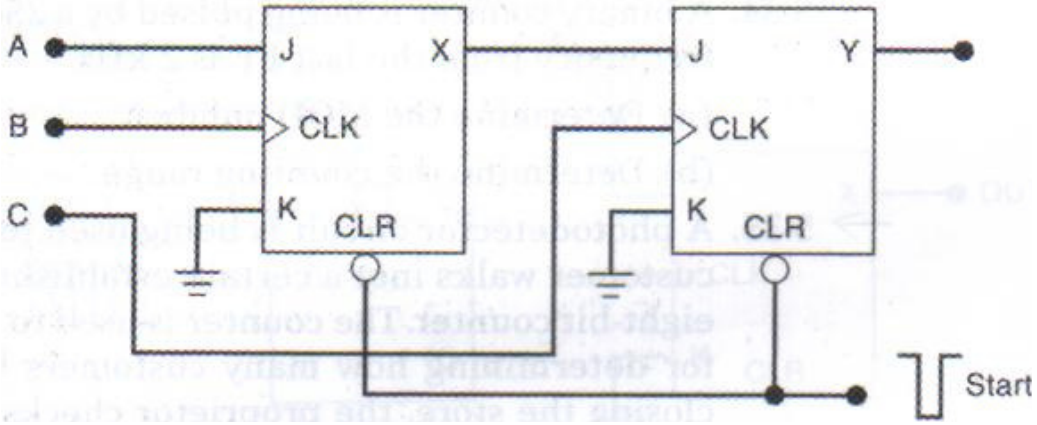
		TTL		CMOS	
		7474	74LS112	74C74	74HC112
t_S		20	20	60	25
t_H		5	0	0	0
t_{PHL}	from *CLK* to *Q*	40	24	200	31
t_{PLH}	from *CLK* to *Q*	25	16	200	31
t_{PHL}	from $\overline{CLR}$ to *Q*	40	24	225	41
t_{PLH}	from $\overline{PRE}$ to *Q*	25	16	225	41
$t_W(L)$	*CLK* LOW time	37	15	100	25
$t_W(H)$	*CLK* HIGH time	30	20	100	25
$t_W(L)$	at $\overline{PRE}$ or $\overline{CLR}$	30	15	60	25
f_{MAX}	in MHz	15	30	5	20

5-26. In the circuit of Figure 5-83, inputs *A*, *B*, and *C* are all initially LOW. Output *Y* is supposed to go HIGH only when *A*, *B*, and *C* go HIGH in a certain sequence.

(a) Determine the sequence that will make *Y* go HIGH.

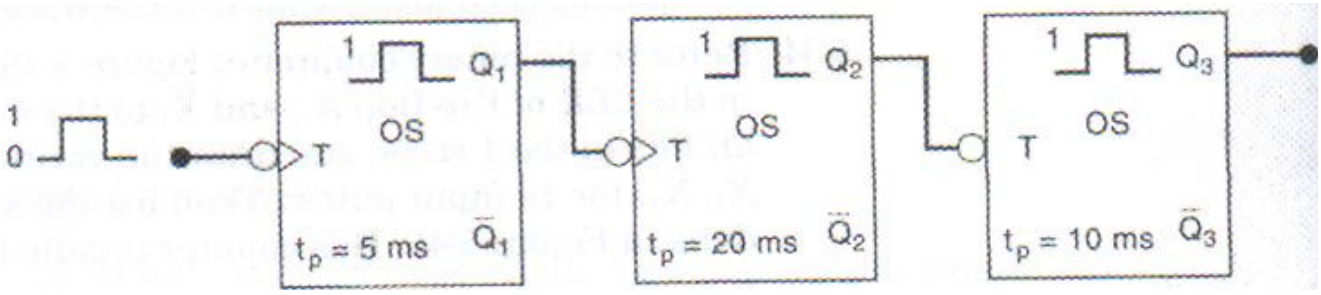
(b) Explain why the START pulse is needed.

(c) Modify this circuit to use D FFs.



5-35. A photodetector circuit is being used to generate a pulse each time a customer walks into a certain establishment. The pulses are fed to an eight-bit counter. The counter is used to count these pulses as a means for determining how many customers have entered the store. After closing the store, the proprietor checks the counter and finds that it shows a count of $00001001_2 = 9_{10}$. He knows that this is incorrect because there were many more than nine people in his store. Assuming that the counter circuit is working properly, what could be the reason for the discrepancy?

5-40. Figure 5-84 shows three nonretriggerable one-shots connected in a timing chain that produces three sequential output pulses. Note the "1" in front of the pulse on each OS symbol to indicate nonretriggerable operation. Draw a timing diagram showing the relationship between the input pulse and the three OS outputs. Assume an input pulse duration of 10 ms.

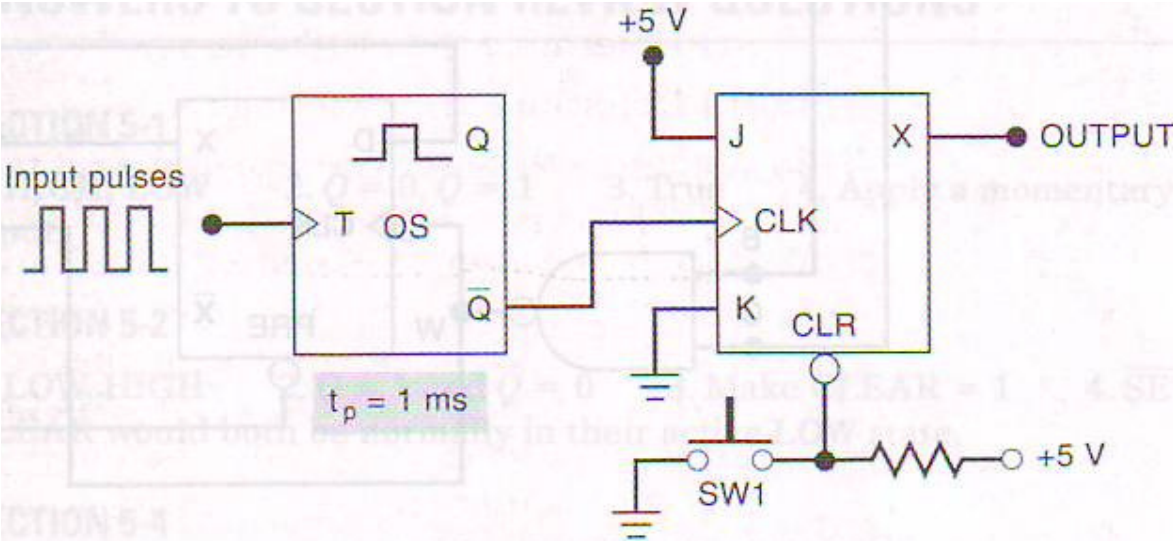


5-41. A *retriggerable* OS can be used as a pulse-frequency detector that detects when the frequency of a pulse input is below a predetermined value. A simple example of this application is shown in Figure 5-85. The operation begins by momentarily closing switch SW1.

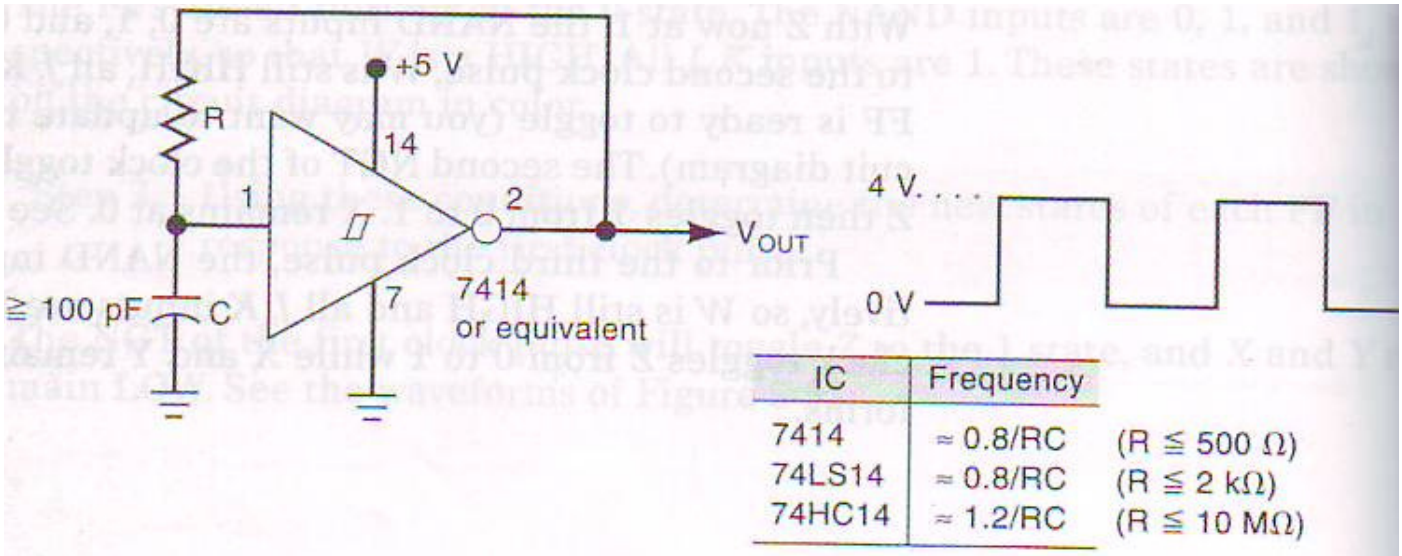
(a) Describe how the circuit responds to input frequencies above 1 kHz.

(b) Describe how the circuit responds to input frequencies below 1 kHz.

(c) How would you modify the circuit to detect when the input frequency drops below 50 kHz?



→ 5-45. Show how to use a 74LS14 Schmitt-trigger INVERTER to produce a approximate square wave with a frequency of 10 kHz.



IC	Frequency	
7414	≈ 0.8/RC	(R ≦ 500 Ω)
74LS14	≈ 0.8/RC	(R ≦ 2 kΩ)
74HC14	≈ 1.2/RC	(R ≦ 10 MΩ)

FIGURE 5-54 Schmitt-trigger oscillator using a 7414 INVERTER. A 7413 Schmitt-trigger NAND may also be used.