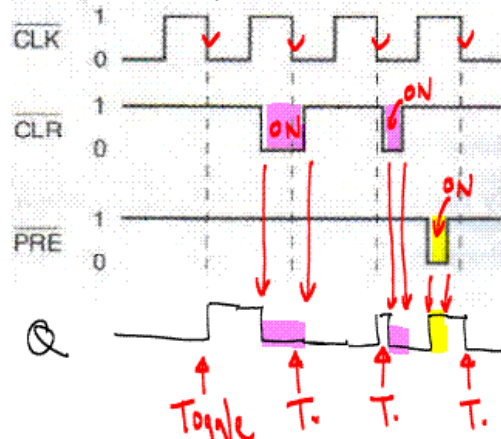


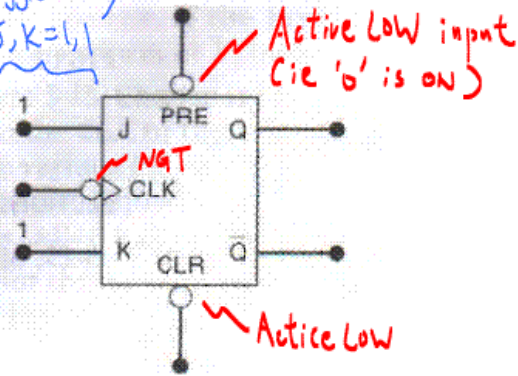
5-20. Determine the  $Q$  waveform for the FF in Figure 5-81. Assume that  $Q = 0$  initially, and remember that the asynchronous inputs override all other inputs.  
 (below)  
 ie PRE & CLR

$Q$  can change only when either this is a NGT or the PRE/CLR is ON.



(Toggle mode)

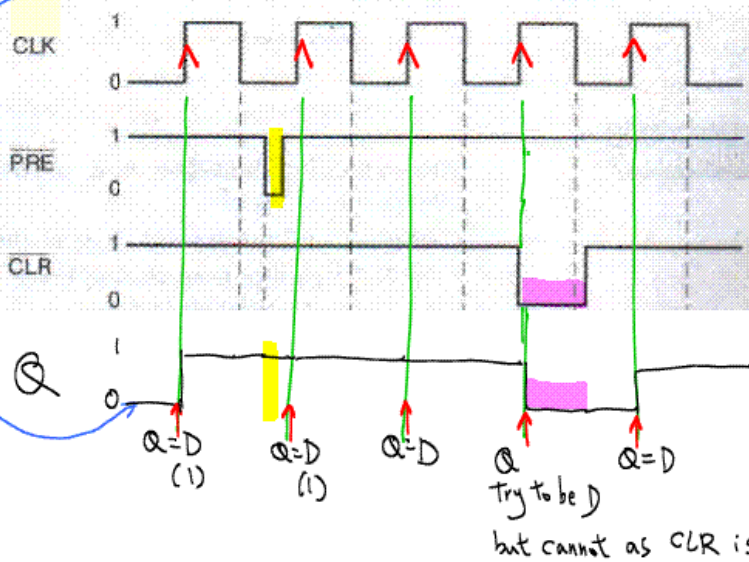
$J, K = 1, 1$



PRESET: immediately make  $Q = 1$   
 CLEAR: " " "  $Q = 0$

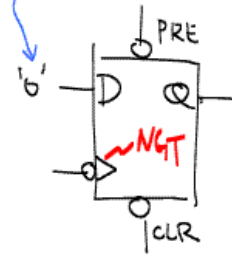
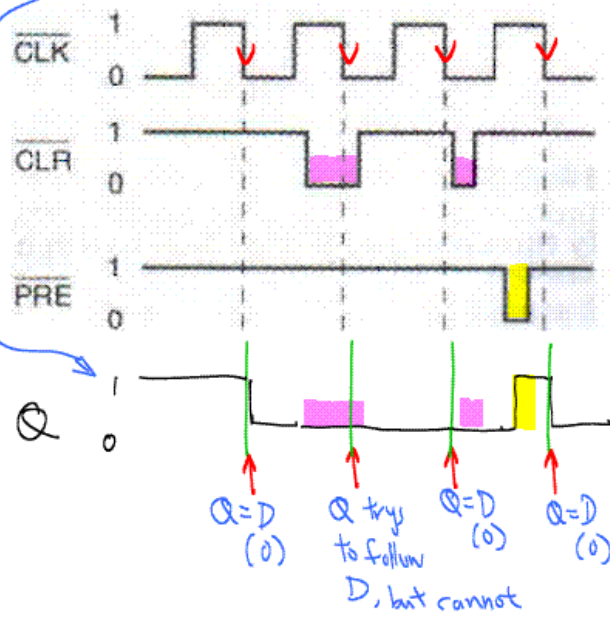
Try to toggle, but cannot as CLR is still ON.

5-21. Apply the CLK, PRE, and CLR waveforms of Figure 5-30 to a positive-edge-triggered D flip-flop with active-LOW asynchronous inputs. Assume that D is kept HIGH and Q is initially LOW. Determine the Q waveform.



PRE & CLR have higher priority than the D and CLK i/p's or J,K

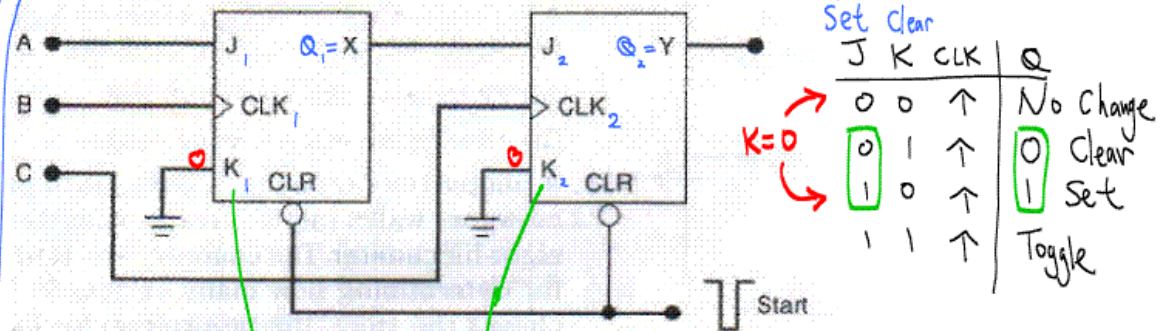
5-22. Apply the waveforms of Figure 5-81 to a D flip-flop that triggers on **NGT's** and has **active-LOW asynchronous inputs**. Assume that **D is kept LOW** and that **Q is initially HIGH**. Draw the resulting Q waveform.



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- 5-23. Use Table 5-2 in Section 5-11 to determine the following.
- How long can it take for the  $Q$  output of a **74C74** to switch from 0 to 1 in response to an active  $CLK$  transition?
  - Which FF in Table 5-2 requires its control inputs to remain stable for the longest time after the active  $CLK$  transition? Before the transition?  
 $\Rightarrow t_H$   $\Rightarrow t_S$   
 $\Rightarrow t_{PHL} / t_{PLH}$
  - What is the narrowest pulse that can be applied to the  $\overline{PRE}$  of a **7474** FF?  
 $\Rightarrow t_W$

		TTL		CMOS	
		<b>7474</b>	74LS112	<b>74C74</b>	74HC112
$t_S$	(Setup time)	20	20	60	25
$t_H$	(Hold time)	5	0	0	0
$t_{PHL}$	from $CLK$ to $Q$	40	24	200	31
$t_{PLH}$	from <b><math>CLK</math> to <math>Q</math></b>	25	16	<b>200</b>	31
$t_{PHL}$	from $\overline{CLR}$ to $Q$	40	24	225	41
$t_{PLH}$	from $\overline{PRE}$ to $Q$	25	16	225	41
$t_{W(L)}$	$CLK$ LOW time	37	15	100	25
$t_{W(H)}$	$CLK$ HIGH time	30	20	100	25
$t_{W(L)}$	at <b><math>\overline{PRE}</math></b> or $\overline{CLR}$	<b>30</b>	15	60	25
$t_{MAX}$	in MHz	15	30	5	20

- (a) Determine the sequence that will make Y go HIGH.  
(b) Explain why the START pulse is needed. — for clearing  $Q_1$  &  $Q_2$  (to 0)  
(c) Modify this circuit to use D FFs.



(a)  $Y = Q_2 \rightarrow 1$  when  $J_2, K_2 = 1, 0$  while  $\text{CLK}_2$  goes 1 (PGT at  $\text{CLK}_2$ )  
 X — when will it go 1? c

$X = Q_1 \rightarrow 1$  when  $\underbrace{J_1}_A, \underbrace{K_1}_B = 1, 0$  while  $\underbrace{CLK_1}_B$  goes 1 (PGT at  $CLK_1$ )

Hence the seq. is :

1. A ( $J_1$ ) goes 1 first (before the PGT at  $CLK_1$ )
2. B ( $CLK_1$ ) then goes 1 (to give the PGT at  $CLK_1$ , hence  $Q_1 \rightarrow 1$ )
3. C ( $CLK_2$ ) then goes 1 (" " " "  $CLK_2$ , "  $Q_2 \rightarrow 1$ )

(c) Compare the truth-table between J-K ff. vs D f.f.:

$K=0$ 

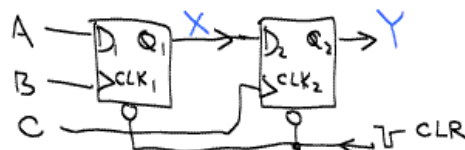
J	K	CLK	Q
0	0	↑	No change
0	1	↑	0
1	0	↑	1
1	1	↑	Toggle

D	CLK	Q
0	↑	0
1	↑	1

Any similarity?

Seq.:

1. A ( $D_1$ ) goes 1 first
2. B ( $CLK_1$ ) then goes 1
3. C ( $CLK_2$ ) " " 1



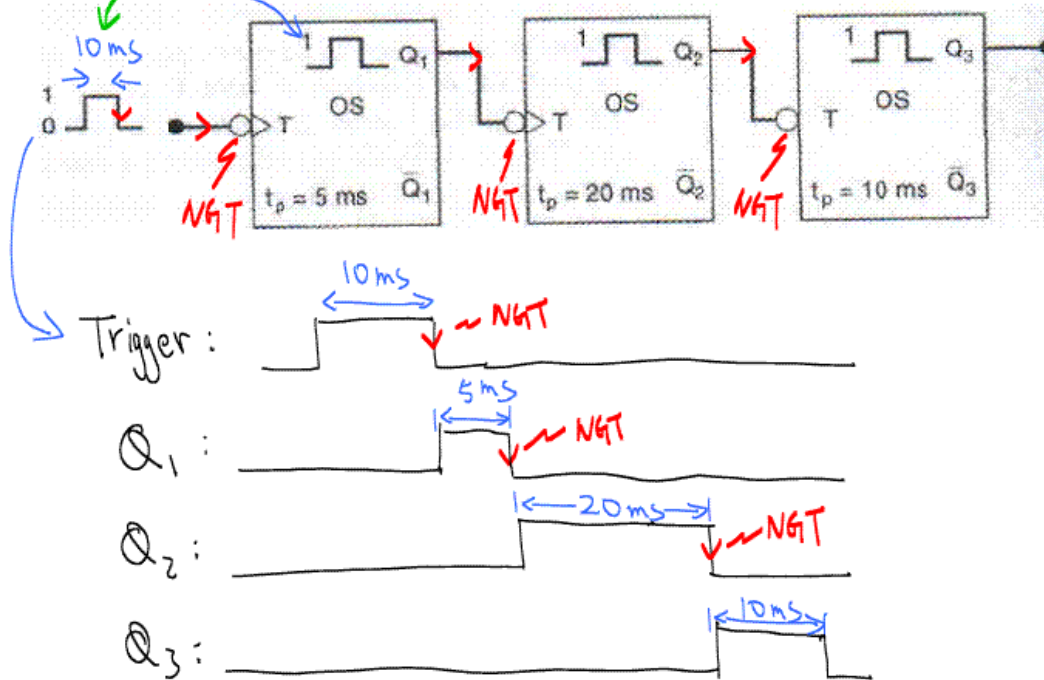


5-35. A photodetector circuit is being used to generate a pulse each time a customer walks into a certain establishment. The pulses are fed to an **eight-bit counter**. The counter is used to count these pulses as a means for determining how many customers have entered the store. After closing the store, the proprietor checks the counter and finds that it shows a count of  $00001001_2 = 9_{10}$ . He knows that this is **incorrect** because there were many more than nine people in his store. Assuming that the counter circuit is working properly, what could be the reason for the discrepancy?

→ 8-bit →  $2^8 = 256$  nos (0 to 255)  
ie 8 ffs

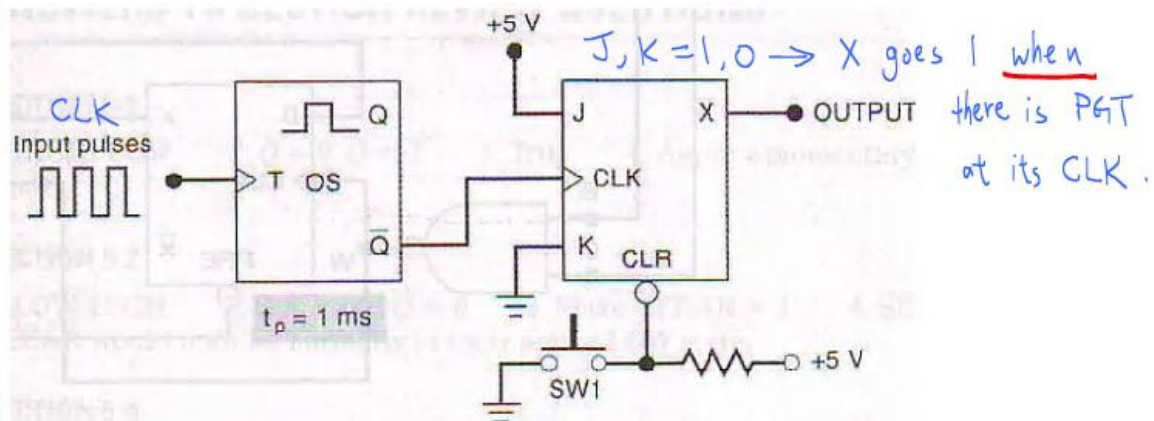
If there were 255 people → count 255  
 " " " 256 " → " 0  
 " " "  $256+9$  " → " 9  
 " " "  $(2 \times 256)+9$  " → " 9  
 " " "  $(N \times 256)+9$  " → " 9

5-40. Figure 5-84 shows three **nonretriggerable** one-shots connected in a timing chain that produces three sequential output pulses. Note the "1" in front of the pulse on each OS symbol to indicate nonretriggerable operation. Draw a timing diagram showing the relationship between the input pulse and the three OS outputs. Assume an input pulse duration of 10 ms.

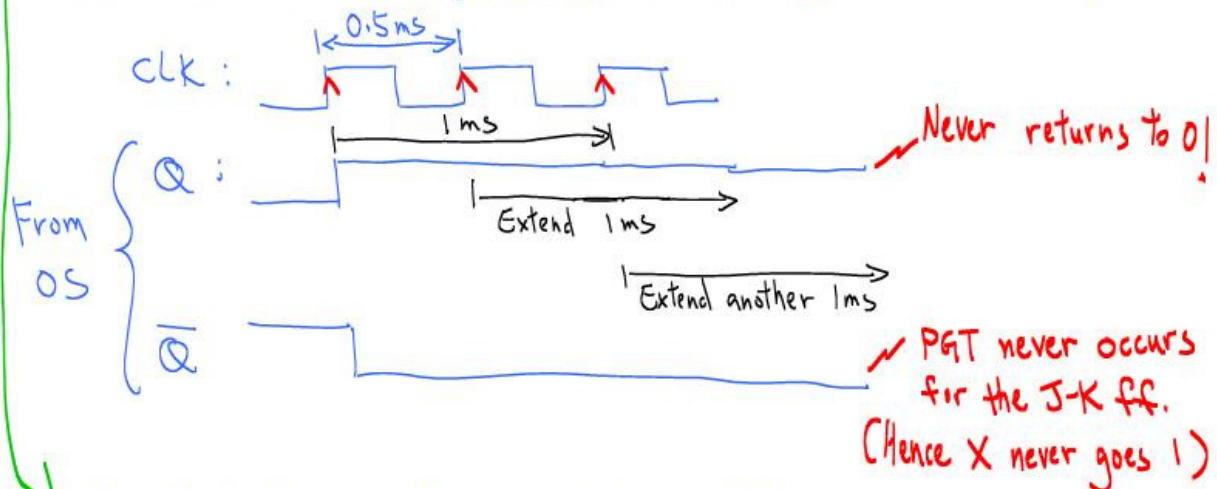


5-41. A **retriggerable** OS can be used as a pulse-frequency detector that detects when the frequency of a pulse input is below a predetermined value. A simple example of this application is shown in Figure 5-85. The operation begins by momentarily closing switch SW1.

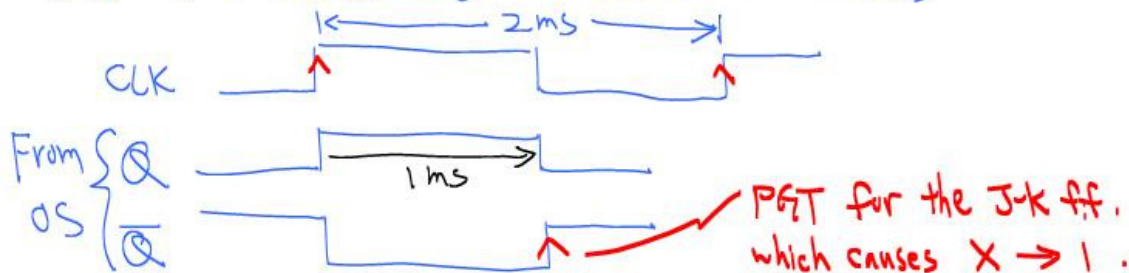
- (a) Describe how the circuit responds to input frequencies above 1 kHz.  
 (b) Describe how the circuit responds to input frequencies below 1 kHz.  
 (c) How would you modify the circuit to detect when the input frequency drops below 50 kHz?



(a)  $f > 1\text{ kHz}$  (e.g.  $2\text{ kHz} \rightarrow T = \frac{1}{2}\text{ ms} = 0.5\text{ ms}$ )



(b)  $f < 1\text{ kHz}$  (e.g.  $0.5\text{ kHz} \rightarrow T = 2\text{ ms}$ )





Q41 (c)

$$t_p = 1 \text{ ms} \xrightarrow[\text{detects}]{\text{of the OS}} f = \frac{1}{1 \text{ ms}} = 1 \text{ kHz}$$

$$\text{For } f = 50 \text{ kHz} \rightarrow t_p = \frac{1}{50 \text{ kHz}} \\ = 0.02 \text{ ms}$$

$$t_p = \underline{\underline{20 \mu\text{s}}}$$

→ 5-45. Show how to use a **74LS14** Schmitt-trigger INVERTER to produce an approximate square wave with a frequency of 10 kHz.

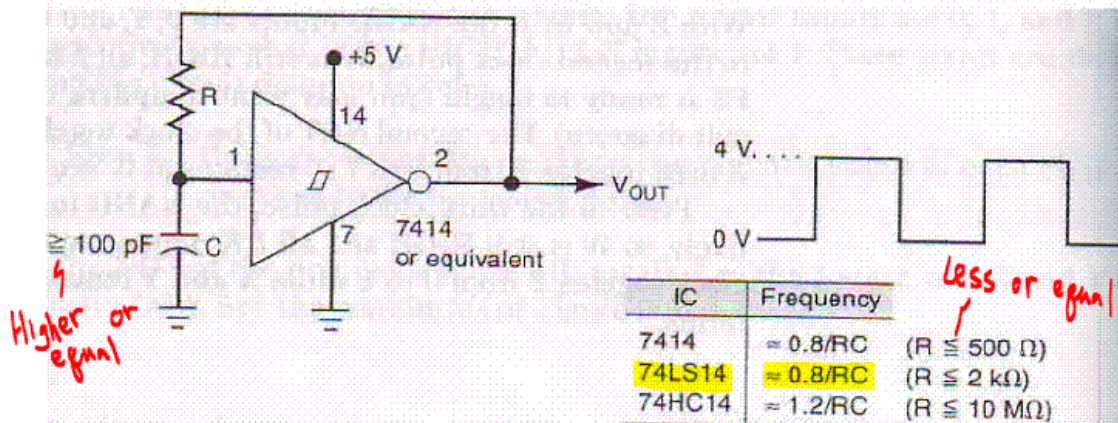
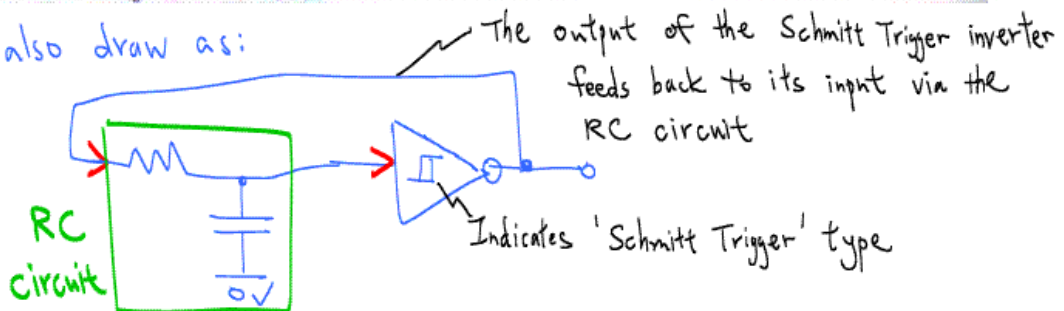


FIGURE 5-54 Schmitt-trigger oscillator using a 7414 INVERTER. A 7413 Schmitt-trigger NAND may also be used.

Can also draw as:



$$f = \frac{0.8}{RC}$$

For example, let us choose  $C = 1 \text{ nF} (10^{-9})$

$$10 \times 10^3 = \frac{0.8}{R \times (1 \times 10^{-9})} \text{ Hz} \Rightarrow R = 0.8 \times 10^5 \Omega = \underline{800 \text{ k}\Omega}$$

Too big; must  $\leq 2 \text{ k}\Omega$

Now try  $C = 1 \mu\text{F} (10^{-6})$

$$10 \times 10^3 = \frac{0.8}{R \times (1 \times 10^{-6})} \text{ Hz} \Rightarrow R = 0.8 \times 10^2 \Omega = \underline{800 \Omega} - \text{OK } \checkmark$$