SINGAPORE POLYTECHNIC ET1004

2013/2014_S2 MID-SEMESTER TEST

SAS code: **TST1**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Clean Energy DCEG 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet, unless indicated otherwise.

4. There are 6 pages in this MST paper.

5. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

1. Which one of the following binary additions will produce a sum result of 0111_2?

(a) 0010_2 added to 0101_2
(b) 0011_2 added to 0101_2
(c) 0010_2 added to 0100_2
(d) 0011_2 added to 0110_2

2. The result of an arithmetic operation in an 8-bit (including the sign bit) 2's complement signed numbering system is 11111000_2. What is the decimal equivalent of this value?

(a) $+8_{10}$ (b) -8_{10} (c) -120_{10} (d) $+120_{10}$

3. What is the binary value at the output of a **mod-16_{10}** up-counter after the application of **63_{10}** clock cycles, assuming that the **initial** state at the counter is **0011_2**?

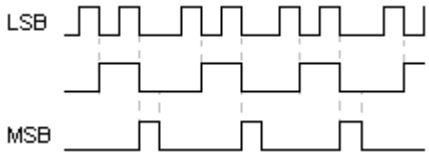
(a) 1111_2 (b) 0011_2 (c) 0010_2 (d) 0001_2

4. A shift register with **many data inputs a**nd a **single data output** is a:

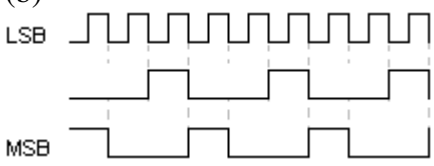
(a) serial-in, parallel-out register
(b) serial-in, serial-out register
(c) parallel-in, parallel-out register
(d) parallel-in, serial-out register

5. Which one of the following set of waveforms in figure A5 corresponds to the output waveforms of a **Mod 6_{10}** binary counter?

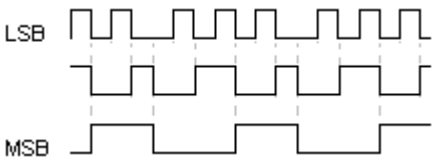
(a)



(b)



(c)



(d)

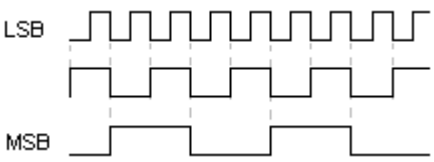


Figure A5

6. Decimal $\mathbf{530_{10}}$ expressed in BCD is _____.

(a) $101\ 011\ 000_2$ (b) $101\ 0011\ 0000_2$

(c) $0101\ 0011\ 0000_2$ (d) $0100\ 0010\ 0000_2$

7. If **t**he frequency of the signal at the **MSB** output of a **mod-$\mathbf{20_{10}}$** counter is **$\mathbf{2000_{10}}$ Hz**, what is the frequency of the **CLK** signal applied at its CLK input?

(a) 20_{10} Hz (b) 100_{10} Hz

(c) 2000_{10} Hz (d) 40000_{10} Hz

8. A binary counter that counts sequentially from **$\mathbf{0000_2}$ to $\mathbf{1100_2}$** is a mod ____ counter.

(a) 10_{10} (b) 11_{10} (c) 12_{10} (d) 13_{10}

9. Which 2-input logic gate can be made to function as an inverter when one of its inputs is connected to logic High?

(a) AND gate (b) OR gate

(c) XOR gate (d) XNOR gate

10. How long does it take a 1-bit data applied at the data input to appear at the data output X in Figure A10? The clock frequency applied is 1000_{10} Hz.

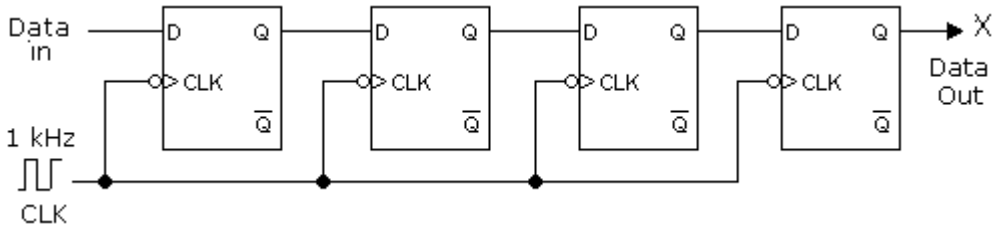


Figure A10

(a) 4 Sec

(b) 40 mSec

(c) 4 mSec

(d) 0**.**4 mSec

Section B (45 marks)

B1 Perform the following operations using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit.

(i) **Add $+51_{10}$ to $+30_{10}$**

(ii) **Add -45_{10} to $+66_{10}$**

(15 marks)

NB: All workings in question B1 must be shown or marks will not be awarded.

B2 The 74283 (see figure B2.1) is a 4-bit parallel adder IC.

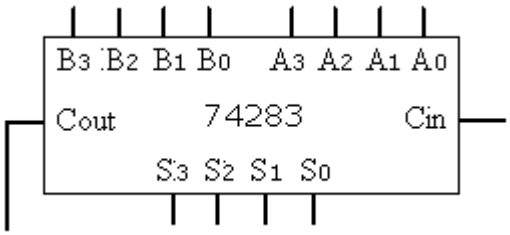


Figure B2.1

(a) If this 4-bit adder is to be constructed using the Full Adder unit, how many full-adder units are required for the 4-bit Adder? Using the correct number of Full Adders, draw the equivalent functional circuit of this 4-bit Parallel Adder. The symbol of the Full Adder is shown in figure B2.2. Label your circuit according to figure B2.1.

(7 marks)

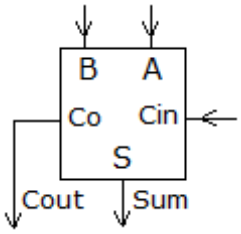


Figure B2.2

(b) If $A_3\ A_2\ A_1\ A_0 = 0101_2$ and, $B_3\ B_2\ B_1\ B_0 = 1010_2$, determine the resultant output values of the 74283 Adder at Cout $S_3\ S_2\ S_1\ S_0$ for (i) Cin = 0 and, (ii) Cin = 1.

(4 marks)

(c) How many 74283 ICs are required to construct the following Parallel Adders?

(4 marks)

(i) 12-bit Parallel Adder
(ii) 32-bit Parallel Adder

B3(a) Three NGT JK flip-flops are given in figure B3.1. Copy to your answer booklet figure B3.1 and complete the connections for the 3 flip-flops so that the circuit functions as a **mod-2^3 (mod-8_{10})** counter**.**

(6 marks)

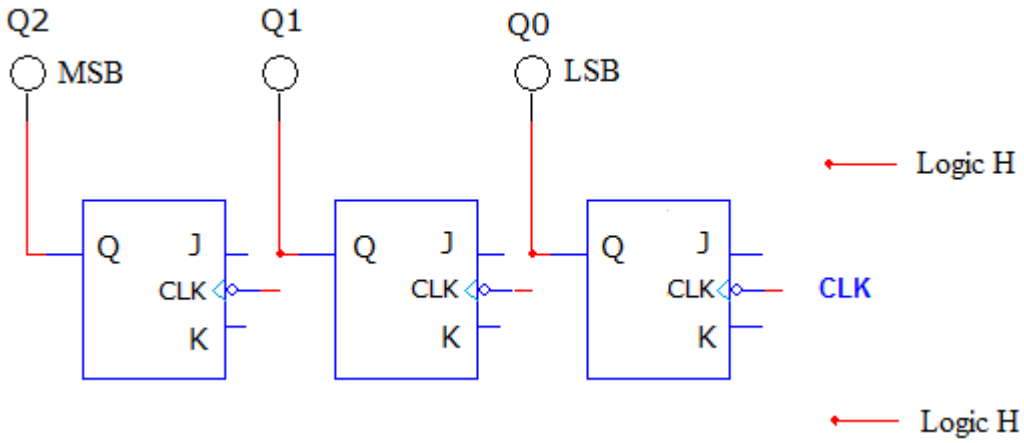


Figure B3.1

B3(b) For the clock signal waveform shown in figure B3,2, copy the diagram to your answer booklet and draw the output signal waveforms of the mod-8_{10} counter that you constructed in figure B3.1. You are to assume that the initial values of the 3 flip-flops are logic Low and, all propagation delays may be neglected.

(5 marks)

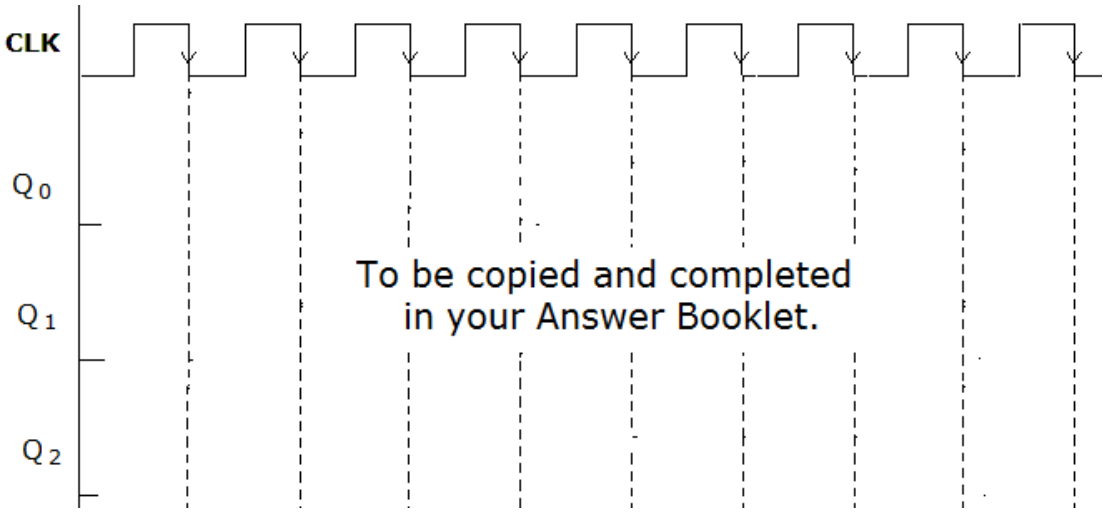


Figure B3.2

B3(c) If the clock signal frequency in figure B3.2 is **2000_{10}** Hz, what are the signal frequencies at outputs Q0 and Q2?

(4 marks)

Section C (25 marks)

C1. Refer to the diagram shown in Figure C1.1 which shows a cascade of three different counters.

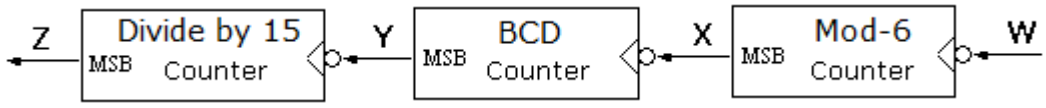


Figure C1.1

(a) Which counter has the **lowest** MOD number? What is its MOD number?

(4 marks)

(b) If the frequency of the signal at point **Y** is **600_{10} Hz**, what are the frequencies of the signals at points **W**, **X** and **Z**?

(6 marks)

(c) Using the 7493 counter IC (symbol and internal circuit as shown in Figure C1.2), construct the mod-6_{10} counter. Ensure that all inputs and outputs are clearly labeled or marks will be deducted.

(5 marks)

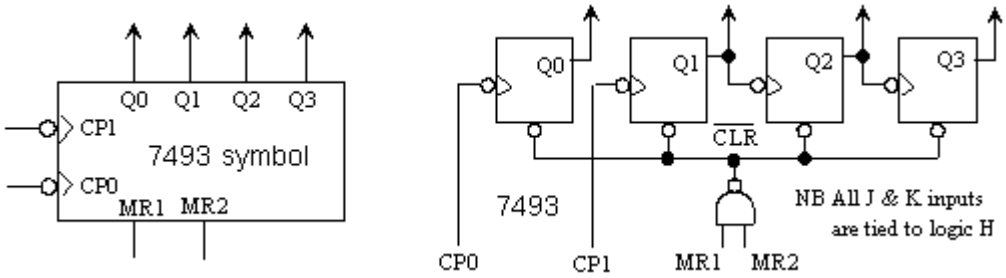


Figure C1.2

(d) Using the 7493 counter IC and any other gates as necessary, construct the divide-by-15_{10} counter. Draw the circuit in your answer booklet using the 7493 symbol. Ensure that all inputs and outputs are clearly labeled or marks will be deducted.

(6 marks)

(e) What is the overall modulus (mod-number) of the cascade of three counters? If the current output values of the cascade of three counters are $1000\ 1001\ 101_2$ (with left-most bit being the MSB and right-most bit the LSB), what will be the new output values after the application of 2_{10} clock cycles at W?

(4 marks)

---------- End of Paper ----------