SINGAPORE POLYTECHNIC

2013/2014/S2 – MST

SAS code: **TST1**

MODULE: DIGITAL ELECTRONICS 2 MODULE CODE: ET1004

COURSE/YEAR: DASE/DEEE/DCPE/DCEG/DCEP/1FT

No	SOLUTION
	SECTION – A (10 MCQ, 3 marks each)
A	1. (a) 2. (b) 3. (c) 4. (d) 5. (b) 6. (c) 7. (d) 8. (d) 9. (c) 10. (c)
B1.	**SECTION – B (10 marks each)**
(a)	Add $+51_{10}$ to $+30_{10}$

	sign	64	32	16	8	4	2	1	
+51 =	**0**	**0**	**1**	**1**	**0**	**0**	**1**	**1**	← true binary value of 51_{10}
+30 =	**0**	**0**	**0**	**1**	**1**	**1**	**1**	**0**	← true binary value of 30_{10}
81 =	**0**	**1**	**0**	**1**	**0**	**0**	**0**	**1**	← +Sum result

(b) **Add -45_{10} to $+66_{10}$**

	sign	64	32	16	8	4	2	1	
+45 =	**0**	**0**	**1**	**0**	**1**	**1**	**0**	**1**	← true binary value of 45_{10}
-45 =	**1**	**1**	**0**	**1**	**0**	**0**	**1**	**1**	← 2's complement of binary 45_{10}
+66 =	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**0**	← true binary value of 66_{10}
+21 =	~~1~~ **0**	**0**	**0**	**1**	**0**	**1**	**0**	**1**	← +sum result; 9th bit discarded

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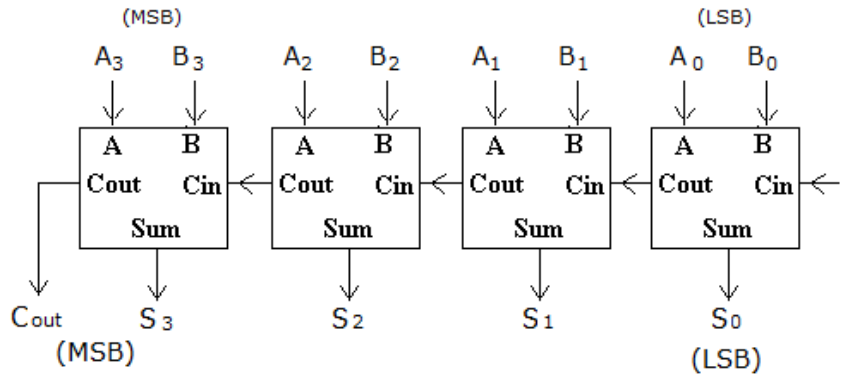
B2 (a)	**4** full adder units are required to build a 4-bit parallel Adder  Important points to note Correct connection of between FA units Indicate LSB and MSB at inputs and outputs Correct labeling at each input and output, where LSB denoted as bit 0.
(b)	Given (i) A3 A2 A1 A0 = 0 1 0 1 B3 B2 B1 B0 = 1 0 1 0 Cin = 0 0 1 1 1 1 Cout S3 S2 S1 S0 (ii) A3 A2 A1 A0 = 0 1 0 1 B3 B2 B1 B0 = 1 0 1 0 Cin = 1 1 0 0 0 0 Cout S3 S2 S1 S0
(c)	Number of 74283 ICs required for: (i) 12-bit Parallel Adder = 12/4 = 3 ICs (ii) 32-bit Parallel Adder = 32/4 = 8 ICs

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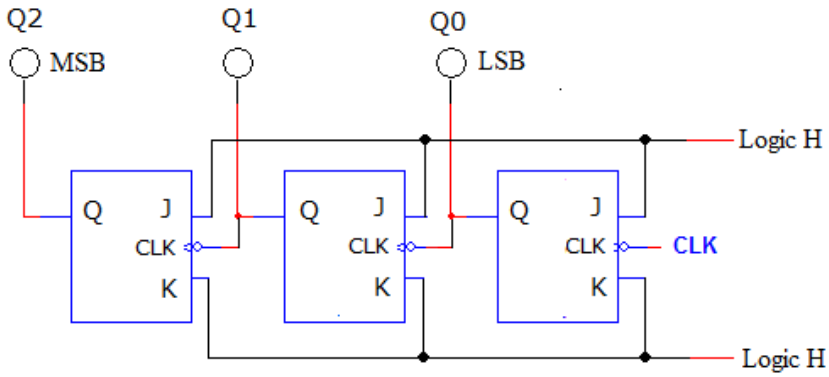
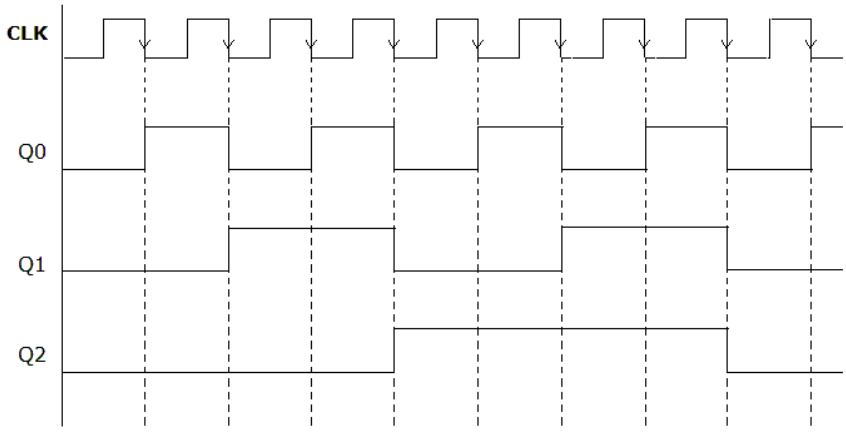
No	SOLUTION
B3 (a)	 Marks distribution Correct Connections between the three flip-flops → 3 marks Logic H to the J and K inputs of each JK flip-flop → 3 marks
(b)	
(c)	Given the clock frequency is 2000 Hz Frequency at Q0 (LSB) = 2000/2 = 1000 Hz Frequency at Q2 (MSB) = 2000/8 = 250 Hz

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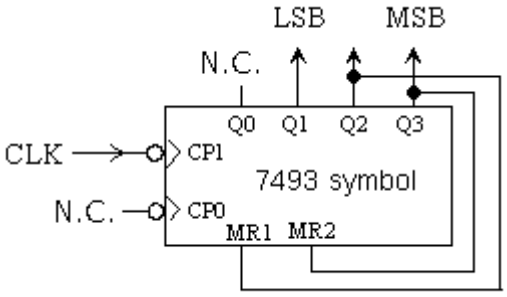
	SOLUTION
C1	**Section C (25 marks)**
(a)	Counter with lowest Mod-number is the Mod-6 counter
(b)	Given frequency at Y = 600 Hz frequencies at the outputs Z = 600/15 = 40 Hz X = 600 X 10 = 6000 Hz or 6 kHz W = 6000 X 6 = 36 kHz
(c)	

NB: Important to note

Use of 3 flip-flops & connection between flip-flops if Q0 is used instead.

Indicate correct MSB & LSB outputs.

Correct CLK input used.

Correct feedback from outputs to MR1 and MR2.

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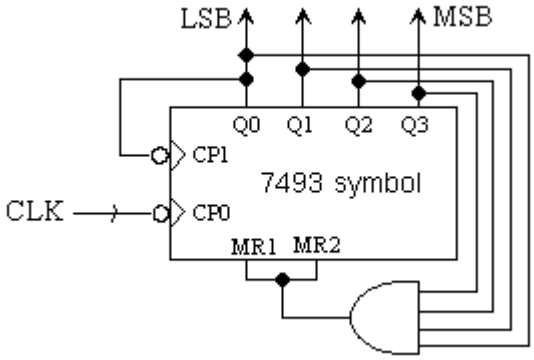
No	SOLUTION
(d)	Divide by 15 or Mod-15 counter  Important points Q0 to CP1 connection. CLK to CP0. MSB and LSB indication. Feedback from outputs & AND-4 to MR1/MR2.
(e)	Overall modulus = 6 X 10 X 15 = 900 If current output values is 1000 1001 101_2 and 2 clock cycles is applied at W m the new output values will be 1001 0000 000 after 1 clock 1001 0000 001_2 after 2 clock

SOLUTIONS