SINGAPORE POLYTECHNIC

2015/2016 S2 MID-SEMESTER TEST

SAS code: **MST**

MODULE: DIGITAL ELECTRONICS MOD. CODE: ET1004

COURSE/YEAR: DASE/DCEP/DESM/DCPE/ DEEE 1FT

Section A

1 (d) 2 (d) 3 (b) 4 (c) 5 (d) 6 (b) 7 (a) 8 (c) 9 (c) 10 (b)

SECTION – B

ADD $+23_{10}$ to $+66_{10}$ in BCD format

+23	=		**0**	**0**	**1**	**0**	**0**	**0**	**1**	**1**
+66	=		**0**	**1**	**1**	**0**	**0**	**1**	**1**	**0**
89	=		**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**

ADD $+76_{10}$ to $+17_{10}$ in BCD format

+76	=		**0**	**1**	**1**	**1**	**0**	**1**	**1**	**0**
+37	=		**0**	**0**	**1**	**1**	**0**	**1**	**1**	**1**
	=		**1**	**0**	**1**	**0^1**	**1**	**1**	**0**	**1**
				+1	**1**	**0**		**+1**	**1**	**0**
+113	=	**0**	**0**	**0**	**1**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**

Add -48_{10} to $+67_{10}$ in 8 bits 2's complement system

		sign	64	32	16	8	4	2	1
+48	=	**0**	**0**	**1**	**1**	**0**	**0**	**0**	**0**
-48	=	**1**	**1**	**0**	**1**	**0**	**0**	**0**	**0**
+67	=	**0**	**1**	**0**	**0**	**0**	**0**	**1**	**1**
+19	=	**~~1~~**	**0**	**0**	**0**	**1**	**0**	**0**	**1**	**1**

SOLUTIONS

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No	SOLUTION
B2 a)	Given: $A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0 = 0\ 1\ 0\ 0\ 0\ 1\ 1\ 1_2$ $B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0 = 1\ 1\ 0\ 1\ 1\ 1\ 1\ 0_2$ And, $Ci = 1_2$. $Co\ S_7\ S_6\ S_5\ S_4\ S_3\ S_2\ S_1\ S_0 = 1\ 0\ 0\ 1\ 0\ 0\ 1\ 1\ 0_2$ Co S7 S0
b)	If 8 bits two's complement signed arithmetic is used the equivalent decimal values are: For input A, the decimal value is +ve 71 since sign bit is 0 & input B, is in 1's complement form as the sign bit is 1 & Cin = 1 Therefore the B input is -ve 33 and the sum result = +ve 38
c)	Eight (8) 74LS283 Adder ICs are required to build a 32-bit parallel Adder.

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No	SOLUTION
B3 (a)	Frequency = 0.8 / RC = $0.8/(200 * 10^{-6})$ = 4000 Hz
(b)	Flip-flop X is the LSB and Flip-flop Z is the MSB
(c)	Mod-5 counter
(d)	Frequency at Output Z = 4000/5 = 800Hz Z Y X 0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 0 0 0 from count sequence, waveform at Z is: 0 0 0 0 1 Thus duty cycle of waveform at Z = 1/5 * 100 = 20%

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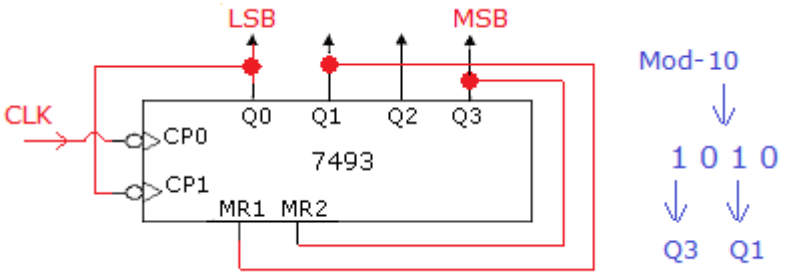
No	SOLUTION
C1 (a)	Mod number of BCD counter = **mod -10_{10}**
(b)	Given Clk = 100_{10} kHz Frequency at P = 100000/8 = **12500 Hz** Frequency at Q = 12500/10 = **1250 Hz**
(c)	Mod number of **3rd** counter = 1250/250 = **Mod -5_{10}** Overall Modulus = 8 X 10 X 5 = **Mod 400**
(d)	 Important Correct number of flip-flops, i.e. 4 FFs & connection. Correct clock input is used. Indication of correct LSB and MSB outputs. MR1 & MR2 connections to the correct outputs.
(e)	To obtain 50% duty cycle for output R, reconfigure the cascade such that the **Mod-8** is the 3rd or last counter in the cascade.

SOLUTIONS