SINGAPORE POLYTECHNIC ET1004

2014/2015_S2 MID-SEMESTER TEST

SAS code: **TST1**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Energy Systems Management DESM 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet.

4. There are 6 pages in this MST paper.

5. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

1. For a positive decimal number **<** 127 in magnitude and is Even, what are the general characteristics of the LSB (**b0**) and the bit in the MSB position (**b7**) when it is converted into an 8-bit 2's complement signed binary number?

(a) $b_7 = 1, \ b_0 = 0$.
(b) $b_7 = 0, \ b_0 = 0$
(c) $b_7 = 1, \ b_0 = 1$
(d) $b_7 = 0, \ b_0 = 1$

2. In an 8-bit two's complement signed numbering system, the largest positive decimal value is represented by _____.

(a) 11111111_2 (b) 10000000_2 (c) 01111111_2. (d) 01000000_2

3. A shift register with one data input **a**nd many data outputs is a:

(a) serial-in, parallel-out register
(b) serial-in, serial-out register
(c) parallel-in, parallel-out register
(d) parallel-in, serial-out register

4. What is the binary value at the output of a mod-12_{10} binary up-counter after the application of 59_{10} clock cycles, assuming that the initial state of the counter is 0011_2?

(a) 0100_2 (b) 0011_2 (c) 0010_2 (d) 0001_2

5. Two sets of 8-bit numbers A and B are to be subtracted (i.e. A - B), using an 8-bit parallel adder circuit, how should the circuit and data be set up to perform this operation, assuming the 8-bit 2's complement signed numbering system is used?

(a) The Carry-input of the adder should set to 0 and the B data should be expressed in the 1's complement form.

(b) The Carry-input of the adder should be set to 1 and the B data should be expressed in the 2's complement form.

(c) The Carry-input of the adder should be set to 0 and the B data is expressed in its true binary form.

(d) The Carry-input of the adder should be set to 1 and the B data should be expressed in the 1's complement form

6. If the inputs to a Full-Adder are augend A = 0, addend B =1, carry-input Cin = 1, the outputs will be:

(a) Cout = 1, Sum = 1 (b) Cout = 1, Sum = 0

(c) Cout = 0, Sum = 1 (d) Cout = 0 Sum = 0

7. To obtain a 16_{10} kHz signal from a 160_{10} kHz clock source, which one of the following counters would you use?

(a) Decade counter

(b) Mod-20_{10} down counter

(c) Mod-100_{10} ripple-counter

(d) A divide by 16_{10} asynchronous counter

8. A binary counter that counts sequentially from 0000_2 to 1011_2 is a mod ____ binary counter.

(a) 10_{10} (b) 11_{10} (c) 12_{10} (d) 13_{10}

9. How many JK flip-flops are required to build a mod-100_{10} counter that counts in the binary sequence?

(a) 100_{10} (b) 10_{10} (c) 8_{10} (d) 7_{10}

10. Identify the circuit shown in Figure A10.

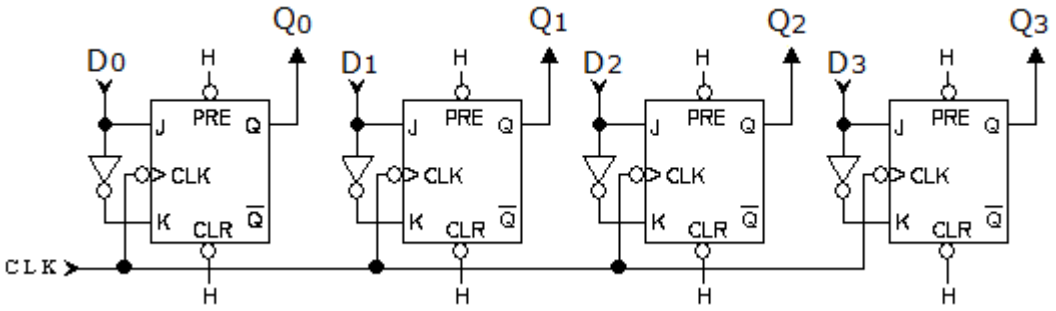

Figure A10

(a) 4-bit mod 2^N ripple counter

(b) 4-bit Decade counter

(c) 4-bit parallel-in, parallel-out shift register

(d) 4-bit serial-in, serial-out shift register

Section B (45 marks)

B1(a) Perform the following operation using the **2's complement signed numbering** system. You are to assume that each number is to be represented by 8 bits, including the sign bit.

Add $+88_{10}$ to -53_{10}

(8 marks)

B1(b) Express the following pair of numbers in the **BCD** format and hence perform the addition of the numbers using **BCD arithmetic**.

Add $+57_{10}$ to $+35_{10}$

(7 marks)

NB: All workings in question B1 must be shown or marks will not be awarded.

B2(a) A Full Adder (FA) adds 3 bits: A, B and Cin to produce 2 output bits usually labeled as Sum and Cout. Draw the symbol of the Full Adder, appropriately labeled as described..

(2 marks)

(b) Complete the truth table for the full adder (FA) circuit in your Answer Booklet using a table format as shown in Table B2(b) and derive the Boolean equations for both Sum and Cout outputs.

(10 marks)

A	B	Cin	Cout	Sum
0	0	0	?	?
:	:	:	:	:
1	1	1	?	?

Table B2(b)

(c) Using Boolean theorems only, show how the Boolean equation of the Sum output can be transformed to an expression that uses only two XOR gates.

(3 marks)

B3(a) Three NGT JK flip-flops and a NAND gate are given in figure B3.1. Copy to your answer booklet figure B3.1 and complete the connections for the three flip-flops and NAND gate so that the circuit functions as a **mod-6_{10}** asynchronous counter**.**

(6 marks)

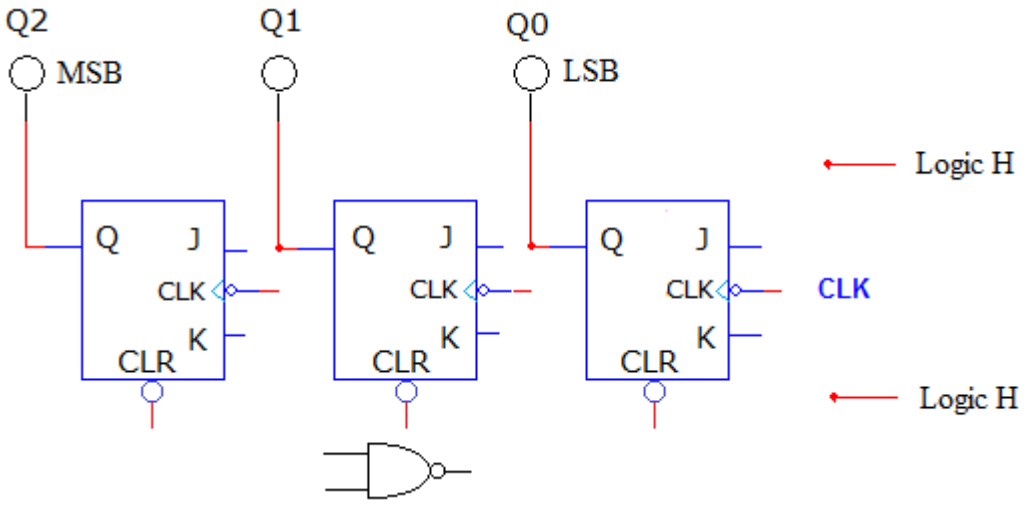

Figure B3.1

B3(b) For the clock signal waveform shown in figure B3.2, copy the diagram to your answer booklet and draw the output signal waveforms of the mod-6_{10} counter that you constructed in figure B3.1. You are to assume that the initial values of the three flip-flops are logic Low and, all propagation delays may be neglected.

(5 marks)

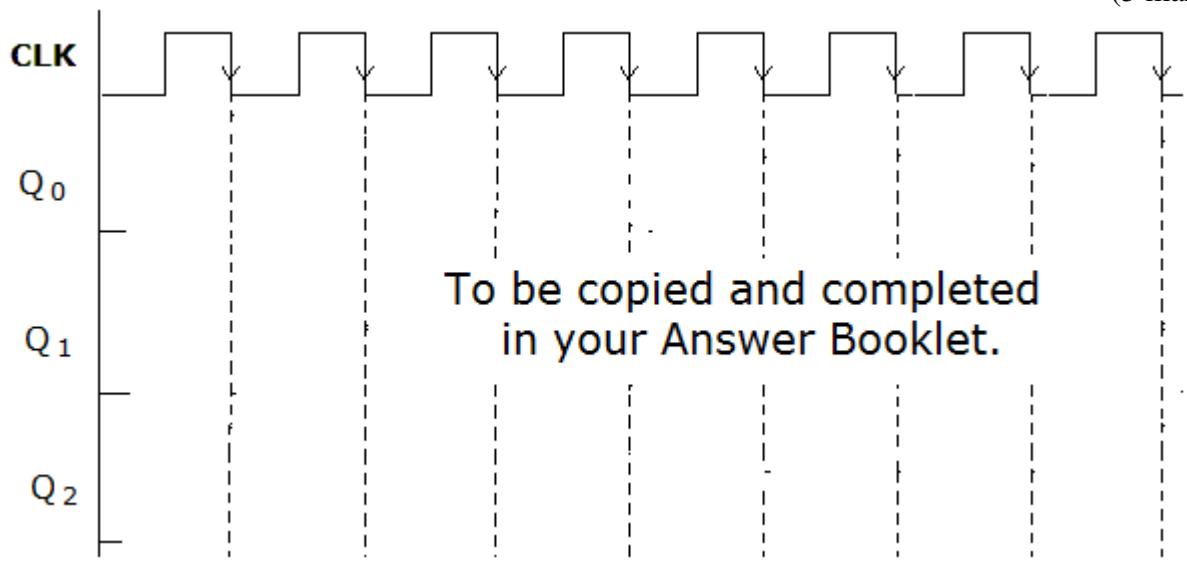

Figure B3.2

B3(c) If the clock signal frequency in figure B3.2 is 3000_{10} Hz, what is the signal frequency and duty cycle at the MSB output Q2?

(4 marks)

Section C (25 marks)

C1. A 4-bit asynchronous binary counter has a count sequence as illustrated in Table C1.

	Outputs			
Clock	Q3 (MSB)	Q2	Q1	Q0 (LSB)
↓	0	0	0	0
↓	0	0	0	1
↓	0	0	1	0
↓	0	0	1	1
↓	0	1	0	0
↓	0	1	0	1
↓	0	1	1	0
↓	0	1	1	1
↓	1	0	0	0
↓	0	0	0	0

Table C1

(a) Analyze the table carefully and determine the mod-number of the counter. (4 marks)

(b) Draw the state transition diagram for the counter you identified in part (a). (4 marks)

(c) Using one 7493 counter IC (symbol and internal circuit as shown in Figure C1.2), construct the counter you have identified in part (a). Ensure that all inputs and outputs are clearly labeled or marks will be deducted. (8 marks)

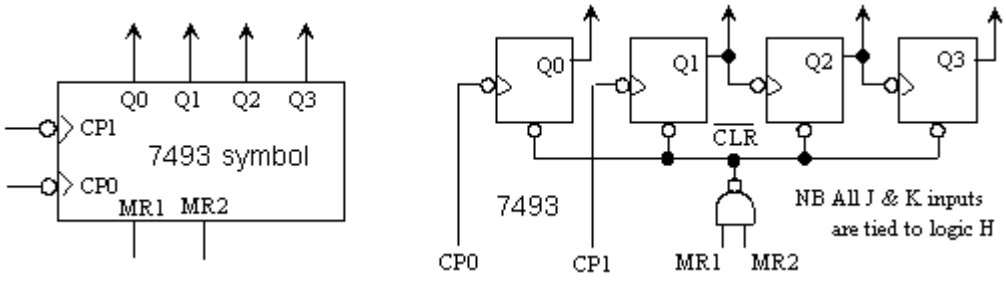

Figure C1.2

(d) If the frequency of the signal at the MSB output of the counter of part (c) is 10_{10} kHz, what is the frequency of the signal applied at its CLK (clock) input?

(3 marks)

(e) If the signal frequency at the MSB output of the counter in part (c) is to be further divided by 10_{10} so that a 1 kHz signal is obtained, show how another 7493 IC must be connected to achieve this. Ensure your circuit drawn is clearly labeled or marks will be deducted.

(6 marks)

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