2010/2011 S2

SINGAPORE POLYTECHNIC ET1004

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

(BCD - represents each decimal digit with 4-bit)

1. If the BCD representation of a Decimal number is 0011 1001 0111 0000_2, what is the equivalent decimal number?

(a) 3870_{10} (b) 2860_{10} (c) 2970_{10} (d) 3970_{10}

Ans: (d)

2. To operate a JK flip-flop in the Toggle mode, the required settings for the JK inputs should be:

(a) K = NOT J (b) J = 0, K = 0

(c) J shorted to K (d) J = 1, K = 1

Ans: (d)

3. If the result of an addition of two signed numbers in the 8-bit two's complement numbering system is 1000 0000_2, what is the decimal equivalent?

8-bit gives 2^8 = 256 numbers: 128 +ve and 128 -ve numbers

(a) Arithmetic overflow has occurred. (b) -128_{10}

(c) $+127_{10}$ (d) Zero

Ans: (b)

0000 0000= 0
0000 0001= +1
etc. etc.
0111 1111= +127
1000 0000= -128
etc. etc.
1111 1111= -1

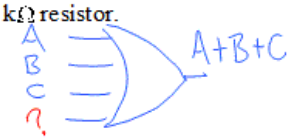
4. How should the unused input of a 4 input OR gate be treated if only 3 inputs are required? *(Remember an unconnected TTL input reads a weak '1' while an unconnected CMOS input is driven by noise.)*

(a) The unused input should be connected to logic High through a 1 kΩ resistor.

(b) The unused input should be connected to ground or logic Low.

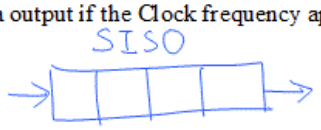
(c) The unused input should be left floating, i.e. unconnected.

(d) The unused input pin should be cut-off.



Ans: (b) *Note that A+B+C+0 = A+B+C; but A+B+C+1 = 1*

5. How long does it take for a 1-bit data applied at the input of a 4-bit serial-in, serial-out shift register to appear at its data output if the Clock frequency applied is 1 kHz?



(1k bits per sec. or 1 bit per ms.)

(a) approximately 4 Sec.

(b) approximately 4 mSec.

(c) approximately 4 µSec.

(d) approximately 4 times the propagation delay of 1 flip-flop.

Ans: (b)

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6. How many **Select inputs** are required for a Decoder with **1** enable input and **16** data outputs? *Binary decoder - only one of the outputs will be active, depending on the binary code at the select inputs.*

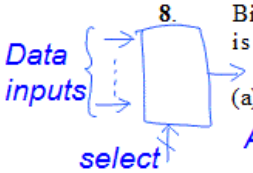
(a) 1_{10} (b) 4_{10} (c) 6_{10} (d) 64_{10}

Ans: (b) $2^4 = 16$

7. What is the maximum mod-number that can be attained for a **ripple** counter that uses 7 JK flip-flops?

(a) mod 7_{10} (b) mod 64_{10} (c) mod 128_{10} (d) mod 256_{10}

Ans: (c) $2^7 = 128$

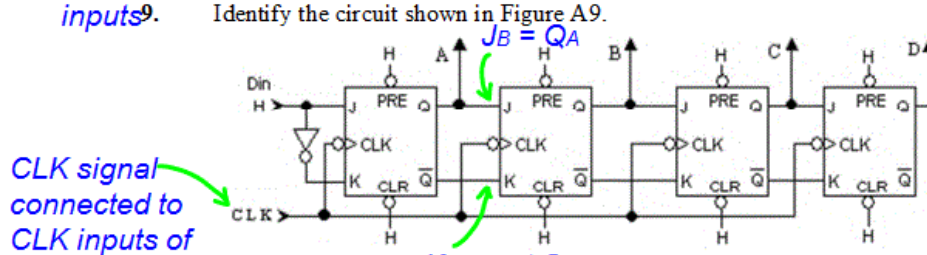


8. Binary data from several data sources are to be combined into a single stream before it is transmitted. Which one of the following devices would be used for this purpose?

(a) Multiplexer (b) Demultiplexer (c) Decoder (d) Encoder

Ans: (a)

9. Identify the circuit shown in Figure A9.



J K	CLK	Q
0 0	NGT	No change
0 1	NGT	0 (Clear)
1 0	NGT	1 (Set)
1 1	NGT	Toggle

CLK signal connected to CLK inputs of all flip-flops

Figure A9

(a) 4 bit mod 2^N ripple counter
(b) 4-bit parallel-in, parallel-out shift register
(c) 4-bit Decade counter
(d) 4-bit serial-in, parallel-out shift register

When $Q_A = 0$, $= J_B$, $K_B = 0, 1$ makes $Q_B = 0$ after NGT

When $Q_A = 1$, $= J_B$, $K_B = 1, 0$ makes $Q_B = 1$ after NGT

Ans: (d)

10. In an 8-bit two's complement signed numbering system, the addition of two negative numbers produces a resultant sign bit of 0. What does this indicate?

Indicates +ve number

(a) The sum result is valid and positive.
(b) The sum result is a valid and negative.
(c) An arithmetic overflow has occurred.
(d) The result cannot be interpreted unless the actual magnitudes are known.

Ans: (c) *(Overflow - the number is too big to be represented by the given number of bits.)*

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Section B Short Questions (60 marks)

B1(a). Convert decimal 283_{10} to Binary, and Hexadecimal.

283 / 2 = 141 r.1
141 / 2 = 70 r.1
70 / 2 = 35 r.0
35 / 2 = 17 r.1
17 / 2 = 8 r.1
8 / 2 = 4 r.0
4 / 2 = 2 r.0
2 / 2 = 1 r.0
1 / 2 = 0 r.1

283 = 1 0001 1011 (in bin.)
1 1 B (in hex.)

(4 marks)

(b) Perform the following operation using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit.

Add -53_{10} to $+86_{10}$

(8-bit)
+53 = 0011 0101
Invert: 1100 1010
Add 1: **1100 1011** = -53

(6 marks)

NB: ***All workings in question B1 must be shown or marks will not be awarded.***

-53 = 1100 1011
+86 = 0101 0110
Sum: **0010 0001** = +33 (in 8-bit)

Discard carry-out to the 9-th bit.

B2(a) The Full Adder (FA) circuit has three inputs: augend **A**, addend **B** and, carry-input **Cin**. The FA circuit adds the three input bits together to produce a **Sum** and a carry-output **Cout**. Complete the truth table of the FA circuit in your Answer Booklet using a table format as shown in Table B2.

(4 marks)

A	B	Cin	Cout	Sum
0	0	0	?	?
:	:	:	:	:
:	:	:	:	:
1	1	1	?	?

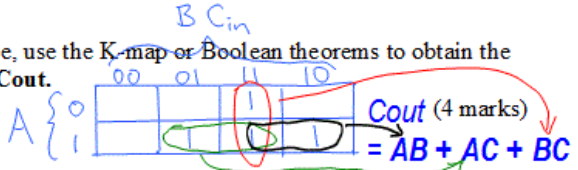
Table B2

Inputs Outputs

Rules for this truth-table:
0 + 0 + 0 = 0
0 + 0 + 1 = 1
0 + 1 + 1 = 2
1 + 1 + 1 = 3
Inputs Outputs

A B Cin	Cout	Sum
0 0 0	0	0
0 0 1	0	1
0 1 0	0	1
0 1 1	1	0
1 0 0	0	1
1 0 1	1	0
1 1 0	1	0
1 1 1	1	1

(b) Based on your completed truth table, use the K-map or Boolean theorems to obtain the simplified Boolean expression for **Cout**.



Cout (4 marks)
= AB + AC + BC

(c) An **8-bit parallel adder** is to be constructed from the Full Adder (FA) circuit. **How many** of these **FA** units are required to construct this **8-bit parallel Adder**? You are **not required** to draw the circuit of this adder.

(2 marks)

An 8-bit adder requires 8 FAs.

B3. Each of the 5 statements comprising this question describes a particular type of **counter or shift register** circuit. You are required to state in your answer booklet, the type of counter or register circuit being described by each statement. Ensure that your answers are labelled exactly according to each of the statements i.e. **[(a), (b)....(e)]** or marks will not be awarded.

(10 marks)

(a) The output states run in this binary sequence: 0000, 0001, 0010, 0011, 0100, 0101, 0110, 0111, 1000, 1001 and repeats from 0000. *MOD-10 counter*

(b) This shift register circuit has several data inputs and one data output.
PISO (Parallel-In Serial-Out) shift register

(c) Each flip-flop in this counter divides its clock input frequency by 2.
Ripple counter (On contrast, sychronous counters are not so.)

(d) This counter can count with increasing or decreasing count.
Up/down counter

(e) This counter divides its input frequency by its Mod number.
Frequency divider

B4(a) The 74138 is a **1-of-8** decoder device and has a symbol as shown in figure B4.1. Briefly explain what the description **1-of-8** decoder means. Give another **name** for the 1-of-8 decoder.

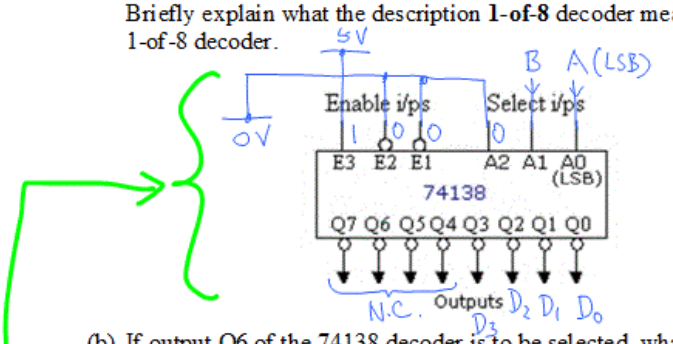


Figure B4.1

Only 1 of the 8 outputs can be active.
(3 marks)

Also called: 3-to-8 decoder
(It has 3 select inputs and 8 outputs.)

(b) If output Q6 of the 74138 decoder is to be selected, what logic levels are required at both the **Enable** and **Select** inputs?
***E3,E2,E1 = 100** and **A2,A1,A0 =110 (=6)** .* (3 marks)

(c) Show how the 74138 decoder can be connected as a 1-of-4 decoder. Indicate and label clearly all required connections and/or logic levels at the inputs. Outputs which are used should be labelled as D0 to D3. Unused outputs, if any, should be marked as N.C. which is the abbreviation for no connection.

(4 marks)

B5 A 3-variable combinational logic circuit has a truth-table as given in Table B5:

Inputs Output

C MSB	B	A LSB	Z
0	0	0	1
0	0	1	1
0	1	0	0
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

Table B5

(a) Given the logic symbol of the 74151, an **8-to-1 multiplexer** IC as shown in figure B5.1, show how you would configure the device to implement the expression for output Z. Your solution should be clearly labelled or marks will be deducted.

(7 marks)

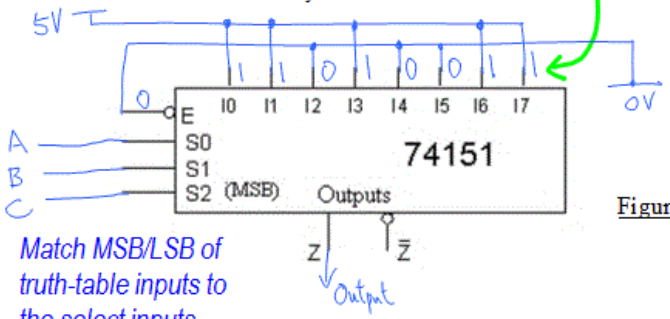


Figure B5.1

Match MSB/LSB of truth-table inputs to the select inputs

(b) For the 74147 **decimal-to-BCD** priority encoder circuit shown in figure B5.2, what is the code (in binary) generated at the inverter outputs Z_3 Z_2 Z_1 Z_0?

(3 marks)

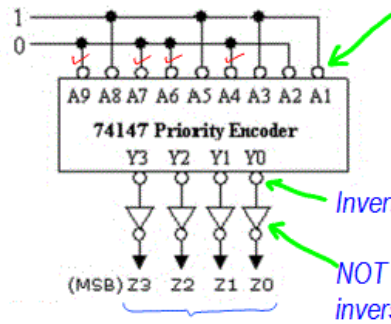


Figure B5.2

The inputs are active-LOW (i.e. activated by '0')

Inverted outputs (i.e. active-LOW)

NOT gates to cancel off the above inversion.

1001 = 9

(Priority encoder outputs a binary code to indicate the highest input which is active.)

B6 Typical performance ratings and voltage parameters for five series of the TTL family of logic devices are given in the table B6. The values shown in the table are on a **per gate basis.**

	74	74S	74LS	74AS	74ALS
*Performance ratings **per gate***					
Propagation delay (ns)	10	3	9.5	1.7	4
Power dissipation (mW)	10	20	2	8	1.2
Speed-power product (pJ)	90	60	19	13.6	4.8
Max. clock rate (MHz)	35	125	45	200	70
Fan-out (same series)	10	20	20	40	20
Voltage parameters in Volts					
V_{OH} (min)	2.4	2.7	2.7	2.5	2.5
V_{OL} (max)	0.4	0.5	0.5	0.5	0.4
V_{IH} (min)	2	2	2	2	2
VIL (max)	0.8	0.8	0.8	0.8	0.8

Table B6

(a) Which TTL series has the **lowest** guaranteed **output voltage** for logic **High**?

74-series (1 mark)

(b) Which TTL series has the **Highest clock frequency**?

74AS-series (1 mark)

(c) Which TTL series has the **Highest power consumption**?

74S-series (1 mark)

(d) Which TTL series can have the **most number** of **TTL inputs** (of the same series) **connected** to its **single output**?

74AS-series (2 marks)

(e) A simple digital circuit consisting of **8** NAND **gates** from **two** 74**LS**00 ICs is connected to a DC supply voltage of **5V**. What is the total power dissipation for this circuit? Calculate the average supply current **Icc** drawn from this **5V** DC power supply. (5 marks)

Power dissipation for each gate of 74LS-series is 2 mW.
*8 gates --> **16 mW**.*

Power = Vcc x Icc
16 mW = 5V x Icc
*Icc = 16 mW / 5V = **3.2 mA***

Section C Long Question (20 marks)

C1. A **10 kHz** Clock signal is to be derived from an Astable multivibrator connected in cascade with a counter/divider circuit as illustrated in the block diagram of figure C1.1.

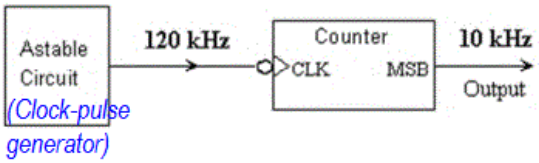


Figure C1.1

(a) If the Astable circuit is oscillating at **120 kHz**, determine the Modulus (i.e. mod number) of the required counter if its MSB output is to be **10 kHz**.

MOD = Clock freq. / MSB freq. = 120 kHz / 10 kHz = ***12***

(3 marks)

(b) Using one 7493 IC, the symbol and internal circuit of which is given in figure C1.2, show how you would connect the IC to function as the counter identified in part (a). Draw your circuit in your answer booklet using only the **7493 symbol**. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will be deducted.

Reset flip-flops when count =12 = 1100 in binary (i.e. when Q3, Q2 = 1,1)

(7 marks)

Connect Q0 to CP1 to link the first flip-flop to the second one.

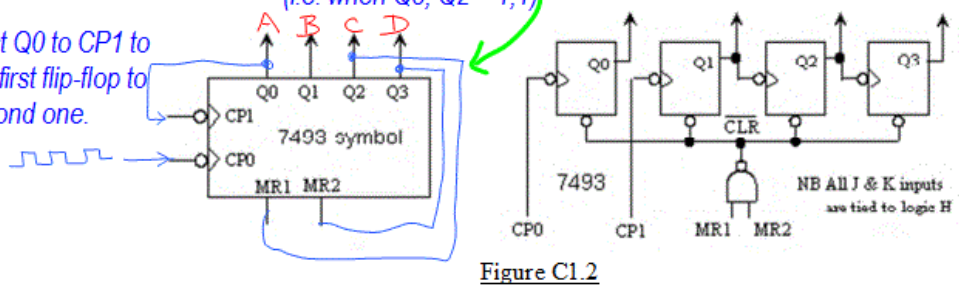


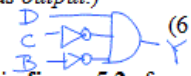
Figure C1.2

(c) If the counter outputs are connected to a decoding circuit such that whenever the counter output is decimal **8** (i.e.**1000_2**) **or** decimal **9**, a logic **High** is obtained at the output of the decoder, Y. Implement this decoder circuit using basic gates of AND, OR and NOT.

Y = D.C'.B'.A' + D.C'.B'.A - i.e. when DCBA = 1000 or 1001

(*Hint: Set up a truth table with Q3 Q2 Q1 Q0 as inputs and Y as output.*)

Y = D.C'.B'.(A + A') = ***D.C'.B'*** *= D C̄ B̄*



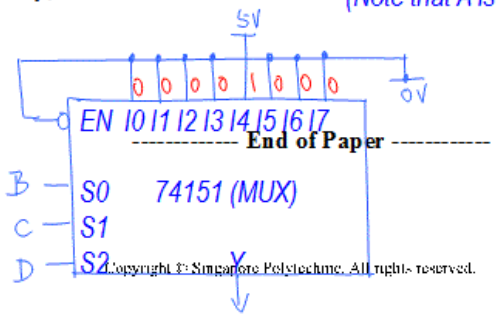
(6 marks)

D	C	B	Y
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	0

(d) Using one 74151 IC, an 8-to-1 multiplexer (symbol as shown in **figure 5.2** of question B5, implement the same decoder circuit of part **(c)** above. Ensure that you labelled your circuit clearly, or marks will be deducted.

(Note that A is not in the expression for Y.)

(4 marks)



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