

REGISTER 21-2: ADCON1: A/D CONTROL REGISTER 1

| | | | | | | | |
|-------|-----|-------|-------|----------------------|--------------------|--------------------|--------------------|
| U-0 | U-0 | R/W-0 | R/W-0 | R/W-0 ⁽¹⁾ | R/W ⁽¹⁾ | R/W ⁽¹⁾ | R/W ⁽¹⁾ |
| — | — | VCFG1 | VCFG0 | PCFG3 | PCFG2 | PCFG1 | PCFG0 |
| bit 7 | 6 | 5 | 4 | 3 | 2 | 1 | bit 0 |

Legend:
 R = Readable bit W = Writable bit U = Unimplemented bit, read as '0'
 -n = Value at POR '1' = Bit is set '0' = Bit is cleared x = Bit is unknown

bit 7-6: **Unimplemented:** Read as '0'

bit 5: **VCFG1:** Voltage Reference Configuration bit (V_{REF-} source)

1 = V_{REF-} (AN2)

0 = V_{SS}

bit 4: **VCFG0:** Voltage Reference Configuration bit (V_{REF+} source)

1 = V_{REF+} (AN3)

0 = V_{DD}

bit 3-0: **PCFG3:PCFG0:** A/D Port Configuration Control bits:

Same pin as: RA5, RA3, RA2, RA1, RA0

| PCFG3:PCFG0 | AN12 | AN11 | AN10 | AN9 | AN8 | AN7 ⁽²⁾ | AN6 ⁽²⁾ | AN5 ⁽²⁾ | AN4 | AN3 | AN2 | AN1 | AN0 |
|---------------------|------|------|------|-----|-----|--------------------|--------------------|--------------------|-----|-----|-----|-----|-----|
| 0000 ⁽¹⁾ | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0001 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0010 | A | A | A | A | A | A | A | A | A | A | A | A | A |
| 0011 | D | A | A | A | A | A | A | A | A | A | A | A | A |
| 0100 | D | D | A | A | A | A | A | A | A | A | A | A | A |
| 0101 | D | D | D | A | A | A | A | A | A | A | A | A | A |
| 0110 | D | D | D | D | A | A | A | A | A | A | A | A | A |
| 0111 ⁽¹⁾ | D | D | D | D | D | A | A | A | A | A | A | A | A |
| 1000 | D | D | D | D | D | D | A | A | A | A | A | A | A |
| 1001 | D | D | D | D | D | D | D | A | A | A | A | A | A |
| 1010 | D | D | D | D | D | D | D | D | A | A | A | A | A |
| 1011 | D | D | D | D | D | D | D | D | D | A | A | A | A |
| 1100 | D | D | D | D | D | D | D | D | D | D | A | A | A |
| 1101 | D | D | D | D | D | D | D | D | D | D | D | A | A |
| 1110 | D | D | D | D | D | D | D | D | D | D | D | D | A |
| 1111 | D | D | D | D | D | D | D | D | D | D | D | D | D |

A = Analog input

D = Digital I/O

RA5, RA3, RA2, RA1, RA0 are setup as Digital I/Os.

RA5 & RA3 are setup as Digital I/Os.

(Whether they are inputs or outputs, it depends on the setup in TRISA.)

Note 1: The POR value of the PCFG bits depends on the value of the PBADEN Configuration bit. When PBADEN = 1, PCFG<3:0> = 0000; when PBADEN = 0, PCFG<3:0> = 0111.

Note 2: AN5 through AN7 are available only on 40/44-pin devices.