TUTORIAL 5 (Chapter 3)

SECTION A

MULTIPLE CHOICE QUESTIONS

Refer to Figure 1 for question A1 and A2.

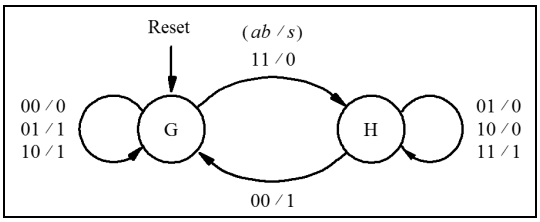

Figure 1

A1. Which one of the followings is the finite state machine's output(s)?

((a) a and b
(b) G and H
(c) s
(d) a, b and s

Ans( )

A2. Which one of the followings is the finite state machine's input(s)?

(a) a and b
(b) G and H
(c) s
(d) a, b and s

Ans( )

A3. Which of the following statement(s) is/are correct?

(I) Any FSM's can be design in either Moore's or Mealy's type.
(II) In Mealy's FSM, the clock must be properly synchronize with input.
(III) For the same design, Mealy's type usually result in simpler circuit.

(a) (I) only
(b) (II) only
(c) (II) and (III)
(d) All the above

Ans( )

SECTION B

B1. Figure 2 shows a state-assigned table for a finite state machine.

(a) Is this a Moore's or Mealy's finite state machine? Support your answer with reason.
(b) Derive the excitation table using D flip-flops.

Present state	Next state		Output	
	$w = 0$	$w = 1$	$w = 0$	$w = 1$
y_2y_1	Y_2Y_1	Y_2Y_1	z	z
00	01	11	0	0
01	01	11	1	0
11	01	11	0	1

Figure 2

B2. Write the Verilog code for the FSM in Figure 2. You may assume that the reset state is "00" and the Reset is asynchronous active low signal and Clock is an active low signal.