TUTORIAL 3 (Chapter 2)

SECTION A

MULTIPLE CHOICE QUESTIONS

A1. What is the time period of clock for the command: **always** #10 clock = ~clock;?

(a) 5
(b) 10
(c) 20
(d) 40

Ans( )

A2. What could be the expression for Figure 1 where in1 and in2 are input reg variables and out is output variable of wire type?

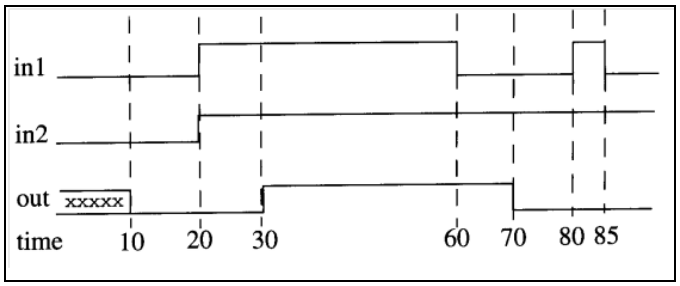

Figure 1

(a) **assign** out = in1& in2;
(b) **assign** out = in1 | in2;
(c) **assign** #10 out = in1& in2;
(d) **assign** #10 out = in1 | in2;

Ans( )

A3. Which of the following loops are supported by Verilog?

(I) forever
(II) if-else
(III) repeat
(IV) while

(a) (I) & (II)
(b) (III) & (IV)
(c) (I), (II) & (III)
(d) (I), (III) & (IV)

Ans( )

SECTION B

B1. Write a Verilog program for the circuit in Figure 1 using gate instantiation.

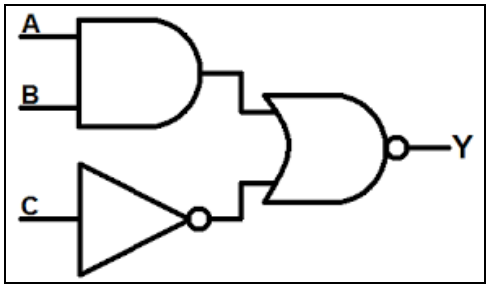

Figure 1

B2. Figure 2 shows the testbench for Figure 1. Draw the waveform of A, B, C and Y after simulation for 80 ns.

```
`timescale 1ns / 1ps
module Figure1_tb();
   wire Y;
   reg A=0;
   reg B=0;
   reg C=0;
    always #40 A=~A;
    always #20 B=~B;
    always #10 C=~C;
    Figure1 dut(A,B,C,Y);
endmodule
```

Figure 2