SINGAPORE POLYTECHNIC **ET1003**

2019/2020 SEMESTER ONE EXAMINATION

Diploma in Aerospace Electronics DASE
Diploma in Computer Engineering DCPE
Diploma in Engineering with Business DEB
Common Engineering Programme DCEP
Diploma in Electrical and Electronic Engineering DEEE
Diploma in Aeronautical Engineering DARE
Diploma in Bioengineering DBEN
Diploma in Mechanical Engineering DME
Diploma in Mechatronics and Robotics DMRO
1st Year Full-Time Time Allowed: 2 Hours

DIGITAL ELECTRONICS 1

Instructions to Candidates:

1. The Singapore Polytechnic examination rules are to be complied with.

2. This paper consists of THREE sections:
   Section A - 10 Multiple Choice Questions, 2 marks each.
   Section B - 4 Short Questions, 15 marks each.
   Section C - 1 Long Question, 20 marks

3. **ALL** questions are **COMPULSORY**.

4. All questions are to be answered in the answer booklet.
   Start each question of Section B and C on a new page.

5. Fill in the Question Number, in the order that it was answered, in the boxes found on the front cover of the answer booklet under the column "Question Answered".

6. Your admission number, class, course of study, module code and module name must be entered in the space provided on the cover page of your Answer Booklet.

7. This paper consists of **9 pages**.

SECTION A

MULTIPLE CHOICE QUESTIONS (2 marks each)

1. Please tick your answers in the MCQ boxes on the front cover of the answer booklet.
2. No marks will be deducted for incorrect answers.

A1. How many different octal numbers can be represented by 12 bits?

(a) 2048_{10}

(b) 4096_{10}

(c) 7778_{10}

(d) 111111111111_{10}

A2. Determine the minimum expression for the K map in Figure A2.

AB \ CD	$\overline{C}\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\overline{B}$	1	0	0	X
$\overline{A}B$	X	X	1	1
AB	0	1	X	X
$A\overline{B}$	0	X	X	0

Figure A2

(a) $\overline{A}\overline{C}\overline{D} + B\overline{C}D + \overline{A}BC$

(b) $\overline{A}\overline{C}\overline{D} + \overline{A}B + A\overline{C}D$

(c) $\overline{A}\overline{D} + BD$

(d) $\overline{A}B + \overline{A}\overline{D}$

A3. Simplify $F = (D + \overline{E})(D + E)(\overline{\overline{F} + D + \overline{G}})$

(a) 1

(b) D + FG

(c) D + F $\overline{D}$ G

(d) 0

A4. The two input waveforms for the Exclusive NOR gate below are given as shown in Figure A4. Which of the following is the correct output waveform?

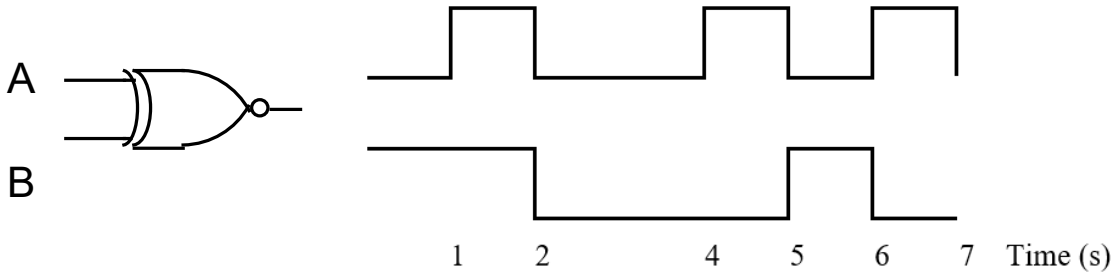
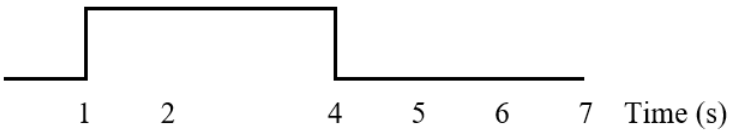
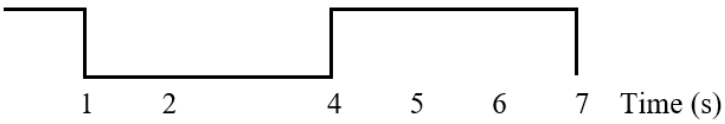


Figure A4

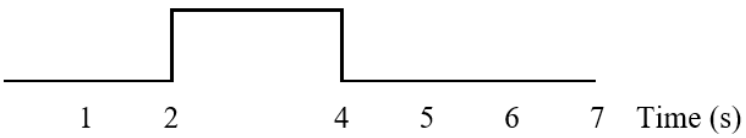
(a)



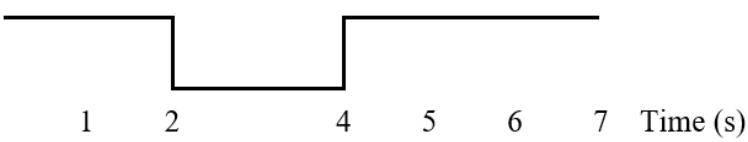
(b)



(c)



(d)



A5. Which of the following statements about the J-K flip flop is false?

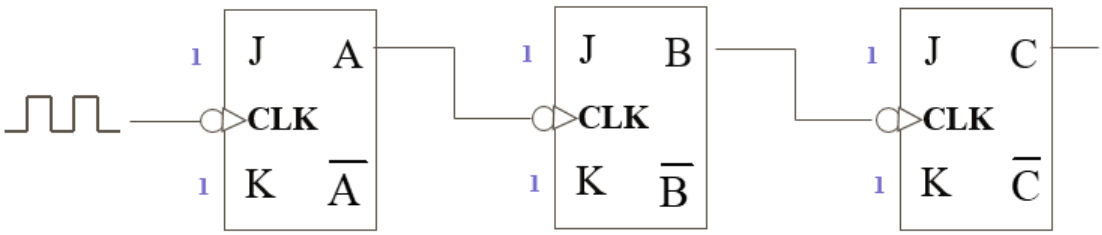
(a) PRESET and CLEAR are asynchronous control inputs.

(b) J, K are synchronous control inputs.

(c) Flip flop cannot be used as latch.

(d) Flip flop is used in sequential circuit design.

A6. Figure A6 shows the circuit of a frequency counter. What is the MOD number of this counter?



PRESET and CLEAR are disabled

Figure A6

(a) 3

(b) 6

(c) 8

(d) 10

A7. Which of the followings is not a multivibrator?

(a) Retriggerable One-Shot

(b) Exclusive OR

(c) Bistable

(d) Schmitt-Trigger

A8. In a 4-input K-map, how many variables will be eliminated for a grouping of 8 '1's?

(a) 4

(b) 3

(c) 2

(d) 1

A9. Implement $A \oplus B$ (A EXOR B) using NAND gates only. How many NAND gates will be required? (Hint: You can use DeMorgan's Theorems)

(a) 3

(b) 4

(c) 5

(d) 6

A10. Analyse the logic circuit in Figure A10. Signal X is the control signal and Signal Y is the data signal. Which of the following set of statements is correct?

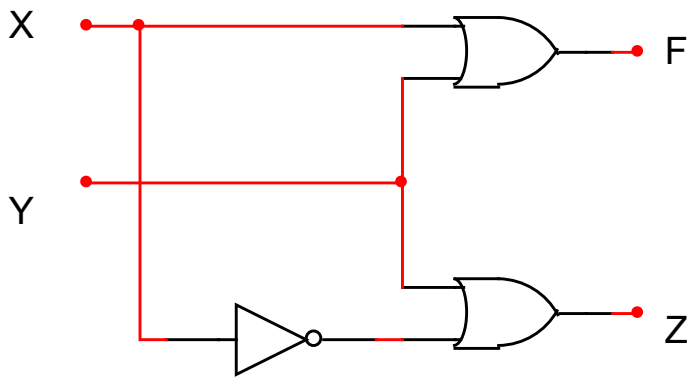


Figure A10

(a) When X = 1 → output F will be disabled and F = 1
When X = 1 → output Z will be enabled and Z will follow Y

(b) When X = 1 → output F will be enabled and F will follow Y
When X = 1 → output Z will be disabled and Z = 1

(c) When X = 0 → output F will be disabled and F = 1
When X = 0 → output Z will be enabled and Z will follow Y

(d) When X = 0 → output F will be enabled and F will follow X
When X = 0 → output Z will be disabled and Z = 0

SECTION B (4 Short Questions, 60 marks)

Note: Write your answers in the answer booklet provided. Start each question on a new page.

B1. **All workings must be shown or marks will NOT be awarded.**

(a) Convert 1021_{10} to octal. (5 marks)

(b) Convert $0001\ 1001\ 0110\ 0011_{BCD}$ to decimal. (5 marks)

(c) Convert $ECAD_{16}$ to binary. (5 marks)

B2.

(a) Write the expression for the output F of the logic circuit in Figure B2.1 (5 marks)

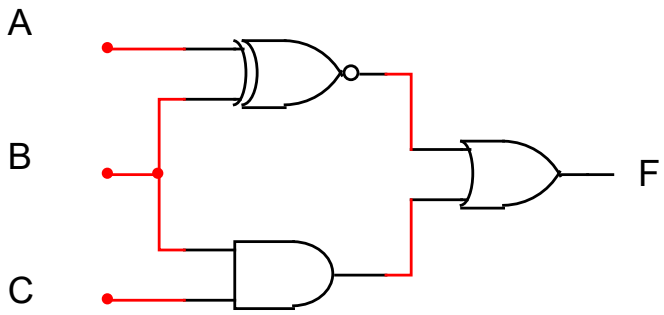


Figure B2.1

(b) Use the expression of output F from part(a) to complete the truth table below. Copy the truth table to the answer booklet.

(10 marks)

A	**B**	**C**	**F**
0	**0**	**0**	
0	**0**	**1**	
: **:**	**:** **:**	**:** **:**	
1	**1**	**1**	

Figure B2.2

B3.

(a) Simplify the logic expression below using Boolean algebra and DeMorgan's theorem.
(5 marks)

$$\overline{\overline{ABC}} + \overline{B}$$

(b) Apply the input waveforms of Figure B3 to logic expression F = AB + $\overline{C}$. Draw the output waveform. Copy the shaded area with output waveform to your answer booklet.
(10 marks)

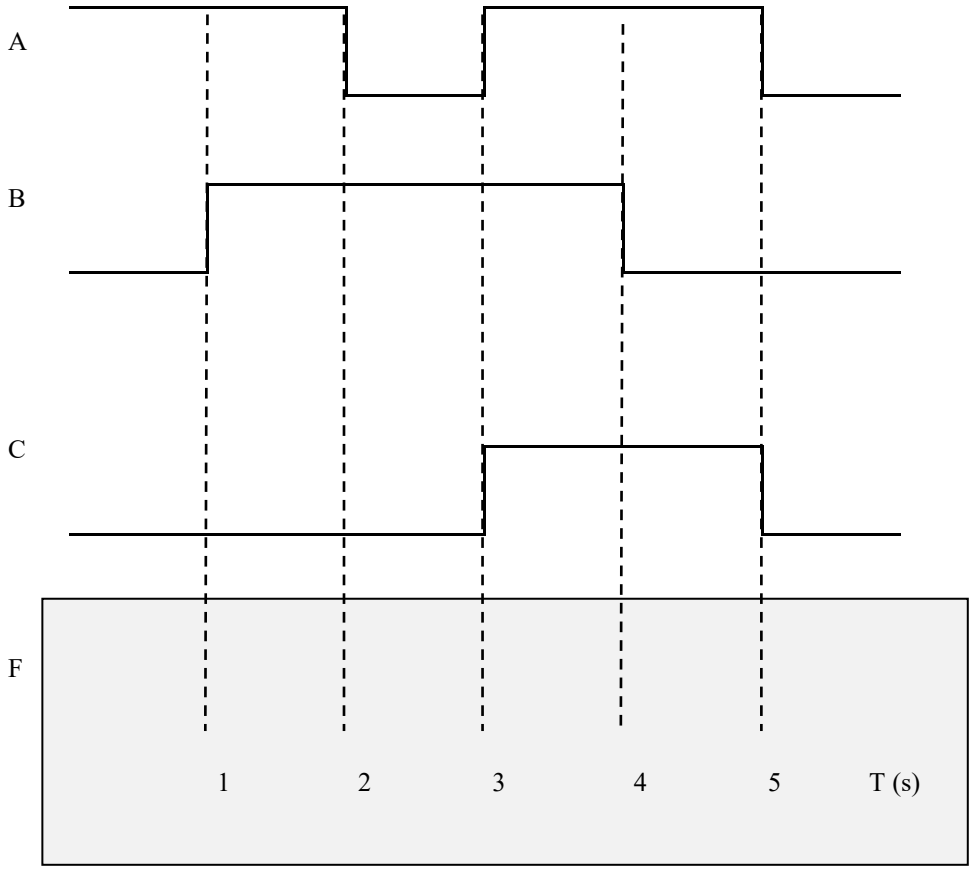


Figure B3

B4.

The typical timing **values (ns)** for various flip flops are shown in Table B4. Study the table and answer the questions B4 (a) and B4 (b).

	TTL		CMOS	
	7474	74LS112	74C74	74HC112
t_S	20	20	60	25
t_H	5	0	0	0
t_{PHL} – from CLK to Q	40	24	200	31
t_{PLH}– from CLK to Q	25	16	200	31
t_{PHL} – from /CLR to Q	40	24	225	41
t_{PLH}– from /PRE to Q	25	16	225	41
t_W(L) – CLK LOW time	37	15	100	25
t_W(H) – CLK HIGH time	30	20	100	25
t_W(L) – at /PRE or /CLR	30	15	60	25
f_{max} – in MHz	15	30	5	20

Table B4

(a) Which flip flop in Table B4 requires its control inputs to remain stable for the longest time after the occurrence of the active clock transition? (2 marks)

(b) Assuming that Q = 1, which flip flop takes the longest time for Q to go LOW in response to the $\overline{CLR}$ input? (2 marks)

(c) A binary counter has an input clock signal with frequency of 128 kHz. The output frequency from the last flip flop is 1 kHz. Determine the MOD number.
(5 marks)

(d) If the counter in part(c) has an initial count of 4, what count will it hold after 1000 clock pulses?
(6 marks)

SECTION C (1 Long Question, 20 marks)

C1. The combinational circuit shown in Figure C1 has 4-bit BCD inputs D, C, B, A and one output Z.

Given that:

- Z = 1 for the BCD coded inputs 1_{10}, 4_{10}, 7_{10}, 9_{10} and
- Z = 0 for the BCD coded inputs 2_{10}, 3_{10} and 8_{10}
- All other BCD codes and invalid entries are to be treated as don't care conditions.

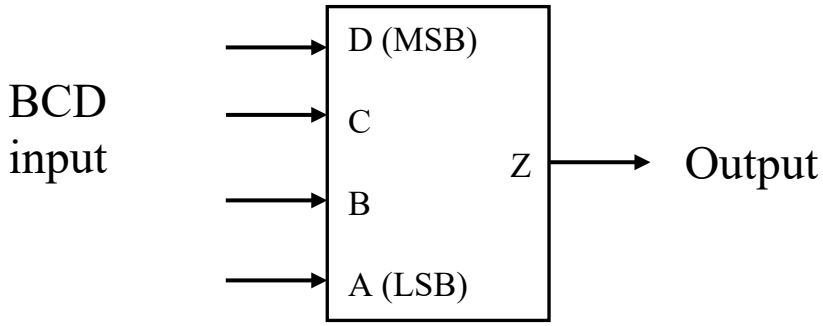


Figure C1

Your task is to design the above circuit using the following steps:

a) Complete the truth table as shown in Table C1. You are required to show all input combinations and expected output responses either '0', '1' or 'X for don't care conditions. (7 marks)

BCD input				Output
D	C	B	A	Z
0	0	0	0	X
0	0	0	1	1
:	:	:	:	:
:	:	:	:	:
1	1	1	1	X

Table C1

b) Use the K-map to derive the simplified logic expression for Z. (5 marks)

c) Implement the logic expression using NOR gates only. What is the minimum number of IC 74LS02 (Quad 2-input NOR) needed to implement the circuit? (8 marks)

- End of Paper -