SINGAPORE POLYTECHNIC

2016/2017 S2 MID-SEMESTER TEST

SAS code: MST

MODULE: DIGITAL ELECTRONICS MOD. CODE: ET1004

COURSE/YEAR: DASE/DCEP/DESM/DCPE/ DEEE 1FT

No	SOLUTION

SECTION – A (10 MCQ, 3 marks each)

1. (d)
2. (d)
3. (b)
4. (c)
5. (d)
6. (c)
7. (a)
8. (c)
9. (b)
10. (b)

	A	B	C	D
1				✓
2				✓
3		✓		
4			✓	
5				✓
6			✓	
7	✓			
8			✓	
9		✓		
10		✓		

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No	SOLUTION

SECTION – B

B1

a) **ADD $+57_{10}$ to $+36_{10}$ in BCD format**

+57 = 0 1 0 1 0 1 1 1 ◄------- BCD

+36 = 0 0 1 1 0 1 1 0 ◄------- BCD

= 1 0 0 0^{1} 1 1 0 1

+ 1 1 0 ◄------- Adjust by adding 6

+93 = 1 0 0 1 0 0 1 1

b) Subtract $+70_{10}$ to $+99_{10}$ =

Equivalent to ADD -70_{10} from $+99_{10}$

sign 64 32 16 8 4 2 1

+70 = 0 1 0 0 0 1 1 0 ◄---------- True binary value

-70 = **1 0 1 1 1 0 1 0** ◄---------- 2's complement

+99 = 0 1 1 0 0 0 1 1 ◄---------- True binary value

+29 = 1 0 0 0 1 1 1 0 1 ◄---------- discard 9th bit

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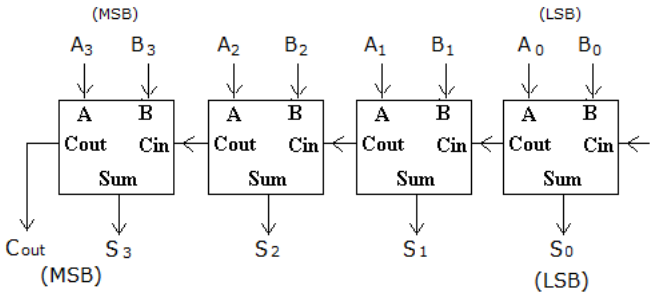
B2 (a)	Given: $A_4\ A_3\ A_2\ A_1\ A_0 = 0\ 1\ 1\ 1\ 0_2$ $B_4\ B_3\ B_2\ B_1\ B_0 = 1\ 1\ 0\ 1\ 1_2$ And $Cin = 1$ $Cout\ S_4\ S_3\ S_2\ S_1\ S_0 = 1\ 0\ 1\ 0\ 1\ 0$
(b)	If 5-bits 2's complement is used, Then the number at the A inputs is +ve since sign bit = 0 And it is = 8+4+2 = $+14_{10}$ The number at the B inputs is -ve as the sign bit = 1 and with Cin = 1; it should be in 1's complement form. Hence the magnitude of the number is = 00100_2 $= 4_{10}$ Hence number at B inputs = -4_{10} The sum result is +ve and = $14 - 4 = +10_{10}$
(c)	To construct the 74LS283 IC, 4 Full Adders are needed. Connection is as shown: 

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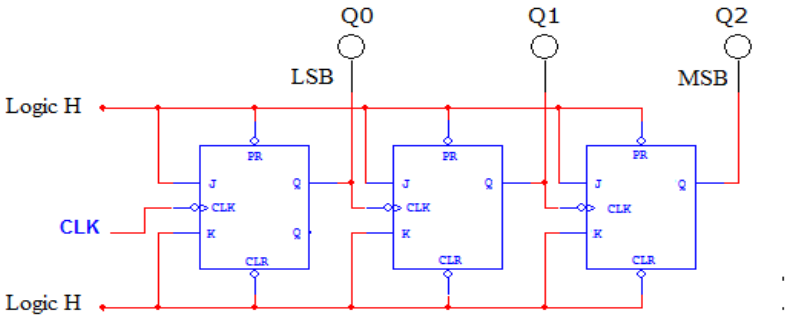
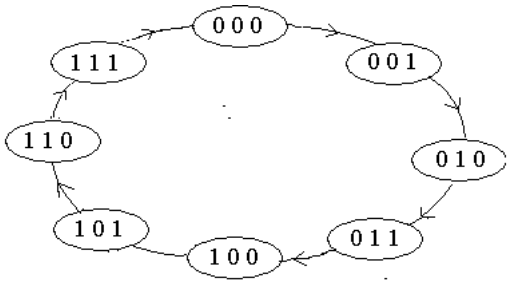
No	SOLUTION
B3 (a)	(i) Frequency = 1/40uS = 25000 Hz or 25 kHz (ii) Duty cycle = 10/40 * 100% = 25%
(b)	Given frequency to mod-8 counter = 25000 Frequency at MSB output = 25000/8 = 3125Hz Duty cycle = 50%
(c)	 Important Use correct number of FFs J=k=PRE=CLR = H Label MSB & LSB
(d)	 Given start state = 000 and 650 Clocks are applied, output values at the end of 650 clks = 010_2

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NOT TO BE GIVEN TO STUDENTS

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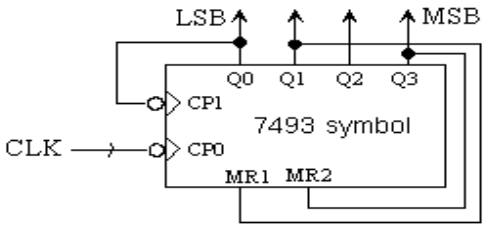
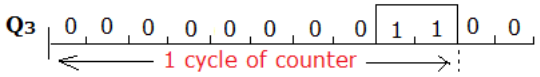
C1 (a)	Frequency at output of Astable Circuit = 10 * 400 = 4000 Hz
(b)	Given $F1 = \frac{0.8}{R1\,C1}$ and C1 = 1uF and with Frequency = 4000 Hz 4000 = 0.8/(R * 10^{-6}) Therefore R = 0.8/(4000 * 10^{-6}) = 200 Ohms
(c)	 Important to Note Q0 to CP1 connection for use of 4 flip-flops CP0 is the clock input MSB and LSB must be labelled clearly Feedback from Q1, Q3 to MR1/MR2 for Mod-10.
(d)	Duty cycle at MSB output = 2/10 * 100% = 20% Since at MSB output Q3, there are 8 periods of 0's and 2 periods of 1's in one cycle of the counter. 

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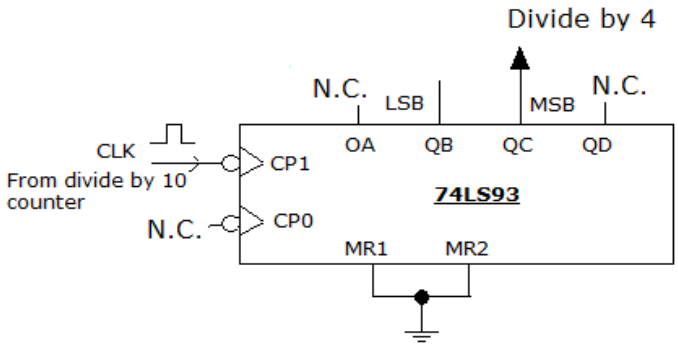
(d)	To further divide the 400Hz signal down to 100 Hz, A Mod-4 counter or divide by 4 counter is required. To build this counter only one 7493 IC is required and being a Mod 2^N counter the output waveform will be 50% duty cycle as required.  NB: A divide by 4 counter is a Mod 2^N which is naturally resetting and hence there is no need to use MR1 and MR2 to force reset. These 2 inputs should be grounded so that the CLR inputs to the flip-flops will be High.