TUTORIAL 2 (Chapter 2)

SECTION A

MULTIPLE CHOICE QUESTIONS

A1. Which of the following statement(s) is(are) legal?

(I) wire aBc1;
(II) wire abc1;
(III) wire 1abc;

(a) I only.
(b) II only.
(c) I and II only.
(d) I, II and III.

Ans( )

A2. If x=4'b1100 then x<<2 is _____.

(a) 4'b0000
(b) 4'b0011
(c) 4'b0110
(d) 4'b1000

Ans( )

A3. -10 % 3 evaluates to _____.

(a) -1
(b) 0
(c) 1
(d) 3

Ans( )

SECTION B

B1. (a) Draw the block diagram for the module B1 in Figure 1.
(b) Derive the truth table for B1 and hence states the function of this design?

```
module B1 (a,b,c,d,S,f);
    input a,b,c,d;
    input  [1:0] S;
    output f;

    assign f = S[1] ? (S[0] ? d : c) : (S[0] ? b : a);

endmodule
```

Figure 1

B2. Write a Verilog code for the 4-bit adder in Figure 2 using only one continuous assignment statement.

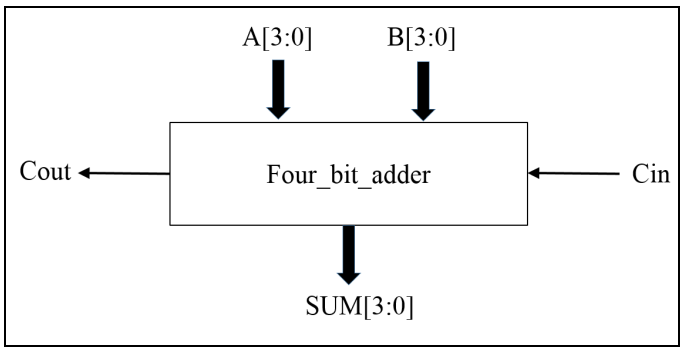

Figure 2