SINGAPORE POLYTECHNIC ET1004

2018/2019 S2 MID-SEMESTER TEST

SAS code: **MST**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Energy Systems Management DESM 1st Year FT

Common Engineering Programme DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet, unless indicated otherwise.

4. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

5. There are 6 pages in this paper.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

A1. A JK flip-flop with J, K, $\overline{PRE}$ and $\overline{CLR}$ connected to logic High, has a CLK signal of 40 kHz applied at its CLK input. What will be the frequency of the signal at its Q output?

(a) 0 Hz or D.C. (b) 40 kHz

(c) 20 kHz (d) 10 kHz

A2. A mod-128_{10} naturally resetting ripple counter is to be constructed using D flip-flops. How many D flip-flops are required?

(a) Not possible to use D flip-flops (b) 5_{10} D-flip-flops

(c) 6_{10} D-flip-flops (d) 7_{10} D-flip-flops

A3. Which one of the following input combinations will result in a Full Adder (FA) having its Sum Output = 1 and, its carry output Cout = 0?

(a) A = 1, B = 1, Cin = 1 (b) A = 1, B = 0, Cin = 1

(c) A = 0, B = 0, Cin = 1 (d) A = 0, B = 0, Cin = 0

A4. What is the mod number of the counter circuit shown in figure A4?

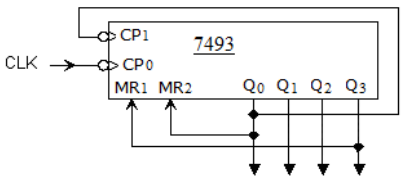


Figure A4

(a) Mod-12_{10} (b) Mod-11_{10} (c) Mod-10_{10} (d) Mod-9_{10}

A5. Which one of the following counters has the most number of flip-flops?

(a) A ripple counter that repeatedly counts from 0 to 32_{10}.

(b) A Mod 16 Up/Down Counter

(c) A Decade Counter

(d) A divide by 30 Asynchronous Counter

A6. In the 2's complement signed numbering system, a positive decimal number will have _____.

(a) a sign bit of 0 in the MSB position.
(b) a sign bit of 1 in the MSB position.
(c) a sign bit of 0 in the LSB position.
(d) a sign bit of 1 in the LSB position.

A7. A mod-32, naturally resetting counter has a signal frequency of 2 kHz at its **MSB** output, what is the signal frequency of the CLK signal applied at its clock input??

(a) 32_{10} kHz (b) 64_{10} kHz (c) 128_{10} kHz (d) 256_{10} kHz

A8. A shift register circuit with **many** data inputs and **one** data output is a _____.

(a) serial-in, serial-out shift register
(b) parallel-in, serial-out shift register
(c) serial-in, parallel-out shift register
(d) parallel-in, parallel-out shift register

A9. A parallel adder which can add signed binary numbers using the 2's complements signed numbering system has a range from -32768_{10} to $+32767_{10}$, is to be constructed using the 74LS83 IC, a 4-bit parallel adder IC. How many of these 74LS83 ICs are required to build this parallel adder circuit?

(a) 1_0 (b) 2_{10} (c) 3_{10} (d) 4_{10}

A10. Which one of the following set of waveforms in figure A10 corresponds to the output waveforms of a Mod 8 binary counter?

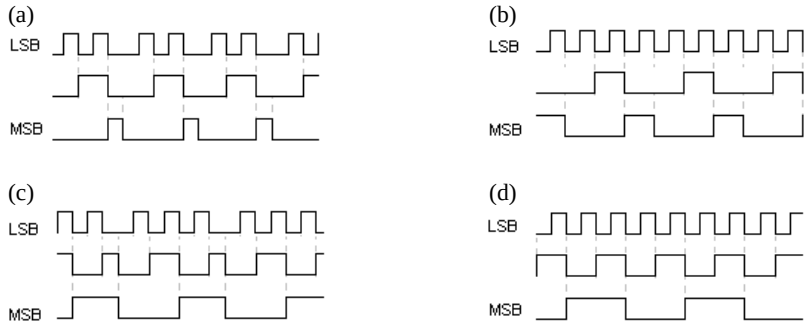


Figure A10

Section B (45 marks)

B1(a) Perform the following calculations using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit. All steps and workings must be shown or marks will be deducted.

(i) Add $+56_{10}$ to $+23_{10}$ (4 marks)

(ii) Subtract $+33_{10}$ from $+72_{10}$ (7 marks)

(b) What is the range of decimal values that can be represented by a 12-bit (including the sign bit) 2's complement signed numbering system?

(4 marks)

B2. A Full Adder is a combinational circuit that is able to add 3 bits which are usually labelled as A, B and Cin (carry-in) and produces two output bits which are appropriately called S (sum) and Cout (for carry-out).

(a) Draw the block diagram of this Full-Adder unit, labelling all the inputs and outputs as specified above.

(3 marks)

(b) List and complete the truth-table of the Full Adder and hence, derive the un-simplified Boolean expressions for outputs Sum and Cout (carry-out). Use the following heading for your truth-table.

(8 marks)

Inputs			Outputs	
A	B	Cin	Cout	Sum

(c) Using Boolean theorems, show that the un-simplified Boolean expression for output Sum can be transformed to one that uses only XOR gates.

(4 marks)

B3(a) Given a periodic clock signal as shown in figure B3.1, calculate its

(i) Period

(ii) Signal frequency.

(iii) Duty cycle.

(6 marks)

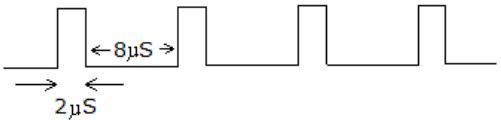
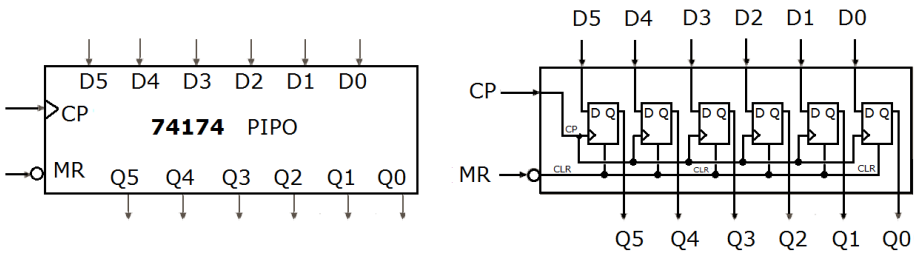


Figure B3.1

(b) The 74174 is a 6-bit, Parallel-in, Parallel-out (PIPO) shift register IC. It has a symbol and internal circuit as shown in figure B3.2. Using one 74174 IC, show how you would connect it as a 4-bit Serial-input, Serial-output (SISO) shift register. Use the symbol and not the internal circuit, for your solution.
Label your circuit clearly or marks will not be awarded. The serial data input should be labelled as D0 and serial output as Z and, unused inputs and outputs, labelled as N.C. Also indicate the logic level required at the MR input.

(9 marks)



Symbol of 74174

Internal Circuit of 74174

Figure B3.2

Section C (25 marks)

C1 The block diagram in figure C1.1 shows the circuit of a Mod-13 counter connected to a decoder that detects the presence of a particular counting sequence.

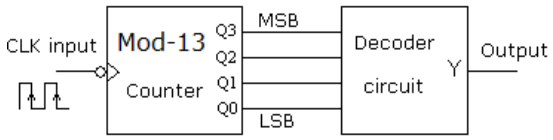


Figure C1.1

Commented [GBH1]:

(a) Given the 7493 (see figure C1.2), a 4-bit binary counter IC, show how you would connect the IC as a Mod-13 counter. You may use any other logic gate(s) as required. Indicate and label clearly all the connections made to the IC.

(8 marks)

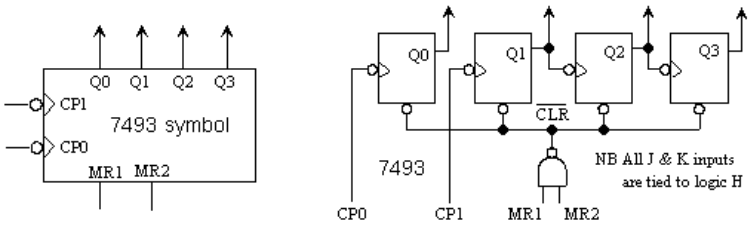


Figure C1.2

(b) Draw the state transition diagram for the Mod -13 counter.

(4 marks)

(c) If the initial state (value) of the Mod-13 counter is 0000 and 145_{10} clock cycles are applied to the counter, what will be the state of the counter at the end of the 145_{10} clock cycles?

(3 marks)

(d) If the decoder circuit is required to produce a logic High output whenever the Mod-13 counter in part (a) **exceeds** the count of 9_{10}, i.e. to produce a logic High output for the counts of 10_{10} through 12_{10}, show how you would design this active-High decoder circuit. You may ignore the effects of propagation delay and use any logic gates as required in your design. (*Hint*: *set up a truth table for this combinational logic circuit with the counter outputs Q3 to Q0 as inputs to the decoder and variable Y as the output and take advantage of any don't care conditions.)*

(10 marks)

---------- **End of Paper** ----------