## **Tutorial for Chapter 8 – Logic Families**

- >8-1. Two different logic circuits have the characteristics shown in Table 8-13
- (a) Which circuit has the best LOW-state dc noise immunity? The best HIGH-state dc noise immunity?
- (b) Which circuit can operate at higher frequencies?
  - (c) Which circuit draws the most supply current?

	Circuit A	Circuit B	
V <sub>supply</sub> (V)	6	5	
V <sub>IH</sub> (min) (V)	1.6	1.8	
V <sub>IL</sub> (max) (V)	0.9	0.7	
V <sub>OH</sub> (min) (V)	2.2	2.5	
V <sub>OL</sub> (max) (V)	0.4	0.3	
t <sub>PLH</sub> (ns)	10	18	
t <sub>PHL</sub> (ns)	8	14	
P <sub>D</sub> (mW)	16	10	

>8-1. (a) A; B (b) A (c) A

→ 8-3. A certain logic family has the following voltage parameters:

$$V_{\rm IH}({\rm min}) = 3.5 \text{ V}$$
  $V_{\rm IL}({\rm max}) = 1.0 \text{ V}$   
 $V_{\rm OH}({\rm min}) = 4.9 \text{ V}$   $V_{\rm OL}({\rm max}) = 0.1 \text{ V}$ 

- (a) What is the largest positive-going noise spike that can be tolerated?
- (b) What is the largest negative-going noise spike that can be tolerated?

⇒8-3. (a) 0.9 V (b) 1.4 V

- 8-4. For each statement, indicate the term or parameter being described.
  - (a) Current at an input when a logic 1 is applied to that input
  - (b) Current drawn from the  $V_{CC}$  source when all outputs are LOW
  - (c) Time required for an output to switch from the 1 to the 0 state
  - (d) A common measure used to compare overall performance of different IC families
  - (e) The size of the voltage spike that can be tolerated on a HIGH input without causing indeterminate operation
  - (f) An IC package that does not require holes to be drilled in the printed circuit board
  - (g) When a LOW output receives current from the input of the circuit it is driving
- (h) Number of different inputs that an output can safely drive
- (i) Arrangement of output transistors in a standard TTL circuit
- (j) Another term that describes pull-down transistor Q<sub>4</sub>
- (k) Range of  $V_{CC}$  values allowed for TTL
  - (1)  $V_{OH}(min)$  and  $V_{IH}(min)$  for the 74ALS series
  - (m)  $V_{\rm IL}(\text{max})$  and  $V_{\rm OL}(\text{max})$  for the 74ALS series
- (n) When a HIGH output supplies current to a load
- ightharpoonup 8-4. (a)  $I_{\rm IH}$  (b)  $I_{\rm CCL}$  (c)  $t_{\rm PHL}$  (d) Speed–power product (e)  $V_{\rm NH}$  (f) Surface-mount (g) Current sinking (h) Fan-out (i) Totem-pole (j) Sinking transistor (k) 4.75 to 5.25 V (l) 2.5 V; 2.0 V (m) 0.8 V: 0.5 V (n) Sourcing

- 8-5. (a) From Table 8-6, determine the noise margins when a 74LS device is driving a 74ALS input.
  - (b) Repeat part (a) for a 74ALS driving a 74LS.
  - (c) What will be the overall noise margin of a logic circuit that uses 74LS and 74ALS circuits in combination?
  - (d) A certain logic circuit has  $V_{\rm IL}({\rm max}) = 450$  mV. Which TTL series can be used with this circuit?

**FABLE 8-6** Typical TTL series characteristics.

	74	748	74LS	74AS	74ALS	74F
Performance ratings		N. A.	Harry Mark			
Propagation delay (ns)	9	3	9.5	1.7	4	3
Power dissipation (mW)	10	20	2	8	1.2	6
Speed-power product (pJ)	90	60	19	13.6	4.8	18
Max. clock rate (MHz)	35	125	45	200	70	100
Fan-out (same series)	10	20	20	40	20	33
Voltage parameters						
V <sub>OH</sub> (min)	2.4	2.7	2.7	2.5	2.5	2.5
V <sub>OL</sub> (max)	0.4	0.5	0.5	0.5	0.5	0.5
V <sub>IH</sub> (min)	2.0	2.0	2.0	2.0	2.0	2.0
V <sub>IL</sub> (max)	0.8	0.8	0.8	0.8	0.8	0.8

3-5. (a) 0.7 V; 0.3 V (b) 0.5 V; 0.4 V (c) 0.5 V; 0.3 V

## ≥8-6. DRILL QUESTION

- (a) Define fan-out.
- (b) In which type of gates do tied-together inputs always count as a single input load in the LOW state?
- (c) Define "floating" inputs.

3-6. (b) AND, NAND (c) Unconnected inputs

- >8-12. How long does it take for the output of a typical 74LS04 to change states in response to a positive-going transition at its input?
- > 8-19. Which of the following are advantages that CMOS generally has over
  - (a) Greater packing density
  - (b) Higher speed
  - (c) Greater fan-out
  - (d) Lower output impedance
  - (e) Simpler fabrication process
  - (f) More suited for LSI
  - (g) Lower P<sub>D</sub> (below 1 MHz)
  - (h) Transistors as only circuit element
- (i) Lower input capacitance
- (j) Less susceptible to ESD

 $\rightarrow$  8-19. a, c, e, f, g, h