

**SINGAPORE POLYTECHNIC**  
**2019/2020 S1 MID-SEMESTER TEST**

**SAS code:****MST**MODULE: DIGITAL ELECTRONICSMOD. CODE: ET1004COURSE/YEAR: DASE/DCEP/DESM/DCPE/ DEEE 1FTSET BY: Lui SK

No	SOLUTION	MARKS	TOTAL MARKS																																																							
	<p><b><u>SECTION – A</u> (10 MCQ, 3 marks each)</b></p> <p>A1 (b)</p> <p>A2 (c)</p> <p>A3 (d)</p> <p>A4 (d)</p> <p>A5 (a)</p> <p>A6 (c)</p> <p>A7 (b)</p> <p>A8 (c)</p> <p>A9 (b)</p> <p>A10 (a)</p> <table><tr><td></td><td>A</td><td>B</td><td>C</td><td>D</td></tr><tr><td>A1</td><td></td><td>✓</td><td></td><td></td></tr><tr><td>A2</td><td></td><td></td><td>✓</td><td></td></tr><tr><td>A3</td><td></td><td></td><td></td><td>✓</td></tr><tr><td>A4</td><td></td><td></td><td></td><td>✓</td></tr><tr><td>A5</td><td>✓</td><td></td><td></td><td></td></tr><tr><td>A6</td><td></td><td></td><td>✓</td><td></td></tr><tr><td>A7</td><td></td><td>✓</td><td></td><td></td></tr><tr><td>A8</td><td></td><td></td><td>✓</td><td></td></tr><tr><td>A9</td><td></td><td>✓</td><td></td><td></td></tr><tr><td>10</td><td>✓</td><td></td><td></td><td></td></tr></table>		A	B	C	D	A1		✓			A2			✓		A3				✓	A4				✓	A5	✓				A6			✓		A7		✓			A8			✓		A9		✓			10	✓				3 marks each	30 marks
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/19/20\_51 MST

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MOD. CODE: ET1004

COURSE/YEAR: DASE/DCEP/DESM/DCPE/ DEEE 1FT

SET BY: Lui SK

No	SOLUTION	MARKS	TOTAL MARKS
B1	<p><b><u>SECTION – B</u> (20 marks each)</b></p> <p>Add <math>+59_{10}</math> to <math>+33_{10}</math></p> <p>sign 64 32 16 8 4 2 1</p> <p><math>+59 = \underline{0 \ 0 \ 1 \ 1 \ 1 \ 0 \ 1 \ 1}</math> ←----- 1 mark</p> <p><math>+33 = \underline{0 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 1}</math> ←----- 1 mark</p> <p><math>+92 = \underline{0 \ 1 \ 0 \ 1 \ 1 \ 1 \ 0 \ 0}</math> ←----- 2 marks</p> <p>Add <math>-21_{10}</math> to <math>+67_{10}</math></p> <p>sign 64 32 16 8 4 2 1</p> <p><math>+21 = \underline{0 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1}</math> ←----- 1 mark</p> <p><math>-21 = \underline{1 \ 1 \ 1 \ 0 \ 1 \ 0 \ 1 \ 1}</math> ←----- 2 marks</p> <p><math>+67 = \underline{0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 1 \ 1}</math> ←----- 1 mark</p> <p><math>+46 = \underline{1 \ 0 \ 0 \ 1 \ 0 \ 1 \ 1 \ 0}</math> ←----- 2 marks</p> <p>b) <b>ADD <math>+27_{10}</math> to <math>+255_{10}</math> in BCD format</b></p> <p><math>+ 255 = 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 1</math> ←----- 1 mark</p> <p><math>+ 27 = \underline{\hspace{2cm} 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 1}</math> ←----- 1 mark</p> <p><math>\hspace{2cm} = 0 \ 0 \ 1 \ 0 \ 0 \ 1 \ 1 \ 1^1 \ 1 \ 1 \ 0 \ 0</math></p> <p><math>\hspace{10cm} + 1 \ 1 \ 0</math> ←----- 1 mark</p> <p><math>+ 282 = \underline{0 \ 0 \ 1 \ 0 \ 1 \ 0 \ 0 \ 0 \ 0 \ 0 \ 1 \ 0}</math> ←----- 2 marks</p>		15 marks

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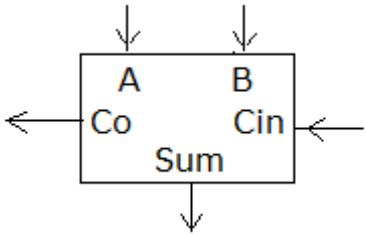
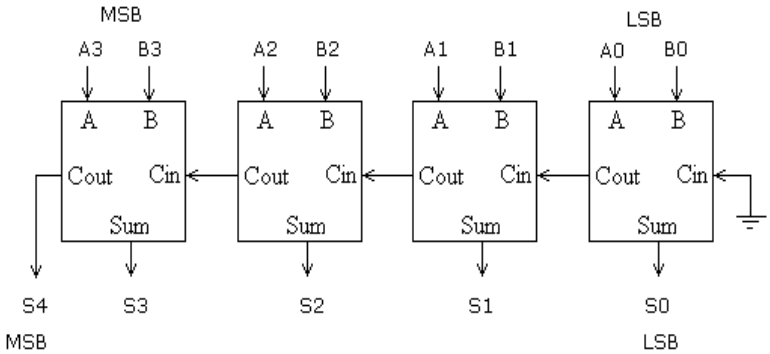
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No	SOLUTION	MARKS	TOTAL MARKS
B2 (a)		3 marks	
(b)	<p>A 4-bit parallel adder is a circuit that is able to add two sets of 4-bit numbers simultaneously to produce a sum result of up to 5 bits.</p> <p>If the 4-bit adder is to be constructed using the FA unit, 4 FAs are required</p> 	3 marks  2 marks  4 marks	
(c)	Three (3) 74283 ICs are required to build a 12-bit parallel adder	3 marks	15 marks

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No	SOLUTION	MARKS	TOTAL MARKS
B3 (a)	(i) Period = $95 + 35 = 130\text{mS}$	1 mark	
	(ii) Duty cycle = $35/130 * 100\% = 26.92\%$	2 marks	
	(iii) Frequency = $1/130\text{mS} = 7.6923\text{Hz}$	2 marks	
(b)	(i) Decade, Mod-10 or Divide by 10 counters.		
	(ii) Asynchronous or ripple counters		
	(iii) Parallel-in, serial-out shift register		
	(iv) Synchronous or Parallel counters		
	(v) Mod $2^N$ counter	10 marks	
	2 marks for each correct answer		
			15 marks

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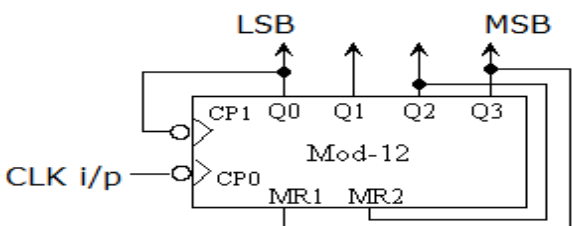
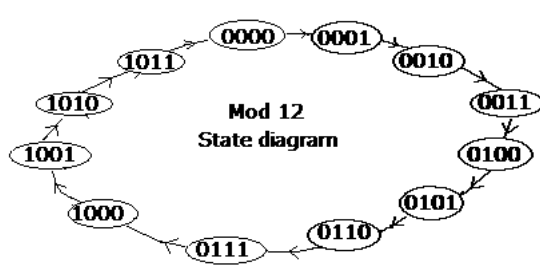
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No	SOLUTION	MARKS	TOTAL MARKS
C1			
(a)	Mod 12 counter (Divide by 12) has the highest Mod number	3 marks	
(b)	<p>Given freq at R = 1 kHz,    Freq at Q = <math>1000 * 12 = 12 \text{ kHz}</math></p> <p>Freq at P = <math>12 * 6 = 72 \text{ kHz}</math></p> <p>Freq at S = <math>1 \text{ kHz} / 2 = 500 \text{ Hz}</math></p> <p>Overall Modulus = <math>6 * 12 * 2 = 144</math></p>	<p>3 marks</p> <p>3 marks</p> <p>3 marks</p> <p>3 marks</p>	
(c)	 <p><b>Marks distribution</b></p> <p>Use of 4 Flip-flops - 1 mark</p> <p>Correct feedback from O/s to MR1 and MR2 - 3 marks</p> <p>Labelling of MSB and LSB - 1 mark</p> <p>Correct Clk i/p - 1 mark</p>	7 marks	
(d)	 <p align="center"><b>Mod 12 State diagram</b></p>	3 marks	
(e)	At the end of 122 Clk cycles , the output values will be 0010 + 0010 ( $2_{10}$ ) = 0100	3 marks	<b>25 marks</b>

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