SINGAPORE POLYTECHNIC ET1004

0000 0000 = 0
0000 0001 = +1
0000 0010 = +2
Etc. etc.
0111 1111 = +127
1000 0000 = -128
1111 1110 = -2
1111 1111 = -1

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

1. What is the maximum positive decimal value that can be represented by an 8-bit (including the sign bit) 2's complement signed numbering system?

(a) $+15_{10}$ (b) $+127_{10}$ (c) $+128_{10}$ (d) $+255_{10}$

Answer: (b)

Max positive 8-bit value = $2^7 - 1$

2. In the 8-bit (including the sign bit) 2's complement signed numbering system, what does the number 10000000_2 equates to when converted to decimal?

(a) an arithmetic overflow (b) -1_{10}
(c) -128_{10} (d) Zero

Answer: (c)

Max negative 8-bit value = -2^7

3. How many JK flip-flops are required to construct a Mod-60_{10} counter that counts in the BCD sequence?

Represent each decimal digit with 4-bit

(a) 6_{10} JK flip-flops (b) 7_{10} JK flip-flops
(c) 10_{10} JK flip-flops (d) 60_{10} JK flip-flops.

Answer: (b)

The x1 BCD (0..9) requires 4-bit (4 flip-flops), the x10 BCD (0..5) requires 3-bit.

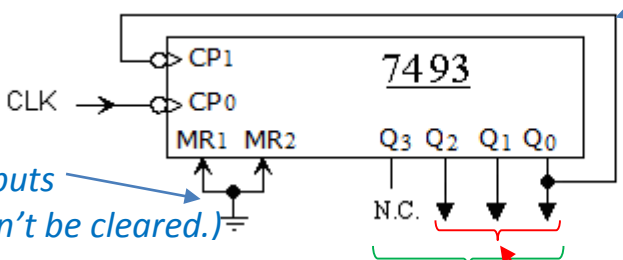
4. To calculate the average power consumed by a digital IC, the expression to use is:

(a) $[(I_{CCH} + I_{OH})/2 + (I_{CCL} + I_{OL})/2] * V_{CC}$
(b) $[(I_{CCH} + I_{IH})/2 + (I_{CCL} + I_{IL})/2] * V_{CC}$
(c) $[(I_{OL} + I_{IL})/2 + (I_{OH} + I_{IH})/2] * V_{CC}$
(d) $(I_{CCH} + I_{CCL})/2 * V_{CC}$

Answer: (d)

Average Power = Average I_{cc} x V_{cc}

5. What is the mod-number of the counter circuit shown in figure A5?



Joining Q_0 to CP_1
(Required when using 4 flip-flops.)

NB: N.C. is abbreviation for No Connection

'0' to the reset inputs
(The flip-flops won't be cleared.)

Figure A5

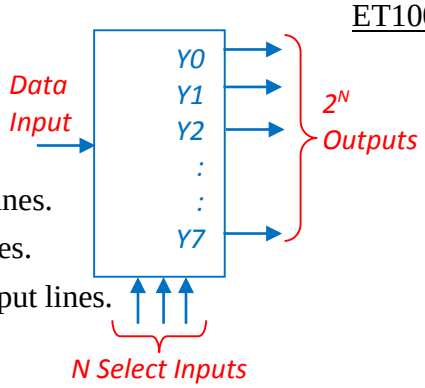
(a) Mod-8_{10} (b) Mod-10_{10} (c) Mod-12_{10} (d) Mod-16_{10}

Answer: (a)

Mod-2^4

Mod-2^3 (since Q_3 is not used)

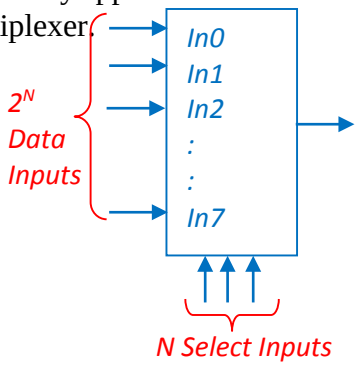
6. A Demultiplexer accepts data from:



(a) one input line and transfers it to one of the select lines.
(b) one input line and transfers it to multiple select lines.
(c) one input line and transfers it to one of several output lines.
(d) one input line and transfers it to one output line.

Answer: (c)

7. A Multiplexer is a very flexible logic device that can be used in many applications. Which one of the following examples is **Not** an application of the Multiplexer.



(a) implementation of combinational logic functions.
(b) data selection and routing of binary data.
(c) storage of binary data.
(d) parallel-to-serial conversion of binary data.

Answer: (c)

8. The 7442 is described as a BCD-to-Decimal Decoder as it is used to decode BCD numbers. If a 7442 has inputs as shown in figure A8, what will be its outputs?

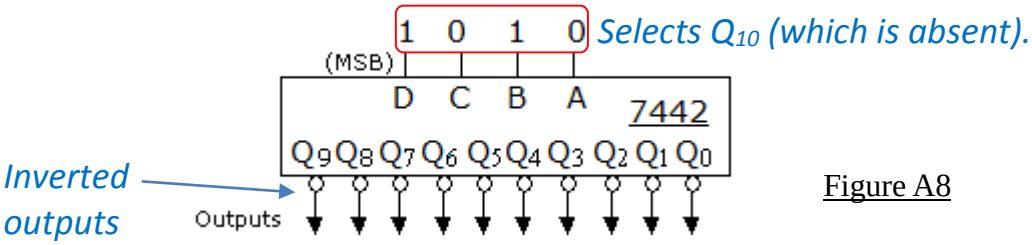


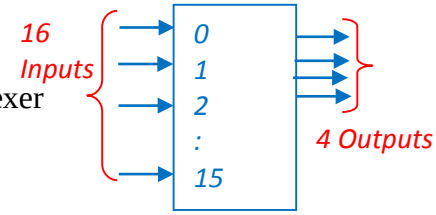
Figure A8

(a) Only Q_9 goes Low.
(b) Only Q_2 goes Low.
(c) All outputs go Low.
(d) All outputs go High.

Answer: (d)

The selected output will be '0', other outputs will be '1'.

9. Which one of the following devices is used to convert key-pad actuations to a binary code?



(a) Encoder
(b) Decoder
(c) Multiplexer
(d) Demultiplexer

Answer: (a)

10. A **Mod-16_{10} down-counter** starts with the output state of **0001_2**. What will be the value at its outputs after the application of **83_{10}** clock cycles?

(a) 0100_2
(b) 1111_2
(c) 0101_2
(d) 1110_2

(It will return to state 1 every 16 clock pulses.)

Answer: (d)

5 x 16 = 80:

80	81	82	83
1 →	0 →	15 →	14

Section B Short Questions (60 marks)

B1. Perform the following operations using the 2's complement signed numbering system.
You are to assume that each number is to be represented by 8 bits, including the sign bit.

(a) Add $+41_{10}$ to $+56_{10}$ (4 marks)

+41 = 0010 1001
+56 = 0011 1000
***0110 0001** = +97*

(b) Subtract $+33_{10}$ from $+76_{10}$ (6 marks)

NB: All workings in question B1 must be shown or marks will not be awarded.

(+76) – (+33)
= (+76) + -(+33)

Negate:
+33: 0010 0001
Invert: 1101 1110
*Add 1: **1101 1111** = -33*

+76: 0100 1100
-33: 1101 1111
*1 **0010 1011***
(Take 8-bit only as result.)

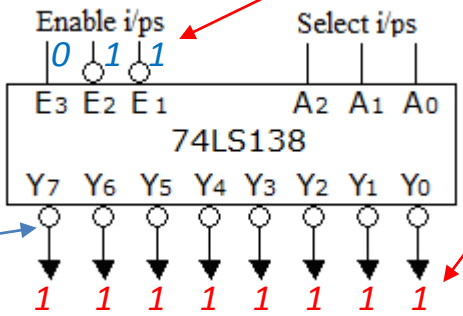
*Another name: **3-to-8 decoder***

B2(a) The 74138 is a **1-of-8** decoder device and has a symbol as shown in figure B2.1. What is another name for this decoder? What will be the logic values at the outputs Y_7 to Y_0 if the inputs to the decoder are: A_2 A_1 A_0 = H L H and, E_1 = H, E_2 = H and E_3 = L?

(5 marks)

The select inputs will be effective only if all enable inputs are enabled.

Disabled. (All outputs will be inactive.)



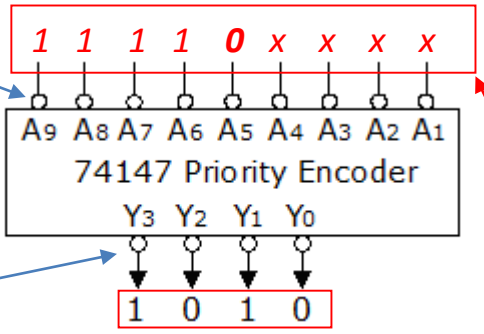
Inverted outputs

Figure B2.1

(b) The outputs of the 74147 **decimal-to-BCD** priority encoder circuit shown in figure B2.2 is 1 0 1 0, as shown, what must be the logic levels at inputs A_9 to A_1 in order for this code to be produced?

(5 marks)

Active-low inputs (i.e. '0' is active).



Inverted outputs

The inversion of 0101 = 5

Hence,
A9 to A4 should be: 1 (inactive)
A5 should be: 0 (active)
A4 to A1: don't care.

Figure B2.2

B3 The 74LS283 as shown in figure B3, is a 4-bit parallel adder IC, i.e. a device that adds two sets of 4-bit numbers simultaneously.

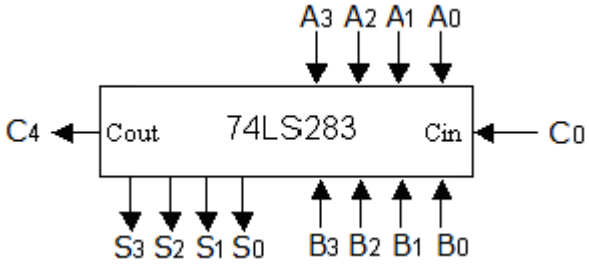


Figure B3

(a) If the 4-bit parallel adder IC is to be constructed using the Full Adder unit, how many Full Adder units are required? *Each 74LS283 IC is a 4-bit parallel adder and it **requires 4 Full Adders**.* (2 marks)

(b) If $A_3\ A_2\ A_1\ A_0 = 0\ 1\ 1\ 1$ and $B_3\ B_2\ B_1\ B_0 = 1\ 1\ 1\ 0$, respectively, what will be the binary value at the outputs C_4, S_3, S_2, S_1, S_0 if $C_0 = 1$?

(2 marks)

*0111 + 1110 + 1 = **1 0110***

(c) If a **4-bit** (including the sign bit) **2's complement** signed numbering system is used, what are the equivalent decimal numbers being added and the equivalent decimal sum result in part(b)? How should the carry-out bit C_4 be treated in this case?

(6 marks)

Answer 1

*Performing **A + B + C_0** where:*

*A = 0111 = **+7**, B = 1110 = **-2**, C_0 = 1 = **+1**,*

*S = 0110 = **+6**, C_4 should be ignored.*

Answer 2

*Performing **A – B' (**i.e. **A + -[B']**) where:*

*A = 0111 = **+7**.*

*B = 1110 (i.e. B' = 0001 **= +1**); B is the 1's complement (i.e. inversion) of B'.*

C_0 performs plus 1 to produce the 2's complement of B' (i.e. –B').

*S = 0110 = **+6**, C_4 should be ignored.*

Answer 3

*Performing **B – A' (**i.e. **B + -[A']**) where:*

*B = 1110 = **-2**.*

*A = 0111 (i.e. A' = 1000 = **-8**); A is the 1's complement (i.e. inversion) of A'.*

C_0 performs plus 1 to produce the 2's complement of A' (i.e. –A').

*S = 0110 = **+6**, C_4 should be ignored.*

B4 Each of the following five statements comprising this question describes a particular **type** of **counter or shift register** circuit. You are required to state in your answer booklet, the type of counter or register circuit being described by each statement. Ensure that your answers are labelled exactly according to each of the statements i.e. [**(a), (b)....(e)**] or marks will not be awarded.

(10 marks)

(a) This shift register circuit has many data inputs but only one data output.

Parallel-In Serial-Out (PISO) shift register.

(b) This counter counts in the following binary sequence 000, 001, 010, 011, 100, 101, 110, repetitively.

Mod-7 counter.

(c) The duty cycle of the output signals of this asynchronous counter is always 50%.

Mod-2^N counter. (Example: Mod-2, 4, 8, 16 etc.)

(d) This shift register inputs data one bit at a time but outputs data multiple bits at a time.

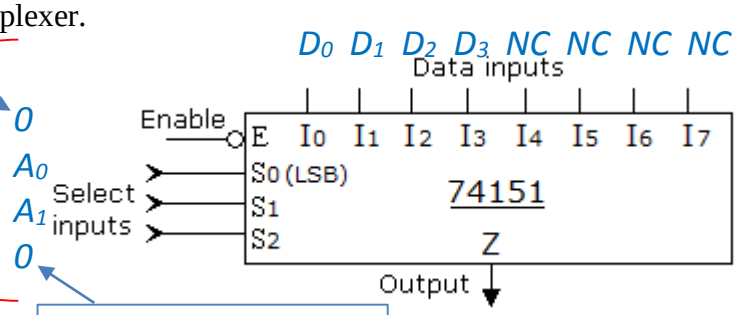
Serial-In Parallel-Out (SIPO) shift register.

(e) This counter divides its Clock signal frequency by its mod number.

Frequency Divider. (Any counter is also a frequency divider).

B5 The 74151 is described as an 8- to-1 multiplexer. Figure B5.1 shows the symbol of this multiplexer.

E = 0 to enable the output.



S2 = 0 → I4 to I7 will not be selected.

Figure B5.1

(a) Using one 74151 8-input multiplexer IC, show how you can connect the 74151 to function as a 4-to-1 multiplexer. In your completed diagram, label the data inputs as D0 D1 D2 D3 and the select inputs as A1 A0, where the subscript of 0 denotes the LSB. Unused inputs should be indicated as N.C. (i.e. No Connection).

(4 marks)

(b) Given the 74151 multiplexer connected as shown in figure B5.2, determine the logic function (i.e. Boolean expression) implemented at both outputs: Z and $\overline{Z}$. From the resultant expressions obtained, what are the generic names of these two output functions?

Hint: Create a truth table with C, B and A as input variables Z and $\overline{Z}$ as outputs.

(6 marks)

Z = 0 (and Z' = 1) only when CBA=111 (when I_7 is selected).
*Hence, Z' = C.B.A (i.e. **Z' is AND** function) while **Z is NAND** function.*

S_2 S_1 S_0	
C B A	**Z**
0 0 0	1
0 0 1	1
0 1 0	1
0 1 1	1
1 0 0	1
1 0 1	1
1 1 0	1
1 1 1	0

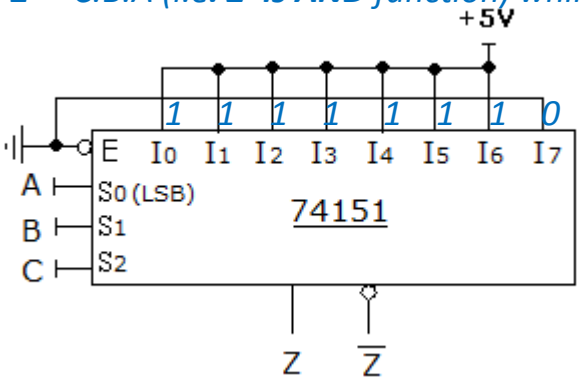
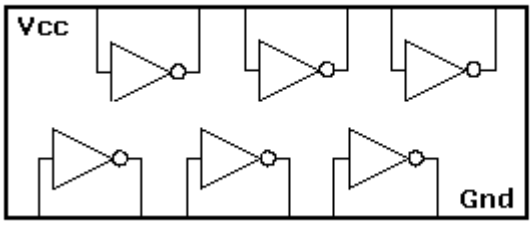


Figure B5.2

$$Z = C'.B'.A' + C'.B'.A + C'.B.A' + C'.B.A + C.B'.A' + C.B'.A + C.B.A'$$
$$(I_0) \quad (I_1) \quad (I_2) \quad (I_3) \quad (I_4) \quad (I_5) \quad (I_6)$$

B6 Table B6 lists the typical values of the AC and DC parameters (characteristics) for three different logic families **of the 7404 Inverter IC**.



Parameter	Unit	Device A	Device B	Device C
Vcc	V	5	5	5
$V_{IH\ (min)}$	V	2	2	2
$V_{IL\ (max)}$	V	0.8	0.8	0.8
$V_{OH\ (min)}$	V	2.4	2.7	2.5
$V_{OL\ (max)}$	V	0.4	0.5	0.5
Icc_H	mA	12	4.4	10
Icc_L	mA	24	7.6	20
tp_{LH}	nS	11	9	2
tp_{HL}	nS	13	11	3

Table B6

(a) Which device has the highest output voltage for logic High and what is the value of this voltage?

Device B**, its V_{OH} (min) = **2.7V

(2 marks)

(b) Which device can operate at the highest signal frequency? Justify your answer by quoting the correct parameter and its value.

(2 marks)

***Device C.** Less delay (t_P) → higher operating frequency.*

(c) Calculate the average power consumption per gate for device **A**, only.

Whole IC: $P = V_{CC}$ x average I_{CC} = 5V x (12+24)/2 mA = 90 mW. (4 marks)

*Per gate: 90 / 6 = **15 mW**.*

(d) Without doing any calculations, which device has the lowest power consumption per gate? Justify your answer by quoting the correct parameter.

(2 marks)

***Device B**.*

All 3 devices has the same V_{CC} (5V) but B has the lowest I_{CC}.

Section C Long Question (20 marks)

C1. The block diagram in figure C1.1 shows a Mod-12 asynchronous counter connected to a decoder that detects the presence of a particular set of counting sequence.

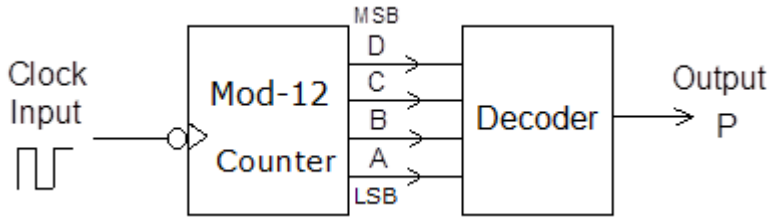
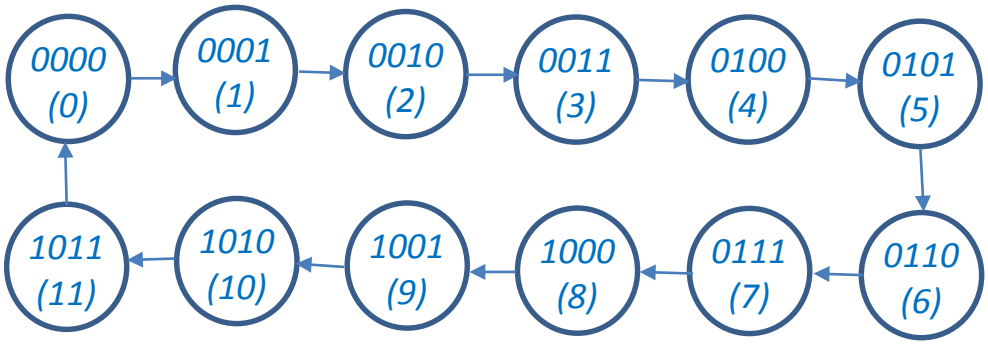
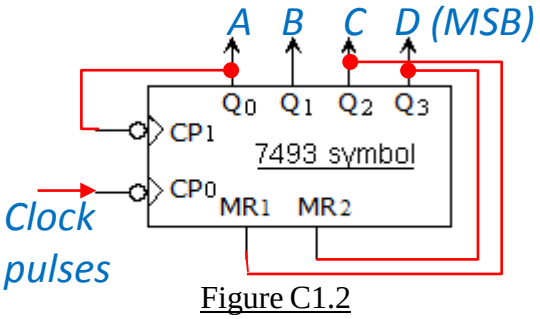


Figure C1.1 *The block diagram of an asynchronous counter with decoder.*

(a) Draw the state transition diagram of the Mod-12 counter. (4 marks)



(b) Using one 7493 IC, symbol and internal circuit as shown in figure C1.2, show how you would configure the mod-12 counter. Draw your circuit in your answer booklet using only the symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will be deducted. (6 marks)



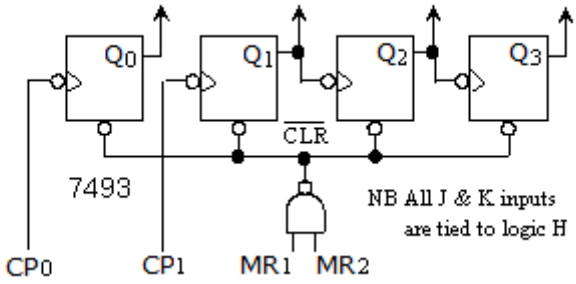


Figure C1.2

Mod-12 → clear all flip-flops when the count becomes 1100 (12);
i.e. when DCBA = 1100 or when D=1 and C=1.
(Hence connect D and C to MR1 and MR2.)

(c) The decoder has an output P that responds as follows:

- Output P = H, whenever the counter outputs D C B A is equal to or greater than 7_{10}.

Determine the truth-table for this decoder, using a table format as shown in Table C1. You are reminded that D is the MSB and A is the LSB and all don't care conditions should be indicated as 'X's. (4 marks)

D	C	B	A	P
0	0	0	0	0
:	:	:	:	?
1	1	1	1	X

Table C1

(d) Using one 74151 multiplexer (symbol as shown in figure B5.1 on page 6) and an inverter, if necessary, design the decoder using the truth-table you completed in part (c). Ensure that you labelled your completed circuit clearly or marks will be deducted.
(*Hint: Assigned variables D, C and B to select inputs S_2, S_1 and S_0, respectively.*)
(6 marks)

	DCBA	P
(0)	0000	0
(1)	0001	0
(2)	0010	0
(3)	0011	0
(4)	0100	0
(5)	0101	0
(6)	0110	0
(7)	0111	1
(8)	1000	1
(9)	1001	1
(10)	1010	1
(11)	1011	1
(12)	1100	x
(13)	1101	x
(14)	1110	x
(15)	1111	x

S_2 S_1 S_0

	DCBA	P	
0	0000	0	0
	0001	0	
1	0010	0	0
	0011	0	
2	0100	0	0
	0101	0	
3	0110	0	A
	0111	1	
4	1000	1	1
	1001	1	
5	1010	1	1
	1011	1	
6	1100	x	X
	1101	x	
7	1110	x	X
	1111	x	

Either 0 or 1. (Don't care.)

**** **End-of-paper** ****