SINGAPORE POLYTECHNIC ET1004

2018/2019 SEMESTER 2 EXAMINATION

Diploma in Electrical & Electronic Engineering DEEE 1st Year FT
Diploma in Computer Engineering DCPE 1st Year FT
Diploma in Aerospace Electronics DASE 1st Year FT
Diploma in Energy Systems and Management DESM 1st Year FT
Common Engineering Programme DCEP 1st Year FT

SAS code:
EXAM

DIGITAL ELECTRONICS II

Time Allowed : 2 hours

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of **THREE** sections:

   Section A - 10 Multiple Choice Questions, 2 marks each.

   Section B - 6 Short Questions, 10 marks each.

   Section C - 1 Long Question of 20 marks.

3. Answer **ALL** questions in the accompanying Answer Booklet. Start each question in Sections B and C on a new page.

4. This Examination Paper consists of 8 pages

5. Your admission number and module class must be entered in the box provided on the cover page of your Answer Booklet.

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

A1. The decimal number -49 (minus 49), when expressed in the 8-bit two's complement signed numbering system, is equal to:

(a) 00110001_2 (b) 11001110_2 (c) 10110001_2 (d) 11001111_2

A2. To configure an 8-bit parallel adder using the 7483 adder IC (Figure A2), a 4-bit adder IC, two of these ICs are required and,

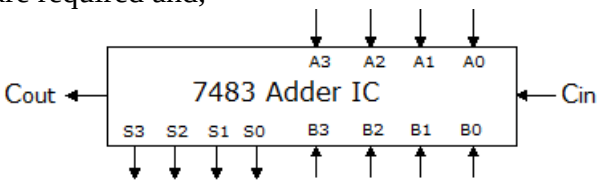

Figure A2

(a) the MSB Sum output S3 of the first adder IC (the LSB unit) must be connected to the LSB data input of the second adder IC (the MSB unit).

(b) the Cout output of the first adder IC must be connected to the Cout output of the second adder IC.

(c) the Cin input of the second adder IC must be connected to the Cout output of the 1st adder IC.

(d) the Cin input of the second adder IC must be connected to the Cin input of the first adder IC

A3. What is the maximum Modulus (Mod-number) that can be attained by a 6_{10} flip-flop ripple counter?

(a) 6_{10} (b) 16_{10} (c) 64_{10} (d) 128_{10}

A4. The signal frequency at the MSB output of a counter is 3 kHz and the clock signal frequency at its input is 120 kHz. What is the modulus (mod number) of this counter?

(a) Mod-16_{10} (b) Mod-20_{10} (c) Mod-40_{10} (d) Mod-60_{10}

A5. How many clock pulses (CLK) are required to load (or input) binary data to a 16-bit parallel-in, serial-out shift register?

(a) 1_{10} CLK (b) 8_{10} CLK (c) 16_{10} CLK (d) 17_{10} CLK

A6. What is the timing parameter that specifies the minimum time required to maintain the logic levels stable at the control inputs of a D flip-flop **prior to** the application of the active clock transition?

(a) Set-up time t_{su}
(b) Propagation delay t_{pd}
(c) Hold time t_{hd}
(d) CLK period T

A7. For the multiplexer circuit connected as shown in Figure A7, select the correct Boolean expression generated at output Y.

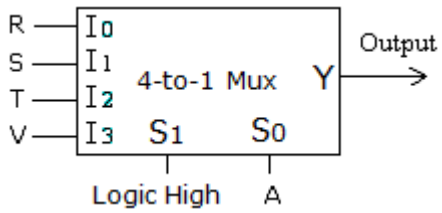

Figure A7

(a) $Y = \overline{A}R + AS$
(b) $Y = \overline{A}TV + ATV$
(c) $Y = \overline{A}T + AV$
(d) $Y = AS + \overline{A}T$

A8. A 74138 decoder IC is connected as shown in Figure A8. Select the correct statement that describes the outcome at the outputs.

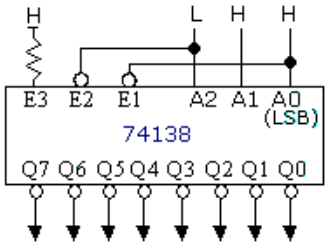

Figure A8

(a) Only output Q3 goes Low
(b) Only output Q6 goes Low
(c) All the outputs go Low
(d) All the outputs remain High.

A9. 'Fan-Out' is defined as the number of logic loads that can be connected to _____ without exceeding the IC manufacturer's specifications.

(a) a single input
(b) a single output
(c) all the inputs and outputs
(d) the Vcc power supply

A10. A shift register which loads data bits one bit at a time, and transfers out multiple bits, simultaneously, is a_____.

(a) parallel-in, parallel-out register
(b) parallel-in, serial-out register
(c) serial-in, parallel-out register
(d) serial-in, serial-out register

Section B Short Questions (60 marks)

B1(a) Express the following pairs of numbers in BCD format and hence, perform the addition of the numbers using BCD arithmetic.

Add $+127_{10}$ to $+93_{10}$

(4 marks)

(b) Use the 8 bits (including the sign bit) 2's complement signed numbering system to perform the following addition

Add -63_{10} to $+92_{10}$

(6 marks)

NB: **All workings** for question B1 must be **shown or marks** will **not** be awarded.

B2(a) Briefly, state and describe two uses of the enable inputs.

(4 marks)

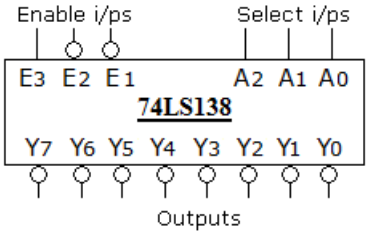

Figure B2

(b) If output Y7 is to be selected, what are the logic levels required at the Enable and Select inputs?

(2 marks)

(c) Using one 74LS138 IC, show how the the IC can be connected as a 2-to-4 decoder. Your circuit diagram, to be drawn in your answer booklet, must be clearly labelled, showing all required inputs and outputs. The select inputs required should be labelled as S_1, S_0 and the four outputs should be labelled respectively as Q_3 to Q_0, where Q_3 is the MSB, and Q_0 is the LSB.

(4 marks)

B3(a) Briefly explain what is the main difference between an BCD ordinary encoder and a BCD priority encoder?

(3 marks)

(b) Determine the outputs (in the order Q_3 Q_2 Q_1 Q_0) of the BCD encoder circuit shown in Figure B3 when:

i) All inputs are logic HIGH

ii) All inputs HIGH except input A4.

iii) All inputs HIGH except input A9.

iv) All inputs HIGH except inputs A4 and A9.

(4 marks)

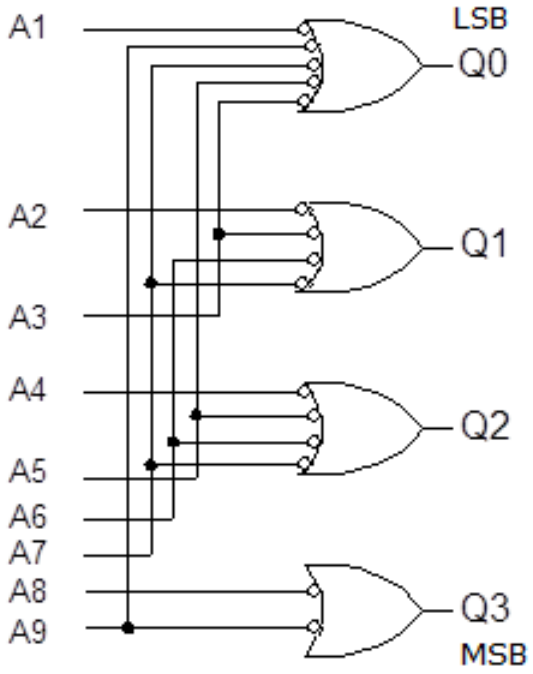

Figure B3

(c) Is the circuit shown in Figure B3 a priority encoder? If it is not, briefly explain why? Hint: Illustrate your answer with an example of the code generated when 2 or more inputs are activated. (3 marks)

B4 The sum-of-products expression for output Z of a logic circuit is given as:

$$Z = \overline{C}\,\overline{B}\,\overline{A} + \overline{C}\,B\,\overline{A} + C\,\overline{B}\,\overline{A} + C\,B\,\overline{A} + C\,B\,A$$

(a) Determine the truth-table for output Z of the logic circuit.

(2 marks)

(b) Using the k-map, simplify the Boolean expression of output Z.

(3 marks)

(c) Given the logic symbol of 74151 as shown in Figure B4, show how you would connect the multiplexer to generate the expression for output Z. Your circuit must be clearly labelled or marks will be deducted. (*Hint: assume variable A to be the LSB and assign it to S0.*)

(5 marks)

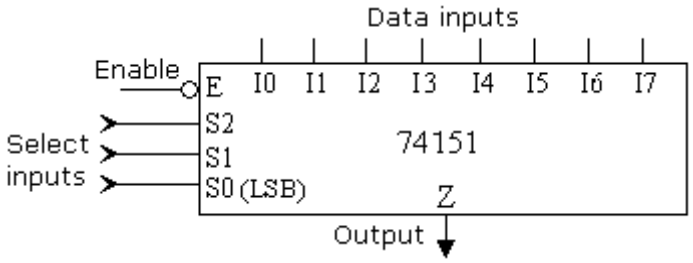

Figure B4

B5 The symbol and internal circuit of the 7493, a 4-bit binary counter IC, is shown in figure B5.

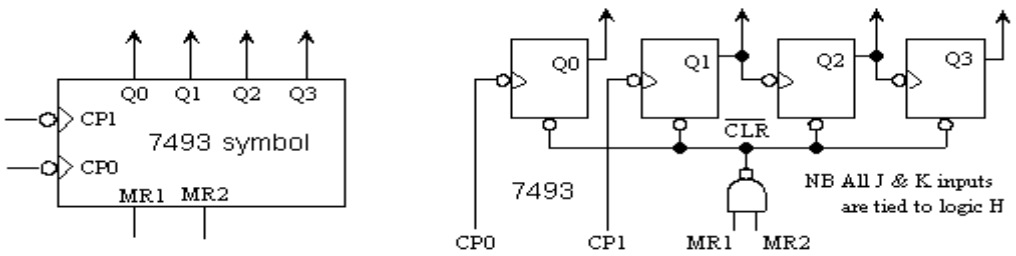

Figure B5

(a) Using one 7493 counter IC, and any other gates as necessary, show how you would connect a mod-14_{10} up-counter. Indicate and label clearly all the connections made to the IC, in particular the CLK input, the LSB and MSB outputs. What is the maximum count in binary for this mod-14_{10} counter?

(6 marks)

(b) If the signal frequency at the MSB output of the mod-14_{10} counter is 14 kHz, what is the signal frequency of the clock signal applied at its CLK input?

(2 marks)

(c) Determine the duty cycle of the signal at the MSB output given that the CLK signal is a perfect square wave.

(2 marks)

B6 The **7402** IC is described as a **Quad 2-input NOR gate IC.**

Table B6 list some of the electrical parameters of the **7402 IC**.

Symbol	Parameters	Max	Min
V_{CC}	Supply voltage (V)	5	
V_{IH}	High level input voltage (V)		2
V_{IL}	Low level input voltage (V)	0.8	
V_{OH}	High level output voltage (V)		2.4
V_{OL}	Low level output voltage (V)	0.4	
$I_{CC(H)}$	Supply current (mA), outputs High	10	
$I_{CC(L)}$	Supply current (mA), outputs Low	22	
tp_{LH}	Propagation delay (nS)	20	
tp_{HL}	Propagation delay (nS)	15	

Table B6

(a) From the description given, how many NOR gates are there in the 7402 IC?

(1 mark)

(b) What is the guaranteed maximum value of the output voltage when the output is at logic Low?

(2 marks)

(c) Calculate the power dissipation for the whole IC and hence, for each gate.

(4 marks)

(d) Using one NOR gate, show how it can be connected as an inverter. Hence, determine the time taken for the **output** to respond to an input signal changing from Low to High?

(3 marks)

Section C Long Question (20 marks)

C1. A **BCD** number detector circuit is required to be designed (see figure C1.1). This combinational circuit has an output **Z**, and responds to BCD numbers as follows:

- **Z = 1** whenever the BCD inputs are 1_{10}, 3_{10}, 8_{10} and, 9_{10}.

You are to assume that **only BCD** numbers are applied to the inputs of this circuit, i.e. there are don't care conditions.

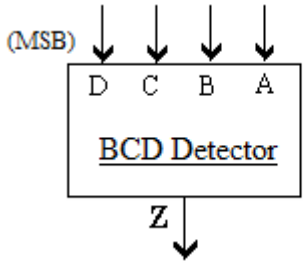

Figure C1.1

(a) Determine the truth-table for this circuit using a table format as shown in Table C1. You are reminded that input D is the MSB and input A is the LSB and all **'don't care'** conditions should be denoted as 'X's.

(8 marks)

Inputs				Output
D	**C**	**B**	**A**	**Z**
0	0	0	0	0
NB: The truth table, listing all input combinations and output values, is to be completed in your Answer Booklet.				
1	1	1	1	X

Table C1

(b) Using the 7442 BCD decoder (symbol is as shown in Figure C1.2) and, any other logic gates as necessary, implement the BCD number detector circuit as specified in the question

(6 marks)

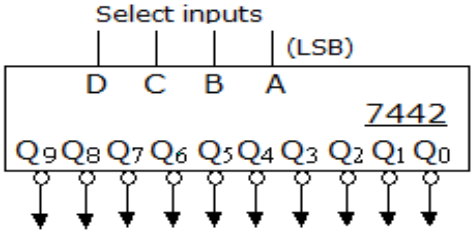

Figure C1.2

(c) Using one 74151 multiplexer IC, the symbol of which is shown in Figure B4, show how you would implement the logic circuit for output Z using the truth-table derived in part (a). The 74151 symbol given in Figure B4 on page 6 is to be used, and input variables D, C, and B should preferably be assigned to multiplexer select inputs S_2, S_1, and S_0, respectively. Your completed circuit must be clearly labelled or marks will be deducted.

(6 marks)

---------- **End of Paper** ----------