A1. How many Full-Adder units are required to construct a 32-bit Parallel Adder circuit?

(a) 16_{10} (b) 32_{10} (c) 64_{10} (d) 128_{10}

Answer: (b)

Full Adder is a 1-bit adder – combine N of them to form N-bit adder.

A2. In the 8-bits two's complement system, what does decimal -127_{10} converts to?

(a) 11111111_2 (b) 10000000_2 (c) 10000001_2 (d) 01111111_2

Answer: (c)

+127 in 8-bit: 01111111. Invert: 10000000, plus 1: 10000001 = -127

A3. What is the maximum Modulus (Mod-number) that can be attained by a 6_{10} flip-flop ripple counter?

(a) 6_{10} (b) 16_{10} (c) 32_{10} (d) 64_{10}

Answer: (d)

6 flip-flops: $2^6 \rightarrow 64$.

A4. A shift register which has a single data input and many data outputs is a _____.

(a) parallel-in, serial-out register (b) parallel-in, parallel-out register

(c) serial-in, parallel-out register (d) serial-in, serial-out register

Answer: (c)

Serial: 1 bit at a time. Parallel: multiple bits simultaneously.

A5. The signal frequency at the Clock input of a counter is 10 kHz and the signal frequency at its MSB output is 125 Hz. What is the modulus (mod number) of this counter?

(a) Mod-16_{10} (b) Mod-60_{10} (c) Mod-80_{10} (d) Mod-125_{10}

Answer: (c)

Mod = f_{CLK} / f_{MSB} = 10 kHz / 125 Hz = 80

A6. What is the timing parameter that specifies the minimum time required to maintain the logic levels stable at the control inputs of a JK flip-flop **prior** to the application of the active clock transition?

(a) Set-up time t_{su} (b) Propagation delay t_{pd}

(c) Hold time t_{hd} (d) CLK period T

Answer: (a)

A7. A 74LS157 IC, which is a quad 2-to-1 multiplexer, is connected as shown in figure A7. What is the output data at outputs Zd Zc Zb Za (in this order)?

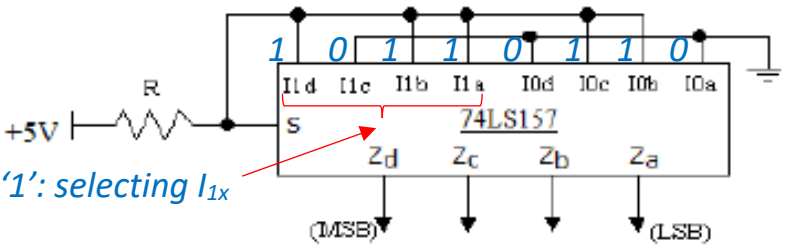


Figure A7

(a) 1111_2 (b) 0110_2 (c) 1101_2 (d) 1011_2

Answer: (d)

A8. A 74LS138 1-of-8 decoder is connected as shown in figure A8, what will be the logic levels at the outputs?

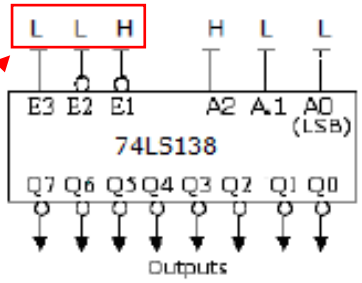


Figure A8

(a) Only Output Q1 goes Low

(b) Only Output Q4 goes Low

(c) All outputs are Low

(d) All outputs are High

Answer: (d)

A9. A parallel adder which can add signed binary numbers using the 2's complement numbering system in the range from $+2047_{10}$ to -2048_{10} is to be constructed using the 74LS83 IC, a 4-bit parallel adder IC. How many of these 74LS83 ICs are required to build this parallel adder circuit?

(a) 3_{10} (b) 4_{10} (c) 6_{10} (d) 8_{10}

Answer: (a)

+2047 to -2048 has 4096 numbers → 2^{12} → 12-bit → 3 ICs

A10. To calculate the power consumed by a TTL digital IC, the supply voltage Vcc is multiplied by:

(a) $(I_{OL} - I_{OH})/2$

(b) $(I_{OL} + I_{OH})/2$

(c) $(I_{CCL} - I_{CCH})/2$

(d) $(I_{CCL} + I_{CCH})/2$

Answer: (d)

The average of I_{CCH} (I_{CC} when all outputs are HIGH) and I_{CCL} (I_{CC} when all outputs are LOW).

B1(a) Express the following pairs of numbers in the BCD format and hence, perform the addition of the numbers using BCD arithmetic.

Add $+168_{10}$ to $+87_{10}$ (4 marks)

+168	=	0	0	0	1^{1}	0	1	1	0	1	0	0	0
+87	=					1	0	0	0	0	1	1	1
	=	0	0	0	1^{1}	1	1	1	0^{1}	1	1	1	1
						+	1	1	0	+	1	1	0
+255	=	0	0	1	0	0	1	0	1	0	1	0	1

The sum of this 4-bit is above 9

Add 6 to compensate

(b) Use the 8 bits (including the sign bit) 2's complement signed numbering system to perform the following operation.

Add -53_{10} to $+82_{10}$

(6 marks)

		sign	64	32	16	8	4	2	1
+53	=	0	0	1	1	0	1	0	1
Invert all bits, then plus 1:									
-53	=	1	1	0	0	1	0	1	1
+82	=	0	1	0	1	0	0	1	0
+29	=	~~1~~	0	0	0	1	1	1	0	1

Discard the 9th bit

8-bit result

B2 The 74LS283 (see figure B2.1) is a 4-bit Parallel Adder IC.

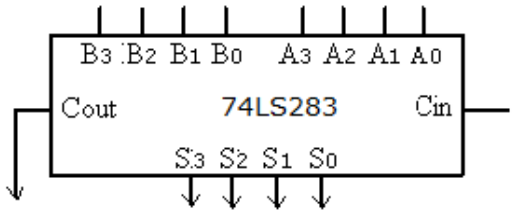


Figure B2.1

(a) Briefly describe what is a 4-bit Parallel Adder?

(3 marks)

It adds two 4-bit numbers to produce a 4-bit sum.

It also has a carry-in and carry-out for cascading with other 4-bit adders to form bigger (e.g. 8-bit or 12-bit) adders.

(b) If the 4-bit parallel Adder of figure B2.1 is to be constructed using the Full-Adder (symbol shown in figure B2.2) how many Full-Adders are required? *4 are required*

(2 marks)

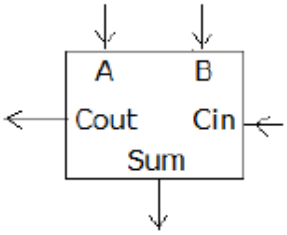
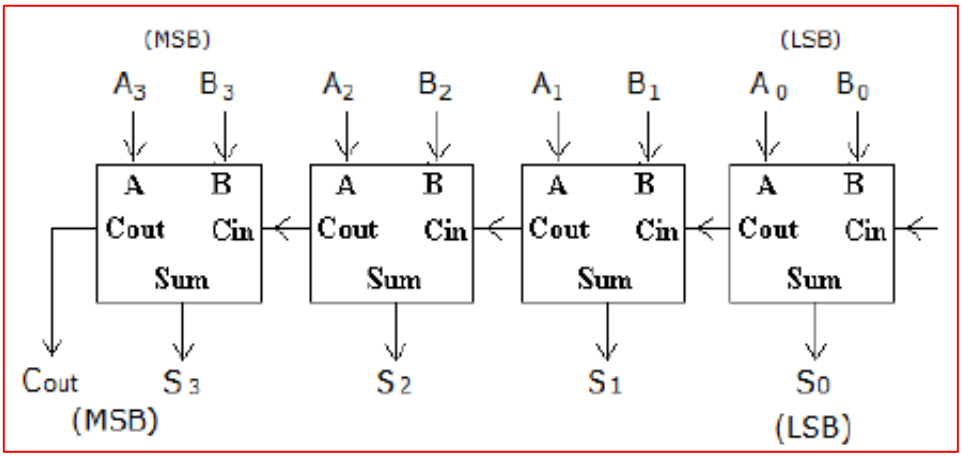


Figure B2.2

(c) Using the correct number of Full- Adders, show how they should be connected together to configure the 4-bit parallel Adder of figure B2.1. Ensure that you use the same labels for the inputs and outputs as shown in figure B2.1 and that the MSBs and LSBs at the inputs and the outputs are indicated, or marks will be deducted.

(5 marks)



B3 Each of the following 5 statements comprising this question describes a particular type of counter or shift register circuit. You are required to state in your answer booklet, the type of counter or shift register circuit being described by each statement. Ensure that your answers are labelled exactly according to each of the statements i.e. [(a), (b)....(e)] or marks will not be awarded.

(10 marks)

(a) This shift register circuit has many data inputs and the same number of data outputs.

Parallel-in, parallel-out (PIPO) register.

(b) The duty cycle of the signals at all outputs of this counter is always 50%.

Mod-2^N counter.

(c) This shift register can be used to delay a signal by a fix number of clock cycles that correspond to the number of flip-flops in the register.

Serial-in, serial-out (SISO) shift register.

(d) This counter repeatedly counts in the following sequence 000, 001, 010, 011, 100, 101, 000, 001, 010 and so on. What is the modulus of this counter?

Mod-6 counter

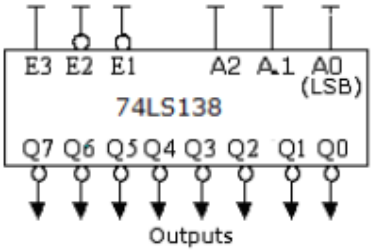
(e) The signal frequency at the MSB output of this counter is one tenth (1/10) of its Clock signal frequency.

Mod-10 counter.

(Also known as: divide-by-10 counter, decade counter or DCB counter.)

B4(a) The 74LS138 is described as a 3-to-8 decoder. What is another name for this decoder?

1-of-8 decoder. (2 marks)



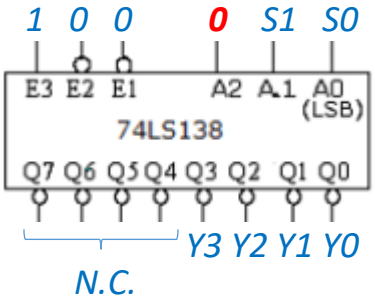
(Only 1 of the 8 outputs will be On.)

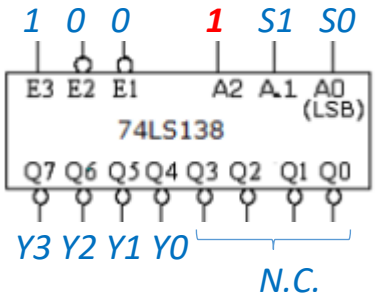
Figure B4.1

(b) Using one 74LS138, show how it can be connected as a 2-to-4 decoder. Label your circuit clearly using the generic label of Sn for the select inputs and Yn for the outputs, where n is numeric label starting from 0. All unused inputs should be appropriately terminated and all unused outputs marked as N.C. (abbreviation for No Connection).

(4 marks)

Alternatively:





(c) State the logic levels at the inputs A1 to A9 in order for the 74LS147 BCD Priority Encoder to generate a code of 1001 at its outputs Y3 Y2 Y1 Y0, respectively.

(4 marks)

Active-low inputs (i.e. '0' is ON)

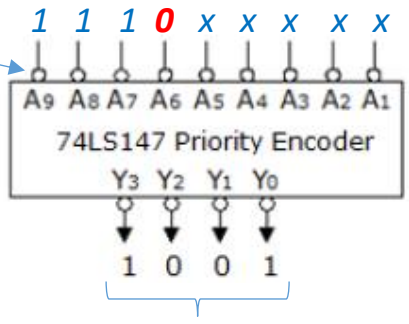


Figure B4.2

B5 The symbol and internal circuitry of the **74LS93** counter IC is given in figure B5.

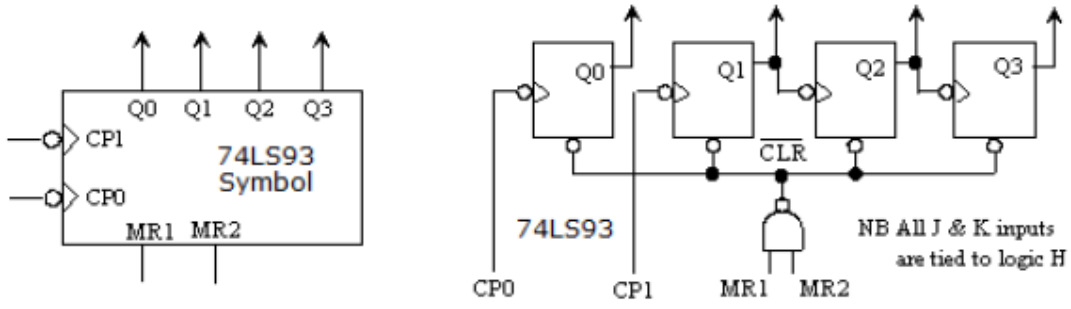
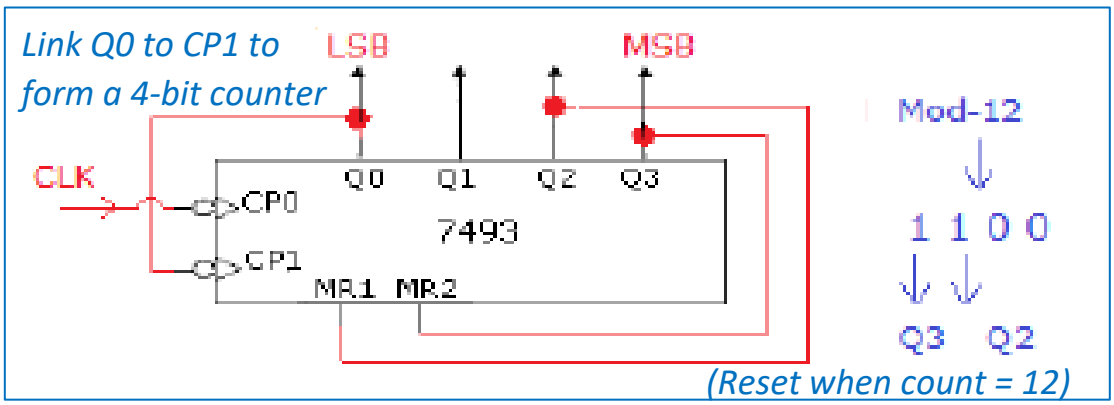


Figure B5

(a) Using one 74LS93 counter IC, show how you would connect the IC as a binary-sequence Mod-12 counter. In your answer, you should label clearly all the connections, in particular, the CLK input, the MSB and LSB outputs.

(4 marks)



(b) A Clock signal frequency of 3600 Hz with duty cycle of 50% is applied at the Clock input of the mod-12 counter. Determine the signal frequency and duty cycle of the signal at the MSB output of the mod-12 counter.

(2 marks)

Q3..Q0

0: 0000
1: 0001
2: 0010
3: 0011
4: 0100
5: 0101
6: 0110
7: 0111
8: 1000
9: 1001
10: 1010
11: 1011
12: 1100 → 0000

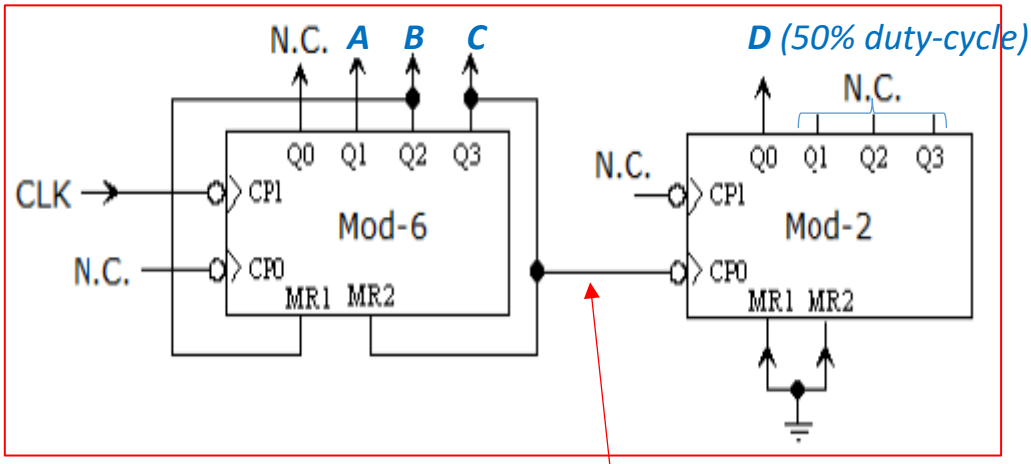
Frequency at MSB** = Clock frequency / Mod = 3600/12 = **300 Hz

Duty-cycle** = 4 /12 = **33.3%

(c) A Mod-12 counter can also be configured by cascading a Mod-6 counter with a Mod-2 counter. This produces a non-binary sequence Mod-12 counter but it has the advantage of giving a 50% duty cycle waveform at the MSB output if the MOD-6 and Mod-2 counters are connected in the right order.

Using two 74LS93 counter ICs (symbol shown in figure B5), configure a Mod-12 counter with 50% duty cycle at its MSB output. Label your circuit diagram clearly or marks will not be awarded.

(4 marks)



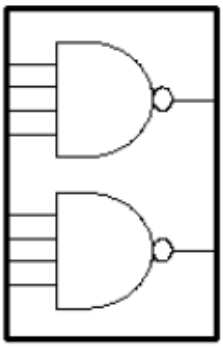
DCBA

0: 0000
1: 0001
2: 0010
3: 0011
4: 0100
5: 0101
8: 1000
9: 1001
10: 1010
11: 1011
12: 1100
13: 1101

Mod-6 counter:

As soon as CBA = 110 (6) they are reset to 000, which produces a NGT at C to toggle D at the Mod-2 counter.

B6 The characteristics of the 74LS20, a dual 4-input NAND gate IC, is as shown in figure B6.



74LS20

Logic Symbol

Symbol	Parameter	Max	Min
Vcc	Supply voltage (V)	5	
V_{IH}	High level input voltage (V)		2
V_{IL}	Low level input voltage (V)	0.8	
V_{OH}	High level output voltage (V)		2.7
V_{OL}	Low level output voltage (V)	0.4	
I_{CCH}	Power Supply Current (mA)	8	
I_{CCL}	Power Supply Current (mA)	20	
t_{pLH}	Propagation delay (nS)	12	
t_{pHL}	Propagation delay (nS)	10	

Figure B6 The logic symbol and characteristics of 74LS20

Calculate the following parameters:

(a) the average propagation delay t_{pd}

$t_{pd} = (t_{pLH} + t_{pHL}) / 2$
$= (12 + 10)/2$
$= 11$ nS

(b) the High and Low level noise margins V_{NH} and V_{NL} and, the overall noise margin.

(c) the average power dissipation P_D per gate

$V_{NH} = V_{OH} - V_{IH}$
$= 2.7 - 2$
$= 0.7$ V

$V_{NL} = V_{IL} - V_{OL}$
$= 0.8 - 0.4$
$= 0.4$ V

P_D for the IC = Vcc * Icc(avg)
$= Vcc * (I_{CCH} + I_{CCL})/ 2$
$= 5 * (8 + 20) /2$
$= 70$ mW

Power dissipation per gate
$= 70/2$
$= 35$ mW

(10 marks)

C1 Single digit decimal numbers coded in BCD (Binary Coded decimal) are applied to a 4-input (D C B A) combinational logic circuit as shown in figure C1.1. The combinational logic circuit has an output labelled Y which responds as follows:

- Output Y goes **High** whenever the **BCD** inputs are **greater** than decimal $\mathbf{5}_{10}$.

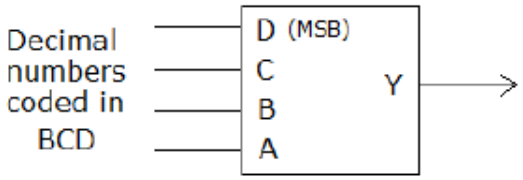


Figure C1.1

(a) Complete in your Answer Booklet, the truth table of the combinational logic circuit using a table format as shown in Table C1.1. Two output values are given as examples. There should be 16 combinations in total, ranging from 0000_2 to 1111_2 and don't care conditions should be indicated as 'X's.

(7 marks)

D	C	B	A	Y
0	0	0	0	0
:	:	:	:	?
1	1	1	1	X

Table C1.1

	D	C	B	A	Y
BCD	0	0	0	0	0
	0	0	0	1	0
	0	0	1	0	0
	0	0	1	1	0
	0	1	0	0	0
	0	1	0	1	0
	0	1	1	0	1
	0	1	1	1	1
	1	0	0	0	1
	1	0	0	1	1
Non-BCD	1	0	1	0	X
	1	0	1	1	X
	1	1	0	0	X
	1	1	0	1	X
	1	1	1	0	X
	1	1	1	1	X

0 1 2 3 4 5 6 7 8 9 10 11 12 13 14 15

Above 5

Don't care

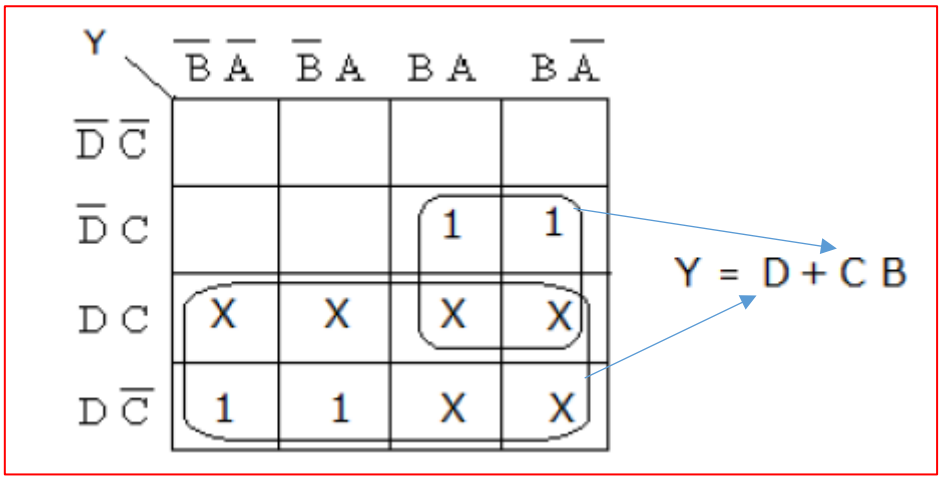
(b) From your completed truth table in part (a), derive the Boolean equation for output Y in a sum-of-products form. You may ignore the don't care terms for this equation.

(2 marks)

$$Y = \overline{D}CB\overline{A} + \overline{D}CBA + D\overline{C}\overline{B}\overline{A} + D\overline{C}\overline{B}A$$

(c) Using the K-Map, obtain the simplest equation of output Y from the truth-table of part (a).

(4 marks)



(d) Given the logic symbol of 74LS151, an 8-to-1 multiplexer IC as shown in figure C1.2, show how you would connect the device to implement the combinational logic circuit of part (a). Your circuit must be clearly labelled or marks will be deducted. (Hint: Assigned variables D, C and B to select inputs S2, S1 and S0, respectively.)

(7 marks)

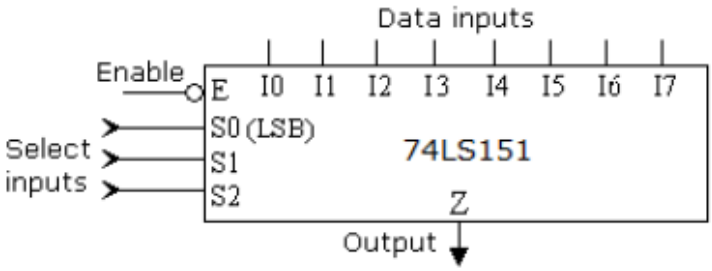


Figure C1.2

S2 S1 S0

	D	C	B	A	Y	
DCB = 0	0	0	0	0	*0*	*Y = 0*
	0	0	0	1	0	
1	0	0	1	0	0	*Y = 0*
	0	0	1	1	0	
2	0	1	0	0	0	*Y = 0*
	0	1	0	1	0	
3	0	1	1	0	1	*Y = 1*
	0	1	1	1	1	
4	1	0	0	0	1	*Y = 1*
	1	0	0	1	1	
5	1	0	1	0	X	*Y = x (0 or 1)*
	1	0	1	1	X	
6	1	1	0	0	X	*Y = x (0 or 1)*
	1	1	0	1	X	
7	1	1	1	0	X	*Y = x (0 or 1)*
	1	1	1	1	X	

Don't care (0 or 1)