2016/2017 S2 MID-SEMESTER TEST

SAS code: **MST**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Energy Systems Management DESM 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet, unless indicated otherwise.

4. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

5. There are 6 pages in this paper.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

1. How many different decimal values are there in a 16-bit (including sign bit) 2's complement signed numbering system?

(a) 32767_{10} (b) 32768_{10}

(c) 65535_{10} (d) 65536_{10}

2. The 2's (two's) complement of binary number 01010101_2, is _____.

(a) 10101010_2 (b) 11101011_2

(c) 10101100_2 (d) 10101011_2

3. In the 2's complement signed numbering system, a positive number has _____

(a) a sign bit of 1 in the MSB position.

(b) a sign bit of 0 in the MSB position.

(c) a sign bit of 1 in the LSB position.

(d) a sign bit of 0 in the LSB position.

4. The result **of a BCD arithmetic operation** is: $1000\ 0010_2$. Which one of the following sets of decimal numbers could have been added?

(a) $8_{10} + 2_{10}$ (b) $78_{10} + 2_{10}$

(c) $40_{10} + 42_{10}$ (d) $8_{10} + 76_{10}$

5. A mod-16 binary sequence counter has four outputs labelled as D C B A, with D being the MSB and A the LSB. If the signal frequency at its 3rd output C is 8 kHz, what is the signal frequency of the CLK signal applied at its clock input??

(a) 1_{10} kHz (b) 16_{10} kHz (c) 32_{10} Hz (d) 64_{10} kHz

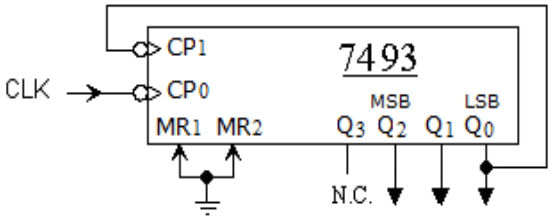
6. How many JK flip-flops are required to build a mod-100_{10} BCD counter?

(a) 6_{10} (b) 7_{10} (c) 8_{10} (d) 100_{10}

7. A mod-16 down counter is clocked by a signal of 256 Hz, at 30% duty cycle. The signal frequency and duty cycle at its MSB output will be_____.

(a) 16 Hz, 50% duty cycle
(b) 16 Hz, 30 % duty cycle
(c) 4096 Hz, 50% duty cycle
(d) 4096 Hz, 30% duty cycle

8. What is the mod-number of the counter circuit shown in figure A8?



NB: N.C. is abbreviation for No Connection

Figure A8

(a) Mod-16_{10}
(b) Mod-6_{10}
(c) Mod-8_{10}
(d) Mod-10_{10}

9. What is the minimum number of 7493 (4-bit) counter ICs required to construct a binary counter that counts to a maximum of 1023_{10}?

(a) 2_{10}
(b) 3_{10}
(c) 4_{10}
(d) 5_{10}

10. Identify the circuit shown in figure A10.

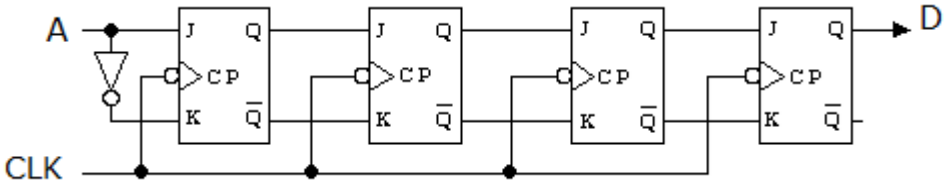


Figure A10

(a) Mod-16_{10} ripple counter.
(b) Serial-in, Serial-out shift register.
(c) Parallel-in, parallel-out shift register.
(d) It is neither a counter nor a register circuit.

Section B (45 marks)

B1. This question consists of two parts that involve numerical calculations and/or number conversions.

(a) Perform the addition of the following set of numbers using **BCD** arithmetic:

Add $+57_{10}$ to $+36_{10}$ (7 marks)

(b) Perform the following operation using the 8 bits (including the sign bit) two's complement signed numbering system.

Subtract $+70_{10}$ from $+99_{10}$ (8 marks)

NB: All steps and **workings** for this question **must be shown** or marks will be deducted.

B2 **A** 74LS283 IC (a 4-bit parallel Adder IC) is connected to a Full Adder unit as shown in figure B2.

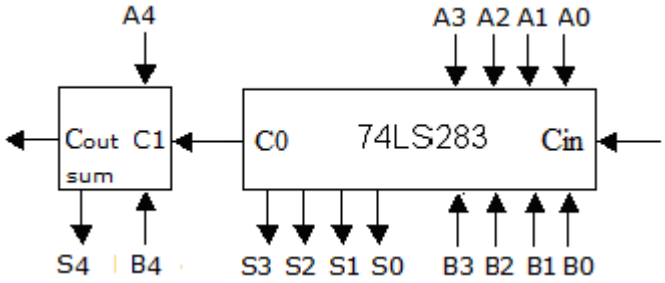


Figure B2

(a) Given: $A_4\ A_3\ A_2\ A_1\ A_0 = 0\ 1\ 1\ 1\ 0_2$ and,

$B_4\ B_3\ B_2\ B_1\ B_0 = 1\ 1\ 0\ 1\ 1_2$ respectively,

What will be the binary value at the outputs: $C_{out}\ S_4\ S_3\ S_2\ S_1\ S_0$ for $C_{in} = \mathbf{1}$?

(4 marks)

(b) If 5 bits (including the sign bit) 2's complement signed arithmetic is used in part (a), what are the equivalent decimal numbers being added at the A & B inputs and, what is the equivalent decimal Sum result?

(6 marks)

(c) If the Full Adder is used to construct the 74LS283 parallel Adder circuit, how many Full Adder units are needed? Show how the Full Adder units should be connected to implement the 74LS283. Label your circuit as according to the 74LS283 IC symbol of figure B2.

(5 marks)

B3(a) Given a periodic clock signal as shown in figure B3.1, calculate its

(i) Signal frequency.

(ii) Duty cycle.

(4 marks)

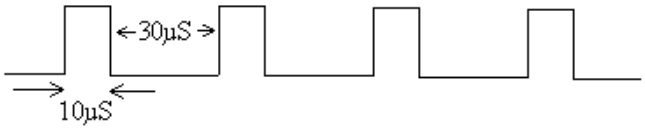


Figure B3.1

(b) The Clock signal in figure B3.1 is applied to the Clock input of a Mod-8 counter, what will be the signal frequency and duty cycle at the MSB output of this Mod-8 counter?

(3 marks)

(c) Using the correct number of negative edged triggered JK flip-flops, the symbol of which is shown in B3.2, implement (draw circuit of) the Mod-8 counter. Ensure that your circuit diagram is clearly labelled, showing all the required logic levels at the inputs. All the outputs must also be appropriately labelled.

(4 marks)

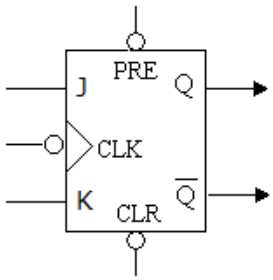


Figure B3.2

(d) Draw the state transition diagram of the mod-8 counter.
If the initial state (starting value) of the counter is 000_2, what will be the state at the outputs (binary values) after the application of 650_{10} clock cycles?

(4 marks)

Section C (25 marks)

C1 An Astable circuit is connected to the CLK input of a frequency-divider circuit (mod-10 counter) as shown in figure C1.1.

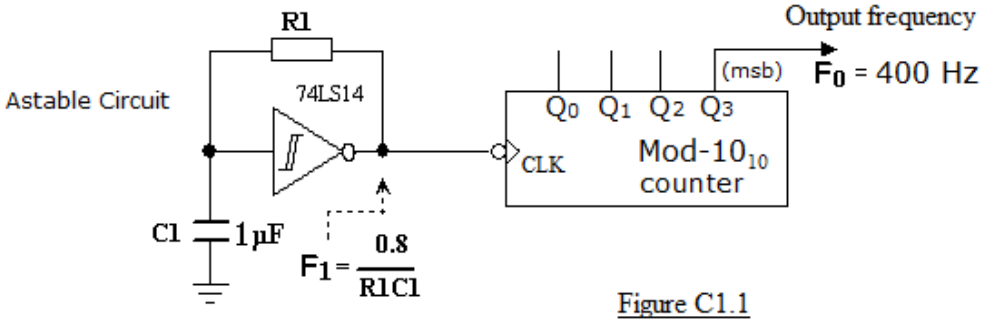


Figure C1.1

(a) What should be the frequency at the output of the **Astable** circuit if the frequency at the MSB output of the Mod-10 **counter** is **400 Hz**?

(4 marks)

(b) Calculate the resistance **R1** of the Astable circuit, given that its frequency $F_1 = \frac{0.8}{R_1 C_1}$ Hz.

(4 marks)

(c) Using one 7493 IC, the symbol and internal circuit of which is given in figure C1.2, show how you would connect the IC to function as the **Mod-10**$_{10}$ counter. Draw your circuit in your answer booklet using only the 7493 symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will be deducted.

(7 marks)

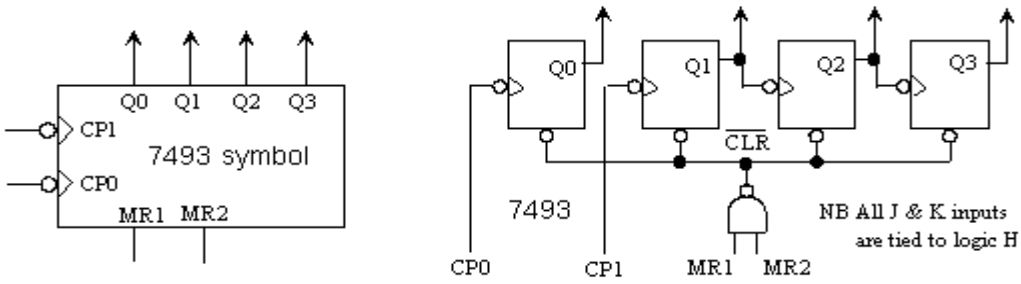


Figure C1.2

(d) Determine the duty cycle of the signal at the MSB output of the Mod-10 counter.

(4 marks)

(e) If the frequency at the MSB output of the Mod-10$_{10}$ counter is to be further divided to **100 Hz** with **50% duty cycle**, what other counter circuit must be connected to the MSB output of the Mod-10$_{10}$ counter? You may use the 7493 IC to implement the required counter circuit which must be clearly labelled, or marks will be deducted.

(6 marks)

---------- End of Paper ----------