SINGAPORE POLYTECHNIC ET1004

2012/2013 SEMESTER 2 EXAMINATION

Diploma in Electrical & Electronic Engineering DEEE 1st Year FT
Diploma in Info-communication Engineering & Design DICD 1st Year FT
Diploma in Computer Engineering DCPE 1st Year FT
Diploma in Aerospace Electronics DASE 1st Year FT
Diploma in Clean Energy DCEG 1st Year FT
Diploma in Common Engineering DCEP 1st Year FT

SAS code:
EXAM

DIGITAL ELECTRONICS II Time Allowed : 2 hours

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of **THREE** sections:
   Section A - 10 Multiple Choice Questions, 2 marks each.
   Section B - 6 Short Questions, 10 marks each.
   Section C - 1 Long Question of 20 marks.

3. Answer **ALL** questions in the accompanying Answer Booklet, unless otherwise indicated. Start each question in Sections B and C on a new page.

4. This Examination Paper consists of 8 pages

5. Your admission number and module class must be entered in the box provided on the cover page of your Answer Booklet.

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

1. What is the range of decimal values that can be represented by a 16-bit (including sign bit) 2's complement signed numbering system?

(a) $+15_{10}$ to -16_{10}
(b) $+63_{10}$ to -64_{10}
(c) $+127_{10}$ to -128_{10}
(d) $+32767_{10}$ to -32768_{10}

2. How many 74LS93 (4-bit) counter ICs are required to construct a BCD counter that counts to a maximum of 999_{10}?

(a) 2_{10}
(b) 3_{10}
(c) 4_{10}
(d) 6_{10}

3. A mod-16 down counter is clocked by a signal of 256 kHz, at 30% duty cycle. The signal frequency and duty cycle at its MSB output will be:

(a) 64 kHz, 30% duty cycle
(b) 64 kHz, 50 % duty cycle
(c) 16 kHz, 30% duty cycle
(d) 16 kHz, 50% duty cycle

4. A Multiplexer accepts data from one of -

(a) many input lines and transfers it to one of the select lines.
(b) many input lines and transfers it to one output line.
(c) many input lines and transfers it to several output lines.
(d) many input lines and transfers it to multiple select lines.

5. How many Select inputs are required for a Decoder with 1 enable input and 64 data outputs?

(a) 1_{10}
(b) 3_{10}
(c) 6_{10}
(d) 64_{10}

6. What is the correct mathematical expression to calculate the average power consumed by a TTL digital IC?

(a) $(I_{OH} + I_{CCH})/2 * V_{OH}$

(b) $(I_{CCL} + I_{OL})/2 * V_{CC}$

(c) $(I_{OL} + I_{OH})/2 * V_{OL}$

(d) $(I_{CCH} + I_{CCL})/2 * V_{CC}$

7. A shift register which inputs multiple data bits simultaneously but transfer out data one bit at a time is a:

(a) parallel-in, serial-out register
(b) parallel-in, parallel-out register
(c) serial-in, parallel-out register
(d) serial-in, serial-out register

8. In the **8-bit** (including the sign bit) two's complement signed numbering system, what does the binary number 10000000 equates to when converted to decimal?

(a) -128_{10}
(b) -1_{10}
(c) $+127_{10}$
(d) Zero

9. What is the maximum possible number of data inputs for a multiplexer with 4 select inputs?

(a) 4_{10} inputs
(b) 16_{10} inputs
(c) 32_{10} inputs
(d) 64_{10} inputs

10. A 74147 Decimal-to-BCD priority encoder circuit is connected as shown in Figure A10. What is the binary code generated at its outputs?

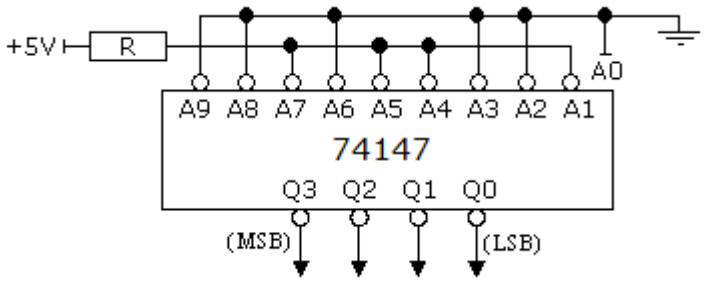


Figure A10

(a) $Q_3\ Q_2\ Q_1\ Q_0 = 1001$
(b) $Q_3\ Q_2\ Q_1\ Q_0 = 1000$
(c) $Q_3\ Q_2\ Q_1\ Q_0 = 0111$
(d) $Q_3\ Q_2\ Q_1\ Q_0 = 0110$

Section B Short Questions (60 marks)

B1. Perform the following operation using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit.

(a) Add $+38_{10}$ to $+53_{10}$

(4 marks)

(b) Add -32_{10} to $+77_{10}$

(6 marks)

NB: All workings in question B1 must be shown or marks will not be awarded.

B2(a) The 74LS138 is a **1-of-8** decoder device and has a symbol as shown in figure B2.1. What is another name for this decoder? If output **Y7** of the 74LS138 decoder is to be selected, what logic levels are required at both the **Enable** and **Select** inputs? (5 marks)

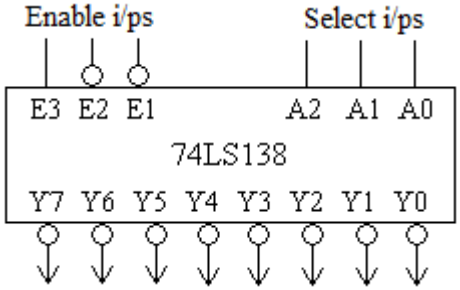


Figure B2.1

(b) Figure B2.2 shows a partially completed circuit diagram of two 74LS138 decoder ICs being connected as a 1-of-16 decoder. Copy figure B2.2 and complete in your answer booklet, the circuit diagram of this 1-of-16 decoder. Ensure that you label all inputs and outputs as according to the labels used in figure B2.2.
Hint: Output O_0 is selected when select inputs S_3 S_2 S_1 S_0 = 0 0 0 0 and Output O_{15} is selected when S_3 S_2 S_1 S_0 = 1 1 1 1.

(5 marks)

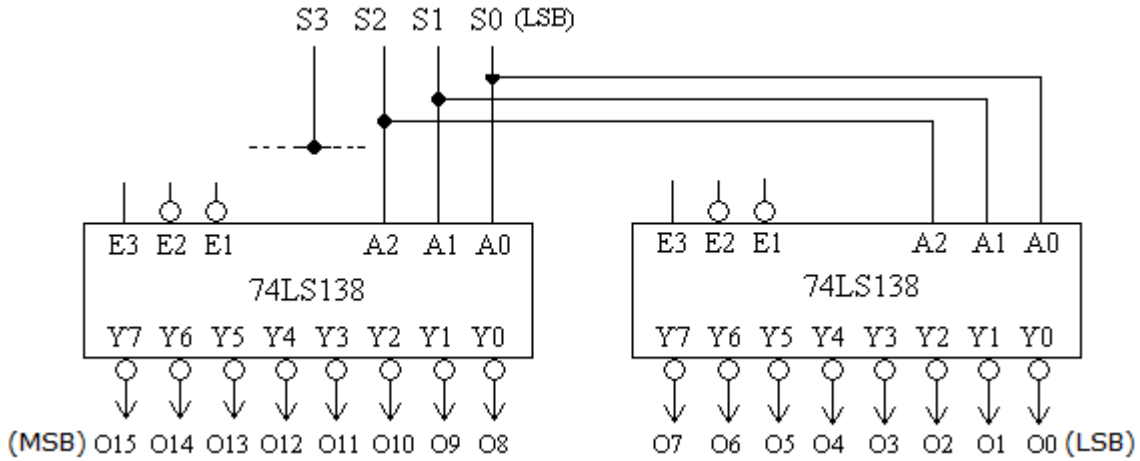


Figure B2.2

B3 The 74LS283 as shown in figure B3, is a 4-bit parallel adder IC, i.e. a device that adds two sets of 4-bit numbers simultaneously.

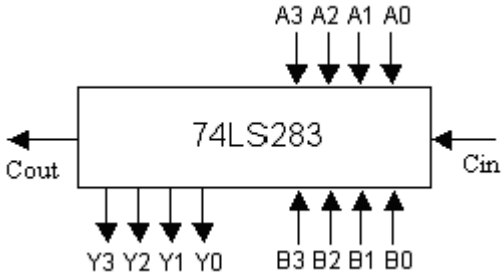


Figure B3

(a) If A3 A2 A1 A0 = 0 1 0 1 and B3 B2 B1 B0 = 1 1 0 1, respectively, what will be the binary value of the outputs Cout, Y3 Y2 Y1 Y0 with Cin = 1? (4 marks)

(b) If 4 bits (including the sign bit) 2's complement signed arithmetic is used in part (a) above, what are the equivalent decimal numbers being added and the decimal sum result? (4 marks)

(c) How many 74LS283 ICs are needed to build a **16 bit** parallel Adder? (2 marks)

B4 Each of the 5 statements comprising this question describes a particular type of counter or shift register. You are required to state in your answer booklet, the type of counter or shift register being described by each statement. Ensure that your answers are labelled exactly according to each of the statements i.e. [**(a), (b)....(e)**] or marks will not be awarded. (10 marks)

(a) This counter allows its outputs to be displayed as decimal digits through the use of the seven-segment LED display and appropriate decoder.

(b) Each flip-flop of this asynchronous counter functions as a divide-by 2 circuit.

(c) This shift register circuit can be used to delay a signal by a fix number of clock cycles that correspond to the number of flip-flops used.

(d) This shift register circuit has only one data input and several data outputs.

(e) This counter divides its input clock signal frequency by its mod-number.

B5 The 74151 is described as an 8- to-1 multiplexer. Figure B5.1 shows the symbol of this multiplexer.

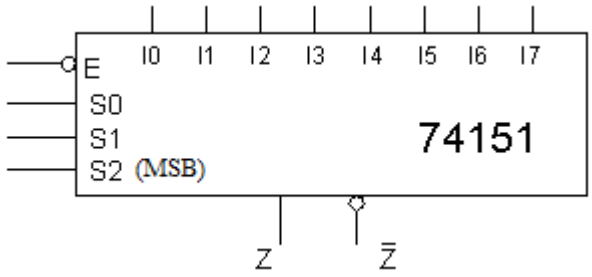


Figure B5.1

(a) Using one 74151 8-input multiplexer IC, show how the 74151 can be connected as a 4-to-1 multiplexer. In your completed diagram, label the required data inputs as D_0 D_1 D_2 D_3 and the select inputs as A_1 A_0, where the subscript of 0 denotes the LSB. Unused inputs should be indicated as N.C.

(4 marks)

(b) Given the 74151 multiplexer connected as shown in figure B5.2, determine the logic function (i.e. Boolean expression) implemented at both outputs: Z and $\overline{Z}$. From the resultant expressions obtained, what are the generic names of these two output functions?

Hint: Create a truth table with B and A as input variables and Z, $\overline{Z}$ as outputs.

(6 marks)

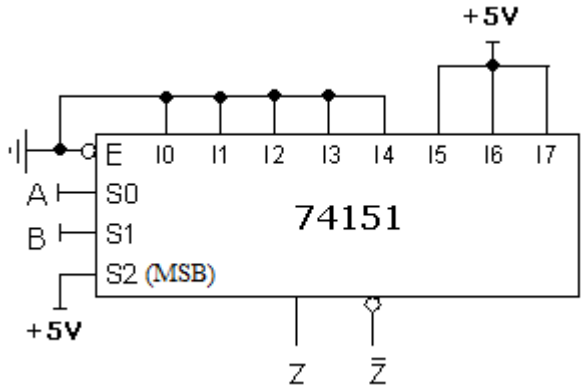
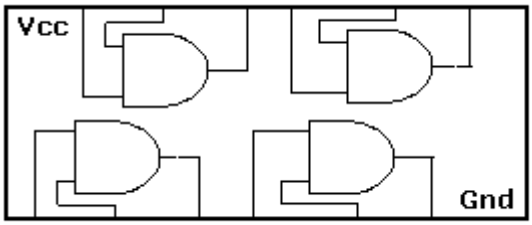


Figure B5.2

B6. Table B6 lists the typical values of the AC and DC **parameters** (characteristics) for three different logic families of the 7408 Quad 2-input AND gate **Integrated Circuit**.



Parameter	Unit	Device A	Device B	Device C
Vcc	V	5	5	5
$V_{IH\ (min)}$	V	2	2	2
$V_{IL\ (max)}$	V	0.8	0.7	0.8
$V_{OH\ (min)}$	V	2.4	2.7	2.5
$V_{OL\ (max)}$	V	0.4	0.5	0.5
Icc_H	mA	16	2.4	10
Icc_L	mA	32	6.6	22
tp_{LH}	nS	15	10	2
tp_{HL}	nS	14	9	2

Table B6

(a) Calculate the average power consumption **per gate** for device **A**.

(4 marks)

(b) By comparing the values of the relevant parameters given in Table B6, which device has the **lowest** power dissipation? Note that **you are not required** to calculate the actual power dissipation for the devices.

(2 marks)

(c) Which device has the lowest value of output voltage for logic High and what is the value of this voltage?

(2 marks)

(d) By comparing the values of the relevant parameters given in Table B6, which device can operate at the **highest** frequency? As in part (b), numerical calculations are not required.

(2 marks)

Section C Long Question (20 marks)

C1 An Astable circuit is connected to the CLK input of a frequency divider circuit as shown in figure C1.1.

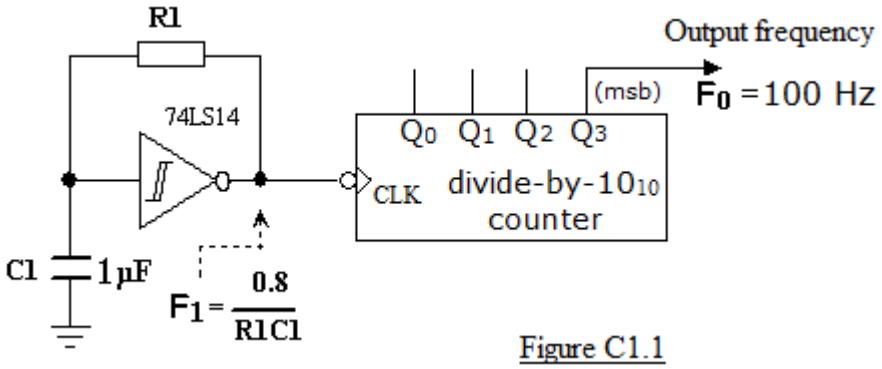


Figure C1.1

(a). What should be the frequency at the output of the **Astable** circuit if the frequency at the MSB output of the **counter** is **100 Hz**?

(3 marks)

(b) Calculate the resistance **R1** of the Astable circuit, given that its frequency $F1 = \frac{0.8}{R1\,C1}$ Hz.

(4 marks)

(c) Using one 7493 IC, the symbol and internal circuit of which is given in figure C1.2, show how you would connect the IC to function as the **divide-by-10_{10}** counter. Draw your circuit in your answer booklet using only the 7493 symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will be deducted.

(7 marks)

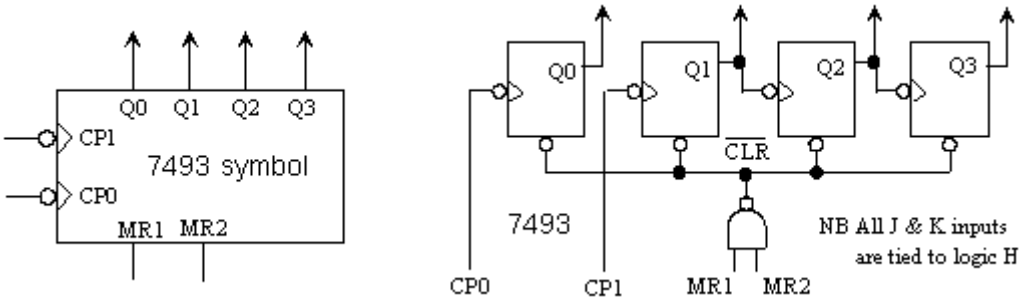


Figure C1.2

(d) If the frequency at the output of the divide-by-10_{10} counter is to be further divided to **10 Hz** at **50% duty cycle**, what other counter circuits must be connected to the MSB output of the divide-by-10_{10} counter? You may use as many 7493 ICs to implement these circuits which must be clearly labelled or marks will be deducted.

(6 marks)

---------- End of Paper ----------