PROBLEMS

SECTION 1-2

1-1. Which of the following are analog quantities, and which are digital?
(a) Number of atoms in a sample of material
(b) Altitude of an aircraft
(c) Pressure in a bicycle tire
(d) Current through a speaker
(e) Timer setting on a microwave oven

SECTION 1-3

1-2. Convert the following binary numbers to their equivalent decimal values:
(a) 11001_2
(b) 1001.1001_2
(c) 10011011001.10110_2

1-3. Using six bits, show the binary counting sequence from 000000 to 111111.

1-4. What is the maximum number that we can count up to using 10 bits?

1-5. How many bits are needed to count up to a maximum of 511?

SECTION 1-4

1-6. Draw the timing diagram for a digital signal that continuously alternates between 0.2 V (binary 0) for 2 ms and 4.4 V (binary 1) for 4 ms.

SECTION 1-6

1-7. Suppose that the decimal integer values from 0 to 15 are to be transmitted in binary.
(a) How many lines will be needed if parallel representation is used?
(b) How many will be needed if serial representation is used?

SECTIONS 1-7 AND 1-8

1-8. How is a microprocessor different from a microcomputer?

1-9. How is a microcontroller different from a microcomputer?

ANSWERS TO SECTION REVIEW QUESTIONS

SECTION 1-1

1. Analog quantities can take on *any* value over a continuous range; digital quantities can take on only *discrete* values.

SECTION 1-2

1. Easier to design; easier to store information; greater accuracy and precision; programmability; less affected by noise; higher degree of integration 2. Real-world physical quantities are analog. Digital processing takes time.

IMPORTANT TERMS

octal number system
hexadecimal number system
straight binary coding
binary-coded-decimal (BCD) code
byte
nibble
word
word size
alphanumeric code
American Standard Code for Information Interchange (ASCII)
parity method
parity bit

PROBLEMS

SECTIONS 2-1 AND 2-2

2-1. Convert these binary numbers to decimal.

(a) 10110
(b) 10001101
(c) 100100001001
(d) 01011011
(e) 11111111
(f) 01110111
(g) 1111010111
(h) 10111111

2-2. Convert the following decimal values to binary.

(a) 37
(b) 14
(c) 189
(d) 1024
(e) 77
(f) 405
(g) 205
(h) 2313
(i) 511

2-3. What is the largest decimal value that can be represented by an eight-bit binary number? A 16-bit number?

SECTION 2-3

2-4. Convert each octal number to its decimal equivalent.

(a) 743
(b) 36
(c) 3777
(d) 2000
(e) 165
(f) 5
(g) 257
(h) 1204

2-5. Convert each of the following decimal numbers to octal.

(a) 59
(b) 372
(c) 919
(d) 1024
(e) 771
(f) 2313
(g) 65,536
(h) 255

2-6. Convert each of the octal values from Problem 2-4 to binary.

2-7. Convert the binary numbers in Problem 2-1 to octal.

2-8. List the octal numbers in sequence from 165_8 to 200_8.

2-9. When a large decimal number is to be converted to binary, it is sometimes easier to convert it first to octal, and then from octal to binary. Try this procedure for 2313_{10} and compare it with the procedure used in Problem 2-2(e).

2-10. How many octal digits are required to represent decimal numbers up to 20,000?

SECTION 2-4

2-11. Convert these hex values to decimal.

(a) 92
(b) 1A6
(c) 37FD
(d) ABCD
(e) 000F
(f) 55
(g) 2C0
(h) 7FF

2-12. Convert these decimal values to hex.

(a) 75 (d) 14 (g) 25,619
(b) 314 (e) 7245 (h) 4095
(c) 2048 (f) 389

2-13. Take each four-bit binary number in the order they are written and write the equivalent hex digit without performing a calculation by hand or by calculator.

(a) 1001 (e) 1111 (i) 1011 (m) 0001
(b) 1101 (f) 0010 (j) 1100 (n) 0101
(c) 1000 (g) 1010 (k) 0011 (o) 0111
(d) 0000 (h) 1001 (l) 0100 (p) 0110

2-14. Take each hex digit and write its four-bit binary value without performing any calculations by hand or by calculator.

(a) 6 (e) 4 (i) 9 (m) 0
(b) 7 (f) 3 (j) A (n) 8
(c) 5 (g) C (k) 2 (o) D
(d) 1 (h) B (l) F (p) 9

2-15. Convert the binary numbers in Problem 2-1 to hexadecimal.

2-16. Convert the hex values in Problem 2-11 to binary.

2-17. List the hex numbers in sequence from 280 to 2A0.

2-18. How many hex digits are required to represent decimal numbers up to 1 million?

SECTION 2-5

2-19. Encode these decimal numbers in BCD.

(a) 47 (d) 6727 (g) 42,689,627
(b) 962 (e) 13 (h) 1204
(c) 187 (f) 888

2-20. How many bits are required to represent the decimal numbers in the range from 0 to 999 using straight binary code? Using BCD code?

2-21. The following numbers are in BCD. Convert them to decimal.

(a) 1001011101010010 (d) 0111011101110101
(b) 000110000100 (e) 010010010010
(c) 011010010101 (f) 010101010101

SECTION 2-7

2-22. (a) How many bits are contained in eight bytes?

(b) What is the largest hex number that can be represented in four bytes?

(c) What is the largest BCD-encoded decimal value that can be represented in three bytes?

2-23. (a) Refer to Table 2-4. What is the most significant nibble of the ASCII code for the letter X?

(b) How many nibbles can be stored in a 16-bit word?

(c) How many bytes does it take to make up a 24-bit word?

SECTIONS 2-8 AND 2-9

2-24. Represent the statement "X = 25/Y" in ASCII code (excluding the quotes). Attach an odd-parity bit.

2-25. Attach an *even*-parity bit to each of the ASCII codes for Problem 2-24, and give the results in hex.

2-26. The following bytes (shown in hex) represent a person's name as it would be stored in a computer's memory. Each byte is a padded ASCII code. Determine the name of the person.

42 45 4E 20 53 4D 49 54 48

2-27. Convert the following decimal numbers to BCD code and then attach an *odd*-parity bit.

(a) 74 (c) 8884 (e) 165

(b) 38 (d) 275 (f) 9201

2-28. In a certain digital system, the decimal numbers from 000 through 999 are represented in BCD code. An *odd*-parity bit is also included at the end of each code group. Examine each of the code groups below, and assume that each one has just been transferred from one location to another. Some of the groups contain errors. Assume that *no more than* two errors have occurred for each group. Determine which of the code groups have a single error and which of them *definitely* have a double error. (*Hint:* Remember that this is a BCD code.)

(a) 1001010110000
↑ parity bit

(b) 0100011101100

(c) 0111110000011

(d) 1000011000101

2-29. Suppose that the receiver received the following data from the transmitter of Example 2-16:

0 1 0 0 1 0 0 0
1 1 0 0 0 1 0 1
1 1 0 0 1 1 0 0
1 1 0 0 1 0 0 0
1 1 0 0 1 1 0 0

What errors can the receiver determine in these received data?

DRILL QUESTIONS

2-30. Perform each of the following conversions. For some of them, you may want to try several methods to see which one works best for you. For example, a binary-to-decimal conversion may be done directly, or it may be done as a binary-to-octal conversion followed by an octal-to-decimal conversion.

(a) 1417_{10} = _____ 2

(b) 255_{10} = _____ 2

(c) 11010001_2 = _____ 10

(d) 1110101000100111_2 = _____ 10

(e) 2497_{10} = _____ 8
(f) 511_{10} = _____ 8
(g) 235_8 = _____ 10
(h) 4316_8 = _____ 10
(i) $7A9_{16}$ = _____ 10
(j) $3E1C_{16}$ = _____ 10
(k) 1600_{10} = _____ 16
(l) $38{,}187_{10}$ = _____ 16
(m) 865_{10} = _____ (BCD)
(n) 100101000111 (BCD) = _____ 10
(o) 465_8 = _____ 16
(p) $B34_{16}$ = _____ 8
(q) 01110100 (BCD) = _____ 2
(r) 111010_2 = _____ (BCD)

2-31. Represent the decimal value 37 in each of the following ways.
(a) straight binary
(b) BCD
(c) hex
(d) ASCII (i.e., treat each digit as a character)
(e) octal

2-32. Fill in the blanks with the correct word or words.
(a) Conversion from decimal to _____ requires repeated division by 8.
(b) Conversion from decimal to hex requires repeated division by _____.
(c) In the BCD code, each _____ is converted to its four-bit binary equivalent.
(d) The _____ code has the characteristic that only one bit changes in going from one step to the next.
(e) A transmitter attaches a _____ to a code group to allow the receiver to detect _____.
(f) The _____ code is the most common alphanumeric code used in computer systems.
(g) _____ and _____ are often used as a convenient way to represent large binary numbers.
(h) A string of eight bits is called a _____.

2-33. Write the binary number that results when each of the following numbers is incremented by one.
(a) 0111 (b) 010000 (c) 1110

2-34. Repeat Problem 2-33 for the decrement operation.

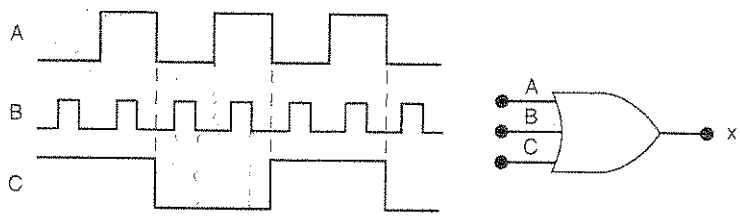
2-35. Write the number that results when each of the following is incremented.
(a) 7777_8 (c) 2000_8 (e) $9FF_{16}$
(b) 7777_{16} (d) 2000_{16} (f) 1000_{16}

2-36. Repeat Problem 2-35 for the decrement operation.

SECTION 3-3

B 3-1. Draw the output waveform for the OR gate of Figure 3-52.

FIGURE 3-52



3-2. Suppose that the *A* input in Figure 3-52 is unintentionally shorted to ground (i.e., $A = 0$). Draw the resulting output waveform.

3-3. Suppose that the *A* input in Figure 3-52 is unintentionally shorted to the +5 V supply line (i.e., $A = 1$). Draw the resulting output waveform.

3-4. Read the statements below concerning an OR gate. At first, they may appear to be valid, but after some thought you should realize that neither one is *always* true. Prove this by showing a specific example to refute each statement.

(a) If the output waveform from an OR gate is the same as the waveform at one of its inputs, the other input is being held permanently LOW.

(b) If the output waveform from an OR gate is always HIGH, one of its inputs is being held permanently HIGH.

3-5. How many different sets of input conditions will produce a HIGH output from a five-input OR gate?

SECTION 3-4

B 3-6. Change the OR gate in Figure 3-52 to an AND gate.

(a) Draw the output waveform.

(b) Draw the output waveform if the *A* input is permanently shorted to ground.

(c) Draw the output waveform if *A* is permanently shorted to +5 V.

D 3-7. Refer to Figure 3-4. Modify the circuit so that the alarm is to be activated only when the pressure and the temperature exceed their maximum limits at the same time.

B 3-8. Change the OR gate in Figure 3-6 to an AND gate and draw the output waveform.

3-9. Suppose that you have an unknown two-input gate that is either an OR gate or an AND gate. What combination of input levels should you apply to the gate's inputs to determine which type of gate it is?

3-10. *True or false:* No matter how many inputs it has, an AND gate will produce a HIGH output for only one combination of input levels.

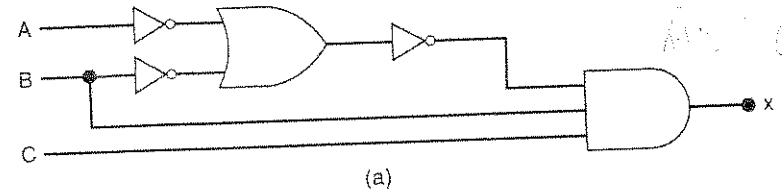
SECTIONS 3-5 TO 3-7

B 3-11. Apply the *A* waveform from Figure 3-23 to the input of an INVERTER. Draw the output waveform. Repeat for waveform *B*.

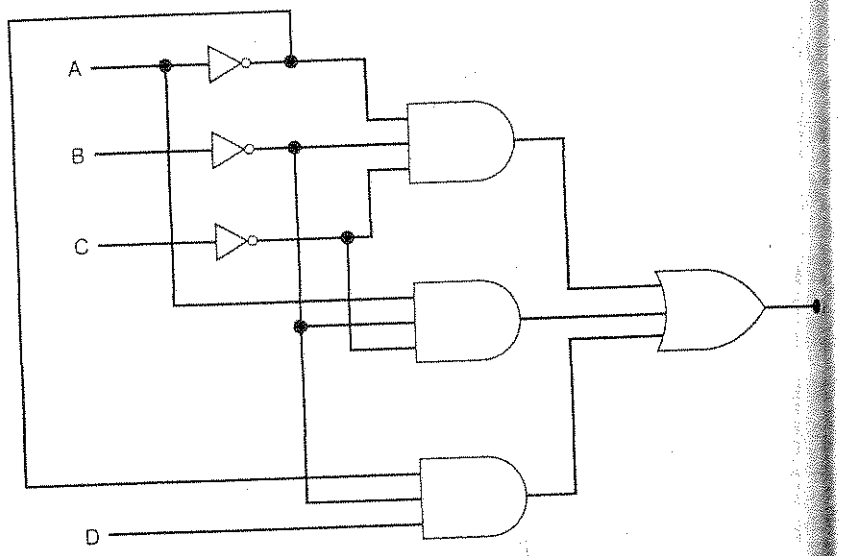
B 3-12. (a) Write the Boolean expression for output x in Figure 3-53(a). Determine the value of x for all possible input conditions, and list the values in a truth table.

(b) Repeat for the circuit in Figure 3-53(b).

FIGURE 3-53



(a)



(b)

3-13. Determine the complete truth table for the circuit of Figure 3-15(b) by finding the logic levels present at each gate output for each of the possible input combinations.

3-14. Change each OR to an AND, and each AND to an OR, in Figure 3-15(b). Then write the expression for the output.

3-15. Determine the complete truth table for the circuit of Figure 3-16 by finding the logic levels present at each gate output for each of the possible combinations of input levels.

SECTION 3-8

B 3-16. For each of the following expressions, construct the corresponding logic circuit, using AND and OR gates and INVERTERs.

(a) $x = \overline{AB(C + D)}$

(b) $z = \overline{A + B + \overline{C}D\overline{E}} + \overline{B}C\overline{D}$

(c) $y = \overline{(M + N} + \overline{P}Q)$

(d) $x = \overline{W + P\overline{Q}}$

(e) $z = MN(P + \overline{N})$

(f) $x = (A + B)(\overline{A} + \overline{B})$

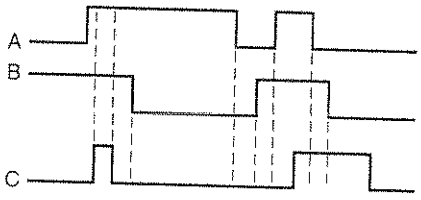
SECTION 3-9

B 3-17. (a) Apply the input waveforms of Figure 3-54 to a NOR gate, and draw the output waveform.

(b) Repeat with C held permanently LOW.

(c) Repeat with C held HIGH.

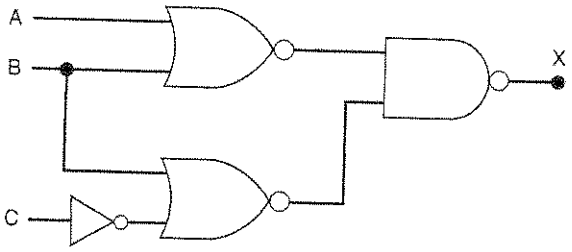
FIGURE 3-54



B 3-18. Repeat Problem 3-17 for a NAND gate.

C 3-19. Write the expression for the output of Figure 3-55, and use it to determine the complete truth table. Then apply the waveforms of Figure 3-54 to the circuit inputs, and draw the resulting output waveform.

FIGURE 3-55



3-20. Determine the truth table for the circuit of Figure 3-24.

3-21. Modify the circuits that were constructed in Problem 3-16 so that NAND gates and NOR gates are used wherever appropriate.

SECTION 3-10

B 3-22. DRILL QUESTION

Complete each expression.

(a) $A + 1 =$ _____

(b) $A \cdot A =$ _____

(c) $B \cdot \overline{B} =$ _____

(d) $C + C =$ _____

(e) $x \cdot 0 =$ _____

(f) $D \cdot 1 =$ _____

(g) $D + 0 =$ _____

(h) $C + \overline{C} =$ _____

(i) $G + GF =$ _____

(j) $y + \overline{w}y =$ _____

3-23. Prove theorems (15a) and (15b) by trying all possible cases.

C 3-24. (a) Simplify the following expression using theorems (13b), (3), and (4):

$$x = (M + N)(\overline{M} + P)(\overline{N} + \overline{P})$$

(b) Simplify the following expression using theorems (13a), (8), and (6):

$$z = \overline{A}B\overline{C} + AB\overline{C} + B\overline{C}D$$

SECTIONS 3-11 AND 3-12

3-25. Prove DeMorgan's theorems by trying all possible cases.

B 3-26. Simplify each of the following expressions using DeMorgan's theorems.

(a) $\overline{\overline{A}B\overline{C}}$ (d) $\overline{\overline{A + \overline{B}}}$ (g) $\overline{\overline{A(\overline{B + \overline{C}})D}}$

(b) $\overline{\overline{A + \overline{B}C}}$ (e) $\overline{\overline{A}\overline{B}}$ (h) $\overline{(M + \overline{N})(\overline{M} + N)}$

(c) $\overline{AB\overline{CD}}$ (f) $\overline{\overline{A + \overline{C} + \overline{D}}}$ (i) $\overline{\overline{ABCD}}$

3-27. Use DeMorgan's theorems to simplify the expression for the output in Figure 3-55.

C 3-28. Convert the circuit of Figure 3-53(b) to one using only NAND gates. Then write the output expression for the new circuit, simplify it using DeMorgan's theorems, and compare it with the expression for the original circuit.

3-29. Convert the circuit of Figure 3-53(a) to one using only NOR gates. Then write the expression for the new circuit, simplify it using DeMorgan's theorems, and compare it with the expression for the original circuit.

B 3-30. Show how a two-input NAND gate can be constructed from two-input NOR gates.

B 3-31. Show how a two-input NOR gate can be constructed from two-input NAND gates.

3-32. A jet aircraft employs a system for monitoring the rpm, pressure, and temperature values of its engines using sensors that operate as follows:

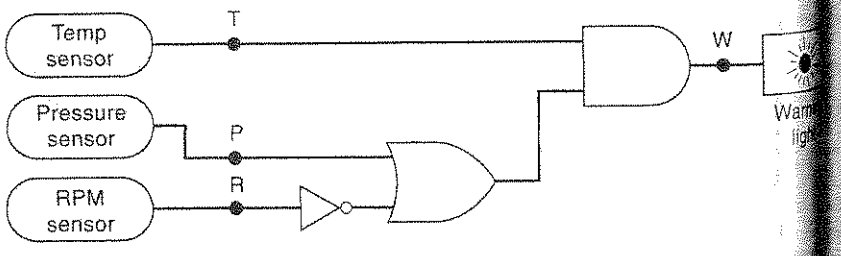
RPM sensor output = 0 only when speed < 4800 rpm
P sensor output = 0 only when pressure < 220 psi
T sensor output = 0 only when temperature < 200° F

Figure 3-56 shows the logic circuit that controls a cockpit warning light for certain combinations of engine conditions. Assume that a HIGH at output *W* activates the warning light.

(a) Determine what engine conditions will give a warning to the pilot.

(b) Change this circuit to one using all NAND gates.

FIGURE 3-56



SECTIONS 3-13 AND 3-14

B 3-33. Draw the standard representations for each of the basic logic gates. Then draw the alternate representations.

3-34. For each statement below, draw the appropriate logic-gate symbol—standard or alternate—for the given operation.

(a) A HIGH output occurs only when all three inputs are LOW.

(b) A LOW output occurs when any of the four inputs is LOW.

(c) A LOW output occurs only when all eight inputs are HIGH.

3-35. The circuit of Figure 3-55 is supposed to be a simple digital combination lock whose output will generate an active-LOW $\overline{UNLOCK}$ signal for only one combination of inputs.

(a) Modify the circuit diagram so that it represents more effectively the circuit operation.

(b) Use the new circuit diagram to determine the input combination that will activate the output. Do this by working back from the output using the information given by the gate symbols, as was done in Examples 3-22 and 3-23. Compare the results with the truth table obtained in Problem 3-19.

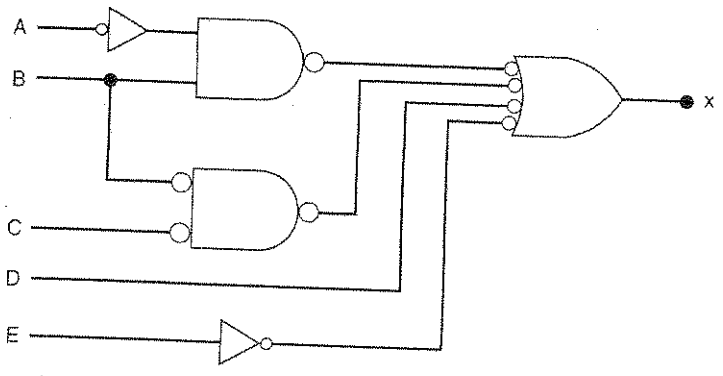
3-36. (a) Determine the input conditions needed to activate output Z in Figure 3-37(b). Do this by working back from the output, as was done in Examples 3-22 and 3-23.

(b) Assume that it is the LOW state of Z that is to activate the alarm. Change the circuit diagram to reflect this, and then use the revised diagram to determine the input conditions needed to activate the alarm.

D 3-37. Modify the circuit of Figure 3-40 so that $A_1 = 0$ is needed to produce $DRIVE = 1$ instead of $A_1 = 1$.

3-38. Determine the input conditions needed to cause the output in Figure 3-57 to go to its active state.

FIGURE 3-57



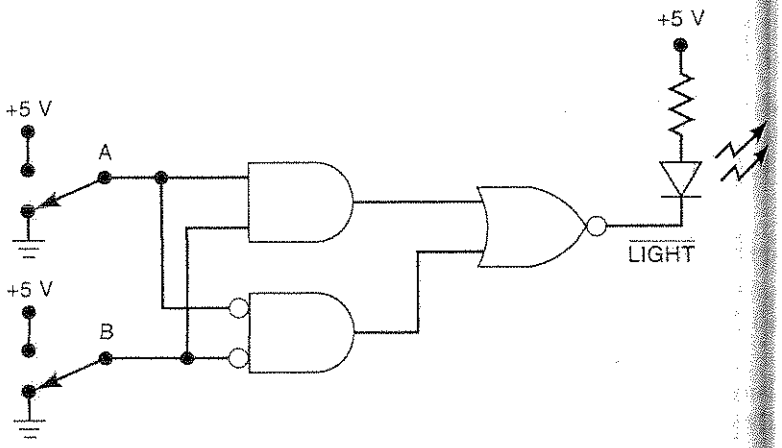
3-39. Use the results of Problem 3-38 to obtain the complete truth table for the circuit of Figure 3-57.

B 3-40. What is the asserted state for the output of Figure 3-57? For the output of Figure 3-36(c)?

3-41. Figure 3-58 shows an application of logic gates that simulates a two-way switch like the ones used in our homes to turn a light on or off from two different switches. Here the light is an LED that will be ON (conducting) when the NOR gate output is LOW. Note that this output is labeled $\overline{LIGHT}$ to indicate that it is active-LOW. Determine the input conditions needed to turn on the LED. Then verify that the circuit

operates as a two-way switch using switches A and B. (In Chapter 4 you will learn how to design circuits like this one to produce a given relationship between inputs and outputs.)

FIGURE 3-58



SECTION 3-15

3-42. Redraw the circuits of (a) Figure 3-57 and (b) Figure 3-58 using the IEEE/ANSI symbols.

ANSWERS TO SECTION REVIEW QUESTIONS

SECTION 3-2

1. $x = 1$ 2. $x = 0$ 3. 32

SECTION 3-3

1. All inputs LOW 2. $x = A + B + C + D + E + F$ 3. Constant HIGH

SECTION 3-4

1. All five inputs = 1 2. A LOW input will keep the output LOW. 3. False; see truth table of each gate.

SECTION 3-5

1. Output of second INVERTER will be same as input A. 2. y will be LOW only for $A = B = 1$.

SECTION 3-6

1. $x = \overline{A} + B + C + \overline{AD}$ 2. $x = D(\overline{AB + C}) + E$

SECTION 3-7

1. $x = 1$ 2. $x = 1$ 3. $x = 1$ for both.

SECTION 3-8

1. See Figure 3-15(a). 2. See Figure 3-17(b). 3. See Figure 3-15(b).

SECTION 3-9

1. All inputs LOW. 2. $x = 0$ 3. $x = \overline{A + B + \overline{CD}}$

SECTION 3-10

1. $y = A\overline{C}$ 2. $y = \overline{A}\overline{B}\overline{D}$ 3. $y = \overline{A}D + BD$

SECTION 3-11

1. $z = \overline{A}\overline{B} + C$ 2. $y = (\overline{R} + S + \overline{T})Q$ 3. Same as Figure 3-28 except NAND is replaced by NOR. 4. $y = \overline{A}B(C + \overline{D})$

SECTION 3-12

1. Three. 2. NOR circuit is more efficient because it can be implemented with one 74LS02 IC. 3. $x = (\overline{AB})\,(\overline{CD}) = \overline{\overline{AB}} + \overline{\overline{(CD)}} + AB + CD$

SECTION 3-13

1. Output goes LOW when any input is HIGH. 2. Output goes HIGH only when all inputs are LOW. 3. Output goes LOW when any input is LOW. 4. Output goes HIGH only when all inputs are HIGH.

SECTION 3-14

1. Z will go HIGH when $A = B = 0$ and $C = D = 1$. 2. Z will go LOW when $A = B = 0$, $E = 1$, and either C or D or both are 0. 3. Two 4. Two 5. LOW 6. $A = B = 0$, $C = D = 1$ 7. $\overline{W}$

SECTION 3-15

1. See Figure 3-41. 2. Rectangle with & inside, and triangles on inputs.

SECTION 3-16

1. Boolean equation, truth table, logic diagram, timing diagram, language.

6. Each of the basic gates (AND, OR, NAND, NOR) can be used to enable or disable the passage of an input signal to its output.
7. The main digital IC families are the TTL and CMOS families. Digital ICs are available in a wide range of complexities (gates per chip), from the basic to the high-complexity logic functions.
8. To perform basic troubleshooting requires—at a minimum—an understanding of circuit operation, a knowledge of the types of possible faults, a complete logic-circuit connection diagram, and a logic probe.
9. A programmable logic device (PLD) is an IC that contains a large number of logic gates whose interconnections can be programmed by the user to generate the desired logic relationship between inputs and outputs.
10. To program a PLD, you need a development system that consists of a computer, PLD development software, and a programmer fixture that does the actual programming of the PLD chip.
11. The Altera system allows convenient hierarchical design techniques using any form of hardware description.
12. The type of data objects must be specified so that the HDL compiler knows the range of numbers to be represented.
13. Truth tables can be entered directly into the source file using the features of HDL.
14. Logical control structures such as IF, ELSE, and CASE can be used to describe the operation of a logic circuit, making the code and the problem's solution much more straightforward.

IMPORTANT TERMS

sum-of-products (SOP)
product-of-sums (POS)
Karnaugh map (K map)
looping
don't-care condition
exclusive-OR (XOR)
exclusive-NOR (XNOR)
parity generator
parity checker
enable/disable
dual-in-line package (DIP)
SSI, MSI, LSI, VLSI, ULSI, GSI
transistor-transistor logic (TTL)
complementary metal-oxide-semiconductor (CMOS)
indeterminate
floating
logic probe
contention
programmer
ZIF socket
JEDEC
JTAG
hierarchical design
top-down
test vectors
literals
bit array
BIT_VECTOR
index
integer
objects
libraries
macrofunction
STD_LOGIC
STD_LOGIC_VECTOR
selected signal assignment
concatenate
decision control structure
concurrent
sequential
PROCESS
sensitivity list
IF/THEN
ELSE
ELSIF
CASE

PROBLEMS

SECTIONS 4-2 AND 4-3

B

4-1. Simplify the following expressions using Boolean algebra.

(a) $x = ABC + \overline{A}C$

(b) $y = (Q + R)(\overline{Q} + \overline{R})$

(c) $w = ABC + A\overline{B}C + \overline{A}$

(d) $q = \overline{RST}(\overline{R + S + T})$

(e) $x = \overline{A}\,\overline{B}\,\overline{C} + \overline{A}BC + ABC + A\overline{B}\,\overline{C} + A\overline{B}C$

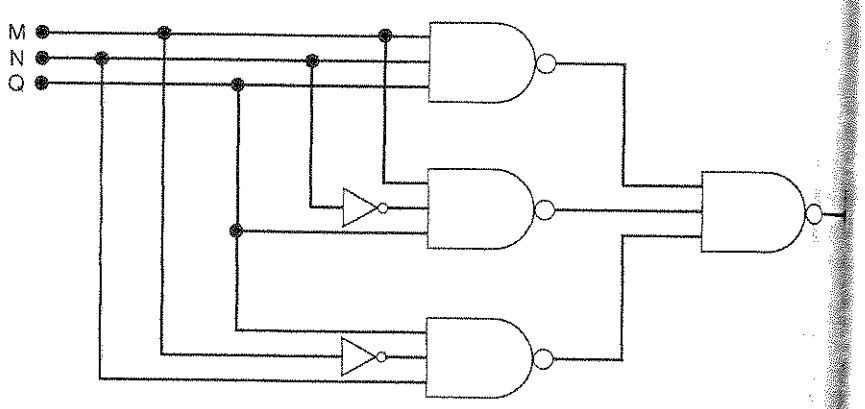
(f) $z = (B + \overline{C})(\overline{B} + C) + \overline{\overline{A} + B + \overline{C}}$

(g) $y = (\overline{C + D}) + \overline{A}C\overline{D} + A\overline{B}\,\overline{C} + \overline{A}\,\overline{B}CD + AC\overline{D}$

(h) $x = AB(\overline{\overline{C}\overline{D}}) + \overline{A}BD + \overline{B}\,\overline{C}\,\overline{D}$

B 4-2. Simplify the circuit of Figure 4-62 using Boolean algebra.

FIGURE 4-62 Problems 4-2 and 4-3.



FIGU

B 4-3. Change each gate in Problem 4-2 to a NOR gate, and simplify the circuit using Boolean algebra.

SECTION 4-4

B, D 4-4. Design the logic circuit corresponding to the truth table shown in Table 4-11.

TABLE 4-11

A	B	C	x
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

Sum of Product expression

B, D 4-5. Design a logic circuit whose output is HIGH *only* when a majority of inputs *A*, *B*, and *C* are LOW.

D 4-6. A manufacturing plant needs to have a horn sound to signal quitting time. The horn should be activated when either of the following conditions is met:

1. It's after 5 o'clock and all machines are shut down.
2. It's Friday, the production run for the day is complete, and all machines are shut down.

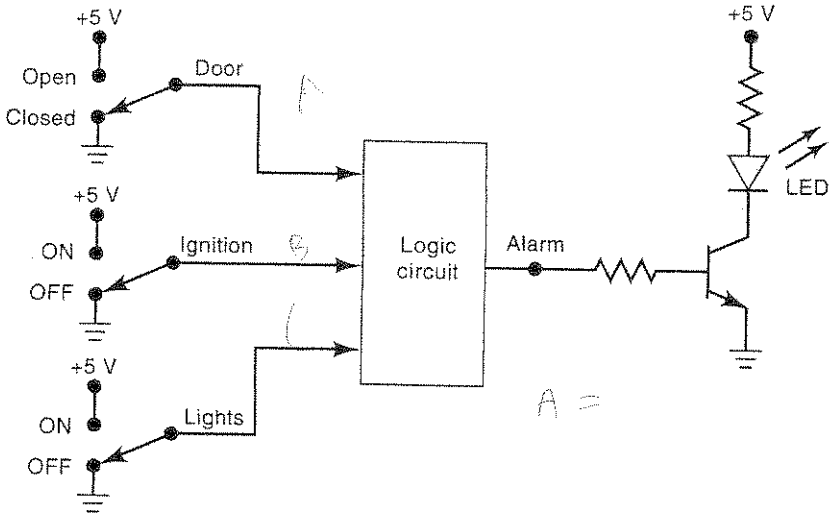
Design a logic circuit that will control the horn. (*Hint:* Use four logic input variables to represent the various conditions; for example, let *A* will be HIGH only when the time of day is 5 o'clock or later.)

D 4-7. A four-bit binary number is represented as $A_3A_2A_1A_0$, where A_3, A_2, A_1, and A_0 represent the individual bits and A_0 is equal to the LSB. Design a logic circuit that will produce a HIGH output whenever the binary number is greater than 0010 and less than 1000.

D 4-8. Figure 4-63 shows a diagram for an automobile alarm circuit used to detect certain undesirable conditions. The three switches are used to indicate the status of the door by the driver's seat, the ignition, and the headlights, respectively. Design the logic circuit with these three switches as inputs so that the alarm will be activated whenever either of the following conditions exists:

- The headlights are on while the ignition is off.
- The door is open while the ignition is on.

FIGURE 4-63 Problem 4-8.



4-9. Implement the circuit of Problem 4-4 using all NAND gates.

4-10. Implement the circuit of Problem 4-5 using all NAND gates.

SECTION 4-5

B 4-11. Determine the minimum expression for each K map in Figure 4-64. Pay particular attention to step 5 for the map in (a).

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	1	1	1
$\bar{A}B$	1	1	0	0
AB	0	0	0	1
$A\bar{B}$	0	0	1	1

(a)

	$\bar{C}\bar{D}$	$\bar{C}D$	CD	$C\bar{D}$
$\bar{A}\bar{B}$	1	0	1	1
$\bar{A}B$	1	0	0	1
AB	0	0	0	0
$A\bar{B}$	1	0	1	1

(b)

	$\bar{C}$	C
$\bar{A}\bar{B}$	0	1
$\bar{A}B$	0	0
AB	1	0
$A\bar{B}$	1	X

(c)

FIGURE 4-64 Problem 4-11.

B 4-12. Simplify the expression in Problem 4-1(e) using a K map.

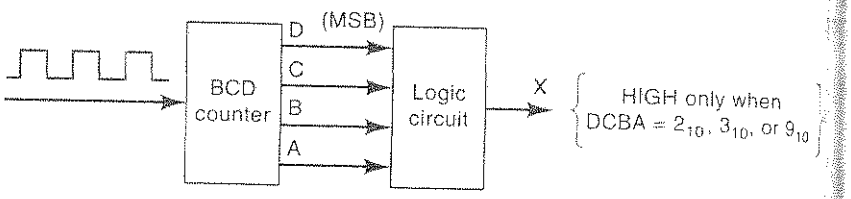
B 4-13. Simplify the expression in Problem 4-1(g) using a K map.

B 4-14. Simplify the expression in Problem 4-1(h) using a K map.

B 4-15. Obtain the output expression for Problem 4-7 using a K map.

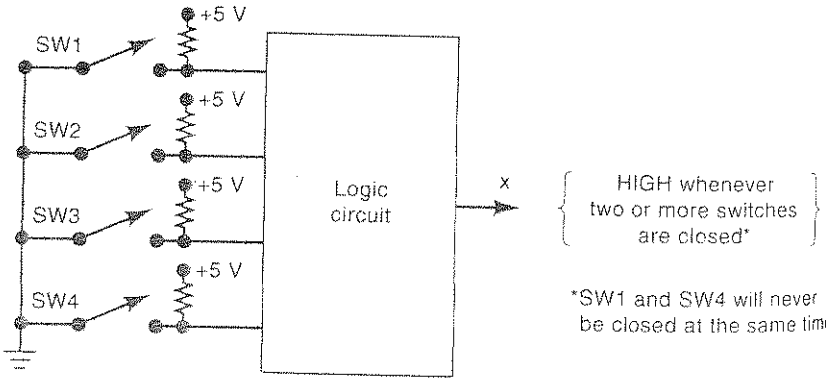
C, D 4-16. Figure 4-65 shows a *BCD counter* that produces a four-bit output resenting the BCD code for the number of pulses that have been plied to the counter input. For example, after four pulses h occurred, the counter outputs are $DCBA = 0100_2 = 4_{10}$. The counter sets to 0000 on the tenth pulse and starts counting over again. In ot words, the *DCBA* outputs will never represent a number greater th $1001_2 = 9_{10}$. Design the logic circuit that produces a HIGH outp whenever the count is 2, 3, or 9. Use K mapping and take advantage the don't-care conditions.

FIGURE 4-65 Problem 4-16.



D 4-17. Figure 4-66 shows four switches that are part of the control circu in a copy machine. The switches are at various points along the p of the copy paper as the paper passes through the machine. Ea switch is normally open, and as the paper passes over a switch, t switch closes. It is impossible for switches SW1 and SW4 to be clos at the same time. Design the logic circuit to produce a HIGH outp whenever *two or more* switches are closed at the same time. Use mapping and take advantage of the don't-care conditions.

FIGURE 4-66 Problem 4-17.



FIGU

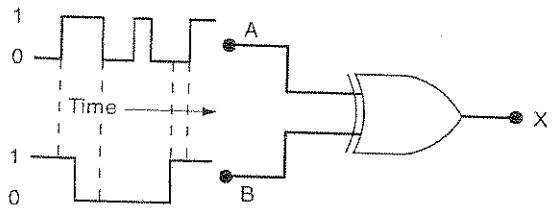
B 4-18. Example 4-3 demonstrated algebraic simplification. Step 3 resulte the SOP equation $z = \bar{A}\bar{B}C + \bar{A}C\bar{D} + \bar{A}B\bar{C}\bar{D} + A\bar{B}\bar{C}$. Use a K map prove that this equation can be simplified further than the ans shown in the example.

C 4-19. Use Boolean algebra to arrive at the same result obtained by the map method of Problem 4-18.

SECTION 4-6

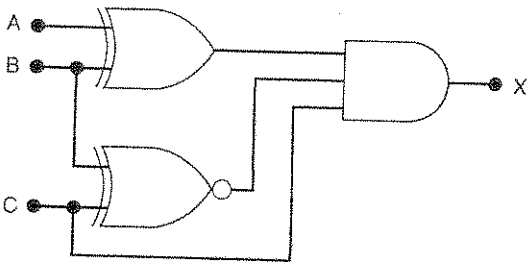
B 4-20. (a) Determine the output waveform for the circuit of Figure 4-67.
(b) Repeat with the *B* input held LOW.
(c) Repeat with *B* held HIGH.

FIGURE 4-67 Problem 4-20.



B 4-21. Determine the input conditions needed to produce $x = 1$ in Figure 4-68.

FIGURE 4-68 Problem 4-21.



B 4-22. A 7486 chip contains four XOR gates. Show how to make an XNOR gate using only a 7486 chip. *Hint:* See Example 4-16.

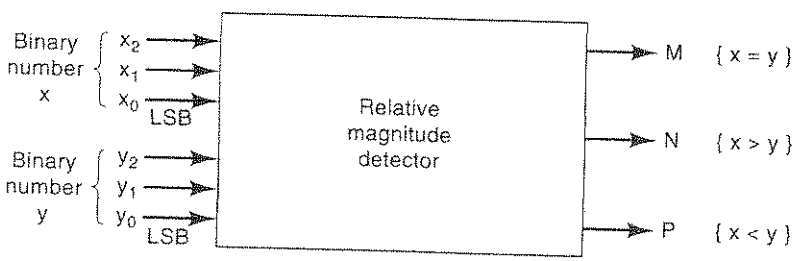
B 4-23. Modify the circuit of Figure 4-23 to compare two 4-bit numbers and produce a HIGH output when the two numbers match exactly.

C 4-24. Figure 4-69 represents a *relative-magnitude detector* that takes two three-bit binary numbers, $x_2x_1x_0$ and $y_2y_1y_0$, and determines whether they are equal and, if not, which one is larger. There are three outputs, defined as follows:

1. $M = 1$ only if the two input numbers are equal.
2. $N = 1$ only if $x_2x_1x_0$ is greater than $y_2y_1y_0$.
3. $P = 1$ only if $y_2y_1y_0$ is greater than $x_2x_1x_0$.

Design the logic circuitry for this detector. The circuit has *six* inputs and *three* outputs and is therefore much too complex to handle using the truth-table approach. Refer to Example 4-17 as a hint about how you might start to solve this problem.

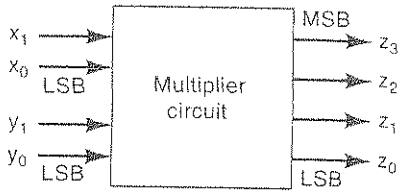
FIGURE 4-69 Problem 4-24.



MORE DESIGN PROBLEMS

C, D 4-25. Figure 4-70 represents a multiplier circuit that takes two-bit bi numbers, x_1x_0 and y_1y_0, and produces an output binary number z_3z_2 that is equal to the arithmetic product of the two input numbers. sign the logic circuit for the multiplier. (*Hint:* The logic circuit have four inputs and four outputs.)

FIGURE 4-70 Problem 4-25.



D 4-26. A BCD code is being transmitted to a remote receiver. The bits are A_2, A_1, and A_0, with A_3 as the MSB. The receiver circuitry include *BCD error detector* circuit that examines the received code to see i is a legal BCD code (i.e., ≤1001). Design this circuit to produce a HIG for any error condition.

D 4-27. Design a logic circuit whose output is HIGH whenever A and B a both HIGH as long as C and D are either both LOW or both HIGH. to do this without using a truth table. Then check your result by co structing a truth table from your circuit to see if it agrees with t problem statement.

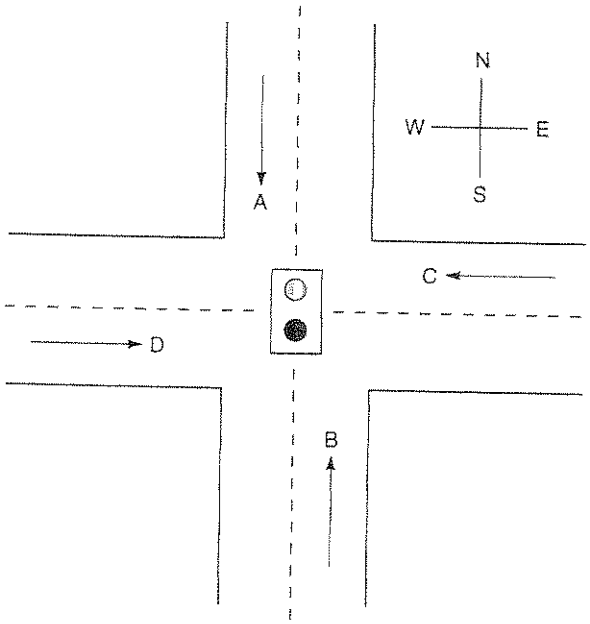
D 4-28. Four large tanks at a chemical plant contain different liquids bei heated. Liquid-level sensors are being used to detect whenever t level in tank A or tank B rises above a predetermined level. Tempe ture sensors in tanks C and D detect when the temperature in eith of these tanks drops below a prescribed temperature limit. Assum that the liquid-level sensor outputs A and B are LOW when the lev is satisfactory and HIGH when the level is too high. Also, t temperature-sensor outputs C and D are LOW when the temperatu is satisfactory and HIGH when the temperature is too low. Design logic circuit that will detect whenever the level in tank A or tank B too high at the same time that the temperature in either tank C or ta D is too low.

C, D 4-29. Figure 4-71 shows the intersection of a main highway with a secon ary access road. Vehicle-detection sensors are placed along lanes and D (main road) and lanes A and B (access road). These sensor o puts are LOW (0) when no vehicle is present and HIGH (1) when a v hicle is present. The intersection traffic light is to be controlle according to the following logic:

1. The east-west (E-W) traffic light will be green whenever bo lanes C and D are occupied.
2. The E-W light will be green whenever *either* C or D is occupied bu lanes A and B are not *both* occupied.
3. The north-south (N-S) light will be green whenever *both* lanes and B are occupied but C and D are not *both* occupied.
4. The N-S light will also be green when *either* A or B is occupie while C and D are *both* vacant.
5. The E-W light will be green when *no* vehicles are present.

Using the sensor outputs *A*, *B*, *C*, and *D* as inputs, design a logic circuit to control the traffic light. There should be two outputs, N-S and E-W, that go HIGH when the corresponding light is to be *green*. Simplify the circuit as much as possible and show *all* steps.

FIGURE 4-71 Problem 4-29.



SECTION 4-7

D 4-30. Redesign the parity generator and checker of Figure 4-25 to operate using odd parity. (*Hint:* What is the relationship between an odd-parity bit and an even-parity bit for the same set of data bits?)

D 4-31. Redesign the parity generator and checker of Figure 4-25 to operate on eight data bits.

SECTION 4-8

B 4-32. (a) Under what conditions will an OR gate allow a logic signal to pass through to its output unchanged?

(b) Repeat (a) for an AND gate.

(c) Repeat for a NAND gate.

(d) Repeat for a NOR gate.

B 4-33. (a) Can an INVERTER be used as an enable/disable circuit? Explain.

(b) Can an XOR gate be used as an enable/disable circuit? Explain.

D 4-34. Design a logic circuit that will allow input signal *A* to pass through to the output only when control input *B* is LOW while control input *C* is HIGH; otherwise, the output is LOW.

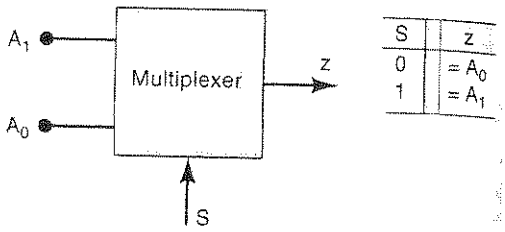
D 4-35. Design a circuit that will *disable* the passage of an input signal only when control inputs *B*, *C*, and *D* are all HIGH; the output is to be HIGH in the disabled condition.

D 4-36. Design a logic circuit that controls the passage of a signal A acco to the following requirements:

1. Output X will equal A when control inputs B and C are the sa
2. X will remain HIGH when B and C are different.

D 4-37. Design a logic circuit that has two signal inputs, A_1 and A_0, and a c trol input S so that it functions according to the requirements give Figure 4-72. (This type of circuit is called a *multiplexer* and will covered in Chapter 9.)

FIGURE 4-72 Problem 4-37.



D 4-38. Use K mapping to design a circuit to meet the requirements of Exa ple 4-17. Compare this circuit with the solution in Figure 4-23. T points out that the K-map method cannot take advantage of the X and XNOR gate logic. The designer must be able to determine wh these gates are applicable.

SECTIONS 4-9 TO 4-13

T* 4-39. (a) A technician testing a logic circuit sees that the output of a pa ticular INVERTER is stuck LOW while its input is pulsing. List many possible reasons as you can for this faulty operation.

(b) Repeat part (a) for the case where the INVERTER output is stu at an indeterminate logic level.

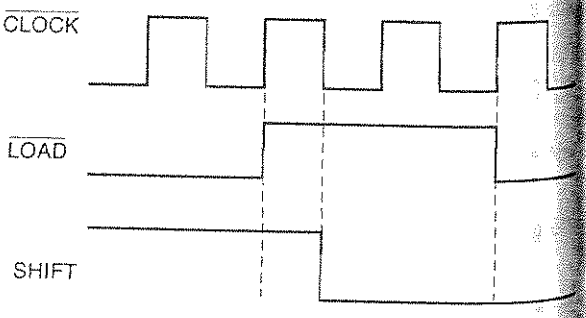
T 4-40. The signals shown in Figure 4-73 are applied to the inputs of the circu of Figure 4-32. Suppose that there is an internal open circuit at Z1-4

(a) What will a logic probe indicate at Z1-4?

(b) What dc voltage reading would you expect a VOM to register at Z 4? (Remember that the ICs are TTL.)

(c) Sketch what you think the $\overline{CLKOUT}$ and $\overline{SHIFTOUT}$ signals wo look like.

FIGURE 4-73 Problem 4-40.



*Recall that T indicates a troubleshooting exercise.

(d) Instead of the open at Z1-4, suppose that pins 9 and 10 of Z2 are internally shorted. Sketch the probable signals at Z2-10, $\overline{CLOCKOUT}$, and $\overline{SHIFTOUT}$.

T 4-41. Assume that the ICs in Figure 4-32 are CMOS. Describe how the circuit operation would be affected by an open circuit in the conductor connecting Z2-2 and Z2-10.

T 4-42. In Example 4-24, we listed three possible faults for the situation of Figure 4-36. What procedure would you follow to determine which of the faults is the actual one?

T 4-43. Refer to the circuit of Figure 4-38. Assume that the devices are CMOS. Also assume that the logic probe indication at Z2-3 is "indeterminate" rather than "pulsing." List the possible faults, and write a procedure to follow to determine the actual fault.

T 4-44. Refer to the logic circuit of Figure 4-41. Recall that output Y is supposed to be HIGH for either of the following conditions:

1. $A = 1, B = 0$, regardless of C
2. $A = 0, B = 1, C = 1$

When testing the circuit, the technician observes that Y goes HIGH only for the first condition but stays LOW for all other input conditions. Consider the following list of possible faults. For each one, write yes or no to indicate whether or not it could be the actual fault. Explain your reasoning for each no response.

(a) An internal short to ground at Z2-13

(b) An open circuit in the connection to Z2-13

(c) An internal short to V_{CC} at Z2-11

(d) An open circuit in the V_{CC} connection to Z2

(e) An internal open circuit at Z2-9

(f) An open in the connection from Z2-11 to Z2-9

(g) A solder bridge between pins 6 and 7 of Z2

T 4-45. Develop a procedure for isolating the fault that is causing the malfunction described in Problem 4-44.

T 4-46. Assume that the gates in Figure 4-41 are all CMOS. When the technician tests the circuit, he finds that it operates correctly except for the following conditions:

1. $A = 1, B = 0, C = 0$
2. $A = 0, B = 1, C = 1$

For these conditions, the logic probe indicates indeterminate levels at Z2-6, Z2-11, and Z2-8. What do you think is the probable fault in the circuit? Explain your reasoning.

T 4-47. Figure 4-74 is a combinational logic circuit that operates an alarm in a car whenever the driver and/or passenger seats are occupied and the seatbelts are not fastened when the car is started. The active-HIGH signals *DRIV* and *PASS* indicate the presence of the driver and passenger, respectively, and are taken from pressure-actuated switches in the seats. The signal *IGN* is active-HIGH when the ignition switch is on. The signal $\overline{BELTD}$ is active-LOW and indicates that the driver's seatbelt is *unfastened*; $\overline{BELTP}$ is the corresponding signal for the passenger seatbelt. The alarm will be activated (LOW) whenever the car is started and either of the front seats is occupied and its seatbelt is not fastened.

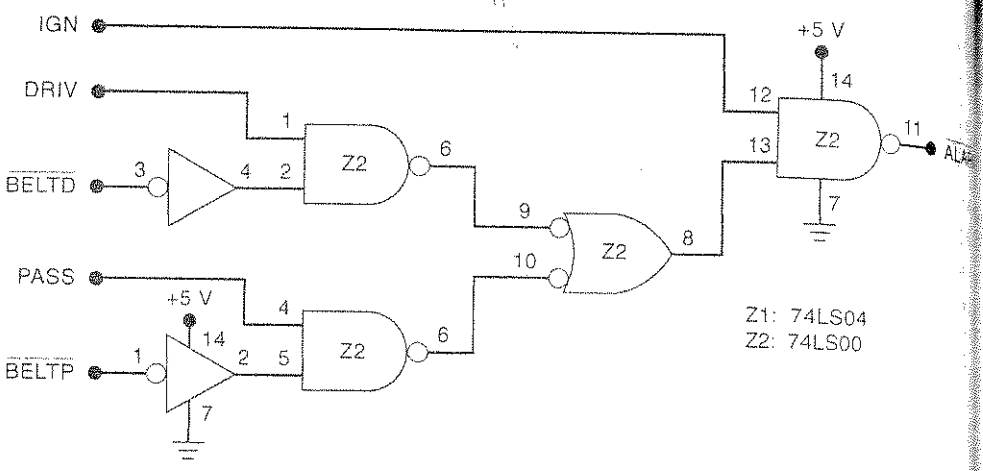


FIGURE 4-74 Problems 4-47, 4-48, and 4-49.

(a) Verify that the circuit will function as described.

(b) Describe how this alarm system would operate if Z1-2 were internally shorted to ground.

(c) Describe how it would operate if there were an open connection from Z2-6 to Z2-10.

T 4-48. Suppose that the system of Figure 4-74 is functioning so that the alarm is activated as soon as the driver and/or passenger are seated and the car is started, regardless of the status of the seatbelts. What are the possible faults? What procedure would you follow to find the actual fault?

T 4-49. Suppose that the alarm system of Figure 4-74 is operating so that the alarm goes on continuously as soon as the car is started, regardless of the state of the other inputs. List the possible faults and write a procedure to isolate the fault.

DRILL QUESTIONS ON PLDs (50 THROUGH 55)

4-50. *True or false*

(a) Top-down design begins with an overall description of the entire system and it specifications.

(b) A JEDEC file can be used as the input file for a programmer.

(c) If an input file compiles with no errors, it means the PLD circuit will work correctly.

(d) A compiler can interpret code in spite of syntax errors.

(e) Test vectors are used to simulate and test a device.

H, B 4-51. What are the % characters used for in the AHDL design file?

H, B 4-52. How are comments indicated in a VHDL design file?

B 4-53. What is a ZIF socket?

B 4-54. Name three entry modes used to input a circuit description into PLD development software.

B 4-55. What do JEDEC and HDL stand for?

ANSWERS TO SECTION REVIEW QUESTIONS

SECTION 4-1

1. Only (a) 2. Only (c)

SECTION 4-3

1. Expression (b) is not in sum-of-products form because of the inversion sign over both the C and D variables (i.e., the $A\overline{CD}$ term). Expression (c) is not in sum-of-products form because of the $(M + \overline{N})P$ term. 3. $x = \overline{A} + \overline{B} + \overline{C}$

SECTION 4-4

1. $x = \overline{A}\,\overline{B}\,\overline{C}D + \overline{A}\,\overline{B}C\overline{D} + \overline{A}B\overline{C}\,\overline{D}$ 2. Eight

SECTION 4-5

1. $x = AB + AC + BC$ 2. $x = A + BCD$ 3. $S = \overline{P} + QR$ 4. An input condition for which there is no specific required output condition; i.e., we are free to make it 0 or 1.

SECTION 4-6

2. A constant LOW 3. No; the available XOR gate can be used as an INVERTER by connecting one of its inputs to a constant HIGH (see Example 4-16).

SECTION 4-8

1. $x = \overline{A(B \oplus C)}$ 2. OR, NAND 3. NAND, NOR

SECTION 4-9

1. DIP 2. SSI, MSI, LSI, VLSI, ULSI, GSI 3. True 4. True 5. 40, 74AC, 74ACT series 6. 0 to 0.8 V; 2.0 to 5.0 V 7. 0 to 1.5 V; 3.5 to 5.0 V 8. As if the input were HIGH 9. Unpredictably; it may overheat and be destroyed. 10. 74HCT and 74ACT 11. They describe exactly how to interconnect the chips for laying out the circuit and troubleshooting. 12. Inputs and outputs are defined, and logical relationships are described.

SECTION 4-11

1. Open inputs or outputs; inputs or outputs shorted to V_{CC}; inputs or outputs shorted to ground; pins shorted together; internal circuit failures 2. Pins shorted together 3. For TTL, a LOW; for CMOS, indeterminate 4. Two or more outputs connected together

SECTION 4-12

1. Open signal lines; shorted signal lines; faulty power supply; output loading
2. Broken wires; poor solder connections; cracks or cuts in PC board; bent or broken IC pins; faulty IC sockets 3. ICs operating erratically or not at all 4. Logic level indeterminate

16. VHDL code can be written to describe clocked logic explicitly without ing logic primitives.
17. VHDL allows HDL files to be used as components in larger systems. P fabricated components are available in the Altera library.
18. HDL can be used to describe interconnected components in a manne much like a graphic schematic capture tool.

IMPORTANT TERMS

flip-flop
SET (states/inputs)
CLEAR (states/inputs)
RESET (states/inputs)
NAND gate latch
contact bounce
NOR gate latch
clock
positive-going transition (PGT)
negative-going transition (NGT)
clocked flip-flop
edge-triggered
control inputs
synchronous control inputs
setup time, t_S
hold time, t_H
clocked S-C flip-flop
trigger
pulse-steering circuit
edge-detector circuit
clocked J-K flip-flop
toggle mode
clocked D flip-flop
parallel data transfer
D latch
asynchronous inputs
override inputs
common-control block
propagation delay
master/slave flip-flop
sequential circuits
registers
data transfer
synchronous transfer
asynchronous (jam) transfer
serial data transfer
shift register
frequency division
binary counter
state table
state transition diagram
MOD number
Schmitt trigger
one-shot (OS)
quasi-stable state
nonretriggerable OS
retriggerable OS
astable multivibrator
555 timer
clock skew
crystal-controlled clock generator
event
logic primitive
nested
COMPONENT
PORT MAP
structural level of abstraction

PROBLEMS

SECTIONS 5-1 TO 5-3

B 5-1. Assuming that $Q = 0$ initially, apply the x and y waveforms of Figure 5-73 to the SET and CLEAR inputs of a NAND latch, and determine the Q and $\overline{Q}$ waveforms.

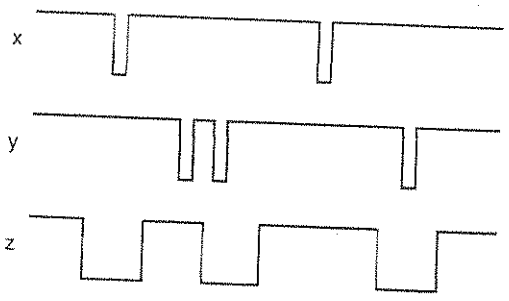
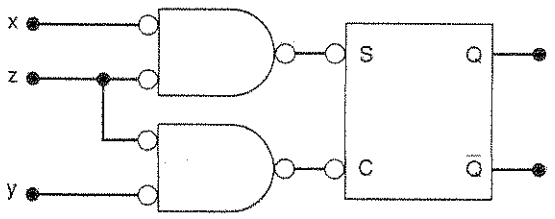


FIGURE 5-73 Problems 5-1 to 5-3.

B 5-2. Invert the x and y waveforms of Figure 5-73, apply them to the SET and CLEAR inputs of a NOR latch, and determine the Q and $\overline{Q}$ waveforms. Assume that $Q = 0$ initially.

5-3. The waveforms of Figure 5-73 are connected to the circuit of Figure 5-74. Assume that $Q = 0$ initially, and determine the Q waveform.

FIGURE 5-74 Problem 5-3.

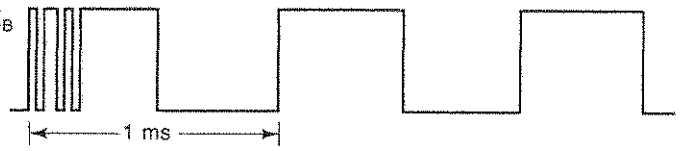


D 5-4. Modify the circuit of Figure 5-9 to use a NOR gate latch.

D 5-5. Modify the circuit of Figure 5-12 to use a NAND gate latch.

T 5-6. Refer to the circuit of Figure 5-13. A technician tests the circuit operation by observing the outputs with a storage oscilloscope while the switch is moved from A to B. When the switch is moved from A to B, the scope display of X_B appears as shown in Figure 5-75. What circuit fault could produce this result? (*Hint:* What is the function of the NAND latch?)

FIGURE 5-75 Problem 5-6.



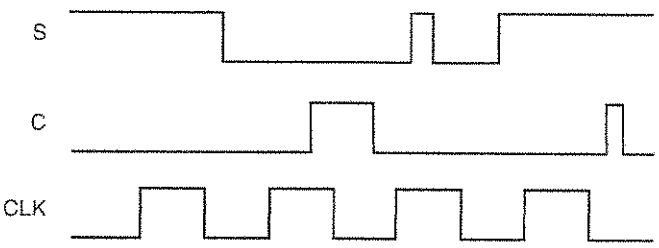
SECTIONS 5-4 AND 5-5

B 5-7. A certain clocked FF has minimum $t_S = 20$ ns and $t_H = 5$ ns. How long must the control inputs be stable prior to the active clock transition?

B 5-8. Apply the S, C, and CLK waveforms of Figure 5-17 to the FF of Figure 5-18, and determine the Q waveform.

B 5-9. Apply the waveforms of Figure 5-76 to the FF of Figure 5-17 and determine the waveform at Q. Repeat for the FF of Figure 5-18. Assume $Q = 0$ initially.

FIGURE 5-76 Problem 5-9.



SECTION 5-6

B 5-10. Apply the J, K, and CLK waveforms of Figure 5-21 to the FF of Figure 5-22. Assume that $Q = 1$ initially, and determine the Q waveform.

5-11. (a) Show how a J-K flip-flop can operate as a *toggle* FF (changes sta on each clock pulse). Then apply a 10-kHz clock signal to its C input and determine the waveform at Q.

(b) Connect Q from this FF to the *CLK* input of a second J-K FF th also has $J = K = 1$. Determine the frequency of the signal at t FF's output.

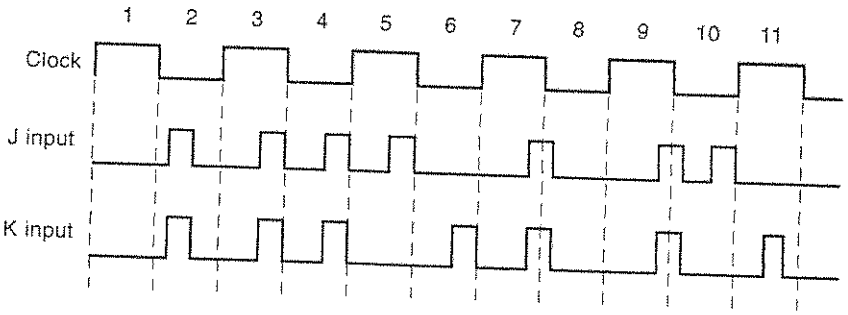
B 5-12. The waveforms shown in Figure 5-77 are to be applied to two differe FFs:

(a) positive-edge-triggered J-K

(b) negative-edge-triggered J-K

Draw the Q waveform response for each of these FFs, assuming th $Q = 0$ initially. Assume that each FF has $t_H = 0$.

FIGURE 5-77 Problem 5-12.



SECTION 5-7

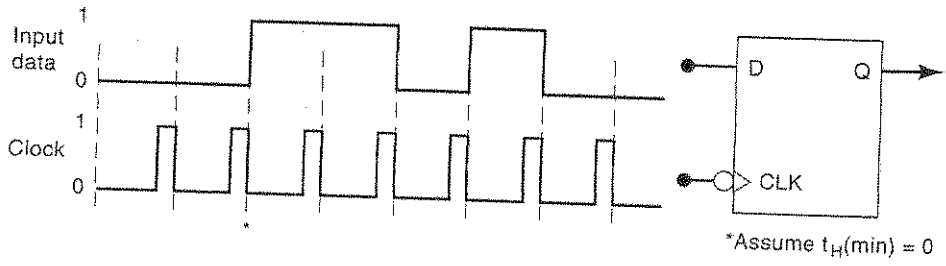
FIGU

N 5-13. A D FF is sometimes used to *delay* a binary waveform so that the bi nary information appears at the output a certain amount of time after it appears at the D input.

(a) Determine the Q waveform in Figure 5-78, and compare it with the input waveform. Note that it is delayed from the input by one clock period.

(b) How can a delay of two clock periods be obtained?

FIGURE 5-78 Problem 5-13.



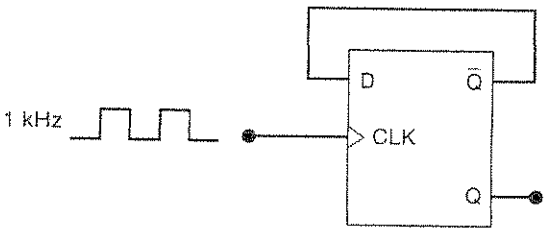
FIG

B 5-14. (a) Apply the S and *CLK* waveforms of Figure 5-76 to the D and *CLK* inputs of a D FF that triggers on PGTs. Then determine the wave form at Q.

(b) Repeat using the C waveform of Figure 5-76 for the D input.

5-15. An edge-triggered D flip-flop can be made to operate in the toggle mode by connecting it as shown in Figure 5-79. Assume that $Q = 0$ initially, and determine the Q waveform.

FIGURE 5-79 D flip-flop connected to toggle (Problems 5-15 and 5-16).



5-16. Change the circuit in Figure 5-79 so that Q is connected back to D. Then determine the Q waveform.

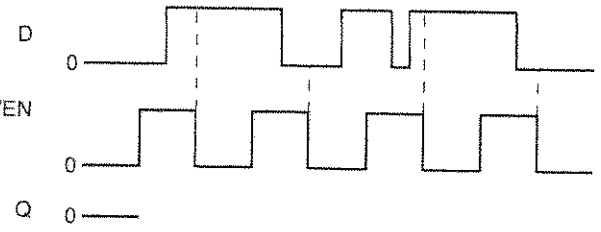
SECTION 5-8

B 5-17. (a) Apply the S and CLK waveforms of Figure 5-76 to the D and EN inputs of a D latch, respectively, and determine the waveform at Q.

(b) Repeat using the C waveform applied to D.

5-18. Compare the operation of the D latch with a negative-edge-triggered D flip-flop by applying the waveforms of Figure 5-80 to each and determining the Q waveforms.

FIGURE 5-80 Problem 5-18.

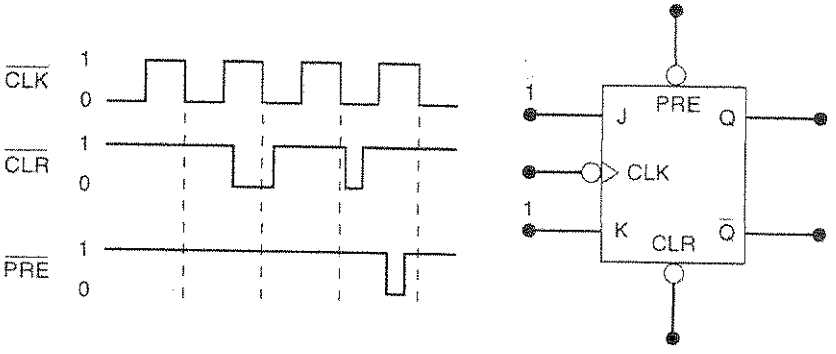


5-19. In Problem 5-15, we saw how an edge-triggered D flip-flop can be operated in the toggle mode. Explain why this same idea will not work for a D latch.

SECTION 5-9

B 5-20. Determine the Q waveform for the FF in Figure 5-81. Assume that $Q = 0$ initially, and remember that the asynchronous inputs override all other inputs.

FIGURE 5-81 Problem 5-20.



B 5-21. Apply the $\overline{CLK}$, $\overline{PRE}$, and $\overline{CLR}$ waveforms of Figure 5-30 to a positive edge-triggered D flip-flop with active-LOW asynchronous inputs. Assume that D is kept HIGH and Q is initially LOW. Determine the Q waveform.

B 5-22. Apply the waveforms of Figure 5-81 to a D flip-flop that triggers on NGTs and has active-LOW asynchronous inputs. Assume that D is kept LOW and that Q is initially HIGH. Draw the resulting Q waveform.

SECTION 5-11

5-23. Use Table 5-2 in Section 5-11 to determine the following.

(a) How long can it take for the Q output of a 74C74 to switch from 0 to 1 in response to an active CLK transition?

(b) Which FF in Table 5-2 requires its control inputs to remain stable for the longest time *after* the active CLK transition? *Before* the transition?

(c) What is the narrowest pulse that can be applied to the $\overline{PRE}$ of a 7474 FF?

5-24. Refer to the circuit of Figure 5-82. It shows a 74HC112 IC with its two J-K flip-flops connected in a certain way. Assume that initially $Q_1 = Q_2 = 1$ and, using Table 5-2, determine the *total* propagation delay between the NGT of the clock pulse and the NGT of Q_2.

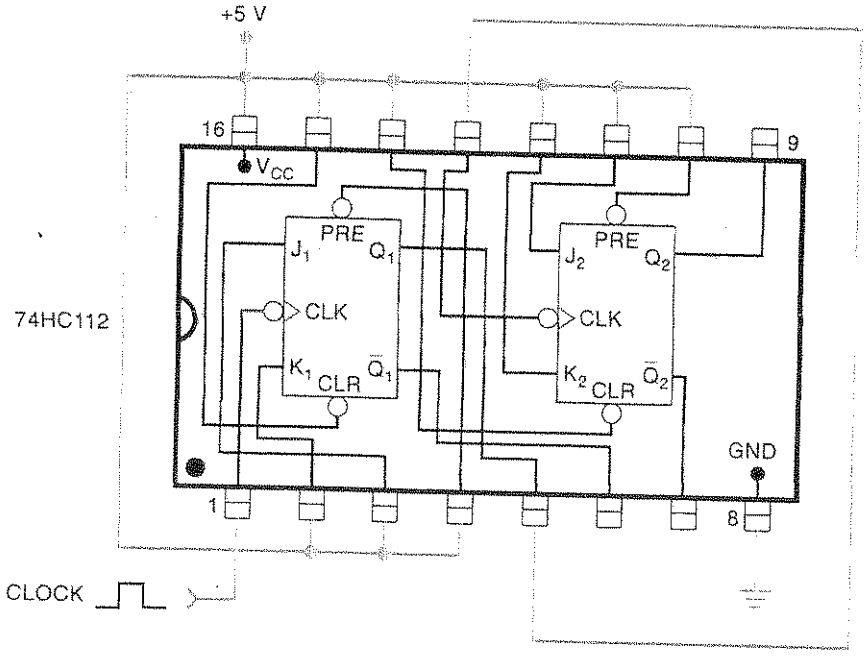


FIGURE 5-82 Connection diagram for Problem 5-24.

SECTIONS 5-15 AND 5-16

D 5-25. Modify the circuit of Figure 5-38 to use a J-K flip-flop.

D 5-26. In the circuit of Figure 5-83, inputs *A*, *B*, and *C* are all initially LOW. Output *Y* is supposed to go HIGH only when *A*, *B*, and *C* go HIGH in a certain sequence.

(a) Determine the sequence that will make *Y* go HIGH.

(b) Explain why the START pulse is needed.

(c) Modify this circuit to use D FFs.

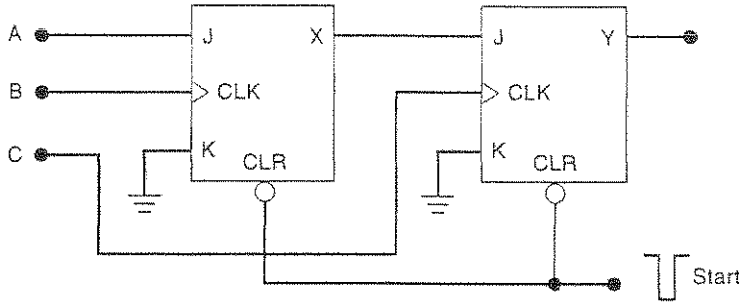


FIGURE 5-83 Problem 5-26.

SECTIONS 5-17 AND 5-18

D 5-27. (a) Draw a circuit diagram for the synchronous parallel transfer of data from one three-bit register to another using J-K flip-flops.

(b) Repeat for asynchronous parallel transfer.

5-28. A *recirculating* shift register is a shift register that keeps the binary information circulating through the register as clock pulses are applied. The shift register of Figure 5-43 can be made into a circulating register by connecting X_0 to the DATA IN line. No external inputs are used. Assume that this circulating register starts out with 1011 stored in it (i.e., $X_3 = 1$, $X_2 = 0$, $X_1 = 1$, and $X_0 = 1$). List the sequence of states that the register FFs go through as eight shift pulses are applied.

D 5-29. Refer to Figure 5-44, where a three-bit number stored in register *X* is serially shifted into register *Y*. How can the circuit be modified so that, at the end of the transfer operation, the original number stored in *X* is present in both registers? (*Hint:* See Problem 5-28.)

SECTION 5-19

B 5-30. Refer to the counter circuit of Figure 5-45 and answer the following:

(a) If the counter starts at 000, what will be the count after 13 clock pulses? After 99 pulses? After 256 pulses?

(b) If the counter starts at 100, what will be the count after 13 pulses? After 99 pulses? After 256 pulses?

(c) Connect a fourth J-K FF (X_3) to this counter and draw the state transition diagram for this 4-bit counter. If the input clock frequency is 80 MHz, what will the waveform at X_3 look like?

5-31. Refer to the binary counter of Figure 5-45. Change it by connecting $\overline{X}_0$ to the *CLK* of flip-flop X_1, and $\overline{X}_1$ to the *CLK* of flip-flop X_2. Start with all FFs in the 1 state, and draw the various FF output waveforms (X_0, X_1, X_2) for 16 input pulses. Then list the sequence of FF states as was done in Figure 5-46. This counter is called a *down counter*. Why?

5-32. Draw the state transition diagram for this down counter, and compare it with the diagram of Figure 5-47. How are they different?

B 5-33. (a) How many FFs are required to build a binary counter that co from 0 to 1023?

(b) Determine the frequency at the output of the last FF of counter for an input clock frequency of 2 MHz.

(c) What is the counter's MOD number?

(d) If the counter is initially at zero, what count will it hold after 2 pulses?

5-34. A binary counter is being pulsed by a 256-kHz clock signal. The ou frequency from the last FF is 2 kHz.

(a) Determine the MOD number.

(b) Determine the counting range.

5-35. A photodetector circuit is being used to generate a pulse each tim customer walks into a certain establishment. The pulses are fed to eight-bit counter. The counter is used to count these pulses as a me for determining how many customers have entered the store. Af closing the store, the proprietor checks the counter and finds that shows a count of $00001001_2 = 9_{10}$. He knows that this is incorrect cause there were many more than nine people in his store. Assum that the counter circuit is working properly, what could be the rea for the discrepancy?

SECTION 5-20

D 5-36. Modify the circuit of Figure 5-48 so that only the presence of addr code 10110110 will allow data to be transferred to register X.

T 5-37. Suppose that the circuit of Figure 5-48 is malfunctioning so that da are being transferred to X for either of the address codes 1111111 11111111. What are some circuit faults that could be causing this?

D 5-38. Modify the circuit of Figure 5-48 so that the MPU has eight data o put lines connected to transfer eight bits of data to an eight-bit reg ter made up of two 74HC175 ICs [Figure 5-32(b)]. Show all circ connections.

SECTION 5-22

B 5-39. Refer to the waveforms in Figure 5-51(a). Change the OS pulse dur tion to 0.5 ms and determine the Q output for both types of OS. Th repeat using a OS pulse duration of 1.5 ms.

N 5-40. Figure 5-84 shows three nonretriggerable one-shots connected i timing chain that produces three sequential output pulses. Note t "1" in front of the pulse on each OS symbol to indicate nonretrigg able operation. Draw a timing diagram showing the relationship b tween the input pulse and the three OS outputs. Assume an inp pulse duration of 10 ms.

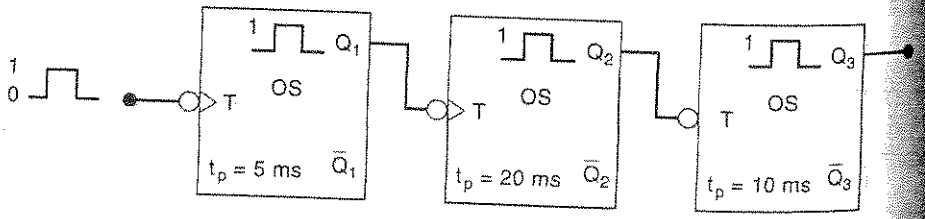


FIGURE 5-84 Problem 5-40.

5-41. A *retriggerable* OS can be used as a pulse-frequency detector that detects when the frequency of a pulse input is below a predetermined value. A simple example of this application is shown in Figure 5-85. The operation begins by momentarily closing switch SW1.

(a) Describe how the circuit responds to input frequencies above 1 kHz.

(b) Describe how the circuit responds to input frequencies below 1 kHz.

(c) How would you modify the circuit to detect when the input frequency drops below 50 kHz?

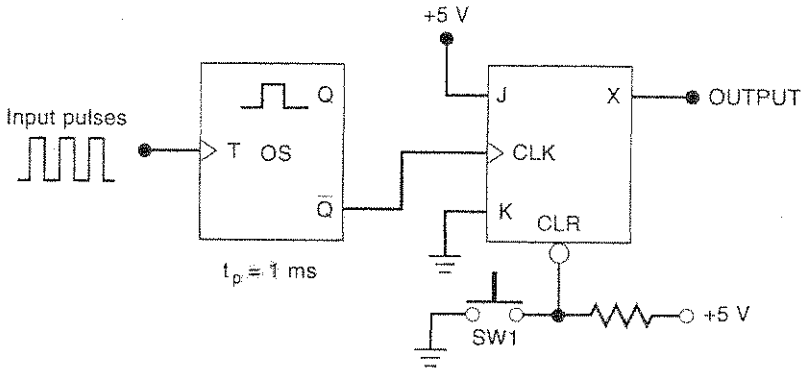


FIGURE 5-85 Problem 5-41.

5-42. Refer to the logic symbol for a 74121 nonretriggerable one-shot in Figure 5-52(a).

(a) What input conditions are necessary for the OS to be triggered by a signal at the B input?

(b) What input conditions are necessary for the OS to be triggered by a signal at the A_1 input?

C, D 5-43. The output pulse width from a 74121 OS is given by the approximate formula

$$t_p \approx 0.7\ R_T C_T$$

where R_T is the resistance connected between the R_{EXT}/C_{EXT} pin and V_{CC}, and C_T is the capacitance connected between the C_{EXT} pin and the R_{EXT}/C_{EXT} pin. The value for R_T can be varied between 2 and 40 kΩ, and C_T can be as large as 1000 μF.

(a) Show how a 74121 can be connected to produce a negative-going pulse with a 5-ms duration whenever either of two logic signals (E or F) makes a NGT. Both E and F are normally in the HIGH state.

(b) Modify the circuit so that a control input signal, G, can disable the OS output pulse, regardless of what occurs at E or F.

SECTION 5-23

C 5-44. Consider the circuit of Figure 5-86. Initially all FFs are in the 0 state. The circuit operation begins with a momentary start pulse applied to the $\overline{\text{PRESET}}$ inputs of FFs X and Y. Determine the waveforms at A, B, C, X, Y, Z, and W for 20 cycles of the clock pulses after the start pulse. State all assumptions.

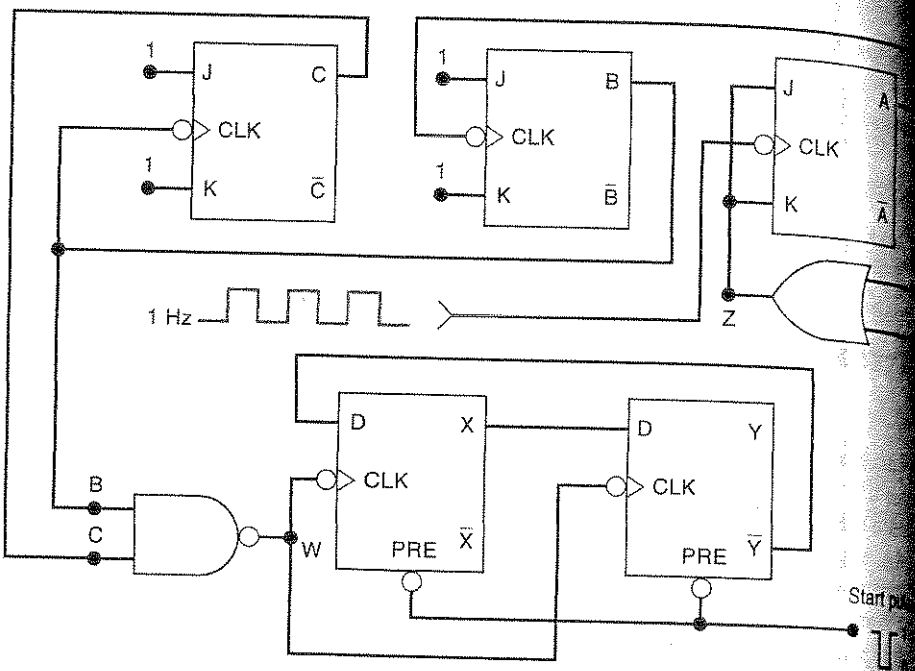


FIGURE 5-86 Problem 5-44.

SECTION 5-24

B, D 5-45. Show how to use a 74LS14 Schmitt-trigger INVERTER to produce an approximate square wave with a frequency of 10 kHz.

B, D 5-46. Design a 555 free-running oscillator to produce an approximate square wave at 40 kHz. *C* should be kept at 500 pF or greater.

D 5-47. A 555 oscillator can be combined with a J-K flip-flop to produce a perfect (50 percent duty cycle) square wave. Modify the circuit of Problem 5-46 to include a J-K flip-flop. The final output is still to be a 40-kHz square wave.

C, N 5-48. The circuit in Figure 5-87 can be used to generate two nonoverlapping clock signals at the same frequency. These clock signals are used in some microprocessor systems that require four different clock transitions to synchronize their operations.

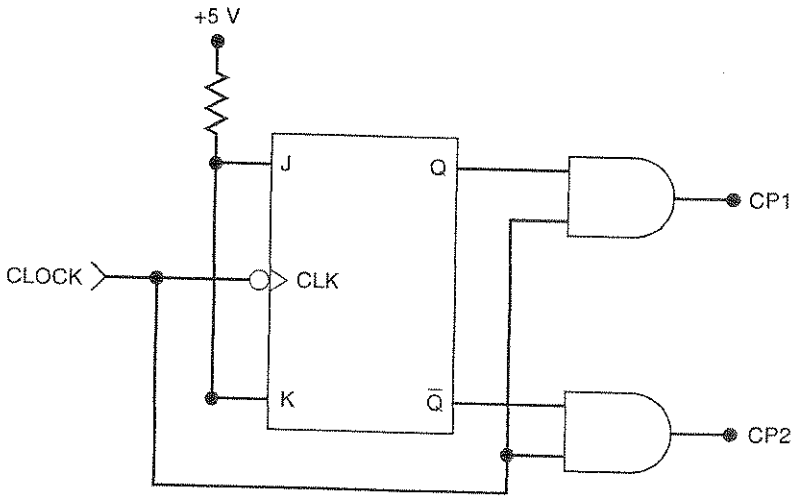


FIGURE 5-87 Problem 5-48.

(a) Draw the CP1 and CP2 timing waveforms if *CLOCK* is a 1-MHz square wave. Assume that t_{PLH} and t_{PHL} are 20 ns for the FF and 10 ns for the AND gates.

(b) This circuit would have a problem if the FF were changed to one that responds to a PGT at *CLK*. Draw the CP1 and CP2 waveforms for that situation. Pay particular attention to conditions that can produce glitches.

ANSWERS TO SECTION REVIEW QUESTIONS

SECTION 5-1

1. HIGH; LOW 2. $Q = 0, \overline{Q} = 1$ 3. True 4. Apply a momentary LOW to $\overline{\text{SET}}$ input.

SECTION 5-2

1. LOW, HIGH 2. $Q = 1$ and $\overline{Q} = 0$ 3. Make CLEAR = 1 4. $\overline{\text{SET}}$ and $\overline{\text{CLEAR}}$ would both be normally in their active-LOW state.

SECTION 5-4

1. Synchronous control inputs and clock input 2. The FF output can change only when the appropriate clock transition occurs. 3. False 4. Setup time is the required interval immediately prior to the active edge of the *CLK* signal during which the control inputs must be held stable. Hold time is the required interval immediately following the active edge of *CLK* during which the control inputs must be held stable.

SECTION 5-5

1. HIGH; LOW; HIGH 2. Because *CLK** is HIGH only for a few nanoseconds

SECTION 5-6

1. True
2. No 3. $J = 1, K = 0$

SECTION 5-7

1. *Q* will go LOW at point *a* and remain LOW. 2. False. The *D* input can change without affecting *Q* because *Q* can change only on the active *CLK* edge. 3. Yes, by converting to D FFs (Figure 5-25).

SECTION 5-8

1. In a *D* latch, the *Q* output can change while *EN* is HIGH. In a D flip-flop, the output can change only on the active edge of *CLK*. 2. False 3. True

SECTION 5-9

1. Asynchronous inputs work independently of the *CLK* input. 2. Yes, because $\overline{PRE}$ is active-LOW 3. $J = K = 1$, $\overline{PRE} = \overline{CLR} = 1$, and a PGT at *CLK*

SECTION 5-10

1. The triangle inside the rectangle indicates edge-triggered operation; the right triangle outside the rectangle indicates triggering on a NGT. 2. It is used to indicate the function of those inputs that are common to more than one circuit on the chip.

SECTION 5-11

1. t_{PLH} and t_{PHL} 2. False; the waveform must also satisfy $t_W(L)$ and $t_W(H)$ requirements.

SECTION 5-17

1. False 2. D flip-flop 3. Six 4. True

SECTION 5-18

1. True 2. Fewer interconnections between registers 3. $X_2X_1X_0 = 111$; $Y_2Y_1Y_0 = 101$ 4. Parallel

SECTION 5-19

1. 10 kHz 2. Eight 3. 256 4. 2 kHz 5. $00001000_2 = 8_{10}$

SECTION 5-21

1. The output may contain oscillations. 2. It will produce clean, fast output signals even for slow-changing input signals.

SECTION 5-22

1. $Q = 0, \overline{Q} = 1$ 2. True 3. External R and C values 4. For a retriggerable OS, each new trigger pulse begins a new t_p interval, regardless of the state of the Q output.

SECTION 5-24

1. 24 kHz 2. 109.3 kHz; 66.7 percent 3. Frequency stability