SINGAPORE POLYTECHNIC ET1004

MID-SEMESTER TEST (Sample)

SAS code: **TST1**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT/EO

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Clean Energy DCEG 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet, unless indicated otherwise.

4. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

5. This Test paper consists of 6 pages.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

1. What is the Boolean expression for the logic gate shown in figure A1?

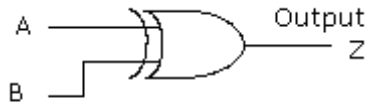


Figure A1

(a) $Z = A + B$

(b) $Z = A\,B + \overline{A}\,\overline{B}$

(c) $Z = \overline{A}\,B + A\,\overline{B}$

(d) $Z = \overline{A + B}$

2. What are positional weights of the MSB and LSB in the number 1100111_2?

(a) 2^7 for MSB and, 2^0 for LSB

(b) 2^7 for MSB and, 2^1 for LSB

(c) 2^6 for the MSB and, 2^0 for LSB

(d) 2^6 for MSB and, 2^1 for LSB

3. How many f lip-flops are required to build a counter that divides its clock frequency by 64_{10}?

(a) 3_{10} (b) 4_{10} (c) 5_{10} (d) 6_{10}

4. What will be the results at the outputs of a Full-Adder if its inputs are: augend A = 1, addend B = 1, carry-input Cin = 1 ?

(a) Sum = 1, Cout = 1

(b) Sum = 0, Cout = 1

(c) Sum = 1, Cout = 0

(d) Sum = 0, Cout = 0

5. A **100 kHz** clock signal of duty cycle of **70 %** is applied to the CLK input of a **Mod-4** ripple counter. What will be the frequency and duty cycle of the signal at its MSB output?

(a) 25 kHz , 70 % duty cycle.

(b) 25 kHz , 30 % duty cycle.

(c) 25 kHz , 50 % duty cycle.

(d) 50 kHz , 50 % duty cycle.

6. Which one of the following counters requires the **most** number of flip-flops?

(a) Decade counter
(b) Mod-22 ripple counter
(c) Mod-64 down-counter
(d) A divide by 32 asynchronous counter

7. Which configuration of shift register circuit has **many** data **inputs** and **1** data **output**?

(a) parallel-in, parallel-out shift register
(b) parallel-in, serial-out shift register
(c) serial-in, parallel-out shift register
(d) serial-in, serial-out shift register

8. How many Full Adders Units are required to build a parallel adder that can add signed binary numbers in the range from $+32767_{10}$ to -32768_{10}?

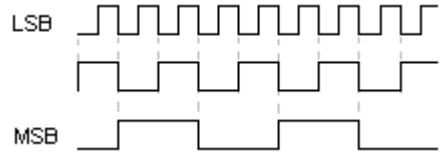
(a) 8_{10} (b) 12_{10} (c) 15_{10} (d) 16_{10}

9. What does the number $1000\ 0000_2$ represent in the 8-bit, including the sign-bit, two's complement signed number system?

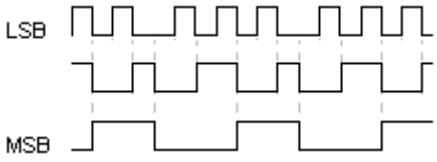
(a) Decimal 0
(b) $+127_{10}$
(c) -128_{10}
(d) Arithmetic Overflow

10. Which one of the following set of waveforms in figure A10 corresponds to the output waveforms of a **Mod 5** binary counter?

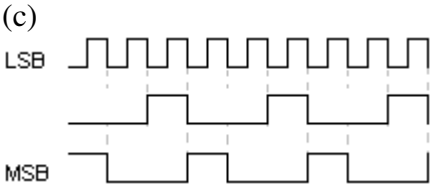
(a)



(b)



(c)



(d)

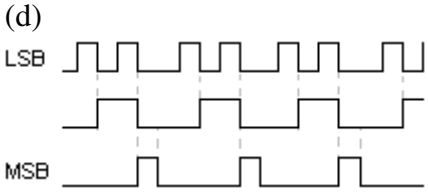


Figure A10

Section B (45 marks)

B1. This question consists of several parts that involve numerical calculations and/or number conversions.

(a) Determine the **range** of unsigned **decimal** values that can be represented by the following systems?

(i) 16-bit binary numbering system.

(ii) 6-digit decimal numbering system

(4 marks)

(b) Perform the following operation using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit. All steps and **workings must be shown** or marks will be deducted.

(i) Add $+65_{10}$ to $+23_{10}$ (5 marks)

(ii) Subtract $+26_{10}$ from -73_{10} (6 marks)

B2 The 74283 (see figure B2) is a 4-bit parallel adder IC.

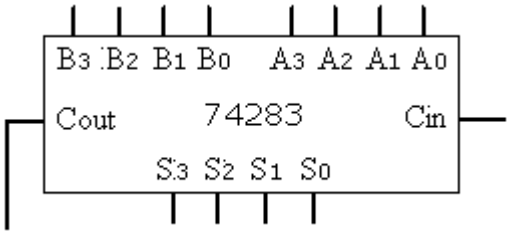


Figure B2

(a) Why is it described as a 4-bit parallel adder? If this 4-bit adder is to be constructed using the Full Adder unit, how many full-adder units are required for the 4-bit Adder? Using the correct number of Full Adders, draw the equivalent functional circuit of this 4-bit Parallel Adder.

(7 marks)

(b) An 8-bit parallel adder is to be constructed using the 74283 IC. How many of these 74283 ICs are required to construct this adder circuit?

(3 marks)

(c) Draw the circuit of this 8-bit Parallel Adder using the 74283 ICs. In your diagram, label the A inputs as A_7 to A_0 and B inputs as B_7 to B_0 and the sum outputs as S_7 to S_0, where the subscript of 7 indicates the MSB and subscript of 0 indicates the LSB.

(5 marks)

B3 An Asynchronous counter has a state transition diagram as shown in Figure B3.1.

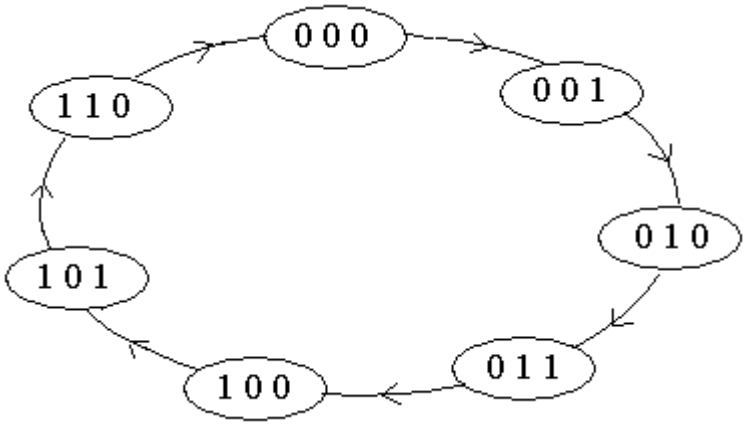


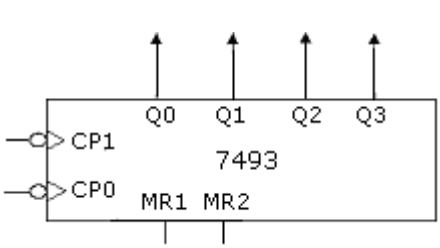
Figure B3.1

(a) From the state transition diagram, determine the modulus (mod-number) of this counter**.**

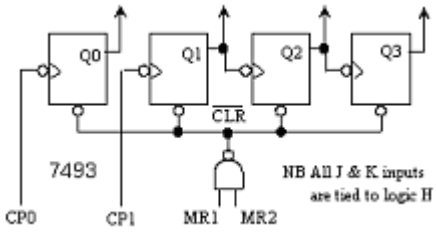
(4 marks)

(b) Using the 7493 Counter IC and any other logic gate(s) as necessary, design the counter of Figure B3.1. In your solution, which must be entered in your answer booklet, use the logic symbol of the 7493 as given in Figure B3.2. Ensure that you label all inputs and outputs clearly or marks will be deducted.

(7 marks)



Logic symbol of 7493



Internal Circuit of 7493

Figure B3.2

(c) If the signal frequency at the MSB output of the counter in part (b) is 10 kHz, what is the frequency of the signal applied at its CLK (clock) input?

(4 marks)

Section C (25 marks)

C1. For the circuit shown in figure C1.1, determine the following:

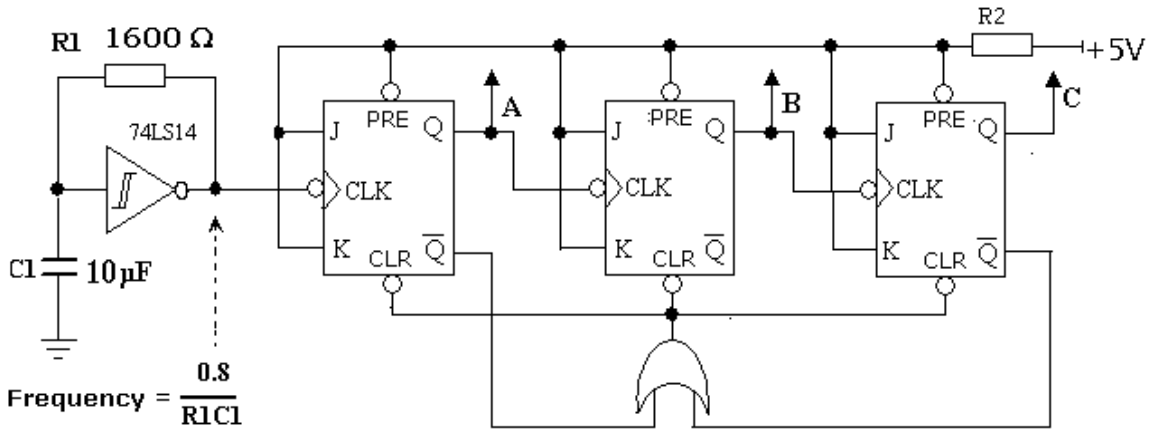


Figure C1.1

(a) Identify the circuit connected to the CLK (clock) input of the 3-bit counter circuit and hence calculate this CLK signal frequency.

(6 marks)

(b) Analyze the counter circuit and determine its modulus (i.e. mod-number)

(6 marks)

(a) Calculate the duty cycle and frequency of the signal at the MSB output of the counter.

(7 marks)

(d) Using the 7493 counter IC, re-design the counter of Figure C1.1. In your solution, which must be entered in your answer booklet, use the logic symbol of the 7493 as given in Figure C1.2. Ensure that you label all inputs and outputs clearly or marks will be deducted.

(6 marks)

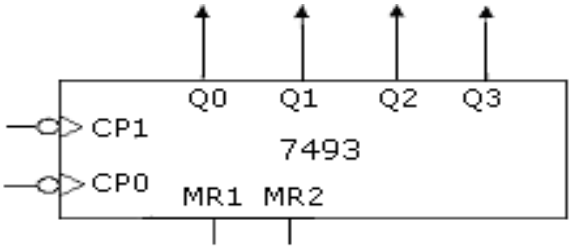


Figure C1.2

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