CHAPTER 1 Introduction to FPGA

OBJECTIVES:

The learning outcome is that student is able to:

- *understand the basic architectures of FPGA,*

1 Introduction

Field Programmable Gate Arrays (FPGAs) are programmable logic devices (PLDs) that support implementation of large logic circuits. FPGAs are quite different from simple PLDs and Complex Programmable Logic Devices (CPLDs) because FPGAs do not contain AND or OR planes. Instead, FPGAs provide *logic blocks* for implementation of the required functions.

2 Basic Architecture

The general structure of an FPGA is illustrated in Figure 1. It contains three main types of resources: logic blocks, I/O blocks for connecting to the pins of the package, and interconnection wires and programmable switches.

The logic blocks are arranged in a two-dimensional array, and the interconnection wires are organized as horizontal and vertical *routing channels* between rows and columns of logic blocks. The routing channels contain wires and programmable switches that allow the logic blocks to be interconnected in many ways. The connect block in Figure 1 connect the logic block input and output terminals to the interconnection wires, and the switch boxes that are diagonally between logic blocks connect one interconnection wire to another (such as a vertical wire to a horizontal wire). Programmable connections also exist between the I/O blocks and the interconnection wires. The actual number of programmable switches and wires in an FPGA varies in commercially available chips.

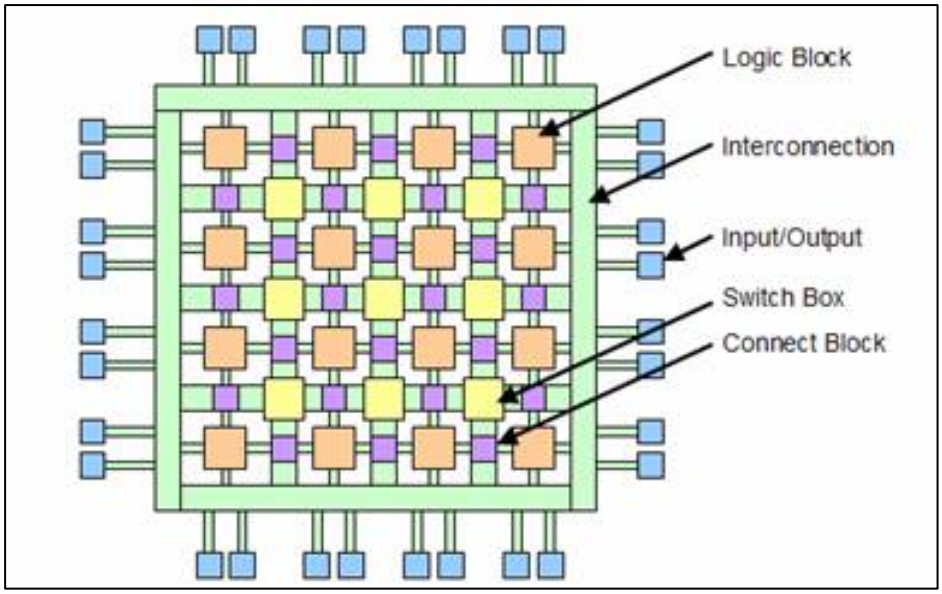

Figure 1. General structure of an FPGA.

Figure 2 shows a logic block from Xilinx called the Configurable Logic Block (CLB). The block contains RAM storage cells for creating arbitrary combinatorial logic functions, also known as lookup tables (LUTs). It also contains flip-flops for clocked storage elements, along with multiplexers in order to route the logic within the block and to and from external resources. The multiplexers also allow polarity selection and reset and clear input selection. Figure 3 shows how to create any combinational logic function by programming the inputs with the correct data in the RAM storage cells.

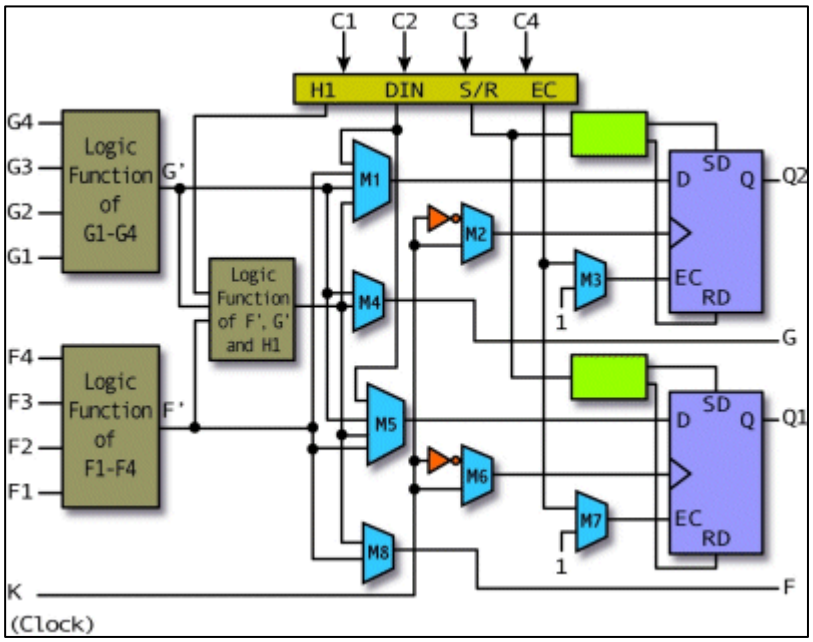

Figure 2. Xilinx FPGA Configurable Logic Block

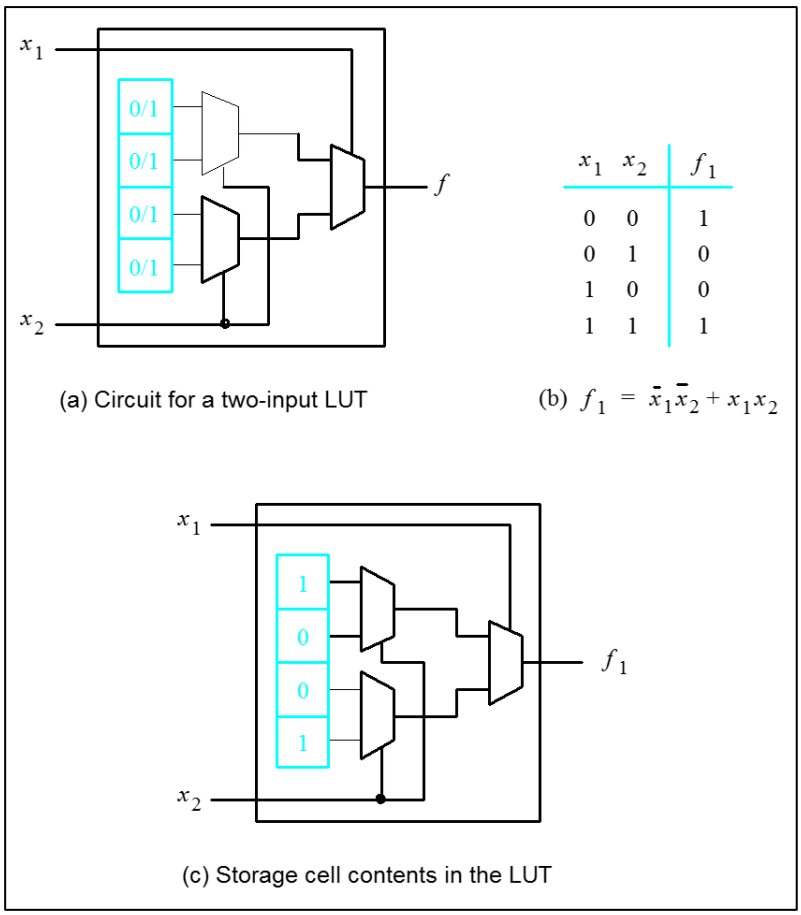

Figure 3. LUT of a CLB.

Figure 4 shows a simple I/O block. The I/O pin can be programmable to be input, output or bidirectional pin. Modern I/O blocks have features that can improve timing and allows programmable i/o voltage and current levels.

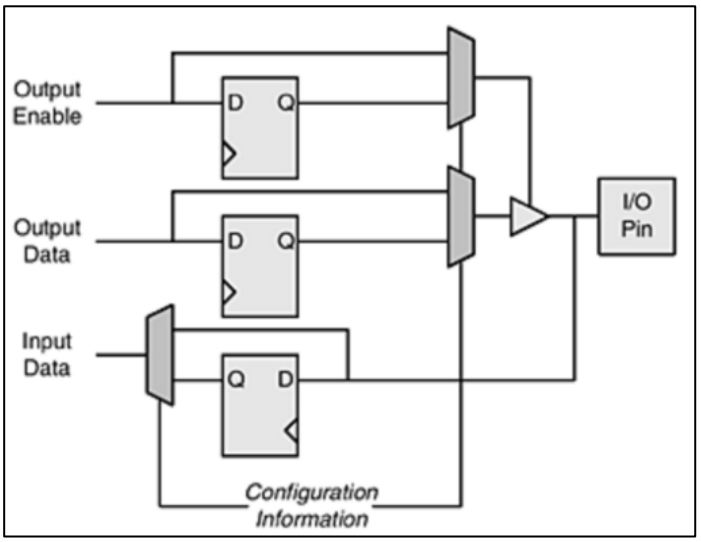

Figure 4. FPGA Configurable I/O Block