A1. Refer to Figure A1, what is the clock frequency at the CLK input to Flip-Flop (F/F) A if the frequency of CLK signal at F/F H is 220 Hz and the counter is a naturally resetting type?

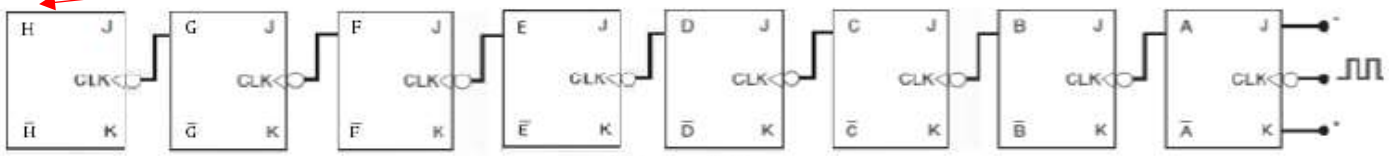


Figure A1

All J and K inputs are tied to Vcc and PRESET inputs are disabled.

(a) 14.08 kHz
(b) 28.16 kHz
(c) 56.32 kHz
(d) 112.64 kHz

8 flip-flops: 2^8 → Mod-256

f_{CLK} = Mod x f_{MSB} = 256 x 220 Hz = 28,160 Hz

Answer: (b)

A2. Refer to Figure A2, what is the new Modulus (Mod-number) that can be attained by the counter of Figure A1 if both of the F/F outputs, H and D, are connected to a two-input NAND gate which output is used to activate all the F/F active-low asynchronous CLEAR (CLR) inputs of the counter?

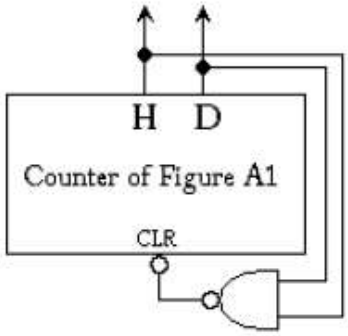


Figure A2

(a) Mod-120
(b) Mod-128
(c) Mod-136
(d) Mod-256

Outputs: HGFE DCBA
Reset at: 1000 1000 = 136 in decimal

Hence, it is a Mod-136 counter.

Answer: (c)

A3. A shift register circuit with **one** data input and **one** data output is a _____.

(a) serial-in, serial-out shift register
(b) parallel-in, serial-out shift register
(c) serial-in, parallel-out shift register
(d) parallel-in, parallel-out shift register

Answer: (a)

A4. In the 8-bits two's complement system, what does $1001\ 1001_2$ convert to in decimal?

(a) -25_{10}
(b) -101_{10}
(c) -103_{10}
(d) -153_{10}

Indicates negative

Let: 1001 1001 = -X
Invert: 0110 0110
+1: 0110 0111 = +X = +103 in decimal

Hence, -X = -103

Answer: (c)

A5. A parallel adder which can add signed binary numbers using the 2's complements signed numbering system has a range from -32768_{10} to $+32767_{10}$, is to be constructed using the 74LS83 IC, a 4-bit parallel adder IC. How many of these 74LS83 ICs are required to build this parallel adder circuit?

(a) 1
(b) 2
(c) 3
(d) 4

The range has 65,536 = 2^{16} numbers.
Hence, it has 16 bits.
Since each IC can add 4-bit, it requires four ICs.

Answer: (d)

A6. The Figure A6 illustrates the current flow conditions between two logic gates. The current flowing at gate-2 I_B is best described by the symbol _____.

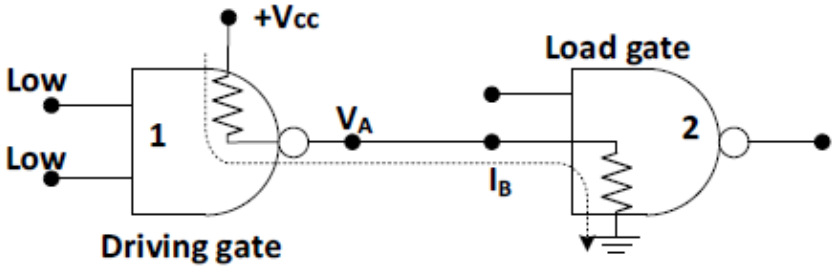


Figure A6

(a) I_{IL}
(b) I_{IH}
(c) I_{OL}
(d) I_{OH}

I_{OH} is the current that the output is able to support when outputting HIGH.

I_{IH} is the current required by the input when driven by a logic '1' signal (HIGH).

Answer: (b)

A7. A common means for comparing and measuring the performance of IC family is the _____.

(a) power consumption
(b) propagation delays
(c) speed-power product
(d) noise immunity

An ideal IC has zero power consumption and zero propagation delay.

ICs which have lower t_P x P_D are considered to be better in performance.

Answer: (c)

Also known as: Delay-Power Product

A8. What is the maximum possible number of data inputs for a multiplexer with 4 select inputs?

(a) 4 inputs
(b) 16 inputs
(c) 32 inputs
(d) 64 inputs

With 4 select inputs, it can select up to $2^4 = 16$ data inputs.

Answer: (b)

A9. A 7442 BCD decoder is connected as shown in Figure A9. Which one of its outputs has a level of low(0) if the select inputs of DCBA are 1010?

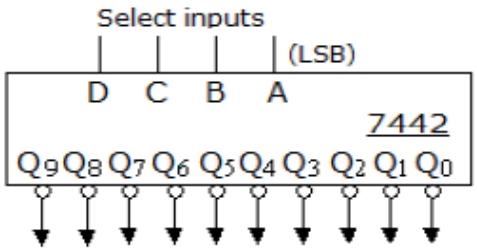


Figure A9

(a) Q_0
(b) Q_7
(c) Q_9
(d) none

When DCBA = 1010 (10 in decimal) output Q_{10} would be active ('0') but this decoder does not have Q_{10}.

Answer: (d)

A10. Which one of the following digital devices can be used to implement any logic function?

(a) Multiplexer
(b) Demultiplexer
(c) Encoder
(d) Decoder

A multiplexer with N select inputs can implement any truth table (logic function) with N inputs.

P.S. - a decoder with N select inputs plus an extra logic gate can also implement any N inputs truth table. (It needs a NAND gate if it has active-low outputs. It needs an OR gate if it has active-high outputs.)

Answer: (a)

B1.(a) Determine the range, and the number of different values (in decimal) for the two following numbering systems. (6 marks)

This system is hardly being use in practice.

(i) 18 bit (including sign bit) signed magnitude signed numbering system

Background:
In signed-magnitude system, it uses the left-most bit to indicate + or –, while the other bits to represent magnitude. The magnitude is represented in the same way for both + and – numbers.

For example, in 3-bit signed-magnitude system:
000 = +0, 001 = +1, 010 = +2, 011 = +3 while 100 = -0, 101 = -1, 110 = -2, 111 = -3.
*(Note that **there are two representations for zero**.)*

Answer:
In 18-bit signed-magnitude system, the range is: ***-N to +N; where N = $2^{17} - 1$.***
There are a total of ***= $2^{18} - 1$*** *numbers.*

(ii) 18 bit (including sign bit) 2's complement signed numbering system

Answer:
In 18-bit 2's complement system, the range is: ***-N to +N-1; where N = 2^{17}.***
There are a total of ***= 2^{18}*** *numbers.*

(b) Use the 8 bits (including the sign bit) 2's complement system to perform the following addition:

Add -68_{10} to $+39_{10}$ (4 marks)

	sign	64	32	16	8	4	2	1
+68 =	0	1	0	0	0	1	0	0

Invert all bits, then plus 1:

-68 =	1	0	1	1	1	1	0	0
+39 =	0	0	1	0	0	1	1	1
-29 =	1	1	1	0	0	0	1	1

B2. The 74LS283 as shown in Figure B2 is a 4-bit parallel adder IC, i.e., a device that adds two sets of 4-bit numbers simultaneously.

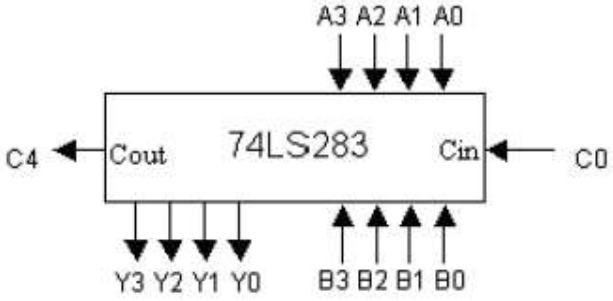


Figure B2

(a) If A3 A2 A1 A0 =1 0 1 1 and B3 B2 B1 B0 = 1 1 0 1, what will be the binary value of the outputs C4, Y3 Y2 Y1 Y0 if C0 = 1? (3 marks)

A3 A2 A1 A0 = 1 0 1 1
B3 B2 B1 B0 = 1 1 0 1
C0 = 1
1 1 0 0 1

Cout Y3 Y2 Y1 Y0

(b) How many magnitude bits (without counting the signed bit) are there in a parallel Adder that is built with ten (10) pieces of 74LS283 ICs for 2's complement numbering system addition? (2 marks)

Each 74LC283 has 4 bits and ten of them have 40 bits in total.

With the left-most bit being the sign bit, there are 39 magnitude bits.

(c) Express the following numbers in BCD format and hence, perform the addition of the numbers using BCD arithmetic. (5 marks)

Add $+81_{10}$ to $+29_{10}$

+ 81 = 0 0 0 0 1 0 0 0 0 0 0 1
+ 29 = 0 0 0 0 0 0 1 0 1 0 0 1
= 0 0 0 0 1 0 1 0 1 0 1 0
= 1 1 0 1 1 0
+110 = 0 0 01 0 0 0 1 0 0 0 0 (BCD)

The sum of this 4-bit is above 9

Add 6 to compensate

B3. Each one of the following five statements comprising this question describes MSI devices, namely: **Encoder**, **Decoder**, **Multiplexer** and **De-multiplexer**. You are required to state in your answer booklet, the type of MSI device(s) being described by each statement. Ensure that your answers are labelled exactly according to each of the statements, i.e. [(a), (b)....(e)] or marks will not be awarded. (10 marks)

(a) This device converts a decimal key input to binary code.

Encoder (usually priority encoder)

(b) A logic circuit that has a single output with 16 data inputs and 4 select input lines.

Multiplexer (16 to 1)

(c) It has a single input which can be switched to one of the 8 outputs and it is also known to be a data distributor.

De-multiplexer (1 to 8)

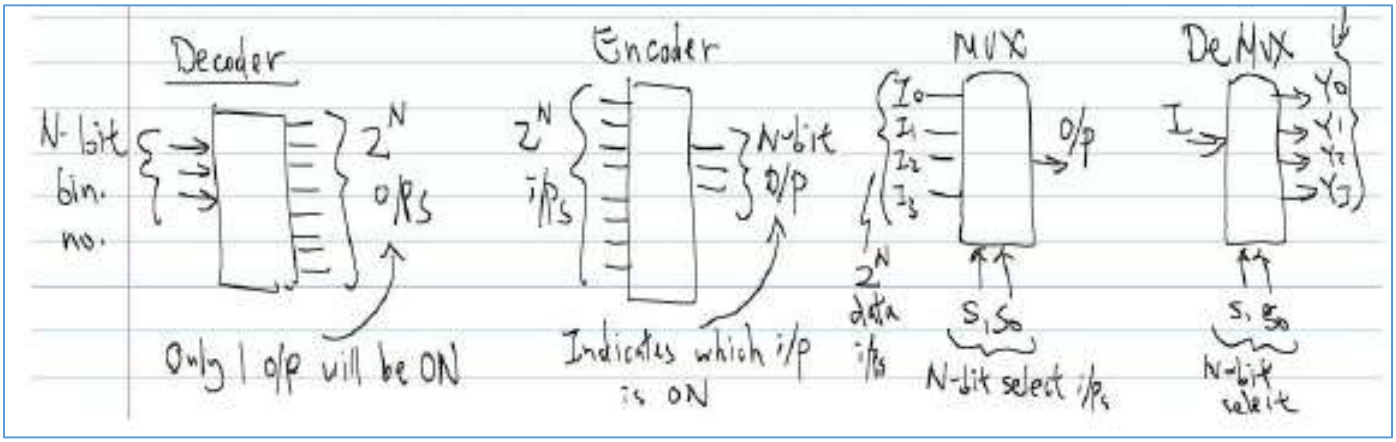
(d) This logic circuit is using a 4 binary input code to activate one of the 16 output lines.

Decoder (4 to 16 binary decoder)

(e) This device can be used for handling numbered key buttons and determines the BCD code generated.

BCD (i.e. 4-bit) priority encoder

From tutorial:



B4. Figure B4 shows a Three-line-to-Eight-line decoder.

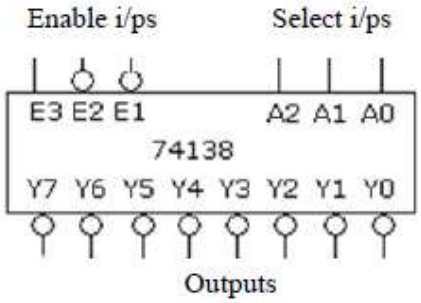


Figure B4

(a) Briefly describe what a Three-line-to-Eight-line decoder is. (2 marks)

The binary number at its 3-bit input will determine which of its 8 outputs will be active (i.e. turned on).

(b) What should the logic levels to apply to the inputs, E3, E2 and E1, to enable the device? (2 marks)

Apply '1' to the active-high input E3 and '0' to the active-low inputs E2 & E1. (E3, E2, E1 = 1, 0, 0 respectively.)

(c) If the data at the inputs, A2 A1 A0 is 101_2 when the decoder is enabled, what will be the output logic states at each output Y_0 to Y_7? (2 marks)

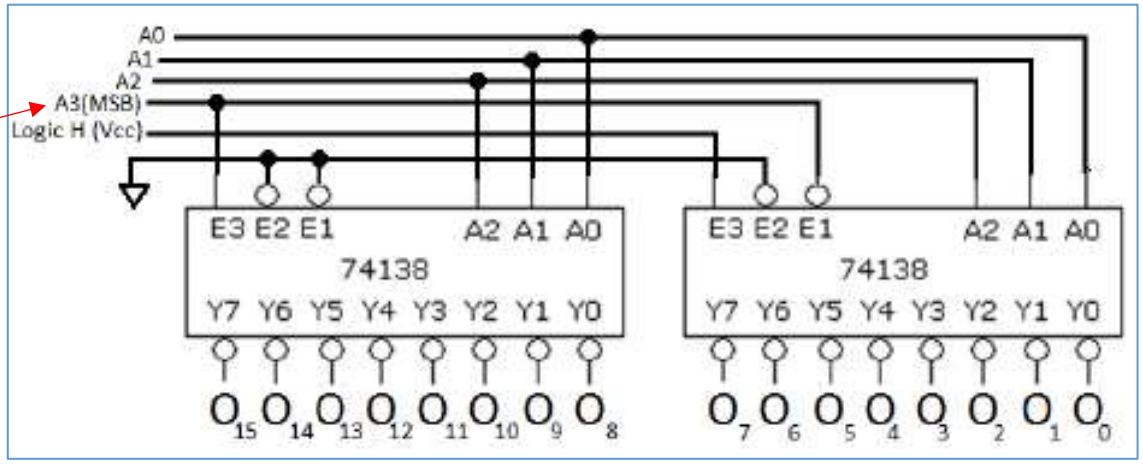
Y5 will be turned on at '0' and other outputs will be turned off at '1' (since they are active-low).

(d) Assuming the decoder is enabled, what must be the combination applied to the inputs A2 A1 A0 (in this order) to select output Y_3? And what happens to the output Y_3 when it is selected? (1 mark)

A2, A1, A0 should be 011 (i.e. 3 in decimal) for Y3 to be turned on at '0'.

(e) Using two 74138 ICs, show how these ICs can be connected as a 1-of-16 decoder. Ensure you label your circuit clearly or marks will not be awarded. (3 marks)

A3 (MSB) will enable either one of the ICs.



B5. Figure B5.1 shows a Mod-15 counter.

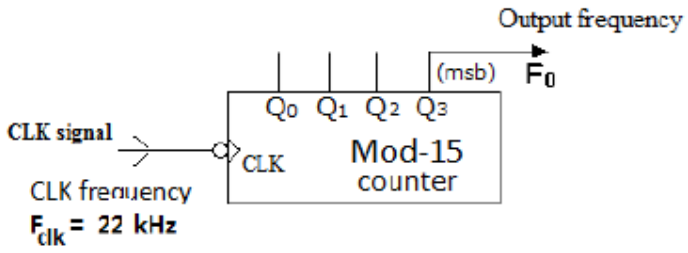


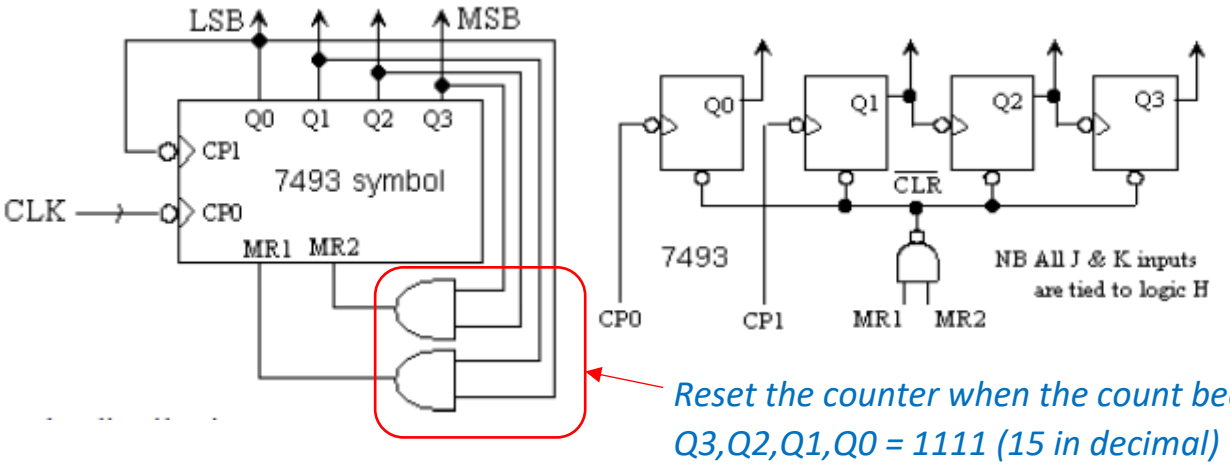
Figure B5.1

(a) What should be the output frequency at the Q3 of the Mod-15 counter if the frequency at its clock input is **22 kHz**? (3 marks)

The frequency at Q3 = clock frequency / MOD = 22 kHz / 15 = 1.47 kHz

(b) Using one 7493 IC, the symbol and internal circuit of which is given in Figure B5.2, show how you would connect the IC to function as the **Mod-15** counter. Draw your circuit in your answer booklet using only the 7493 symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will not be awarded.

(5 marks)



Reset the counter when the count becomes Q3,Q2,Q1,Q0 = 1111 (15 in decimal)

(c) Determine the duty cycle of the signal at the MSB output of the Mod-15 counter. (2 marks)

The mod-15 counter will count from 0 to 14 and repeats:

Count:	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	0	1	2
Q3:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0

Q3 (MSB) outputs '0' from count 0 to 7 and outputs '1' for the rest of the counts.

There are 8 '0's and 7 '1's in a counter cycle of 15 numbers (0 to 14).

Hence, the duty cycle of Q3 (MSB) = 7 / 15 = 0.4667 = 46.67%

B6. Table B6 lists some of the electrical parameters of the **74ALS08 IC,** Quad 2-input AND gate Integrated Circuit.

Symbol	Parameters	Nominal	Min
V_{CC}	Supply voltage (V)	5	
V_{IH}	High level input voltage (V)		2
V_{IL}	Low level input voltage (V)	0.8	
V_{OH}	High level output voltage (V)		3
V_{OL}	Low level output voltage (V)	0.4	
$I_{CC(H)}$	Supply current (mA), outputs High	0.92	
$I_{CC(L)}$	Supply current (mA), outputs Low	3.1	
t_{pLH}	Propagation delay (nS)	11	
t_{pHL}	Propagation delay (nS)	8	

Table B6

(a) What does the description "Quad 2-input AND gate" mean? (2 marks)

'Quad' means four – it means there are four 2-input AND gates in this IC.

(b) What is the parameter for minimum output voltage when the output is at logic High, and what is the value of this voltage? (2 marks)

Minimum V_{OH}: 3V

(c) What is the expression for calculating the power dissipation of an IC? Hence, calculate the power dissipation of the 74ALS08 IC on a per gate basis. (3 marks)

$P_D = V_{CC} \times I_{CC} = V_{CC} \times (I_{CCH} + I_{CCL}) / 2$

Per IC: $P_D = 5 \times (0.92 + 3.1) / 2 = 10.05$ mW

Per gate: $P_D = 10.05 / 4 =$ 2.51 mW

(d) Calculate the High and Low level noise margins for the IC. What is the overall noise margin? (3 marks)

High state noise margin $V_{NH} = V_{OH} - V_{IH} = 3 - 2 =$ 1V

Low state noise margin $V_{NL} = V_{IL} - V_{OL} = 0.8 - 0.4 =$ 0.4V

Overall noise margin: 0.4V (i.e. lower of the above two.)

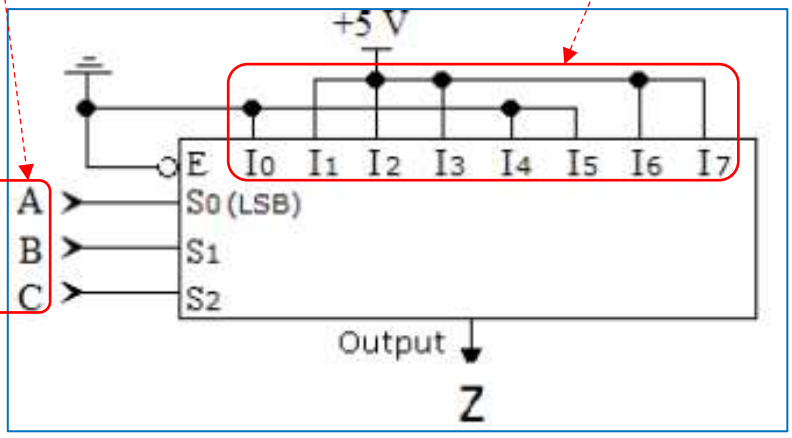
C1. The following Boolean expression is to be implemented with an 8-input multiplexer:

$$Z = CBA + CB\overline{A} + \overline{C}BA + \overline{C}B\overline{A} + \overline{C}\,\overline{B}A$$

(a) From the given Boolean expression, determine the truth table for output Z with the input variable C is the MSB and A is the LSB. (4 marks)

C	B	A	Z
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	1
1	0	0	0
1	0	1	0
1	1	0	1
1	1	1	1

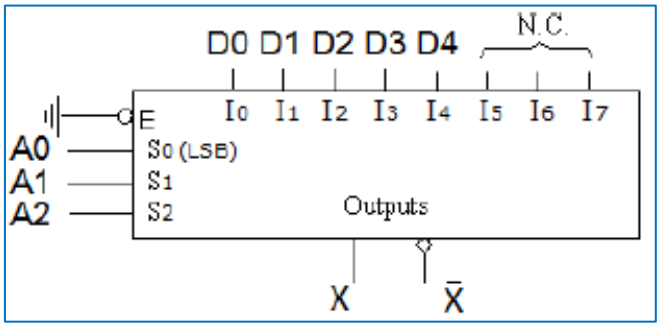
(b) Using one 74151 multiplexer IC, show how you would implement the output Z using the truth-table derived in part (a). The 74151 symbol given in Figure C1.1 is to be used and input C should be assigned to the multiplexer SELECT input S2. Your completed circuit must be clearly labelled or marks will be deducted. (6 marks)



Match the MSB/LSB of the truth table inputs with the MSB/LSB of the MUX select input.

Connect each MUX data input to either '1' or '0' as required in the truth table.

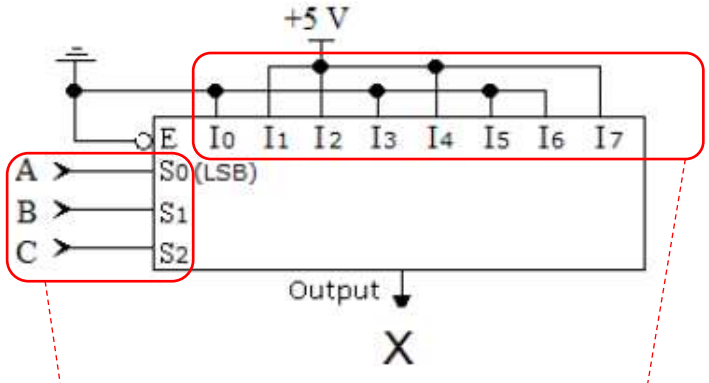
(c) Show how you would connect one 74151 IC (Figure C1.1) to function as a 5-to-1 multiplexer. In your completed diagram, label the data inputs as D0 D1 D2 D3 D4 and the SELECT inputs as A_2 A1 A0, where the subscript of 0 denotes the LSB. Unused inputs should be indicated as N.C. (i.e. No Connection). (4 marks)



Use only the first 5 data inputs and ignore the last 3.

(d) Given the 74151 multiplexer connected as shown in Figure C1.2, determine the logic function (i.e. Boolean expression) implemented at the output X. From the resultant expression obtained, implement the output function with only one logic gate.
Hint: Create a truth table with C, B and A as input variables, X as output.

(6 marks)



C (S2)	B (S1)	A (S0)	X
0	0	0	0
0	0	1	1
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	0
1	1	0	0
1	1	1	1

$$X = \bar{C}B\bar{A} + \bar{C}\bar{B}A + CBA + C\bar{B}\bar{A}$$
$$= C\overline{(B \oplus A)} + \bar{C}(B \oplus A)$$
$$= C \oplus B \oplus A$$