SINGAPORE POLYTECHNIC   ET1004

2011/2012 SEMESTER 2 EXAMINATION

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT /EO

Diploma in Info-communication Engineering and Design DICD 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Clean Energy DCEG 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 2   Time Allowed : 2 hours

Instructions to Candidates

1.   The attention of candidates is drawn to the Rules of Conduct of Examination found on
        the back of the Answer Booklet.

2.   This paper consists of **THREE** sections:
        Section A - 10 Multiple Choice Questions, 2 marks each.
        Section B -   6 Short Questions, 10 marks each.
        Section C -   1 Long Question of 20 marks.

3.   Answer **ALL** questions in the accompanying Answer Booklet, unless otherwise
        indicated.   Start each question in Sections B and C on a new page.

4.   This Examination Paper consists of 8 pages.

5.   Your admission number and module class must be entered in the box provided on the
        cover page of your Answer Booklet.

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A   Multiple Choice Questions (20 Marks)

1.   What is the **range of decimal** values that can be represented by an **8-bit** (including sign bit) **2's complement** signed numbering system?

   (a) $+7_{10}$ to -8_{10} (b) $+31_{10}$ to -32_{10}

   (c) $+63_{10}$ to -64_{10} (d) $+127_{10}$ to -128_{10}

2.   How many **D flip-flops** are required to store a **2-digit decimal** number expressed in the **BCD** format?

   (a) 4_{10} (b) 8_{10}

   (c) 16_{10} (d) 32_{10}

3.   In the **8-bit** (including the sign bit) two's complement signed numbering system, what does the number 11111111_2 equates to?

   (a) -1_{10} (b) -128_{10}

   (c) $+127_{10}$ (d)   Zero

4.   A 160_{10} kHz square wave clocks a naturally resetting (i.e. mod 2^N) **4-bit** ripple counter. What is the frequency of the signal at its MSB output?

   (a) 80_{10} kHz   (b) 40_{10} kHz

   (c) 10_{10} kHz   (d) 2_{10} kHz

5.   A shift register which has only **one data input** and **multiple data outputs** is a:

   (a)   parallel-in, serial-out register   (b)   serial-in, parallel-out register

   (c)   parallel-in, parallel-out register   (d)   serial-in, serial-out register

6. How many **Select inputs** are required for a Multiplexer with **16** data inputs and **1** data output?

   (a) 1_{10} (b) 4_{10} (c) 16_{10} (d) 64_{10}

7. In the addition of 2 signed numbers using the **8-bit** (including the sign bit) **two's complement signed numbering system**, a **9th bit** is produced in the sum result. How should the 9th bit be interpreted?

   (a) If the 9th bit is a 1 while the sign bit is a 0, it indicates an overflow.

   (b) If the 9th bit is a 1 and the sign bit is a 1, it indicates positive result.

   (c) The 9th bit should be discarded.

   (d) It is impossible for the 9th bit to be generated.

8. How many JK flip-flops are required to construct a **Mod-8_{10}** binary counter?

   (a) 16_{10} JK flip-flops (b) 8_{10} JK flip-flops

   (c) 3_{10} JK flip-flops (d) 2_{10} JK flip-flops

9. A **1-of-8 decoder** can also be described as a:

   (a) 3_{10} to 8_{10} decoder

   (b) 4_{10} to 16_{10} decoder

   (c) 9_{10} outputs decoder

   (d) BCD decoder.

10. Which one of the following equations is the correct mathematical expression for calculating the average power consumed by a TTL digital IC?

    (a) $(I_{OH} + I_{IH})/2 * V_{OH}$

    (b) $(I_{OL} + I_{IL})/2 * V_{OL}$

    (c) $(I_{OH} + I_{OL})/2 * V_{CC}$

    (d) $(I_{CCH} + I_{CCL})/2 * V_{CC}$

Section B   Short Questions (60 marks)

B1.   Perform the following operation using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit.

(a)   Add $+30_{10}$ to $+53_{10}$

(5 marks)

(b)   Subtract $+31_{10}$ from $+88_{10}$

(5 marks)

NB: All workings in question B1 must be shown or marks will not be awarded.

B2.   Each of the five statements comprising this question describes MSI devices, namely: Encoder, Decoder, Multiplexer and De-multiplexer. You are required to state in your answer booklet, the type of MSI device (or device**s**) being described by each statement. Ensure that your answers are labelled exactly according to each of the statements, i.e. [(a), (b)....(e)] or marks will not be awarded.

(10 marks)

(a)   This MSI device can be used to implement combinational logic functions.

(b)   Only one of its 8_{10} outputs can be active (E.g. goes Low) at a time.

(c)   When multiple inputs are active simultaneously, the 'highest-number' input active, determines the BCD code generated.

(d)   This device can be used to route a signal at its single data input to one of several data outputs.

(e)   These MSI devices have SELECT inputs.

B3   The 74LS93, with symbol and internal circuit as shown in figure B3, is described as a 4-bit asynchronous counter IC.
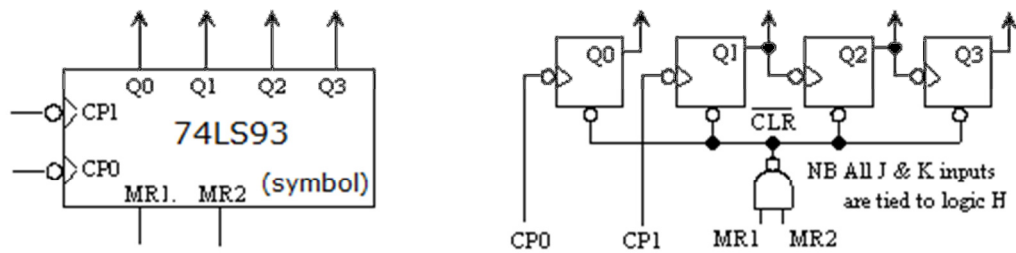

Figure B3

(a)   Using one 74LS93 counter IC (symbol), show how you would connect it as a **mod-12$_{10}$** binary counter. You must ensure that all your connections are properly labelled or marks will be deducted.   (7 marks)

(b)   If the clock frequency to the mod-12$_{10}$ counter is **24$_{10}$ kHz,** determine the **frequency** of the si**gnal** at its **MSB** output**.**

    (3 marks)

B4(a)   The 74138 is a **1-of-8** decoder device and has a symbol as shown in figure B4.1. If output **Q5** of the 74138 decoder is to be selected, what logic levels are required at both the **Enable** and **Select** inputs?
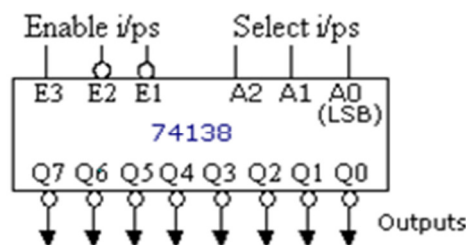
    (4 marks)

Figure B4.1

(b)   For the 74147 **decimal-to-BCD** priority encoder circuit shown in figure B4.2, what is the code (in binary) generated at the outputs Y3 Y2 Y1 Y0?
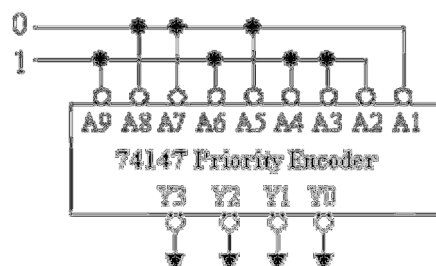
    (3 marks)

Figure B4.2

(c)   If the **true** value of the BCD code is to be generated, what devices must be connected to the outputs of the 74147 priority encoder?   (3 marks)

B5   A **Full Adder** (Figure B5.1) is a combinational circuit that adds 3 bits, Augend **A**, Addend **B** and carry-input **Cin** to produce a 2 bit output appropriately labelled as **Cout** (carry-out) and **Sum.**
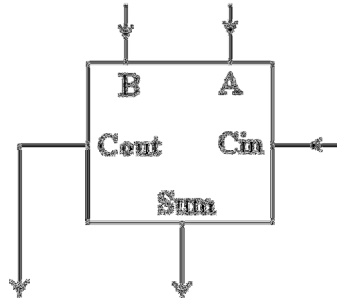

Figure B5.1

(a)   Complete in your Answer Booklet, the truth table of the Full Adder using a table format as shown in Table B5.1

(4 marks)

A	B	Cin	Cout	Sum
0	0	0		
:	:	:		
1	1	1		

Table B5.1

(b)   Given the logic symbol of 74151, an 8-to-1 multiplexer IC as shown in figure B5.2, show how you should connect the device to implement the **Cout** output only. Your circuit must be clearly labelled or marks will be deducted. (*Hint: assume variable Cin to be the LSB and assign it to S0.*)
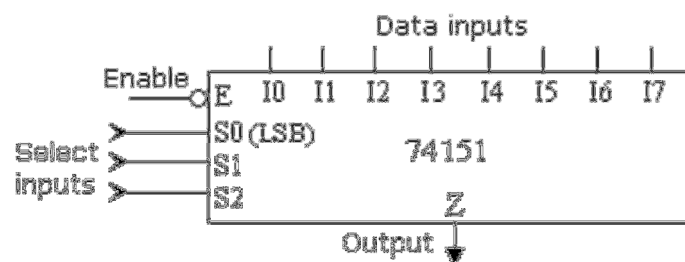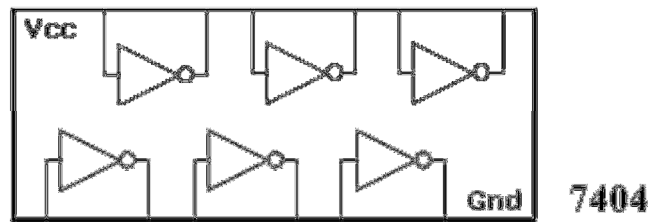
(6 marks)

Figure B5.2

B6   Table B6 lists the typical values of the AC and DC parameters (characteristics) for 2 different logic families **of the 7404 Inverter IC**.

Parameter	Unit	Device A	Device B
Vcc	V	5	5
V_{IH} (min)	V	2	2
V_{IL} (max)	V	0.8	0.7
V_{OH} (min)	V	2.4	2.7
V_{OL} (max)	V	0.4	0.5
Icc_H	mA	12	2.4
Icc_L	mA	24	6.6
t_{PLH}	nS	13	9
t_{PHL}	nS	15	8

Table B6

(a)   Which device has the higher **output voltage** for logic **High** and what is the value of this voltage?

(2 marks)

(b)   Which device can operate at a higher signal frequency? Justify your answer by quoting the correct parameter.

(2 marks)

(c)   Calculate the High level Noise margin V_{NH} for both devices. Which device has the better noise margin at logic High?

(3 marks)

(d)   Calculate the average power consumption **per gate** for device **A**, only.

(3 marks)

Section C Long Question (20 marks)

C1. A BCD (mod-10) counter (i.e. a counter that counts from 0 to 9 decimal) is connected to a decoder as shown in figure C1. The decoder has an output **Z**, which responds in the following manner:

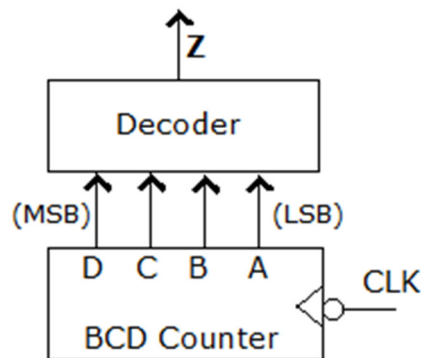- **Z = H** whenever the BCD counter output is **equal to and greater than 8_{10}**.

Figure C1

Your task in this question is to design the decoder circuit using two different methods.

(a) Determine the **truth-table** for this **decoder**, showing all the possible input combinations and expected responses at the output **Z**. Use the table format as shown in table C1, where two expected output values are also given as examples. You are reminded that A is the LSB and D is the MSB and all don't care conditions should be indicated as 'X's.

(8 marks)

(MSB)	**Inputs**		(LSB)	**Output**
D	**C**	**B**	**A**	**Z**
0	0	0	0	0
⋮	⋮	⋮	⋮	
⋮	⋮	⋮	⋮	
1	1	1	1	X

Table C1

(b) Using one **74151,** an **8 to 1 multiplexer** IC, show how you would implement the decoder logic circuit for output **Z** using the truth-table derived in part (a). The 74151 symbol given in figure B5.2 of question B5 is to be used. Your completed circuit must be clearly labelled or marks will not be awarded.

(7 marks)

(c) Using one **74138** decoder IC (see figure B4.1 on page 5) and a NOT gate to invert the output, implement the decoder circuit for output **Z**. Ensure that your circuit is appropriately labelled or marks will not be awarded.

(5 marks)

------------ **End of Paper** ------------