SINGAPORE POLYTECHNIC ET1004

2017/2018 S2 MID-SEMESTER TEST

SAS code: **MST**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Energy Systems Management DESM 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet, unless indicated otherwise.

4. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

5. There are 6 pages in this paper.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

A1. An edge-triggered JK flip-flop with $\overline{PRE}$ and $\overline{CLR}$ inputs has all its inputs except the CLK input, connected to logic High. If the signal applied at its CLK input is 20 kHz with a duty cycle of 20 %, what will be the frequency and duty cycle of the signal at its Q output?

(a) 10 kHz, 20 % duty cycle
(b) 10 kHz, 50 % duty cycle
(c) 40 kHz, 20 % duty cycle
(d) 40 kHz, 50 % duty cycle

A2. What is the minimum number of JK flip-flops required to build a **mod-48**$_{10}$ binary-sequence counter?

(a) 4_{10} (b) 5_{10} (c) 6_{10} (d) 7_{10}

A3. What is the mod-number of the counter circuit shown in figure A3?

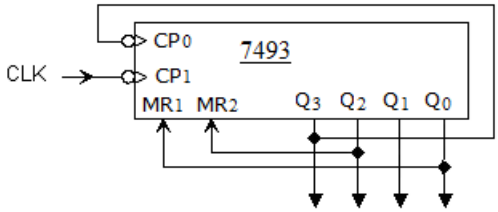

Figure A3

(a) Mod-13_{10} (b) Mod-12_{10} (c) Mod-11_{10} (d) Mod-10_{10}

A4. Which one of the following counters requires the most number of flip-flops?

(a) Mod 23 Ripple Counter
(b) Decade Counter
(c) Mod 16 Up/Down Counter
(d) A divide by 36 Asynchronous Counter

A5. A counter transforms an input clock frequency of 256 kHz to 8 kHz at its MSB output. This counter is a:

(a) 8-bit Asynchronous counter.
(b) mod-8 ripple counter and a mod-4 ripple counter connected in cascade.
(c) 4-bit BCD counter.
(d) 32-bit ripple counter.

A6. In the 8 bits 2's complement signed numbering system, the decimal value of **zero** has _____

(a) a sign bit of 0 in the MSB position.
(b) a sign bit of 1 in the MSB position.
(c) a sign bit of 0 in the LSB position.
(d) a sign bit of 1 in the LSB position.

A7. A mod-32 naturally resetting counter has five outputs labelled as E D C B A, with E being the MSB and A the LSB. If the signal frequency at its 3rd output C is 8 kHz, what is the signal frequency of the CLK signal applied at its clock input??

(a) 16_{10} kHz (b) 32_{10} kHz (c) 64_{10} kHz (d) 128_{10} kHz

A8. A shift register circuit with **many** data inputs and **one** data output is a _____.

(a) serial-in, serial-out shift register
(b) parallel-in, serial-out shift register
(c) serial-in, parallel-out shift register
(d) parallel-in, parallel-out shift register

A9. A parallel adder which can add signed binary numbers using the 2's complement numbering system in the range from $+32767_{10}$ to -32768_{10} is to be constructed using the 74LS83 IC, a 4-bit parallel adder IC. How many of these 74LS83 ICs are required to build this parallel adder circuit?

(a) 4_{10} (b) 5_{10} (c) 6_{10} (d) 8_{10}

A10. In the addition of two signed numbers using the 8-bit (including the sign bit) two's complement system, a ninth (9^{th}) bit is produced in the result. How should the ninth bit be interpreted?

(a) If the 9^{th} bit is a 1 while the sign bit is a 0, it indicates an overflow.
(b) If the 9^{th} bit is a 0 and the sign bit is a 1, it indicates a positive result.
(c) The 9^{th} has no significance and should be discarded.
(d) It is impossible for the 9^{th} bit to be generated.

Section B (45 marks)

B1(a) Perform the following calculations using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit. All steps and **workings must be shown** or marks will be deducted.

(i) Add $+54_{10}$ to $+61_{10}$ (4 marks)

(ii) Subtract $+36_{10}$ from $+53_{10}$ (6 marks)

(b) Express the following pairs of numbers in BCD format and hence, perform the addition of the numbers using BCD arithmetic.

(i) Add $+137_{10}$ to $+25_{10}$ (5 marks)

B2 The Full Adder (FA) symbol is shown in Figure B2.

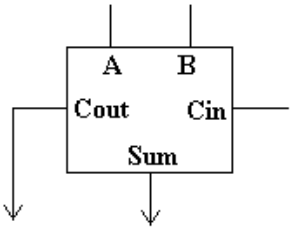

Figure B2

(a) Complete the truth table of the FA circuit in your Answer Booklet using a table heading as shown in Table B2.

(6 marks)

Inputs			Outputs	
A	B	Cin	Cout	Sum

Table B2

(b) From the completed truth table, obtain the un-simplified Boolean expressions for outputs Cout and Sum in a sum-of-products (SOP) form.

(4 marks)

(c) Use Boolean Algebra to transform the Boolean expression for the Sum output to one that uses only XOR gates and hence draw the resultant circuit for the Sum output.

(5 marks)

B3(a) Given a periodic clock signal as shown in figure B3, calculate its

(i) Period

(ii) Signal frequency.

(iii) Duty cycle.

(6 marks)

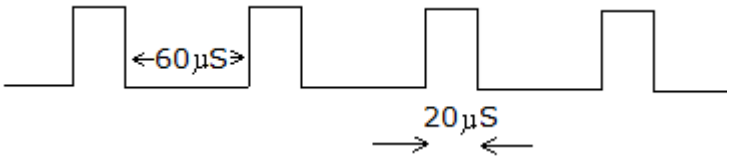

Figure B3

(b) A counter has a count sequence as shown in Table B3. Analyze the sequence and determine the Modulus (or Mod number) of this counter.
Hence determine the frequency and duty cycle of the signal at its MSB output Q_2, if the clock signal applied is 1000_{10} Hz with a duty cycle of 50%.

(6 marks)

Q_2 (MSB)	Q_1	Q_0 (LSB)	Clock
0	0	0	↓
0	0	1	↓
0	1	0	↓
0	1	1	↓
1	0	0	↓
0	0	0	↓
0	0	1	↓

Table B3

(c) If the initial (starting) value of the counter in Table B3 is 010_2 and 62_{10} clock cycles are continuously applied, what will be the values at its outputs Q_2 Q_1 Q_0 (in this order) at the end of the 62_{10} clock cycles?

(3 marks)

Section C (25 marks)

C1 Figure C1.1 shows the block diagram of two different ripple counters with modulus (or mod numbers) to be determined. You are required to design a divide-by-18_{10} counter as a cascade of **two** separate and different counters.

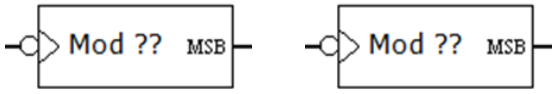

Figure C1.1

(a) How many possible ways are there to configure a divide-by-18 counter using the approach stated? List down all the possible configurations by stating the mod-number of each counter required and drawing the block diagrams showing how the 2 separate counters should be connected together to achieve the overall modulus of mod-18_{10}.

(8 marks)

(b) Which one of the possible configurations you listed in part (a) provides a symmetrical square wave signal (50% duty cycle) at the divide-by-18_{10} output of the cascade of two counters?

(4 marks)

(c) Using two 7493 counter ICs (see figure C1.2), implement the cascaded configuration you identified in part (b). Your implemented circuit must be labelled clearly or marks will be deducted.

(10 marks)

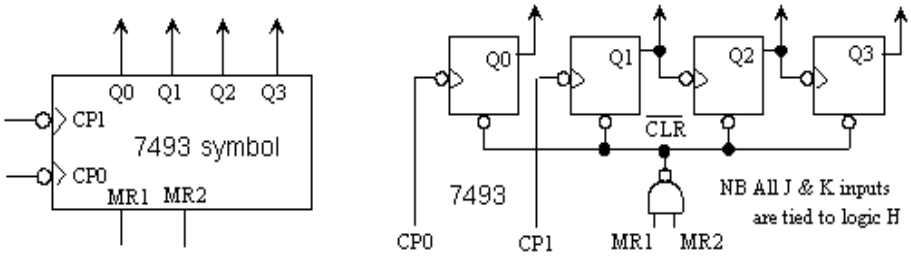

Figure C1.2

(d) Draw the state transition diagram of the first counter unit of the cascade of 2 counters in part (c).

(3 marks)

---------- End of Paper ----------