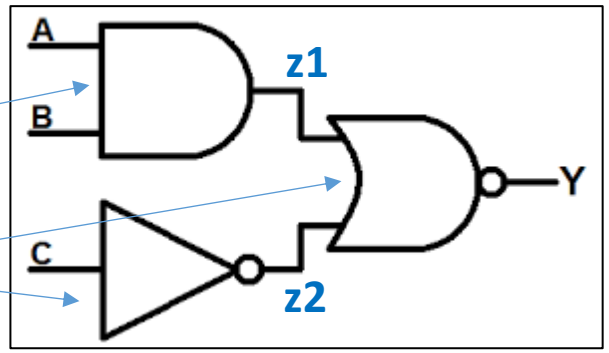
Tutorial 3

B1. Write a Verilog program for the circuit in Figure 1 using gate instantiation.

```
module Figure1 (A, B, C, Y);
        input A,B,C;
        output Y;
        wire z1 ,z2;
        and Gate1 (z1 , A, B);
        not Gate2 (z2, C);
        nor Gate3 (Y, z1, z2);
endmodule
```

Structural description



The above statements can be replaced by its ***behaviour description*** equivalent:

```
assign Y = ~(A & B | ~C);
```

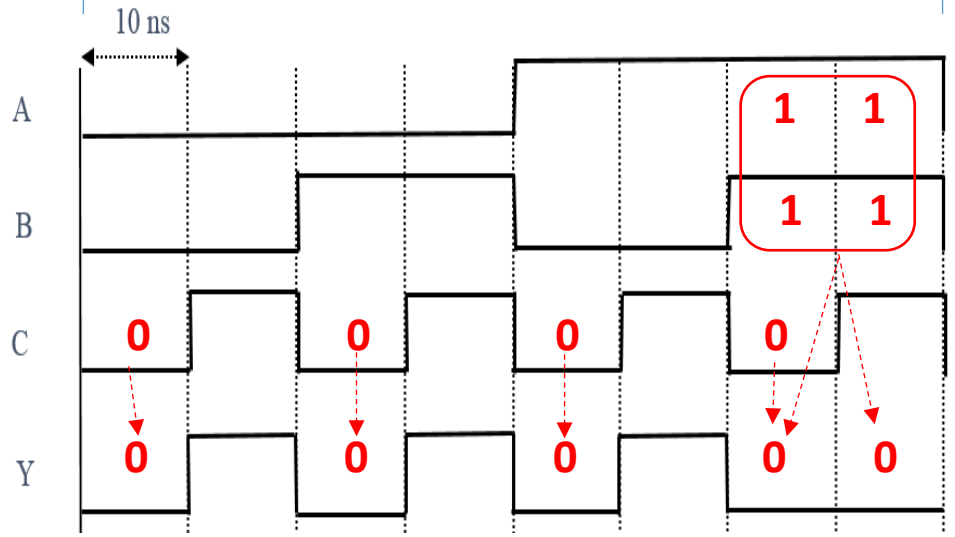
In boolean equation:

$$Y = \overline{A.B + \overline{C}}$$

B2. Figure 2 shows the testbench for Figure 1.

Draw the waveform of A, B, C and Y after simulation for 80 ns.

```
`timescale 1ns / 1ps
module Figure1_tb();
        wire Y;
        reg A=0;
        reg B=0;
        reg C=0;
        always #40 A=~A;
        always #20 B=~B;
        always #10 C=~C;
        Figure1 dut(A,B,C,Y);
endmodule
```



Y = ~(A & B | ~C)

In boolean equation:

$$Y = A.B + \overline{C}$$

$$\overline{Y} = \overline{A.B + \overline{C}}$$

Y=0 when either:

- A=1 & B=1
- C=0