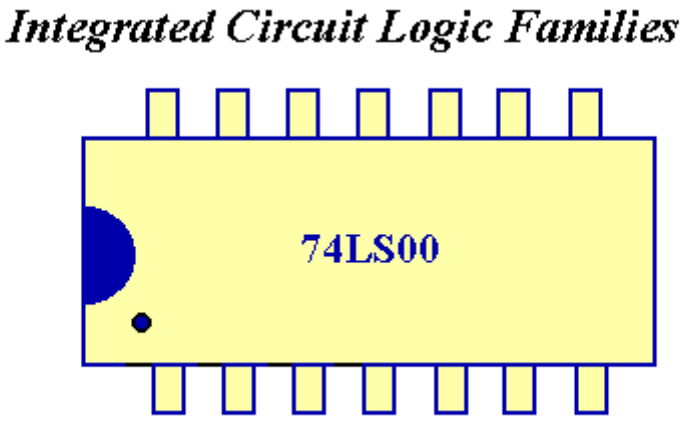
Integrated Logic Families



Objectives:

- **Read and interpret digital IC terminology as specified in the IC manufacturers' data sheets.**
- **Compare the characteristics of standard TTL with the other TTL series.**
- **Calculate and determine the worst case characteristics of a simple digital logic circuit in terms of maximum clock frequency, noise margin, etc.**
- **Describe the major characteristics and differences amongst the TTL, and CMOS logic families.**

- There are many IC manufacturers in the world today, examples of which includes:

	Motorola Texas Instruments (TI) Intel Samsung Nippon Electric Company (NEC) etc.

- With so many different manufacturers, sometimes manufacturing the same category of ICs or even the same type of devices, IC parameters and terminology need to be standardized.

- Generally, Digital IC parameters and characteristics are broadly classified into three categories, namely:

1.	Functional parameter
2.	DC parameters
3.	AC parameters

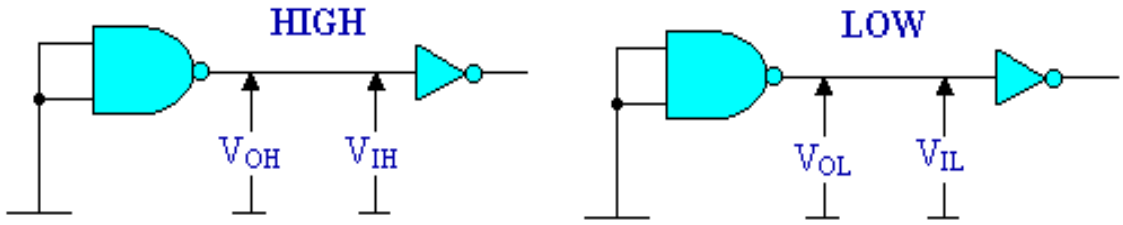
- The functional parameter describes the functional specification of the device and usually takes the form of Truth and State tables.

- DC parameters describes the dc characteristics of the ICs such as power consumption, the output voltage for logic High and Low, the dc current flowing in and out of logic gates, etc.

- The AC parameters specify the timing and frequency characteristics of the ICs such as response time or propagation delay, maximum clocking frequency, etc.

- This topic is concerned mainly with the DC and AC parameters

DC Voltage Parameters



V_{IH}(min) High-Level Input Voltage

The voltage level required for a logical H at an *input*. Any voltage below this level will not be accepted as a HIGH by the logic circuit.

V_{IL}(max) Low-Level Input Voltage The voltage level required for a logical L at an *input*. Any voltage above this level will not be accepted as a LOW by the logic circuit.

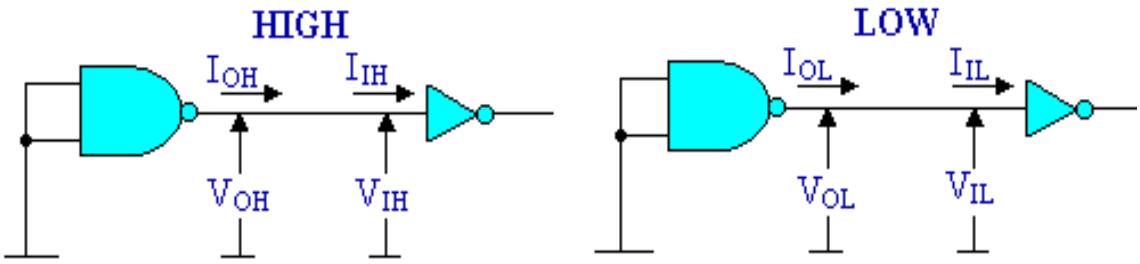
V_{OH}(min) High-Level Output Voltage

The voltage level at a logic circuit *output* in the logical H state. The minimum value of V_{OH} is usually specified.

V_{OL}(max) Low-Level Output Voltage

The voltage level at a logic circuit *output* in the logical L state. The maximum value of V_{OL} is usually specified.

DC Current Parameters



- **$I_{IH(Max)}$ High-Level Input Current**: The current that flows into an *input* when a specified high level voltage is applied. The maximum value of I_{IH} is usually specified.

- **$I_{IL(Max)}$ Low-Level Input Current**: The current that flows into an *input* when a specified high level voltage is applied. The maximum value of I_{IL} is usually specified.

- **$I_{OH(Max)}$ High-Level Output Current**: The current that flows from an *output* in the logical 1 state under specified load conditions. The maximum value of I_{OH} is usually specified.

- **$I_{OL(Max)}$ Low-Level Output Current**: The current that flows from an *output* in the logical 0 state under specified load conditions. The maximum value of I_{OL} is usually specified.

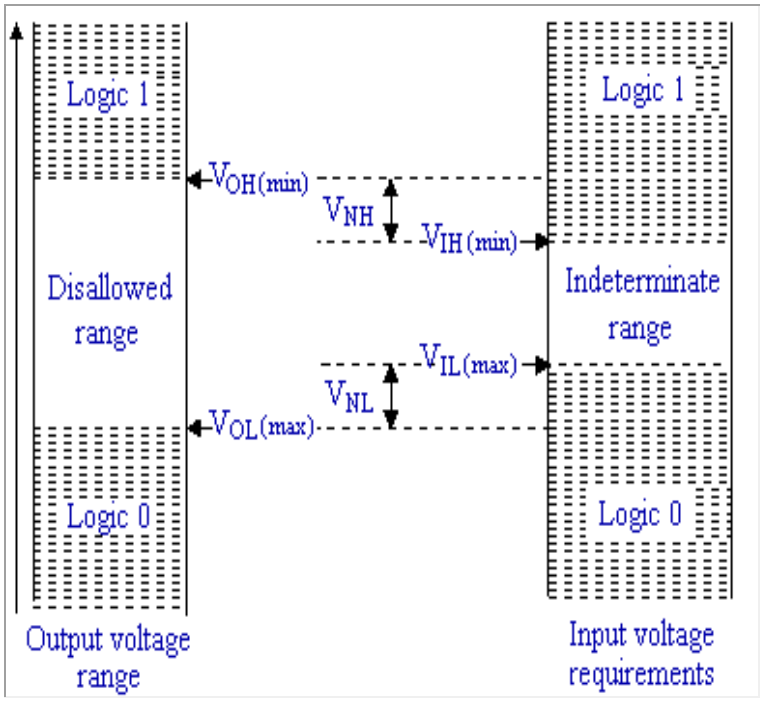
Noise Immunity

Stray electric and magnetic fields can affect logic circuits.

Unwanted signals are called *noise*.

Noise immunity of a circuit is its ability to tolerate noise.

Noise Margin is a quantitative measure of noise immunity.



Low-Level Noise Margin is given by:

$V_{NL} = V_{IL} - V_{OL}$

High-Level Noise Margin is given by:

$V_{NH} = V_{OH} - V_{IH}$

Power Requirements

All ICs require electrical power to function. This power is supplied by one or more power supply voltages.

1.	Power-supply pins are usually denoted as V_{CC} for TTL and V_{DD} for MOS devices.
2.	The amount of power an IC requires is determined by its supply current - I_{CC}.
3.	Power consumption = $I_{CC} \times V_{CC}$
4.	Current drain will usually vary with IC's logic states. There are 2 values of current drain to consider:
	I_{CCH} - supply current when all outputs are HIGH
	I_{CCL} - supply current when all outputs are LOW
5.	In general I_{CCL} and I_{CCH} will usually be different. The average value is used instead. This is given as $Icc(avg) = (I_{CCL} + I_{CCH}) / 2$
6.	Therefore power consumption
	$P_D(avg) = I_{CC}(avg) \times V_{CC}$

Fan-Out:

Is also called *loading factor* is defined as the maximum number of standard logic inputs that an input can drive reliably.

Propagation Delay, for review see topic ➪

Speed-Power Product

- Ideally you want the gate to have zero propagation delay and consume zero power. *This is not possible.*

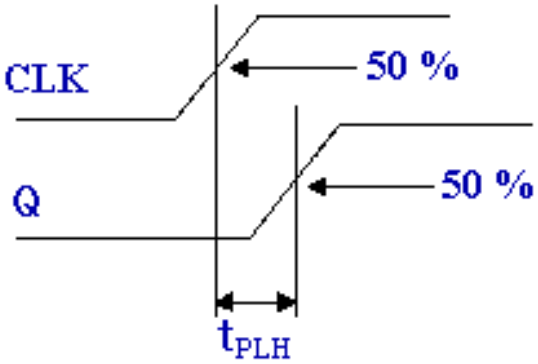
- The *speed-power product* for a gate is a measure of its efficiency. *The lower the better.*

- speed-power product =
  propagation delay x power dissipation

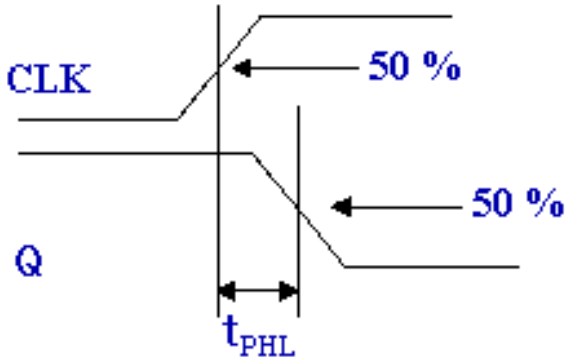
E.g.for a device with tpd of 10nS

10 ns x 5 mW = 50 x 10^{-12} watt-second
= 50 pj

Propagation Delays



Delay with Output going from LOW to HIGH.



Delay with Output going from HIGH to LOW

Propagation delay basically measures the response times of the devices.
Two values are quoted: t_{PLH} and t_{PHL}.

t_{PLH} is the delay that results when the output state changes from Low to High in response to the input stimulus, whereas

t_{PHL} is the delay when the output changes from High to Low.

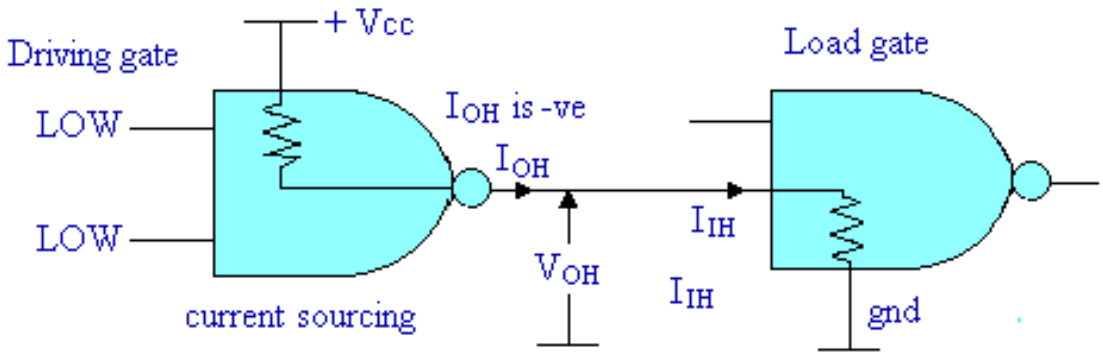
These two delays are usually different & IC manufactures specify their maximum values.

Current-Sourcing

When the output of a driving gate is High, the output current I_{OH} flows out and into the load gate.

The driving gate is said to be sourcing the load. This current I_{OH} becomes I_{IH} if there is only one load connected to the output.

From the two-port convention, I_{OH} is thus given a positive sign and I_{IH} is given a negative sign.



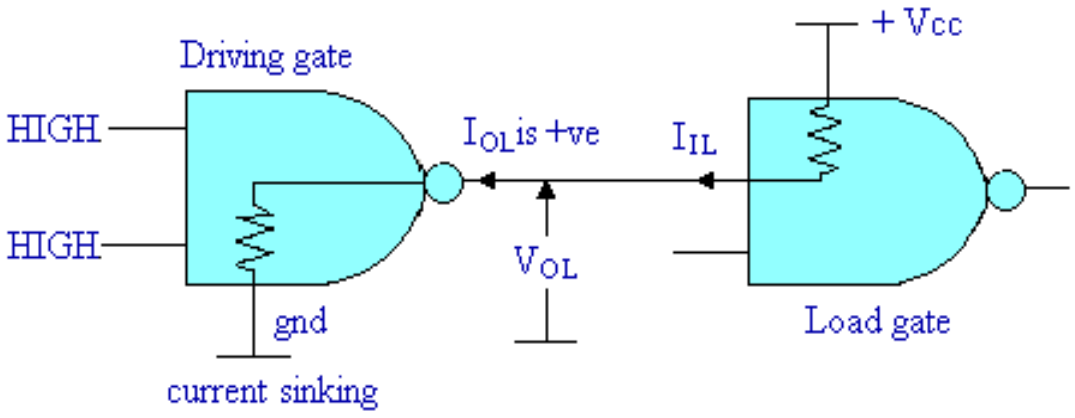
Current-Sinking

When the driving gate output is Low, the current flow is reverse and the output current I_{OL} flow into the output terminal.

This current is equal to I_{IL} if there is only one load connected to the output.

In this instance, the output gate is said to be sinking the load current.

By 2-port convention, I_{OL} will be considered positive and I_{IL} considered negative.



Example:

SN5400, SN7400 TTL IC

Quad 2-input positive NAND gate recommended operating conditions

Parameter	5400			7400			Unit
	min	nom	max	min	nom	max	
V_{CC} Supply Voltage	4.5	5	5.5	4.75	5	5.25	V
V_{IH} High-level i/p voltage	2			2			V
V_{IL} Low-level i/p voltage			0.8			0.8	V
I_{OH} High-lever o/p current			-0.4			-0.4	mA
I_{OL} Low-lever o/p current			16			16	mA
T_A Operating free-air temperature	-55		125	0		70	C

Electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

Parameter	Test condition	5400			7400			Unit
		min	nom	max	min	nom	max	
V_{IK}	V_{CC} = MIN, I_I = -12mA			-1.5			-1.5	V
V_{OH}	V_{CC} = MIN, V_{IL} = 0.8v, I_{OH} = -0.4mA	2.4	3.4		2.4	3.4		V
V_{OL}	V_{CC} = MIN, V_{IH} = 2v, I_{OL} = 16mA		0.2	0.4		0.2	0.4	V
I_I	V_{CC} = MAX, V_I = 5.5v			1			1	mA
I_{IH}	V_{CC} = MAX, V_I = 2.4v			40			40	µA
I_{IL}	V_{CC} = MAX, V_I = 0.4v			-1.6			-1.6	mA
I_{OS} -	V_{CC} = MAX,	-20		-55	-18		-55	mA
I_{CCH}	V_{CC} = MAX, V_I = 0v		4	8		4	8	mA
I_{CCL}	V_{CC} = MAX, V_I = 4.5		12	22		12	22	mA

Switching characteristics,
V_{CC} = 5V
T_A = 25C

Parameter	From (input)	To (output)	Test Conditions	min	typ	max	unit
t_{PLH}	A or B	Y	$R_L = 400$ $C_L = 15pF$		11	22	ns
t_{PHL}					7	15	ns

Standard 74 Series Characteristics

Noise margins (worst case)	$V_{NL} = V_{NH} = 400mV$
Average power dissipation (basic gate)	$P_D = 10mW$
Average propagation delay (basic gate)	9ns
Typical fanout	10

Other TTL Series

Series	Comments	P_D (mW)	t_P (ns)
74L	Similar to 74 series except all resistor values have been ***increased***.	1	33
74H	Similar to 74 series except all resistor values have been ***decreased***.	23	6
74S	Uses Schottky barrier diode so that the transistors does not go into such deep saturation.	20	3
74LS	Similar to 74S series except all resistor values have been ***increased***.	2	9.5
74AS	Technologically improved version of 74S series	8	1.7
74ALS	Similar to 74AS series except all resistor values have been ***increased***.	1.2	4

Typical TTL Series Characteristics

	74	74L	74H	74S	74LS	74AS	74ALS
Performance ratings							
Propagation delay (ns)	9	33	6	3	9.5	1.7	4
Power dissipation (mW)	10	1	23	20	2	8	1.2
Speed-power product (pj)	90	33	138	60	19	13.6	4.8
Max. clock rate (MHz)	35	3	50	125	45	200	70
Fan-out (same series)	10	20	10	20	20	40	20
Voltage Parameters							
V_{OH}(min)	2.4	2.4	2.4	2.7	2.7	2.5	2.5
V_{OL}(max)	0.4	0.4	0.4	0.5	0.5	0.5	0.4
V_{IH}(min)	2.0	2.0	2.0	2.0	2.0	2.0	2.0
V_{IL}(max)	0.8	0.8	0.8	0.8	0.8	0.8	0.8

Unconnected Inputs (floating)

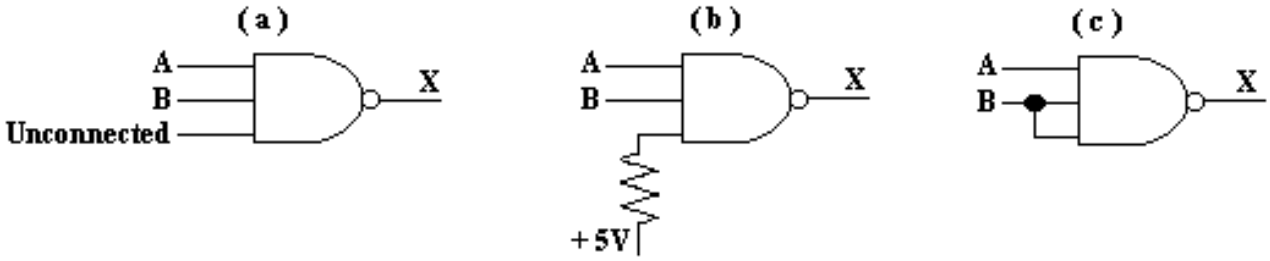
- when an input is not connected it is said to be "floating".

- in general, unconnected inputs will act as if a logic H is being applied to the input.

Unused inputs

- frequently, not all inputs of a TTL IC are used.

- E.g, the function $X = \overline{A\,B}$ is required and only 3 input NAND gates are available.



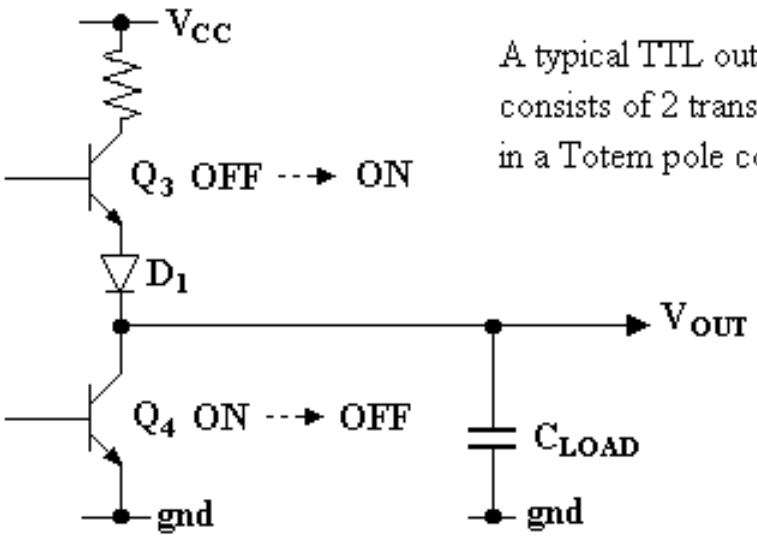
Three different ways to handle unconnected logic inputs.

Current Transients

- TTL logic circuits suffer from internally generated current transients when its output switches from Logic L to H.

- This is due to the totem-pole output transistors Q3 and Q4 being momentarily conducting at the same time. When this happens, a large current flows momentarily from Vcc to ground, resulting in current transients. These transients may be conveyed through the power lines to other TTL devices causing erroneous operation.

- To prevent current transients from affecting other TTL circuits, the normal practice is to connect a decoupling capacitor directly and in close proximity to Vcc and ground pins of each TTL IC that is used.



A typical TTL output stage consists of 2 transistors connected in a Totem pole configuration.

MOS

Stands for **M**etal **O**xide **S**emiconductor.

Logic families classified as MOS uses *field-effect transistors* called MOSFETs.

Main advantages of using MOSFET in logic devices are:

1)	Simplicity in design
2)	Cheaper to fabricate
3)	Consume little power
4)	MOS devices also occupy much less space on a chip than bipolar transistors.
5)	MOS digital ICs don't normally require resistors.
6)	MOS ICs can accommodate greater number of circuit elements on a single chip than bipolar ICs.

Main disadvantage of MOS ICs is their relatively slow operating speed.

The MOS logic family is based on the MOSFET transistor.

There are 2 types of MOSFET:

1.	Depletion Mode:	The transistor is normally ON and an appropriate Gate-Source voltage Vgs will turn it OFF.
2.	Enhancement Mode:	The transistor is normally OFF and application of an appropriate Gate-Source Voltage Vgs will turn it ON.

MOS Digital ICs use the enhancement mode MOSFETs.

MOS Digital ICs are basically categorized into 3 types:

1.	PMOS	Uses only P-channel enhancement mode MOSFETs
2.	NMOS	Uses only N-channel enhancement mode MOSFETs
3.	CMOS	Uses both N-channel and P-channel enhancement mode MOSFETs

MOS Applications

General Purpose Microprocessors	NMOS eg. 8085, Z80
High speed/low power microprocessors	CMOS eg. 68030, 80C286

P-MOS and N-MOS digital ICs have greater packing density and are more economical than CMOS.

N-MOS has about twice packaging density of P-MOS, i.e. for a given chip area, NMOS yields about twice the number of transistors.

N-MOS is about twice as fast as P-MOS.

CMOS has the highest complexity and lowest packing density of the MOS families but has highest speed and lowest power consumption.

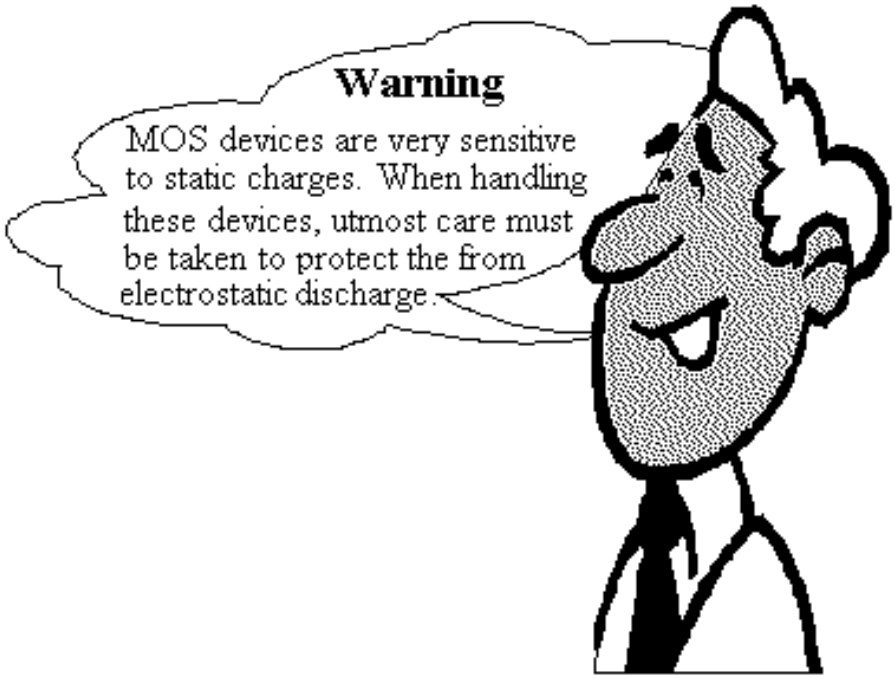
Comparison between MOS and TTL

Parameter	MOS Logic	TTL
Speed of operation	slow	fast
Noise margin	large	small
Fan-out	very high	small
Power consumption	low	high
Transistor 'real estate'	small	large
Supply voltage	2 to 15v	5v only
Fabrication process complexity	simple	complex
Static sensitivity	high	low

All electronic devices are sensitive to static - some more than others.

The human body is a great storehouse of electrostatic charges.

- Walking across a carpet can generate a static charge of over 30KV.



CMOS

Uses both P-channel and N-channel enhancement mode MOSFETs

Advantages of CMOS over P-MOS and N-MOS

1.	Faster
2.	Consumes less power

Disadvantages of CMOS over P-MOS & N-MOS

1.	Increased complexity in IC fabrication
2.	Lower packing density

CMOS logic Applications

Used in products where very low power is a priority.

eg. Calculators, watches, lap-top PCs

Used in products where a very high level of integration is necessary

eg. 486 PC computers, 68040 Apple computers

Used in products where the is lots of noise and high ambient temperatures.

eg. Electronic engine management, electronic fuel injection

Used in products where heat dissipation is a priority

eg. Satellites

CMOS series

4000/14000	These are mainly hybrid ICs, i.e ICs for analog and digital applications.
4000A	Is the original 4000 series without output buffers - are hence very sensitive to static.
4000B	Improved 4000A series with higher output drive capabilities and input protection and output buffers - are therefore not so sensitive to static as the 4000A .
74C	CMOS logic devices which are pin-for-pin and function-for-function compatible with TTL series, eg. 74C74 is compatible with TTL 7474. The 74Cxx and 74xx devices are however not electrically compatible.
74HC (Hi-Speed CMOS)	Improved version of 74C series. Main improvement is in speed. About 10 times faster.
74HCT	Same as 74HC series with the advantage that they are also electrically compatible with TTL series.
74AC/ACT (Advanced CMOS)	This series is functionally equivalent to various TTL series. It is however not electrically and pin-compatible with TTL. The ACT series offers advantages over the HC series in terms of noise immunity, propagation delay, and max. clock speed.
74AHC/AHCT (Advanced Hi-Speed CMOS)	This is a direct upgrade of the HC series. The devices are 3 times faster, consumes lower power and can be used as direct replacements for the HC/HCT series.
BiCMOS 5-Volt Logic	Combines the best features of TTL & CMOS in terms of having the high speed of TTL and low power consumption of CMOS. BiCMOS are however not available in most SSI and MSI functions, but are limited to functions used in coprocessor and bus interfacing functions, such as latches, buffers and drivers, etc.

Power Supply Voltage

4000 and 74C series will operate with V_{DD} values from 3 to 15V.

74HC and 74HCT series will operate with V_{DD} values from 2 to 6 V.

Voltage Levels

CMOS outputs will only drive CMOS inputs with the exception of the 74HCT series.

$V_{OL}(max) = 0v$	$V_{IL}(max) = 30\%$ of V_{DD}
$V_{OH}(min) = V_{DD}$	$V_{IH}(min) = 70\%$ of V_{DD}

Noise Margins

V_{NH}	$=V_{OH}(min) - V_{IH}(min)$	V_{NL}	$=V_{IL}(max) - V_{OL}(max)$
	$=V_{DD} - 70\%$ of V_{DD}		$=30\%$ of $V_{DD} - 0$
	$=30\%$ of V_{DD}		$=30\%$ of V_{DD}

Power Dissipation

Power dissipation is very small - typically 2.5nW per gate when V_{DD} = 5v

As the frequency increases, the power consumption P_D increases proportionally.

Fan-out

CMOS fan-out is dependant upon the maximum propagation delay and frequency of operation. Typically a at frequencies less than 1 Mhz the fan-out would be limited to 50.

Unused Inputs

*CMOS inputs should **never** be left disconnected*. All CMOS inputs have to be tied either to V_{DD} or 0v or to another input.

Static Charge Susceptibility

WARNING - CMOS devices are very susceptible to static charge.
Good handling procedures must always be observed.

Tristate devices

Are digital devices with 3 states: the digital logic levels of High, Low, and the 3rd state, which is High impedance (equivalent to open circuit).

Tri-state devices come with an enable input that allows the output to operate in its normal High-Low states or to switch to high impedance (open circuit) state.

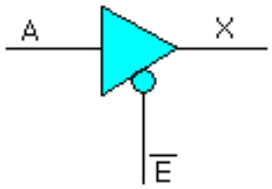
They are normally used in applications where outputs of digital devices need to be connected together, i.e. share the use of a common wire (i.e. a bus connection).

Without the tristate, normal digital outputs should never be connected together as the situation could arise where one output is High while the other is Low, leading to large output currents and permanent damage to the devices.

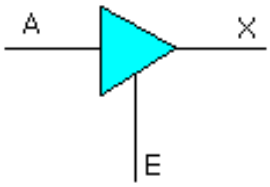
With tristate, each output that is connected together can be enabled one at a time, thus preventing the situation of High-Low contention.

Tristate devices are available for both TTL and CMOS and are usually available as buffers.

Tristate Buffers



Active Low Enable



Active High Enable

$\overline{E}$	X
0	A
1	Hi-Z

E	X
0	Hi-Z
1	A

A tristate buffer is a circuit that is used to control the passage of a logic signal from input to output. It does not change the logic level unless it is an inverting buffer (i.e. an inverter with tristate output).

When enabled, the logic level applied at the input A will pass through to the output X.

When disabled, the logic level applied at input A does not pass to the output which is in high impedance (Hi-Z). To put it simply, it is as though output X is disconnected from input A.