Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

1111

Section A Multiple Choice Questions (20 Marks)

1. What is the maximum positive decimal value that can be represented by a 16-bit (including sign bit) 2's complement signed numbering system?

(a) $+15_{10}$ (b) $+16383_{10}$

(c) $+32767_{10}$ (d) $+65535_{10}$

0000 0000 0000 0000 = 0
0000 0000 0000 0001 = +1
0000 0000 0000 0010 = +2
Etc. etc.
0111 1111 1111 1111 = +32767
1000 0000 0000 0000 = -32768
1111 1111 1111 1110 = -2
1111 1111 1111 1111 = -1

Answer: (c)

Max positive 16-bit value = 2^{15} -1

2. In the 8-bit (including the sign bit) two's complement signed numbering system, what does the number 11111111_2 equates to when converted to decimal?

(a) -128_{10} (b) -1_{10}

(c) $+127_{10}$ (d) Zero

Answer: (b)

3. A shift-register which accepts multiple data bits simultaneously and transfers out multiple data bits simultaneously is a:

(a) parallel-in, serial-out register (b) serial-in, parallel-out register

(c) parallel-in, parallel-out register (d) serial-in, serial-out register

Answer: (c)

4. How many JK flip-flops are required to construct an asynchronous binary counter that counts to a maximum value of FF_{16}?

255

(a) 4_{10} JK flip-flops (b) 16_{10} JK flip-flops

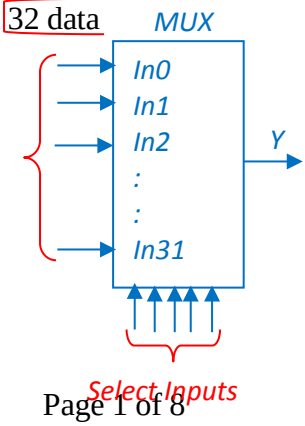
(c) 8_{10} JK flip-flops (d) 32_{10} JK flip-flops.

Answer: (c)

5. How many Select inputs are required for a Multiplexer with 1 enable input and 32 data inputs?

(a) 1_{10} (b) 5_{10}

(c) 6_{10} (d) 32_{10}



Answer: (b)

***MUX**: its N 'select inputs' will select one out of its 2^N data inputs to the output.*

6. The correct mathematical expression to calculate the average power consumed by a TTL digital IC is:

(a) $(I_{OL} + I_{OH})/2 \ * \ V_{CC}$

(b) $(I_{OL} + I_{CCL})/2 \ * \ V_{CC}$

(c) $(I_{OH} + I_{CCH})/2 \ * \ V_{CC}$

(d) $(I_{CCH} + I_{CCL})/2 \ * \ V_{CC}$

Answer: (d)

Average Power = Average Icc x Vcc

7. For the counter shown in figure A7, what is its modulus (i.e. mod-number)?

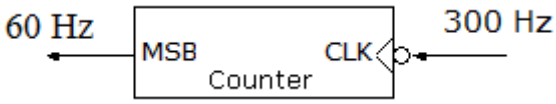


Figure A7

(a) Mod-60_{10} (b) Mod-300_{10}

(c) Mod-5_{10} (d) Mod-6_{10}

Answer: (c)

$f_{MSB} = f_{clock} / MOD \rightarrow \mathbf{MOD = f_{clock} / f_{MSB}}$

8. How many 74LS93 (4-bit) counter ICs are required to construct a BCD counter that counts to a maximum of 59_{10}?

2-digit

Represent each decimal digit with 4-bit

(a) 2_{10} (b) 3_{10}

(c) 4_{10} (d) 7_{10}

Answer: (a)

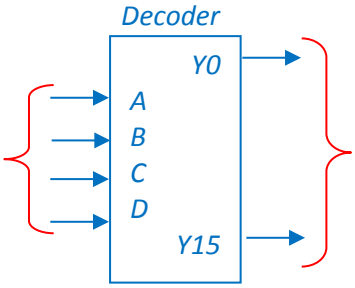
9. What is the maximum number of possible outputs for a Decoder with 4 select inputs and 1 enable input?

(a) 4_{10} (b) 5_{10}

(c) 8_{10} (d) 16_{10}

Answer: (d)

***Decoder**: only 1 of the outputs can be ON, the rest are OFF.*



10. A Demultiplexer accepts data from -

(a) one input line and transfers it to several output lines.

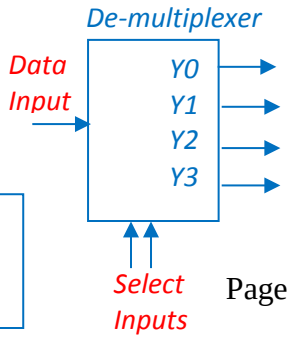
(b) one input line and transfers it to one output line.

(c) many input lines and transfers it to several output lines.

(d) many input lines and transfers it to one output line.

Answer: (a)

***De-multiplexer**: its select inputs will select its data input to one of its outputs.*



Section B Short Questions (60 marks)

B1. This question consists of two parts that involve numerical calculations and/or number conversions.

(a) Perform the following operation using the **2's complement signed numbering system**. You are to assume that each number is to be represented by **8 bits**, including the sign bit.

Add -26_{10} to $+57_{10}$ (6 marks)

+26: 0001 1010
Invert: 1110 0101
Add 1: 1110 0110 = -26

+57: 0011 1001
-26: 1110 0110
*= **0001 1111** = +31*
(Take 8-bit only as result.)

(b) Perform the addition of the following set of numbers using **BCD arithmetic:**

Add $+55_{10}$ to $+36_{10}$ (4 marks)

***BCD**: Binary Coded Decimal*
- using 4 bits to represent each decimal

NB: All steps and workings for this question must be shown or marks will be deducted

55 (BCD): 0101 0101
36 (BCD): 0011 0110
1000 1011
1 0110
*91 (BCD): **1001 0001***

If any digit of the sum > 9 (1001), correction is required by adding 6 (0110) to it, and carry out 1 to the next digit.

B2 Figure B2.1 shows two counters connected in cascade.

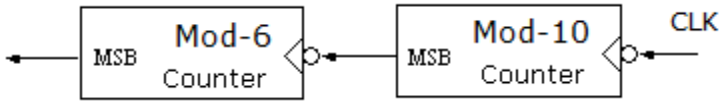


Figure B2.1

(a) What is overall Mod number of the counter circuit of figure B2.1?

6 x 10 = ***60***

(2 marks)

(b) If the frequency of the signal at the MSB output of the Mod-6_{10} counter is 100_{10} Hz, what is the frequency of the CLK signal applied at CLK input of the Mod-10_{10} counter?

Frequency at MSB = Clock frequency / Mod number

→ f_{clock} *= 60 x 100 Hz =* ***6 KHz***

(3 marks)

(c) Using the 7493 counter IC, symbol and internal circuit as shown in Figure B2.2, construct the Mod-10_{10} counter. Draw the circuit in your answer booklet using the 7493 symbol. Ensure that all inputs and outputs are clearly labelled

(5 marks)

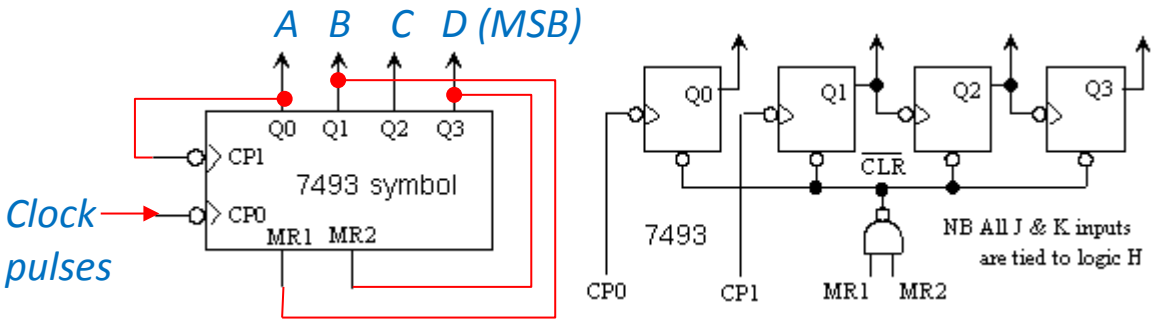


Figure B2.2

Mod-10 → clear all flip-flops when the count becomes 1010;
i.e. when DCBA = 1010 or when D=1 and B=1.
(Hence connect D and B to MR1 and MR2.)

B3 Two 74LS283 ICs (each a 4-bit Parallel Adder IC) are connected as shown in figure B3.

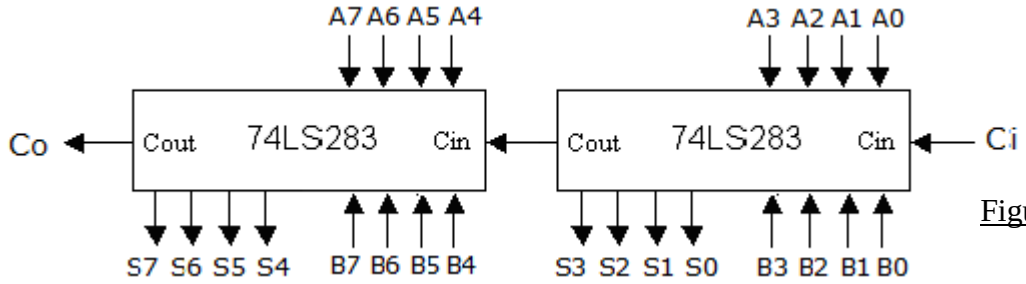


Figure B3

(a) Given: $A_7\ A_6\ A_5\ A_4\ A_3\ A_2\ A_1\ A_0 = 0\ 1\ 0\ 0\ 1\ 0\ 0\ 1_2$ and,

$B_7\ B_6\ B_5\ B_4\ B_3\ B_2\ B_1\ B_0 = 1\ 1\ 0\ 1\ 1\ 1\ 1\ 0_2$

What will be the binary value at the outputs: Co $S_7\ S_6\ S_5\ S_4\ S_3\ S_2\ S_1\ S_0$ for Ci = 1_2. (3 marks)

+1

1 0 0 1 0 1 0 0 0

(b) If the 8 bits (including the sign bit) 2's complement signed arithmetic is used in part (a) above, what are the equivalent decimal numbers being added and the decimal sum result? Note that the value of Ci in this case should be considered as '1' added to number B. (4 marks)

*A = 0100 1001 = **+73***
*B = 1101 1110 = **-34***
*C_{in} = **+1***
*Sum = 0010 1000 = **+40***
(Take only 8-bit as result.)

Let B: 1101 1110 = -X
Invert: 0010 0001
Add 1: 0010 0010 = +X = +34
*Hence, **B** = -X = **-34***

*Note: Some combine C_{in} with B and say B = **-33***
(I disagree but consider it as correct.)

(c) If the Full Adder unit is used to construct the Parallel Adder circuit of figure B3, how many Full Adder units are required? (3 marks)

Each 74LS283 IC is a 4-bit parallel adder and it requires 4 Full Adders.
*The above circuit with two 74LS283 ICs hence **requires 8 Full Adders**.*

(Full Adders are 1-bit adders which can be combined together to form N-bit adder.)

B4 Each of the five statements comprising this question describes MSI devices, namely: **Encoder**, **Decoder**, **Multiplexer** and **De-multiplexer**. You are required to state in your answer booklet, the type of MSI device (or MSI device**s)** being described by each statement. Ensure that your answers are labelled exactly according to each of the statements, i.e. [(a), (b)....(e)] or marks will not be awarded.

(10 marks)

(a) Only one of its 16_{10} outputs can be active (e.g. goes Low) at a time.
Decoder.

(b) A combinational circuit can be easily implemented using this device.
Multiplexer.

(c) When multiple inputs are active simultaneously, the 'highest-number' input active, determines the BCD code generated.
Encoder. (Priority encoder.)

(d) This device can be used to route a signal at its single data input to one of several data outputs.
De-multiplexer.

(e) These MSI devices have SELECT inputs.
Decoder, Multiplexer & De-multiplexer.

B5(a) Give two different names for the decoder device shown in figure B5.1. Briefly describe the purpose of the enable inputs. *3-to-8 decoder, or 1-of-8 decoder.*

(4 marks)

All outputs will be disabled ('1') unless all enable inputs are active. (E3,E2,E1=1,0,0)

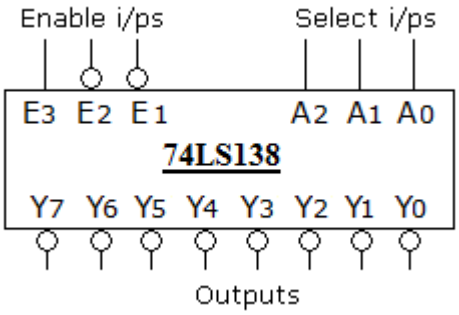


Figure B5.1

(b) If output Y7 is to be selected, what are the logic levels required at the Enable and Select inputs? And what is the logic level of Y7 when it is selected?

(3 marks)

*Enable inputs: E3, E2, E1 = **1,0,0**.*
*Select inputs: A2, A1, A0 = **1,1,1**.*

(c) For the 74147 **decimal-to-BCD** priority encoder circuit shown in figure B5.2,

(i) What is the highest number input that is active given the connections shown? *A8*

(ii) What is binary code generated at its outputs: $Y_3\ Y_2\ Y_1\ Y_0$ and hence, at the inverter outputs $Z_3\ Z_2\ Z_1\ Z_0$?

(3 marks)

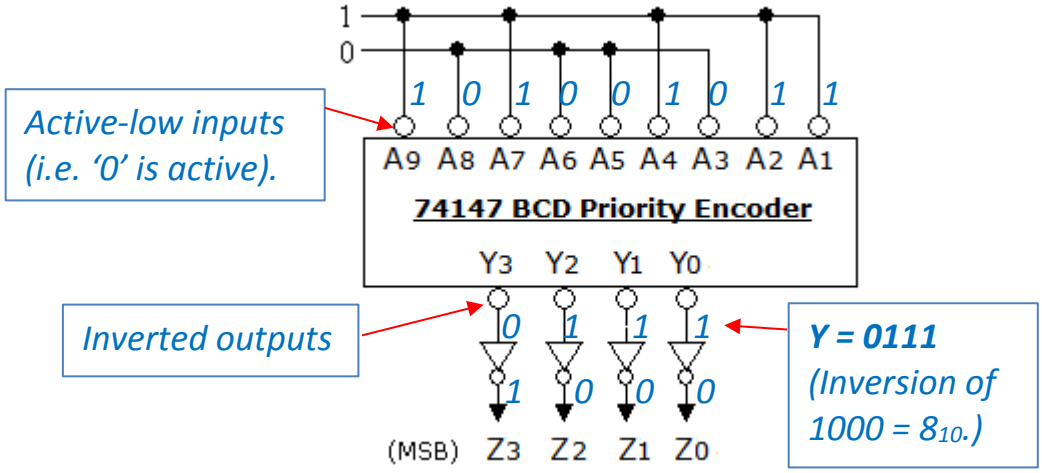


Figure B5.2

B6 The **7400** IC is described as a **Quad 2-input NAND gate.**

Table B6 list some of the electrical parameters of the **7400 IC**.

Symbol	Parameters	Max	Min
V_{CC}	Supply voltage (V)	5	
V_{IH}	High level input voltage (V)		2
V_{IL}	Low level input voltage (V)	0.8	
V_{OH}	High level output voltage (V)		2.4
V_{OL}	Low level output voltage (V)	0.4	
$I_{CC(H)}$	Supply current (mA), outputs High	10	
$I_{CC(L)}$	Supply current (mA), outputs Low	22	
tp_{LH}	Propagation delay (nS)	21	
tp_{HL}	Propagation delay (nS)	15	

Table B6

(a) From the description given, how many NAND gates are there in the 7400 IC? (2 marks)

*"Quad" means four → there are **4** gates in the IC.*

(b) What is the maximum value of the output voltage when the output is at logic Low? (2 marks)

*V_{OL} (max) = **0.4V***

(c) Calculate the power dissipation for the whole IC and hence, for each gate. (4 marks)

*Whole IC: $P = V_{CC}$ x average I_{CC} = 5V x (10+22)/2 mA = **80 mW**.*
*Each gate: 80 / 4 = **20 mW**.*

(d) Calculate the noise margin when the output is at logic High (2 marks)

***$V_{NH} = V_{OH} - V_{IH}$ = 2.4 – 2.0 = 0.4 V**.*

Section C Long Question (20 marks)

C1. A 2-bit number comparator (figure C1.1) that compares the magnitude (or size) of two sets of 2-bit numbers labelled as A_1 A_0 and B_1 B_0 is required to be designed. This 2-bit comparator has an output G such that:

- **G goes High** whenever number **A** is **g**reater than number **B**, i.e. $A_1A_0 > B_1B_0$

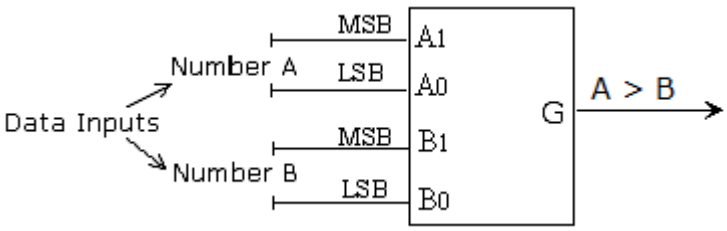


Figure C1.1

(a) Complete the truth-table of this 2-bit comparator circuit in your answer booklet using the format shown in Table C1. The 'Remarks' column is not needed in your answer. It is given to help you to complete the truth-table. Six input combinations (of the 16_{10} required) and their expected output values have also been completed for you.

(10 marks)

Number A		Number B		Output	Remarks
A_1	A_0	B_1	B_0	G	
0	0	0	0	0	A = B ; (0_{10} = 0_{10})
:	:	:	:	:	
1	0	0	1	1	A > B ; (2_{10} > 1_{10})
1	0	1	0	0	A = B ; (2_{10} = 2_{10})
1	0	1	1	0	A < B ; (2_{10} < 3_{10})
:	:	:	:	:	
1	1	1	0	1	A > B ; (3_{10} > 2_{10})
1	1	1	1	0	A = B ; (3_{10} = 3_{10})

Table C1

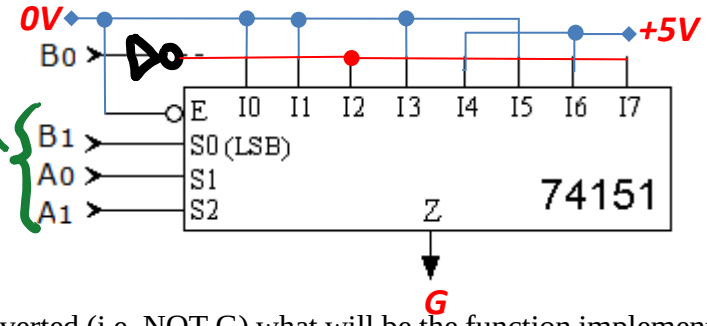
A_1 A_0	B_1 B_0	G
0 0	0 0	0
0 0	0 1	0
0 0	1 0	0
0 0	1 1	0
0 1	0 0	1
0 1	0 1	0
0 1	1 0	0
0 1	1 1	0

(Continue)

A_1 A_0	B_1 B_0	G
1 0	0 0	1
1 0	0 1	1
1 0	1 0	0
1 0	1 1	0
1 1	0 0	1
1 1	0 1	1
1 1	1 0	1
1 1	1 1	0

(b) Using the 74151 multiplexer IC (figure C1.2) and a NOT gate (if necessary), implement the 2-bit comparator circuit for output **G**. You must label clearly, all inputs and output using the same variable names as those used in the block diagram and truth table. Note that input variables A_1 A_0 and B_1 have been assigned to the select inputs as shown.

(7 marks)



A_1 A_0	B_1 B_0	G	
0 0	0 0	0	(0)
0 0	0 1	0	G=0
0 0	1 0	0	(1)
0 0	1 1	0	G=0
0 1	0 0	1	(2)
0 1	0 1	0	$G=B_0'$
0 1	1 0	0	(3)
0 1	1 1	0	G=0

(Continue)

A_1 A_0	B_1 B_0	G	
1 0	0 0	1	(4)
1 0	0 1	1	G=1
1 0	1 0	0	(5)
1 0	1 1	0	G=0
1 1	0 0	1	(6)
1 1	0 1	1	G=1
1 1	1 0	1	(7)
1 1	1 1	0	$G= B_0'$

(c) If output G is inverted (i.e. NOT G) what will be the function implemented?

(3 marks)

*As G = A > B, NOT G = **A <= B** (less or equal to).*

---------- **End of Paper** ----------