
TUTORIAL 4 (Chapter 3)**SECTION A****MULTIPLE CHOICE QUESTIONS**

A1. The Moore's output of a finite state machine depends on _____.

- (a) the present state only
- (b) the next state only
- (c) the present state and primary input
- (d) the next state and primary input

Ans()

A2. A finite state machine has 6 states. Using simple binary state assignment system, how many flip flops are required?

- (a) 3
- (b) 4
- (c) 5
- (d) 6

Ans()

A3. Which of the following shows a Mealy's output Z, given that K and L are the external inputs to a finite state machine while Q_1 and Q_2 are the flip-flop outputs?

- (a) $Z=Q_1(K+L)$
- (b) $Z=Q_1 + Q_2$
- (c) $Z= Q_1 Q_2$
- (d) $Z=Q_1(Q_1 + Q_2)$

Ans()

SECTION B

B1. A finite state machine has an input w and an output z. The machine is a sequence detector that produces $z = 1$ when the previous two values of w were 00 or 11; otherwise $z = 0$.

- (a) Draw the Moore's state diagram.
- (b) Derive the state table from part (a).

- B2. Figure 1 shows the excitation table for an FSM. The FSM has an input P, and two output Y and Z. Both flip-flops response to a PGT clock signal.

Present state		Input	Output		Next state		Excitation	
Q _A	Q _B	P	Y	Z	Q _A	Q _B	D _A	D _B
0	0	0	0	0	0	0	0	0
		1	0	0	1	1	1	1
0	1	0	0	1	0	1	0	1
		1	0	0	1	1	1	1
1	0	0	0	1	0	0	0	0
		1	0	0	1	1	1	1
1	1	0	1	1	0	1	0	1
		1	1	0	1	1	1	1

Figure 1

- Derive the minimized Boolean equations for Y, Z, D_A and D_B.
- Draw the schematic diagram for the FSM using the *minimum number of logic gates*.