2011/2012 S2

SINGAPORE POLYTECHNIC ET1004

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

8-bit gives 2^8 = 256 numbers; half being +ve and half being -ve.

1. What is the **range of decimal** values that can be represented by an **8-bit** (including sign bit) **2's complement** signed numbering system?

(a) $+7_{10}$ to -8_{10} (b) $+31_{10}$ to -32_{10}

(c) $+63_{10}$ to -64_{10} (d) $+127_{10}$ to -128_{10}

Ans: (d)

2. How many **D flip-flops** are required to store a **2-digit decimal** number expressed in the **BCD** format? *BCD (Binary Decimal Digit) - using 4-bit to represent each decimal digit.*

(a) 4_{10} (b) 8_{10}

(c) 16_{10} (d) 32_{10}

Ans: (b)

0000 0000= 0
0000 0001= +1
etc. etc.
0111 1111= +127
1000 0000= -128
etc. etc.
1111 1111= -1

3. In the **8-bit** (including the sign bit) two's complement signed numbering system, what does the number 11111111_2 equates to?

(a) -1_{10} (b) -128_{10}

(c) $+127_{10}$ (d) Zero

Ans: (a)

4. A 160_{10} kHz square wave clocks a naturally resetting (i.e. mod 2^N) **4-bit** ripple counter. What is the frequency of the signal at its MSB output? *MSB freq. = Clock freq. / MOD*

(a) 80_{10} kHz (b) 40_{10} kHz

(c) 10_{10} kHz (d) 2_{10} kHz *where MOD = 2^4 = 16*

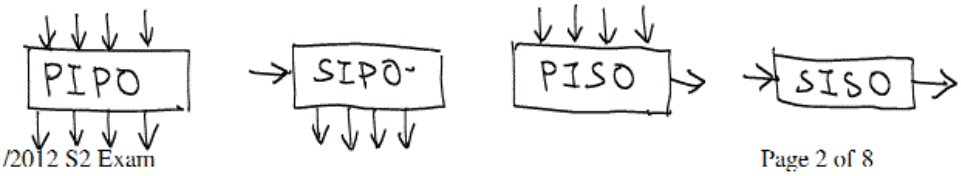
Ans: (c)

5. A shift register which has only **one data input** and **multiple data outputs** is a:

(a) parallel-in, serial-out register (b) serial-in, parallel-out register

(c) parallel-in, parallel-out register (d) serial-in, serial-out register

Ans: (b)



6. How many **Select inputs** are required for a Multiplexer with **16** data inputs and **1** data output?

(a) 1_{10} (b) 4_{10} (c) 16_{10} (d) 64_{10}

Ans: (b)

7. In the addition of 2 signed numbers using the **8-bit** (including the sign bit) **two's complement signed numbering system**, a **9th bit** is produced in the sum result. How should the 9th bit be interpreted?

(a) If the 9th bit is a 1 while the sign bit is a 0, it indicates an overflow.

(b) If the 9th bit is a 1 and the sign bit is a 1, it indicates positive result.

(c) The 9th bit should be discarded.

(d) It is impossible for the 9th bit to be generated.

Ans: (c)

8. How many JK flip-flops are required to construct a **Mod-8_{10}** binary counter?

(a) 16_{10} JK flip-flops (b) 8_{10} JK flip-flops

(c) 3_{10} JK flip-flops (d) 2_{10} JK flip-flops

Ans: (c) *(N-bit gives MOD = 2^N)*

9. A **1-of-8 decoder** can also be described as a:

(a) 3_{10} to 8_{10} decoder

(b) 4_{10} to 16_{10} decoder

(c) 9_{10} outputs decoder

(d) BCD decoder.

Ans: (a)

10. Which one of the following equations is the correct mathematical expression for calculating the average power consumed by a TTL digital IC?

(a) $(I_{OH} + I_{IH})/2 * V_{CC}$

(b) $(I_{OL} + I_{IL})/2 * V_{CC}$

(c) $(I_{OH} + I_{OL})/2 * V_{CC}$

(d) $(I_{CCH} + I_{CCL})/2 * V_{CC}$

Ans: (d) *(Avg. Power = Vcc x Avg. Icc)*

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Section B Short Questions (60 marks)

B1. Perform the following operation using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit.

(a) Add $+30_{10}$ to $+53_{10}$ (5 marks)

(8-bit)
+30 = 0001 1110
+53 = 0011 0101
+83 = 0101 0011

(b) Subtract $+31_{10}$ from $+88_{10}$ (5 marks)

i.e. (+88) - (+31)
i.e. ***(+88) + (-31)***

NB: All workings in question B1 must be shown or marks will not be awarded.

(8-bit)
+31 = 0001 1111
Invert: 1110 0000
Add 1: ***1110 0001*** *= -31*

(8-bit)
-31 = 1110 0001
+88 = 0101 1000
+57 = 0011 1001

Discard carry-out to the 9-th bit.

B2. Each of the five statements comprising this question describes MSI devices, namely: Encoder, Decoder, Multiplexer and De-multiplexer. You are required to state in your answer booklet, the type of MSI device (or devices) being described by each statement. Ensure that your answers are labelled exactly according to each of the statements, i.e. [(a), (b)....(e)] or marks will not be awarded.

(10 marks)

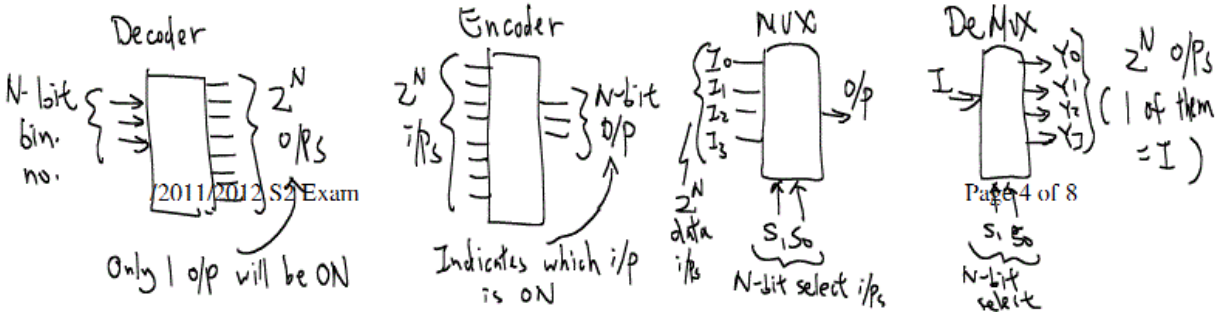
(a) This MSI device can be used to implement combinational logic functions.
Multiplexer

(b) Only one of its 8_{10} outputs can be active (E.g. goes Low) at a time.
Decoder

(c) When multiple inputs are active simultaneously, the 'highest-number' input active, determines the BCD code generated.
Priority Encoder

(d) This device can be used to route a signal at its single data input to one of several data outputs.
De-multiplexer

(e) These MSI devices have SELECT inputs.
Decoder, Multiplexer & De-multiplexer



B3 The 74LS93, with symbol and internal circuit as shown in figure B3, is described as a 4-bit asynchronous counter IC.

Connect Q0 to CP1 to link the first flip-flop to the second one.

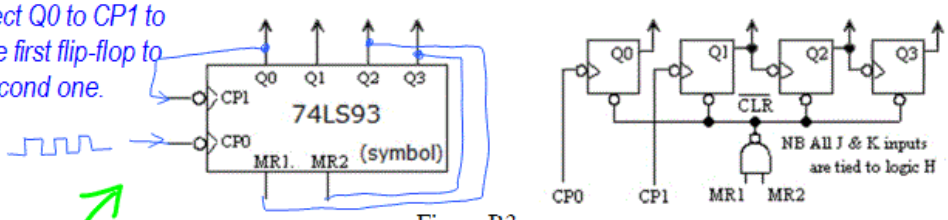


Figure B3

(a) Using one 74LS93 counter IC (symbol), show how you would connect it as a **mod-12$_{10}$** binary counter. You must ensure that all your connections are properly labelled or marks will be deducted. (7 marks)

Reset flip-flops when count =12 = 1100 in binary (i.e. when Q3, Q2 = 1,1)

(b) If the clock frequency to the mod-12$_{10}$ counter is **24$_{10}$ kHz,** determine the **frequency** of the **signal** at its **MSB** output. (3 marks)

MSB freq. = Clock freq. / MOD
= 24 kHz / 12
*= **2 kHz***

B4(a) The 74138 is a **1-of-8** decoder device and has a symbol as shown in figure B4.1. If output **Q5** of the 74138 decoder is to be selected, what logic levels are required at both the **Enable** and **Select** inputs? (4 marks)

***E3,E2,E1 = 100** and **A2,A1,A0 =101** (=5)*

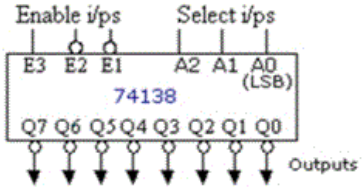
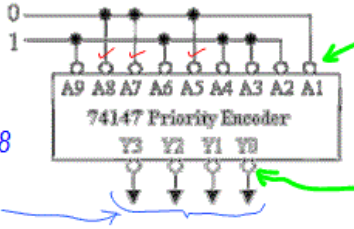


Figure B4.1

(b) For the 74147 **decimal-to-BCD** priority encoder circuit shown in figure B4.2, what is the code (in binary) generated at the outputs Y3 Y2 Y1 Y0? (3 marks)

Priority encoder outputs a binary code to indicate the highest input which is active.



The inputs are active-LOW (i.e. activated by '0')

Figure B4.2

Highest input : 8
In binary: 1000
*Inverted: **0111***

Inverted outputs (i.e. active-LOW)

(c) If the **true** value of the BCD code is to be generated, what devices must be connected to the outputs of the 74147 priority encoder? (3 marks)

Connect NOT gates at the outputs to cancel off the above inversion.

B5 A **Full Adder** (Figure B5.1) is a combinational circuit that adds 3 bits, Augend **A**, Addend **B** and carry-input **Cin** to produce a 2 bit output appropriately labelled as **Cout** (carry-out) and **Sum.**

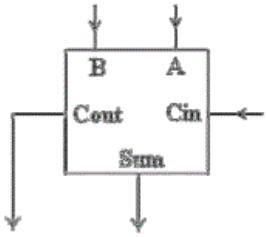


Figure B5.1

(a) Complete in your Answer Booklet, the truth table of the Full Adder using a table format as shown in Table B5.1

(4 marks)

A	B	Cin	Cout	Sum
0	0	0		
:	:	:		
1	1	1		

Table B5.1

Rules for this truth-table:
0 + 0 + 0 = 0 = 00 (bin.)
0 + 0 + 1 = 1 = 01
0 + 1 + 1 = 2 = 10
1 + 1 + 1 = 3 = 11
Inputs Outputs

A B Cin	Cout	Sum
0 0 0	0	0
0 0 1	0	1
0 1 0	0	1
0 1 1	1	0
1 0 0	0	1
1 0 1	1	0
1 1 0	1	0
1 1 1	1	1

(b) Given the logic symbol of 74151, an 8-to-1 multiplexer IC as shown in figure B5.2, show how you should connect the device to implement the **Cout** output only. Your circuit must be clearly labelled or marks will be deducted. (*Hint: assume variable Cin to be the LSB and assign it to S0.*)

(6 marks)

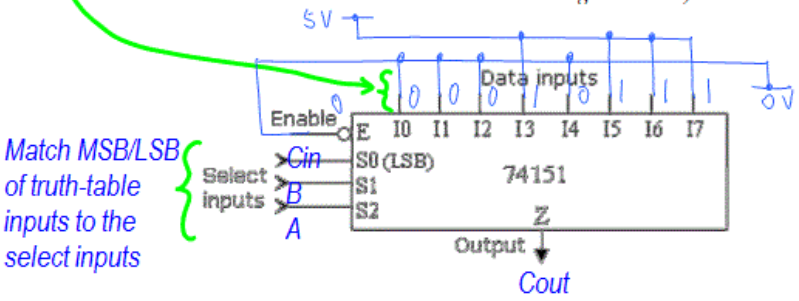
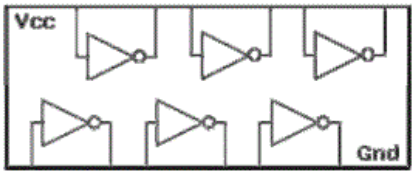


Figure B5.2

B6 Table B6 lists the typical values of the AC and DC parameters (characteristics) for 2 different logic families **of the 7404 Inverter IC**.



7404

Parameter	Unit	Device A	Device B
Vcc	V	5	5
V_{IH} (min)	V	2	2
V_{IL} (max)	V	0.8	0.7
V_{OH} (min)	V	2.4	2.7
V_{OL} (max)	V	0.4	0.5
Icc_H	mA	12	2.4
Icc_L	mA	24	6.6
t_{PLH}	nS	13	9
t_{PHL}	nS	15	8

Table B6

(a) Which device has the higher **output voltage** for logic **High** and what is the value of this voltage?

Device B (2.7V) (2 marks)

(b) Which device can operate at a higher signal frequency? Justify your answer by quoting the correct parameter.

Device B - it has lower propagation delays. (2 marks)

(c) Calculate the High level Noise margin V_{NH} for both devices. Which device has the better noise margin at logic High?

*Device A: 2.4 - 2 = **0.4V** Device B: 2.7 - 2 = **0.7V*** (3 marks)

(Device B has a higher and thus better V_{NH}.)

(d) Calculate the average power consumption **per gate** for device **A**, only. (3 marks)

For device A:

Average Icc = (12 + 24) / 2 = 18 mA.

Average Power = Vcc x Icc(avg) = 5V x 18 mA = 90 mW - per device (with 6 NOT gates).

*Average Power per gate: 90 mW / 6 = **15 mW***

Section C Long Question (20 marks)

C1. A BCD (mod-10) counter (i.e. a counter that counts from 0 to 9 decimal) is connected to a decoder as shown in figure C1. The decoder has an output **Z**, which responds in the following manner:

DCBA	Z
0000	0
0001	0
0010	0
0011	0
0100	0
0101	0
0110	0
0111	0
1000	1
1001	1
1010	x
1011	x
1100	x
1101	x
1110	x
1111	x

- **Z = H** whenever the BCD counter output is **equal to and greater than 8_{10}.**

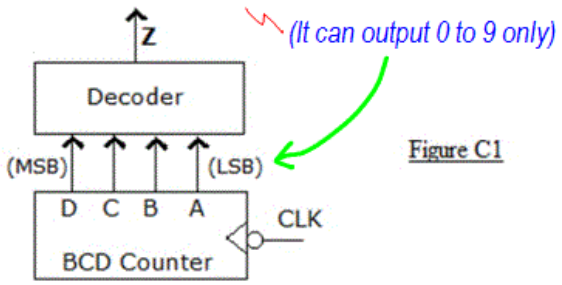


Figure C1

Your task in this question is to design the decoder circuit using two different methods.

(a) Determine the **truth-table** for this **decoder**, showing all the possible input combinations and expected responses at the output **Z**. Use the table format as shown in table C1, where two expected output values are also given as examples. You are reminded that A is the LSB and D is the MSB and all don't care conditions should be indicated as 'X's.

(8 marks)

(MSB)		Inputs	(LSB)	Output
D	**C**	**B**	**A**	**Z**
0	0	0	0	0
:	:	:	:	
:	:	:	:	
1	1	1	1	X

Table C1

(b) Using one **74151,** an **8 to 1 multiplexer** IC, show how you would implement the decoder logic circuit for output **Z** using the truth-table derived in part (a). The 74151 symbol given in figure B5.2 of question B5 is to be used. Your completed circuit must be clearly labelled or marks will not be awarded.

(7 marks)

(c) Using one **74138** decoder IC (see figure B4.1 on page 5) and a NOT gate to invert the output, implement the decoder circuit for output **Z**. Ensure that your circuit is appropriately labelled or marks will not be awarded.

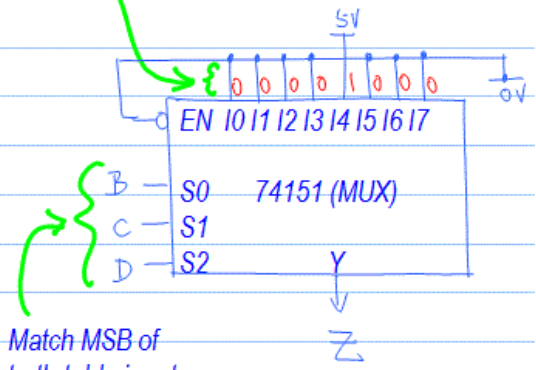
(5 marks)

---------- End of Paper ----------

C1 (b)

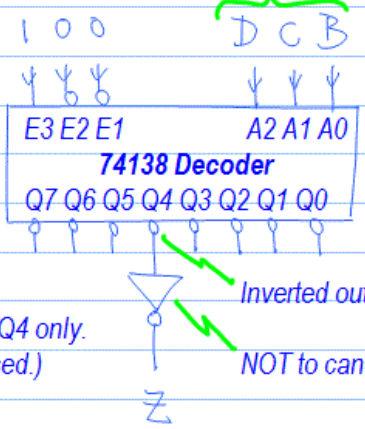
D C B A	Z	
0 0 0 0	0	Z = 0 when DCB = 000 = 0
0 0 0 1	0	
0 0 1 0	0	Z = 0 when DCB = 001 = 1
0 0 1 1	0	
0 1 0 0	0	Z = 0 when DCB = 010 = 2
0 1 0 1	0	
0 1 1 0	0	Z = 0 when DCB = 011 = 3
0 1 1 1	0	
1 0 0 0	1	Z = 1 when DCB = 100 = 4
1 0 0 1	1	
1 0 1 0	x	Z = x when DCB = 101 = 5
1 0 1 1	x	
1 1 0 0	x	Z = x when DCB = 110 = 6
1 1 0 1	x	
1 1 1 0	x	Z = x when DCB = 111 = 7
1 1 1 1	x	

Let's make "don't care" x = 0 here.
(Making x = 1 is also OK.)



Match MSB of truth-table inputs to the select inputs

C1 (c) From part (b) we can see that Z is dependent on D,C,B - not affected by A at all.
Output Z = 1 only when D,C,B = 100 (=4); Z = 0 for other combinations of D,C,B.
Hence we can use a decoder:



Inverted outputs (i.e. active-LOW)

Take output from Q4 only.
(Others are not used.)

NOT to cancel the above inversion