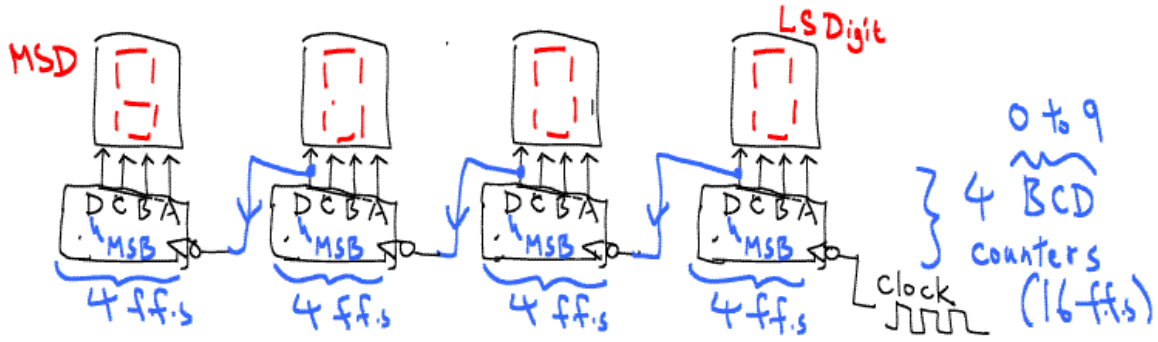
ie one connected to another one

7-35. How many cascaded BCD counters are needed to be able to count up to 8000? How many FFs does this operation require? Compare this with the number of FFs required for a normal binary counter to count up to 8000. Even though it uses more FFs, why is the cascaded BCD method used?

**Recall:**
BCD (Binary Coded Decimal) always uses 4-bit to represent each decimal digit.
The possible BCD values are: 0000 to 1001 (for 0 to 9 in decimal).




Compare with binary counter :

$8000_{10} = \underbrace{1\ 1111\ 0100\ 0000_2}_{13\text{-bit (ie needs 13 f.f.s)}}$

BCD method is used **in some cases** although it uses more flip-flops than binary counter as it can show the decimal digits directly on the 7-segment displays without any conversion.

7-55. Suppose a 74ALS174 is connected as follows:

$$\overline{MR} = \text{HIGH};\ Q_5 \rightarrow D_2;\ Q_4 \rightarrow D_1;\ Q_3 \rightarrow D_0$$

$$D_5 = D_3 = \text{HIGH};\ D_4 = \text{LOW}$$

Assume all FFs have a zero hold-time and are initially LOW.

(a) Determine the states of each FF after a single pulse is applied to *CP*.

(b) Repeat for a second clock pulse.

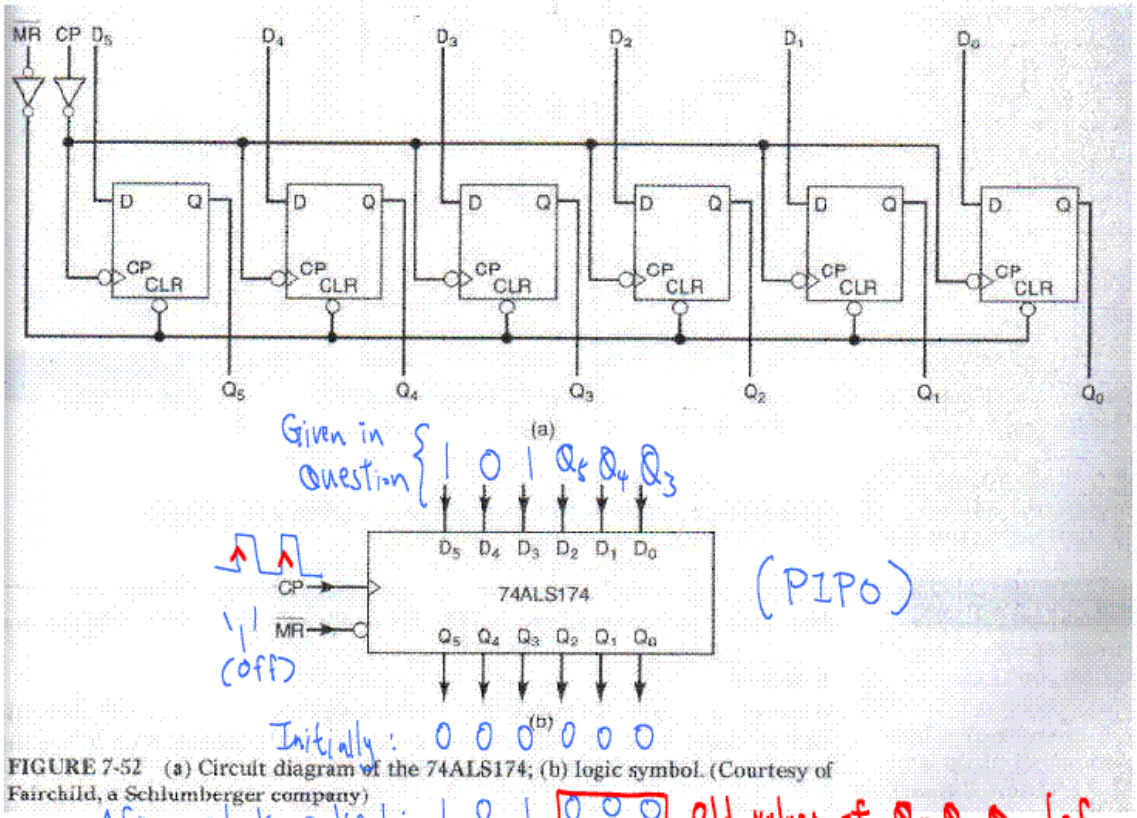



FIGURE 7-52 (a) Circuit diagram of the 74ALS174; (b) logic symbol. (Courtesy of Fairchild, a Schlumberger company)

After clock pulse 1: 1 0 1 [0 0 0] old values of $Q_5\ Q_4\ Q_3$ before PGT

" " " 2: 1 0 1 [1 0 1] old values of $Q_5\ Q_4\ Q_3$ before PGT

7-57. Show how the 4731B chip can be connected as a 256-bit shift register

(SISO)

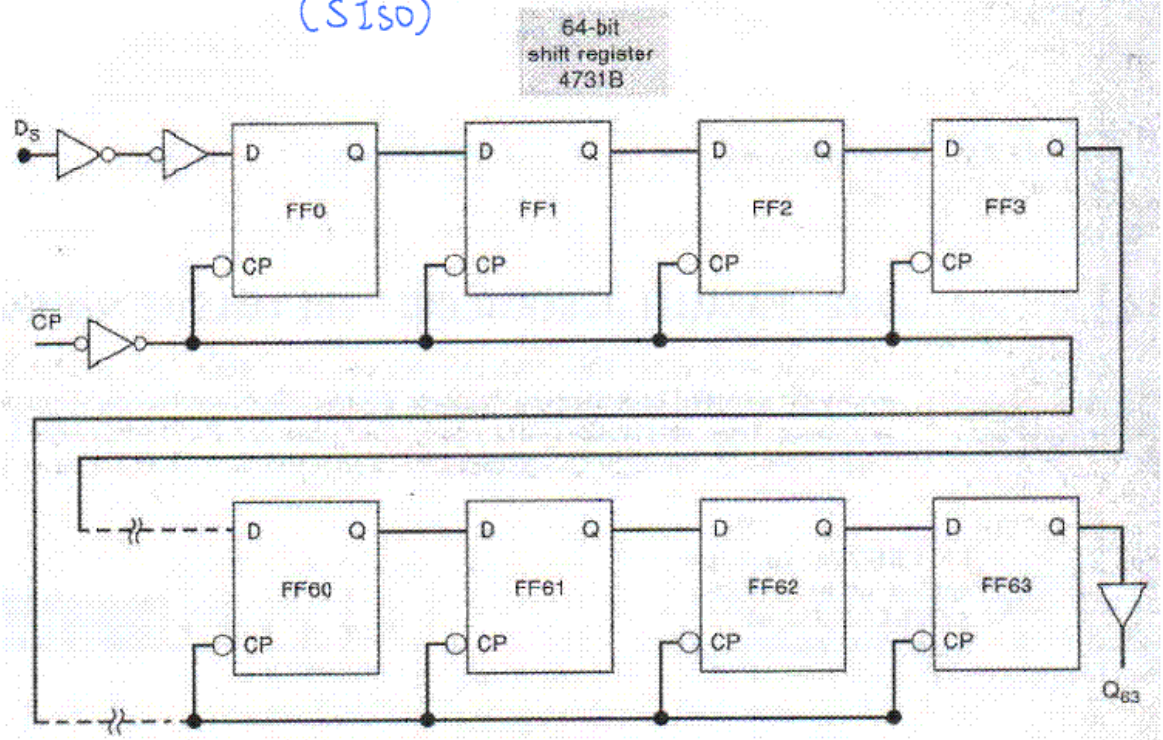



**FIGURE 7-54** Logic diagram for one of four 64-bit shift registers on a 4731B. (Courtesy of Fairchild, a Schlumberger company)