SINGAPORE POLYTECHNIC ET0901

SAMPLE SUMMATIVE CLASS TEST
Diploma in Electrical & Electronic Engineering (DEEE)
2nd Year FT

CA8

DIGITAL SYSTEM DESIGN (ET0901) Time Allowed: 50 Minutes

Instructions to Candidates:

1. This paper consists of TWO sections:
   Section A - 10 Multiple Choice Questions, (40%)
   Section B - 2 Long Questions, (60%)

2. All questions are COMPULSORY.

3. **Section A** : ONLINE using Blackboard . Require Lockdown Browser.
   Go to BB => Assessment < Tab > => SummativeClassTest_MCQ
   Note: Questions similar to Tutorials MCQs. No sample questions for MCQs in this SAMPLE paper.

4. **Section B** : Write your working in this question paper.

5. This test paper consists of 5 pages.

6. Submit this question paper to the invigilator after the test.

7. Ask the lecturer to fill in the Section A (MCQ) marks

Name :_____ Admin_____ Class_____

QUESTION ANSWERED	MARKS	
A(MCQ)		
B1		
B2		
Total		
Percentage		

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SECTION B

ANSWER ALL QUESTIONS

B1 (a) Derive the simplified Boolean expressions for D & E in the lookup table shown in Figure B1(a). [10 marks]

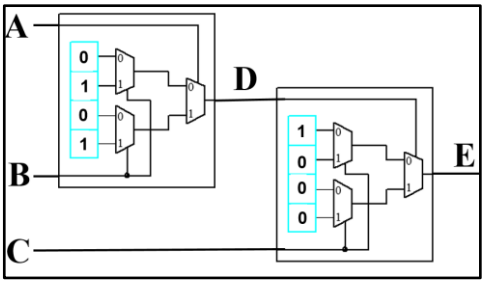

Figure B1(a)

Answer for B1(a)

(b) Write the Verilog code for the circuit in Figure B1(b) using gate instantiations. [20 marks]

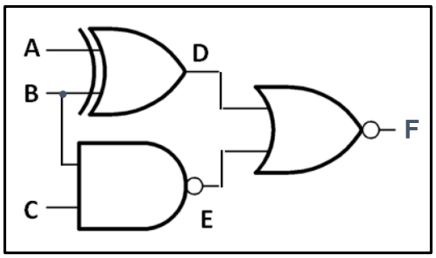

Figure B1(b)

Answer for B1(b)

B2. Figure B2 shows a Verilog code for a sequence detector.

(a) Draw the state diagram for this sequence detector showing the state name, input w and output z. Label the reset state. [20 marks]
(b) Determine the number of flip-flops required for this sequence detector. [5 marks]
(c) What is the input sequence that it is able to detect? [5 marks]

```
module detector (Clock, Reset, w, z);
    input Clock, Reset, w;
    output z;
    reg [2: l] y, Y;
    parameter [2:1] A=2'b00, B=2'b01, C=2'b10, D=2'b11;
    // Define the next state combinational circuit
    always @(w,y)
      case (y)
        A: if (w) Y=B;
            else Y=A;
        B: if (w) Y=B;
            else Y=C;
        C: if (w) Y=D;
            else Y=A;
        D: if (w) Y=B;
            else Y=C;
        default: Y = 2'bxx;
      endcase
    // Define the sequential block
    always @(posedge Reset, posedge Clock)
       if (Reset==1)  y<= A;
       else y <= Y;
    // Define output
    assign z = (y == D);
endmodule
```

Figure 2

Answer for B2

******* End of Paper *******