## Section A Multiple Choice Questions (20 Marks)

**A1.** What is the BCD representation of decimal number 37?

(a) $100101_2$ (b) $11111_2$ (c) $00110111_2$ (d) $110111_2$

Answer: (c)

*BCD – uses 4-bit to represent a decimal digit. 3: $0011_2$, 7: $0111_2$.*

**A2.** How many Full Adder units are required to build a 16-bit parallel Adder?

(a) $8_{10}$ (b) $16_{10}$ (c) $32_{10}$ (d) $64_{10}$

Answer: (b)

*Full Adder is a 1-bit adder – combine N of them to form N-bit adder.*

**A3.** A shift register which inputs data, one bit at a time, but transfer out multiple data bits simultaneously is a:

(a) parallel-in, serial-out register (b) parallel-in, parallel-out register

(c) serial-in, parallel-out register (d) serial-in, serial-out register

Answer: (c)

*Serial: 1 bit at a time. Parallel: multiple bits simultaneously.*

**A4.** To build a Mod-$4096_{10}$ binary counter, the number of JK flip-flops required is:

(a) $9_{10}$ (b) $10_{10}$ (c) $11_{10}$ (d) $12_{10}$

Answer: (d)

*$4096 = 2^{12}$ → 12-bit.*

**A5.** What is the binary code generated at the outputs of the 74147 BCD priority encoder shown in figure A5?

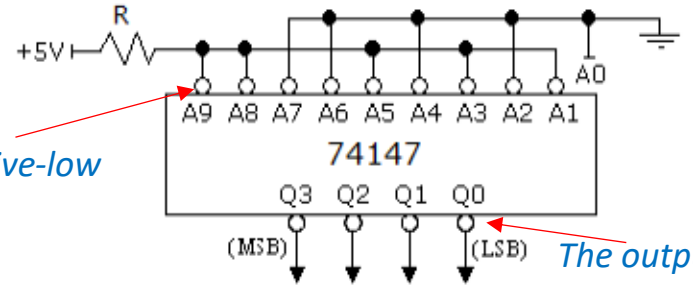



Figure A5

*The inputs are active-low (i.e. '0' is active.)*

*The outputs are inverted*

(a) $Q_3\,Q_2\,Q_1\,Q_0 = 1001_2$ (b) $Q_3\,Q_2\,Q_1\,Q_0 = 0111_2$

(c) $Q_3\,Q_2\,Q_1\,Q_0 = 1000_2$ (d) $Q_3\,Q_2\,Q_1\,Q_0 = 0110_2$

Answer: (c)

*Priority encoder: the output code indicates the highest active input.*

*Highest active input: A7 → Output: $0111_2$ → Inverted output $1000_2$.*

**A6.** The mathematical expression use for calculating the average power consumed by a TTL digital IC is:

(a) $(I_{OL} + I_{OH})/2 * V_{CC}$

(b) $(I_{OL} + I_{CCL})/2 * V_{CC}$

(c) $(I_{OH} + I_{CCH})/2 * V_{CC}$

(d) $(I_{CCH} + I_{CCL})/2 * V_{CC}$

*Answer: (d)*

*Average power = Average Icc x Vcc. (Vcc is constant at 5V.)*

**A7.** There are _____ outputs in a **1-of-64** decoder.

(a) $1_{10}$ (b) $4_{10}$ (c) $6_{10}$ (d) $64_{10}$

*Answer: (d)*

*1-of-64: It means only 1 of the 64 outputs is active.*

**A8.** A Multiplexer accepts data from:

(a) one of many input lines and transfers it to one output line.

(b) one input line and transfers it to one output line.

(c) one of many input lines and transfers it to several output lines.

(d) one input line and transfers it to one of several output lines.

*Answer: (a)*

*Multiplexer: the selected input signal will be channelled to its output.*

**A9.** What is the CLK signal frequency applied to the CLK input of the Mod-10 counter in figure A9?


Figure A9

(a) $2000_{10}$ Hz (b) $3000_{10}$ Hz

(c) $4500_{10}$ Hz (d) $6000_{10}$ Hz

*Answer: (d)*

*The combined MOD = 4 x 10 = 40, hence $f_{CLK}$ = 40 x 150 Hz = 600 Hz.*

**A10.** 'Fan-Out' is defined as the number of logic loads that can be connected to _____ without exceeding the IC manufacturer's specifications.

(a) a single input (b) a single output

(c) all the inputs and outputs (d) the Vcc power supply

*Answer: (b)*

*Fan-out: Number of loads (i.e. other gates' inputs) that one output can drive reliably.*

**B1**(a) What is the range of decimal numbers that can be represented by a 10-bit (including the sign bit) 2's complement signed numbering system? How many different decimal values are there in this range?

(4 marks)

*10-bit → $2^{10}$ = 1024.*

*It has **1024 different numbers**: 512 +ve (including 0) and 512 –ve numbers.*

***Range**: -1 to -512 and 0 to +511 → **-512 to +511.***

(b) Use the 8 bits (including the sign bit) 2's complement system to perform the following addition

Add $-53_{10}$ to $+82_{10}$

(6 marks)

| | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| | **+53** | = | 0 | 0 | 1 | 1 | 0 | 1 | 0 | 1 |
| Negate | Invert: | | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 0 |
| | Plus 1: | | | | | | | | | 1 |
| | **-53** | = | 1 | 1 | 0 | 0 | 1 | 0 | 1 | 1 |
| | **+82** | = | 0 | 1 | 0 | 1 | 0 | 0 | 1 | 0 |
| | **+29** | = | 1 | 0 | 0 | 0 | 1 | 1 | 1 | 0 | 1 |

**B2** The Full-Adder is a combinational logic circuit that adds 3 bits namely, A, B and Cin, to produce a summation result of 2 bits, appropriately labelled as Cout (carry-out) and Sum.

(a) Complete the truth-table of the Full-Adder using a table format as shown in Table B2.

(4 marks)

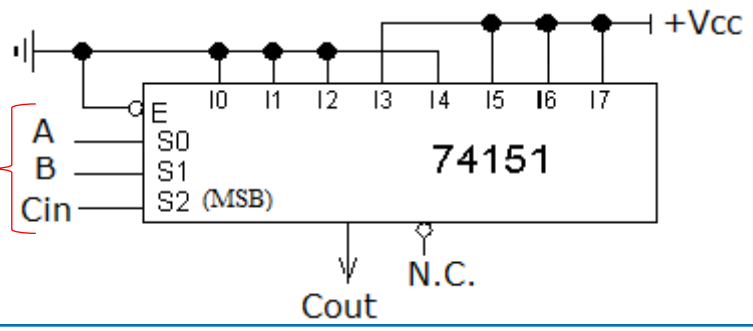
*A + B + $C_{in}$ = $C_{out}$, Sum (2-bit output)*

| Inputs | | | Outputs | |
|---|---|---|---|---|
| Cin | B | A | Cout | Sum |
| 0 | + 0 | + 0 | = 0 | 0 |
| 0 | + 0 | + 1 | = 0 | 1 |
| 0 | + 1 | + 0 | = 0 | 1 |
| 0 | + 1 | + 1 | = 1 | 0 |
| 1 | + 0 | + 0 | = 0 | 1 |
| 1 | + 0 | + 1 | = 1 | 0 |
| 1 | + 1 | + 0 | = 1 | 0 |
| 1 | + 1 | + 1 | = 1 | 1 |

(b) Using one 74151 IC, an 8-input multiplexer (symbol as shown in figure B2), implement the Cout output of the Full Adder. In your implementation, ensure that you label your circuit diagram clearly using the variable names of Cin, B, A and Cout or marks will not be awarded.

(4 marks)

*Match MSB/LSB of MUX select inputs with MSB/LSB of truth-table.*




(c) How many 74151 ICs are required to implement the complete Full Adder circuit?

(2 marks)

***Two 75151 ICs** are required: one for the $C_{out}$ and one for the Sum.*

**B3** Figure B3 shows the circuit of a BCD encoder.

(a) Briefly describe what is an encoder?

*An encoder outputs a binary code indicating which of the inputs is ON.* (2 marks)

(b) Determine the outputs logic levels at Q3, Q2, Q1 and Q0 for the following input conditions:

(i) Inputs A1 to A9 = logic LOW *All inputs are OFF → Output = $0000_2$ (0).*

(ii) Input A7 = logic HIGH. All other inputs = LOW *→ Output = $0111_2$ (7).*

(iii) All Inputs A1 to A9 = logic HIGH *→ Output = $1111_2$ (15).*

(iv) Comment on the code generated in (iii) above and, state whether the encoder is an ordinary or priority encoder. Justify your answer. (8 marks)

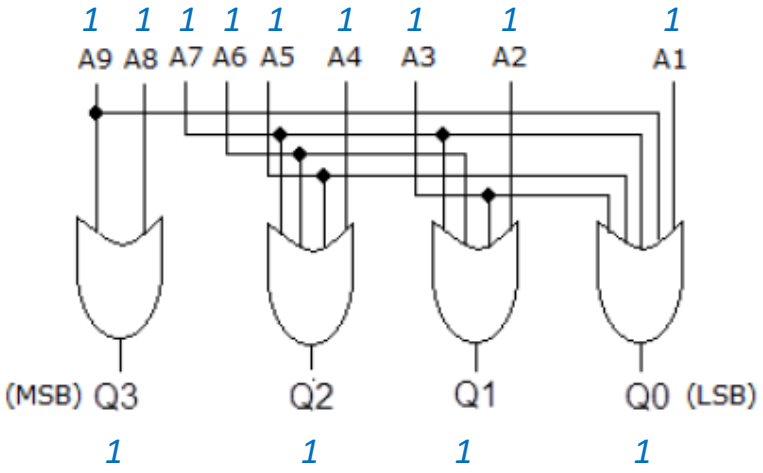



Figure B3

*For a priority encoder, if the highest active input is A9 → Output = $1001_2$ (9).*

*Hence, the above is **not a priority encoder**.*

**B4** Each of the five statements comprising this question describes MSI devices, namely: **Encoder**, **Decoder**, **Multiplexer** and **De-multiplexer**. You are required to state in your answer booklet, the type of MSI device (or MSI devices) being described by each statement. Ensure that your answers are labelled exactly according to each of the statements i.e. [ (a), (b)....(e) ] or marks will not be awarded.

(10 marks)

(a) One of its 10 outputs goes low whenever a BCD code is applied to its inputs.
*BCD decoder.*

(b) A combinational logic circuit can be easily implemented using this device.
*Multiplexer.*

(c) Keyboard actuations on a notebook computer are converted to ASCII codes using this device.
*ASCII encoder.*

(d) This device can be used to route a signal at its single data input to one of its several data outputs.
*De-multiplexer*

(e) These two MSI devices have more inputs than outputs. What are they?
*Multiplexer and Encoder.*

**B5** A counter has a state transition table as shown in Table B5.1.

| CLK | Q3 (MSB) | Q2 | Q1 | Q0 (LSB) |
|---|---|---|---|---|
| ↓ | 0 | 0 | 0 | 0 |
| ↓ | 0 | 0 | 0 | 1 |
| ↓ | 0 | 0 | 1 | 0 |
| ↓ | 0 | 0 | 1 | 1 |
| ↓ | 0 | 1 | 0 | 0 |
| ↓ | 0 | 1 | 0 | 1 |
| ↓ | 0 | 1 | 1 | 0 |
| ↓ | 0 | 1 | 1 | 1 |
| ↓ | 1 | 0 | 0 | 0 |
| ↓ | 0 | 0 | 0 | 0 |
| ↓ | 0 | 0 | 0 | 1 |

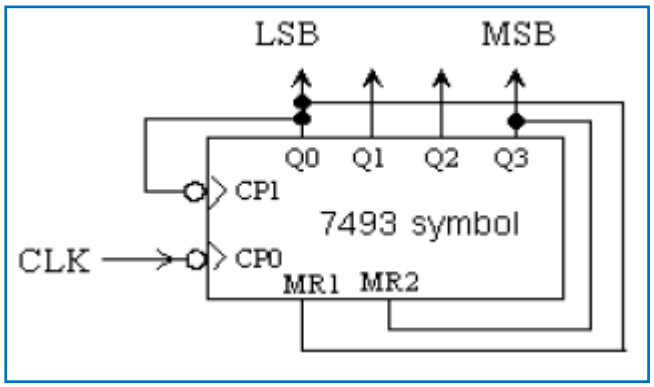
Table B5.1

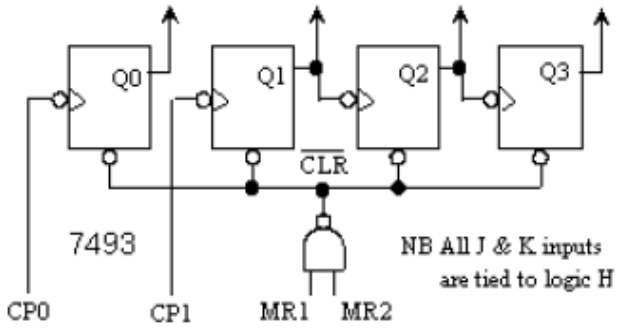
(a) What is the mod-number of this counter? (3 marks)

*One counter cycle: 0 to 8.*
*Hence, **Mod-9.***

(b) Using one 7493 IC, the symbol and internal circuit of which is as given in figure B5.2, show how you would connect the IC to implement the counter of part (a). Draw your circuit in your answer booklet using only the 7493 symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks be deducted. (5 marks)

1. *Connect Q0 to CP1 to form a 4-bit counter.*
2. *For Mod-9 ($1001_2$), connect Q3 (MSB) & Q0 (LSB) to MR1 & MR2.*
3. *Apply clock pulses to CP0.*

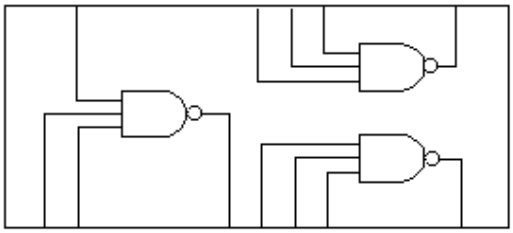



(c) If the signal of frequency at the MSB output of the counter is 900 Hz, what is the frequency of the CLK signal applied to the clock input of this counter? (2 marks)

*Frequency at MSB = Clock frequency / Mod*
*→ Clock frequency = Frequency at MSB x Mod = 900 Hz x 9 = **8100 Hz**.*

**B6** The characteristics of the **74LS10 IC** is as shown in Table B6.



**74LS10**

| Symbol | Parameters | Max | Min |
|---|---|---|---|
| $V_{CC}$ | Supply voltage (v) | 5 | |
| $V_{IH}$ | High level input voltage (v) | | 2 |
| $V_{IL}$ | Low level input voltage (v) | 0.8 | |
| $V_{OH}$ | High level output voltage (v) | | 2.7 |
| $V_{OL}$ | Low level output voltage (v) | 0.4 | |
| $I_{CCH}$ | Power supply current (mA) | 0.8 | |
| $I_{CCL}$ | Power supply current (mA) | 2.2 | |
| $t_{PLH}$ | Propagation delay (nS) | 15 | |
| $t_{PHL}$ | Propagation delay (nS) | 12 | |

(a) Perform the following calculations:

(i) The average power consumption per gate. (3 marks)

*Average power per IC:*

*Average Icc x Vcc = ($I_{CCH}$ + $I_{CCL}$)/2 x Vcc = (0.8+2.2)/2 x 5 = 7.5 mW*

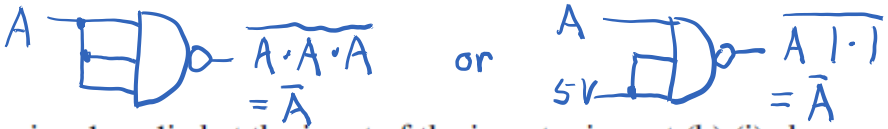
*Average power per gate: 7.5 / 3 =* ***2.5 mW***

(ii) The Low-level noise margin $V_{NL}$. (2 marks)

*$V_{NL}$ = Difference between $V_{OL}$ and $V_{IL}$ = 0.8 – 0.4 =* ***0.4V***

(b) Using one 3-input NAND gate from the 74LS10 IC,

(i) Show how it can be connected as an inverter or NOT gate. (3 marks)




(ii) If the signal applied at the input of the inverter in part (b) (i) changes from logic Low to logic High, how long does it take for the output to respond? (2 marks)

*Input changes from L to H implies output changes from H to L.*

*Hence, the delay is $t_{PHL}$ =* ***12 ns****.*

**C1** Figure C1.1 shows a 2-to-1 Multiplexer with 2 data inputs labelled as $I_0$ and $I_1$ and a single output Z. It has a select input labelled as S which allows either data inputs to be selected and connected to output Z.

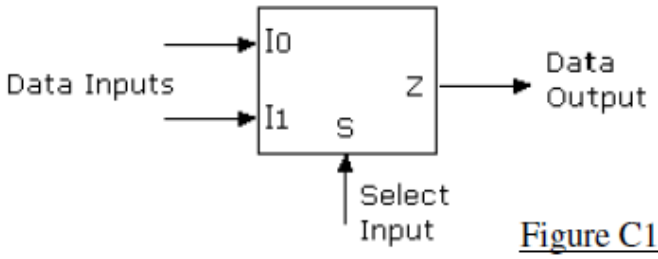



Figure C1.1

| S | Output Z |
|---|---|
| 0 | $Z = I_0$ |
| 1 | $Z = I_1$ |

(a) Complete the truth table of the 2-input multiplexer using a truth table format as shown in Table C1

(4 marks)

| S | $I_1$ | $I_0$ | Z |
|---|---|---|---|
| 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 0 | 1 | 1 | 1 |
| 1 | 0 | 0 | 0 |
| 1 | 0 | 1 | 0 |
| 1 | 1 | 0 | 1 |
| 1 | 1 | 1 | 1 |

*When S = 0, Z = $I_0$*

*When S = 1, Z = $I_1$*

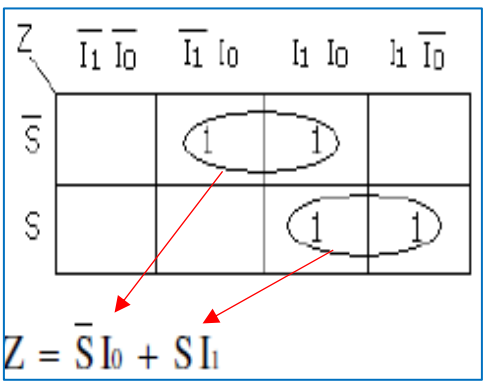
(b) From your completed truth table in part (a), derive the un-simplified Boolean Expression for output Z in a sum-of-products form.

*Z = 1 when (S, $I_1$, $I_0$) are 001, 011, 110 or 111:*

$$Z = \overline{S}\ \overline{I_1}\ I_0 + \overline{S}\ I_1\ I_0 + S\ I_1\ \overline{I_0} + S\ I_1\ I_0$$

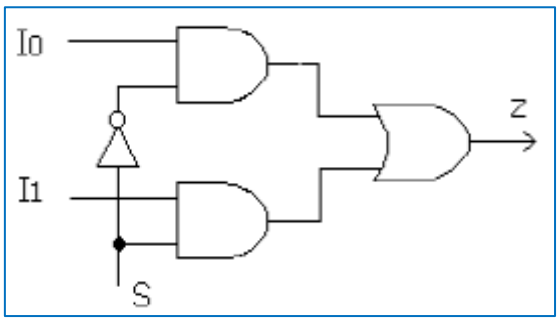
(c) Using the K-map or Boolean theorems, simplify the Boolean expression obtained in part (b).

(4 marks)



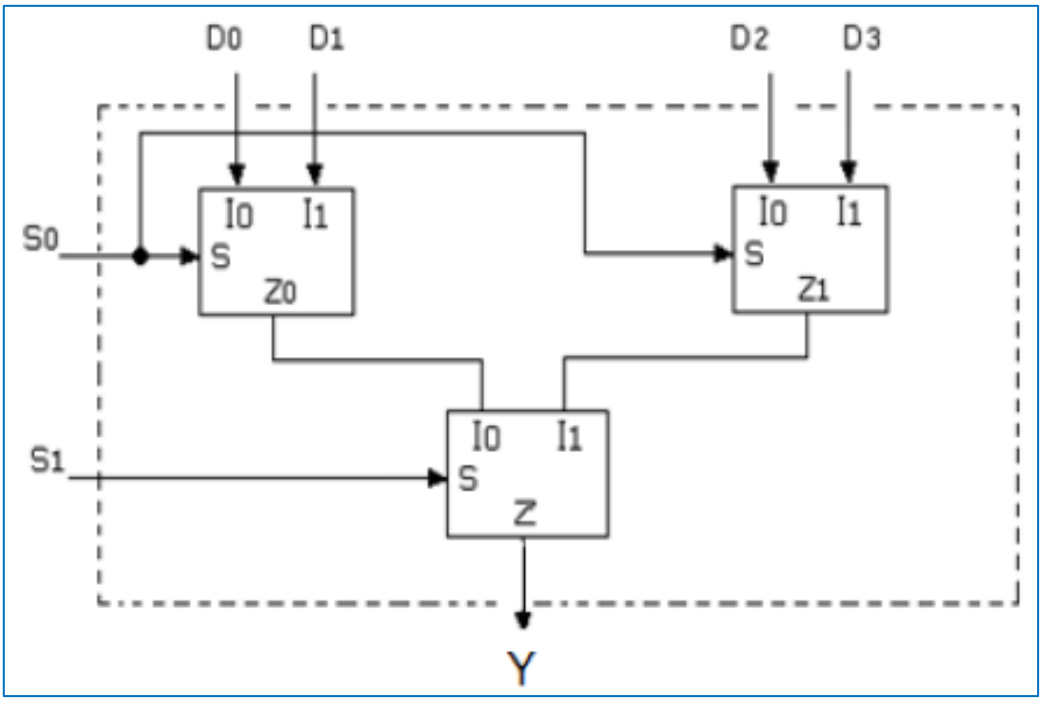
(d) Implement the simplified Boolean expression obtained in part (c) using basic gates of AND, OR and NOT.

(3 marks)




(e) Using three 2-input multiplexer units (see figure C1.1) show how they can be connected together to form a 4-input multiplexer. Use the symbol of the 2-input multiplexer in Figure C1.1 to draw your circuit. Label the the 4 data inputs required as $D_0$, $D_1$, $D_2$, $D_3$ and the two Select inputs required as $S_1$ and $S_0$ and the single output as Y.

(6 marks)




*When* ***($S_1$, $S_0$) = 00***: $Z_0 = D_0$, : $Z_1 = D_2$, : ***$Y = Z_0 = D_0$***

*When* ***($S_1$, $S_0$) = 01***: $Z_0 = D_1$, : $Z_1 = D_3$, : ***$Y = Z_0 = D_1$***

*When* ***($S_1$, $S_0$) = 10***: $Z_0 = D_0$, : $Z_1 = D_2$, : ***$Y = Z_2 = D_2$***

*When* ***($S_1$, $S_0$) = 11***: $Z_0 = D_1$, : $Z_1 = D_3$, : ***$Y = Z_0 = D_3$***