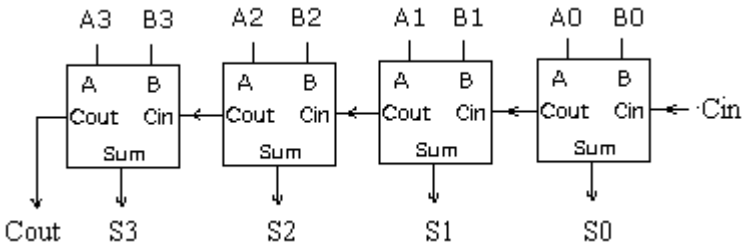
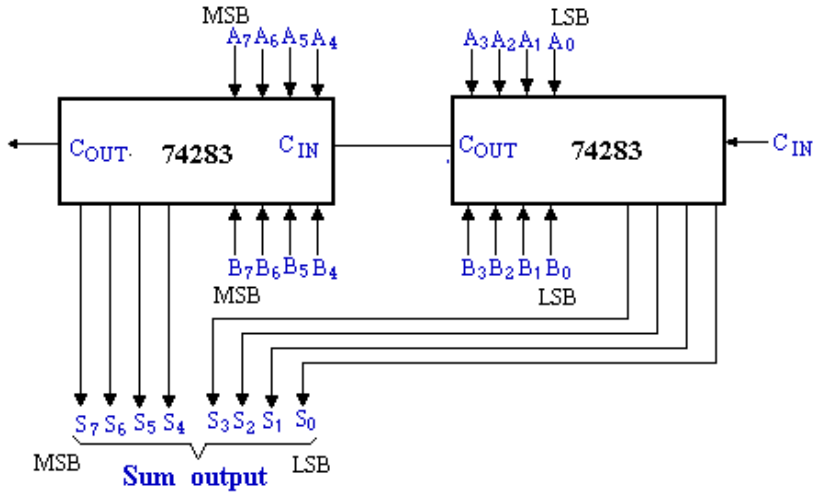
SAMPLE MID-SEMESTER TEST

MODULE: DIGITAL ELECTRONICS 2 MOD. CODE: ET1004

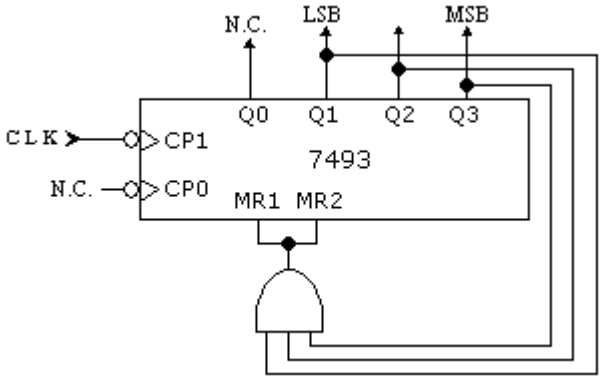
No	SOLUTION
A	**SECTION – A (3 marks each)** 1) (c) 2) (c) 3) (d) 4) (a) 5) (c) 6) (c) 7) (b) 8) (d) 9) (c) 10) (d)
B1 a)	**SECTION – B (15 marks each)** Range in decimal for (i) 16 bits system: 0 to 2^{16}-1 = 0 to 65535_{10} (ii) 6 digit decimal system : 0 to $999{,}999_{10}$
(b)	**i) Add $+65_{10}$ to $+23_{10}$** sign 64 32 16 8 4 2 1 **+65 = 0 1 0 0 0 0 0 1** **+23 = 0 0 0 1 0 1 1 1** **+88 = 0 1 0 1 1 0 0 0**
(c)	ii) Subtract $+26_{10}$ from -73_{10} is = Add -26 to -73 sign 64 32 16 8 4 2 1 **+26 = 0 0 0 1 1 0 1 0** **-26 = 1 1 1 0 0 1 1 0** **+73 = 0 1 0 0 1 0 0 1** **-73 = 1 0 1 1 0 1 1 1** **-99 = ~~1~~ 1 0 0 1 1 1 0 1**

SOLUTIONS

No	SOLUTION
B2 (a)	A 4-BIT Parallel Adder IC contains four interconnected full adders and is able to add two set of 4 bit numbers applied to the A inputs and the B inputs, simultaneously. It produces a sum result of up to 5 bits at the Cout, S3, S2, S1 S0 outputs. 4 Full adder units are required to construct the 7483 4-bit Adder IC. Equivalent functional circuit of 7483: 
(b)	Two 74283 ICs are required.
(c)	

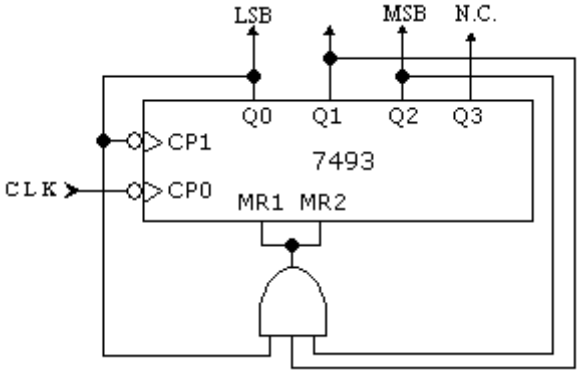
B3 (a) From the given state transition diagram, the modulus of the counter is **Mod-7** as there are 7 unique output states.

(b)



Important for answers
using correct number of flip-flops
use of correct clock input
indicate clearly LSB and MSB outputs
use of external AND gate and connections to the correct counter outputs

OR



(c) Required Clock frequency = 7 * 10 kHz = 70 kHz

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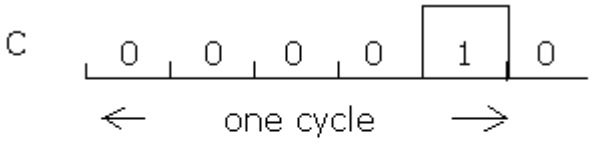
No	SOLUTION
C1 a)	Circuit is an **Astable multivibrator**. Given $F = \frac{0.8}{R1\,C1}$,with R1 = 1600Ω and C1 = 10μF Frequency F $= (0.8 * 10^5)/1600 = 50$ Hz
b)	**Modulus of counter = 5_{10}** because the feedback to the CLR inputs of the flip-flops = $\overline{A} + \overline{C} = \overline{A.C}$ from DeMorgan's theorems. Hence when the counter outputs are momentarily 101, the flip-flops will be cleared. Therefore maximum count is 100 or 4 decimal.
c)	Frequency at output C = 50/5 = 10 Hz. To determine duty cycle at output C, observe the counter sequence at output C ,i.e :

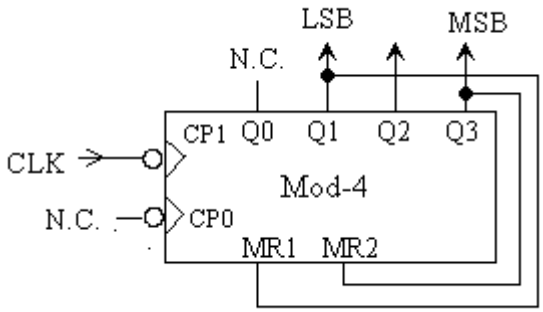
C	B	A
0	0	0
0	0	1
0	1	0
0	1	1
1	0	0
0	0	0
0	0	1



Therefore duty cycle = 1/5 * 100%
= 20 %

SOLUTIONS

No	SOLUTION
C1 (d)	Using the 7493, a mod 5 counter can be constructed as follows:



Important for answers
using correct number of flip-flops i.e. 3 flip-flops
use of correct clock input CP1
indicate clearly LSB and MSB outputs
MR1 MR2 feedback connections to the correct counter outputs

Another possible solution is as shown: