SINGAPORE POLYTECHNIC ET1004

2019/2020 S1 MID-SEMESTER TEST

SAS code: **MST**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Energy Systems Management DESM 1st Year FT

Common Engineering Programme DCEP 1st Year FT

DIGITAL ELECTRONICS 2 Time Allowed : 1.5 Hour

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of Three Sections.

   Section A consists of 10 multiple-choice questions, 3 marks each. No marks will be deducted for blank or wrong answers.

   Section B consists of 3 short questions, each of 15 marks.

   Section C consists of 1 long question of 25 marks

3. Answer **ALL** questions in the accompanying Answer Booklet, unless indicated otherwise.

4. Your admission number and class must be entered in the box provided on the cover page of the Answer Booklet.

5. There are 6 pages in this paper.

Multiple choice question answer procedure

Please **tick** your answers in the **MCQ box** on the back of the cover page of the **Answer Booklet**.

Section A (30 marks)

A1. A JK flip-flop with J, K, $\overline{PRE}$ and $\overline{CLR}$ connected to logic High, has a CLK signal of 30 kHz applied at its CLK input. What will be the frequency of the signal at its Q output?

(a) 0 Hz or D.C. (b) 15 kHz

(c) 30 kHz (d) 60 kHz

A2. A **mod-16**$_{10}$ counter is to be constructed using D flip-flops? How many D flip-flops are required?

(a) 2_{10} (b) 3_{10} (c) 4_{10} (d) 5_{10}

A3. What will be the results at the outputs of a full-adder if its inputs are: augend A = 1, addend B = 1, carry-input Cin = 1 ?

(a) Sum = 0, Cout = 0 (b) Sum = 0, Cout = 1

(c) Sum = 1, Cout = 0 (d) Sum = 1, Cout = 1

A4. What is the mod number of the counter circuit shown in Figure A4?

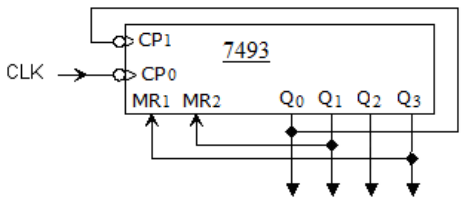

Figure A4

(a) Mod-13_{10} (b) Mod-12_{10} (c) Mod-11_{10} (d) Mod-10_{10}

A5. Which one of the following counters requires the least number of flip-flops?

(a) Decade Counter
(b) A Mod 20 Up/Down counter
(c) A divide by 17 Asynchronous Counter
(d) A ripple counter that repeatedly counts from 0 to 16_{10}

A6. In the 2's complement signed numbering system, a positive decimal number will have _____.

(a) a sign bit of 0 in the LSB position.
(b) a sign bit of 1 in the LSB position.
(c) a sign bit of 0 in the MSB position.
(d) a sign bit of 1 in the MSB position.

A7. A mod-32 naturally resetting counter has five outputs labelled as E D C B A, with E being the MSB and A the LSB. If the signal frequency at its 4^{th} output D is 1 kHz, what is the signal frequency of the CLK signal applied at its clock input??

(a) 8_{10} kHz (b) 16_{10} kHz (c) 32_{10} kHz (d) 64_{10} kHz

A8. A shift register circuit with **one** data input and **one** data output is a _____.

(a) serial-in, parallel-out shift register
(b) parallel-in, serial-out shift register
(c) serial-in, serial-out shift register
(d) parallel-in, parallel-out shift register

A9. A parallel adder which can add unsigned binary numbers in the range from 0 to 63_{10} is to be constructed using the 74LS83 IC, a 4-bit parallel adder IC. How many of these 74LS83 ICs are required to build this parallel adder circuit?

(a) 1_{10} (b) 2_{10} (c) 3_{10} (d) 4_{10}

A10. Which one of the following set of waveforms in Figure A10 corresponds to the output waveforms of a **Mod 5** binary counter?

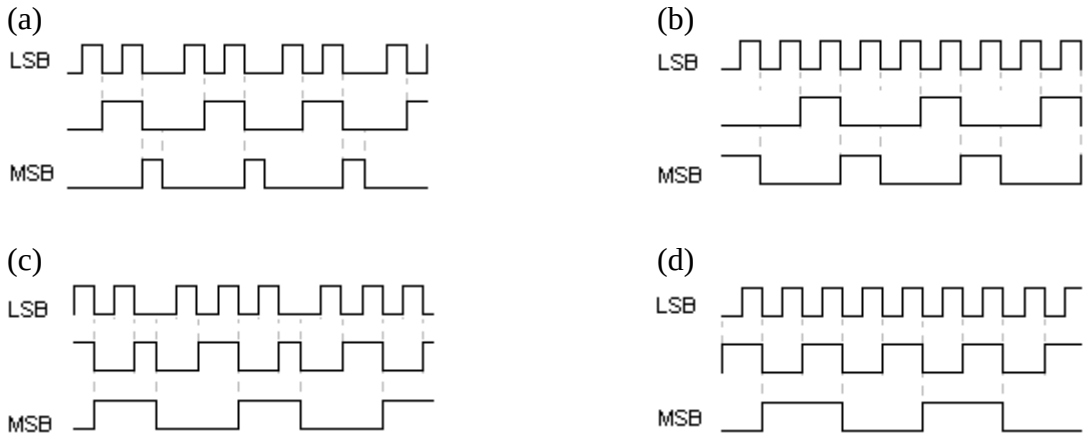

Figure A10

Section B (45 marks)

B1(a) Perform the following calculations using the 2's complement signed numbering system. You are to assume that each number is to be represented by 8 bits, including the sign bit. All steps and **workings must be shown** or marks will be deducted.

(i) Add $+59_{10}$ to $+33_{10}$ (4 marks)

(ii) Add -21_{10} to $+67_{10}$ (6 marks)

(b) Express the following numbers in BCD format and hence, perform the addition of the numbers using BCD arithmetic.

(i) Add $+255_{10}$ to $+27_{10}$ (5 marks)

B2 The full adder is a combinational circuit that adds 3 bits: 'A', 'B', and carry-input 'Cin' to produce a 2-bit summation result appropriately named, as 'Sum' and Carry-out 'Cout'. Draw the symbol of the full adder using the labels: A, B, Cin, Sum and Cout for the inputs and outputs, respectively.

(3 marks)

(b) The 74283 (see Figure B2) is a 4-bit parallel adder IC.
Briefly describe what is a 4-bit parallel adder?
If this 4-bit parallel adder is to be constructed using the full adder unit, how many full-adder units are required for the 4-bit parallel adder? Using the correct number of full adders, draw the equivalent functional circuit of this 4-bit parallel adder.

(9 marks)

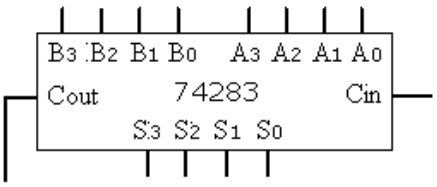

Figure B2

(c) A 12-bit parallel adder is to be constructed using the 74283 IC. How many of these 74283 ICs are required to construct this parallel adder circuit? You are **not** required to draw the circuit.

(3 marks)

B3(a) Given a periodic clock signal as shown in Figure B3, calculate its

(i) Period

(ii) Duty cycle

(iii) Signal frequency

(5 marks)

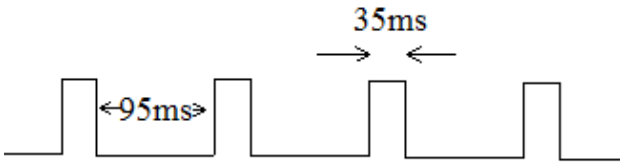

Figure B3

(b) Each of the 5 statements comprising this part of the question describes a counter or shift register circuit. State in your answer booklet, the type of counter or type of shift register circuit being described by each statement. Ensure that your answers are labelled correctly according to each of the statements i.e. [(i), (ii)....(v)] or marks will not be awarded.

(10 marks)

(i) There are ten unique states in this counter.

(ii) The total propagation delay for this type of counters is directly proportional to the number of flip-flops used.

(iii) This circuit inputs multiple data bits simultaneously and outputs a single bit at a time.

(iv) All flip-flops for this category of counters are clocked at the same time.

(v) Each flip-flop in this counter divides its clock input frequency by a factor of 2

Section C (25 marks)

C1 Refer to the diagram shown in Figure C1.1, which shows a cascade of 3 counters.

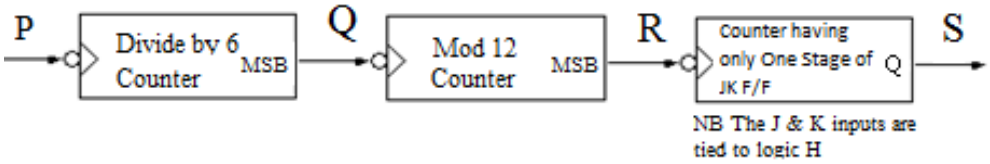

Figure C1.1

(a) Which counter has the highest MOD number? What is its MOD number?

(3 marks)

(b) If the frequency of the signal at point **R** is 1 kHz, what are the frequencies of the signals at points **P** and **S**? What is overall Modulus for the cascade of 3 counters

(9 marks)

(c) Using the 7493 counter IC, symbol and internal circuit as shown in Figure C1.2, construct the MOD 12 counter. Draw the circuit in your answer booklet using the 7493 symbol. Ensure that all inputs and outputs are clearly labelled.

(7 marks)

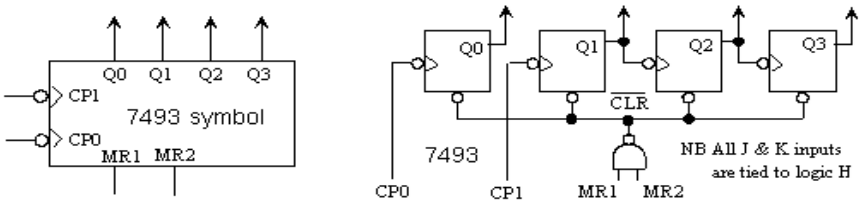

Figure C1.2

(d) Draw the state transition diagram for the MOD 12 counter.

(3 marks)

(e) The MOD 12 counter starts from the state 0010 and 122_{10} clock cycles are applied to its clock input. At the end of the 122_{10} clock cycles, what will be the values at the outputs of the counter?

(3 marks)

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