A1. The decimal number -49 (minus 49), when expressed in the 8-bit two's complement signed numbering system, is equal to:

(a) 00110001_2 (b) 11001110_2 (c) 10110001_2 (d) 11001111_2

Answer: (d)

+49 in 8-bit: 00110001. Invert: 11001110, plus 1: 11001111= -49

A2. To configure an 8-bit parallel adder using the 7483 adder IC (Figure A2), a 4-bit adder IC, two of these ICs are required and,

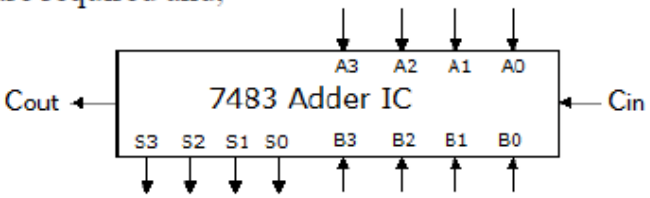


Figure A2

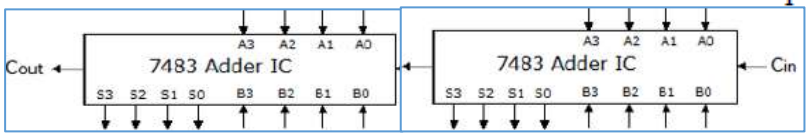
(a) the MSB Sum output S3 of the first adder IC (the LSB unit) must be connected to the LSB data input of the second adder IC (the MSB unit).

(b) the Cout output of the first adder IC must be connected to the Cout output of the second adder IC.

(c) the Cin input of the second adder IC must be connected to the Cout output of the 1st adder IC.

(d) the Cin input of the second adder IC must be connected to the Cin input of the first adder IC

Answer: (c)



A3. What is the maximum Modulus (Mod-number) that can be attained by a 6_{10} flip-flop ripple counter?

(a) 6_{10} (b) 16_{10} (c) 64_{10} (d) 128_{10}

Answer: (c)

6 flip-flops: $2^6 \rightarrow 64$.

A4. The signal frequency at the MSB output of a counter is 3 kHz and the clock signal frequency at its input is 120 kHz. What is the modulus (mod number) of this counter?

(a) Mod-16_{10} (b) Mod-20_{10} (c) Mod-40_{10} (d) Mod-60_{10}

Answer: (c)

Mod = f_{CLK} / f_{MSB} = 120 kHz / 3 kHz = 40

A5. How many clock pulses (CLK) are required to load (or input) binary data to a 16-bit parallel-in, serial-out shift register?

(a) 1_{10} CLK (b) 8_{10} CLK (c) 16_{10} CLK (d) 17_{10} CLK

Answer: (a)

Parallel-in: all bits are loaded in at the same time.

A6. What is the timing parameter that specifies the minimum time required to maintain the logic levels stable at the control inputs of a D flip-flop **prior to** the application of the active clock transition?

Set-up time: the time which D must not change before PGT/NGT.

(a) Set-up time t_{su} (b) Propagation delay t_{pd}

(c) Hold time t_{hd} (d) CLK period T

Answer: (a)

Hold time: the time which D must remain unchanged after PGT/NGT.

A7. For the multiplexer circuit connected as shown in Figure A7, select the correct Boolean expression generated at output Y.

	S_1 S_0	Y
(0)	00	I_0=R
(1)	01	I_1=S
(2)	10	I_2=T
(3)	11	I_3=V

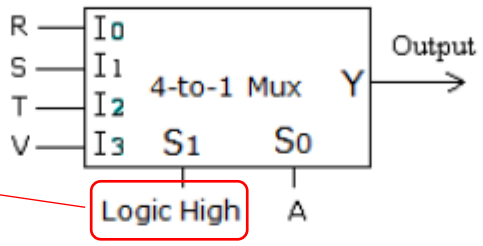


Figure A7

(a) $Y = \overline{A}R + AS$ (b) $Y = \overline{A}TV + ATV$

(c) $Y = \overline{A}T + AV$ (d) $Y = AS + \overline{A}T$

Answer: (c)

*When S_0 = **A = 0, Y = T.** When S_0 = **A = 1, Y = V.***

A8. A 74138 decoder IC is connected as shown in Figure A8. Select the correct statement that describes the outcome at the outputs.

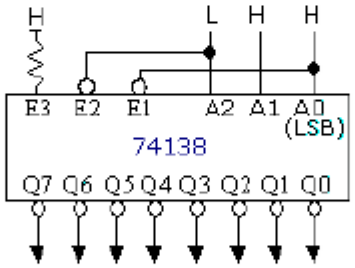


Figure A8

(a) Only output Q3 goes Low (b) Only output Q6 goes Low

(c) All the outputs go Low (d) All the outputs remain High.

Answer: (d)

E3, E2, E1 must be 1, 0, 0 to enable, otherwise all outputs are inactive (1).

A9. 'Fan-Out' is defined as the number of logic loads that can be connected to _____ without exceeding the IC manufacturer's specifications.

(a) a single input (b) a single output

(c) all the inputs and outputs (d) the Vcc power supply

Answer: (b)

Fan-out: how many inputs each output can drive reliably.

A10. A shift register which loads data bits one bit at a time, and transfers out multiple bits, simultaneously, is a_____.

(a) parallel-in, parallel-out register (b) parallel-in, serial-out register

(c) serial-in, parallel-out register (d) serial-in, serial-out register

Answer: (c)

Serial: 1 bit at a time. Parallel: multiple bits simultaneously.

B1(a) Express the following pairs of numbers in BCD format and hence, perform the addition of the numbers using BCD arithmetic.

Add $+127_{10}$ to $+93_{10}$

(4 marks)

+127	=	0	0	0	1^1	0	0	1	0	0	1	1	1
+93	=					1	0	0	1	0	0	1	1
	=	0	0	0	1^1	1	0	1	1^1	1	0	1	0
						+	1	1	0	+	1	1	0
+220	=	0	0	1	0	0	0	1	0	0	0	0	0

The sum of this 4-bit is above 9

Add 6 to compensate

(b) Use the 8 bits (including the sign bit) 2's complement signed numbering system to perform the following addition

Add -63_{10} to $+92_{10}$

(6 marks)

		sign	64	32	16	8	4	2	1
+63	=	0	0	1	1	1	1	1	1
Invert all bits, then plus 1:									
-63	=	1	1	0	0	0	0	0	1
+92	=	0	1	0	1	1	1	0	0
+29	=	~~1~~	0	0	0	1	1	1	0	1

8-bit result

Discard the 9th bit

B2(a) Briefly, state and describe two uses of the enable inputs.

(4 marks)

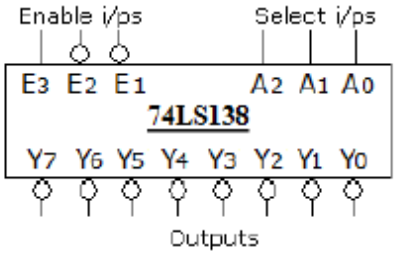


Figure B2

1. *For combining 2 or more 74LS138 ICs to form a bigger decoder.*
2. *Either E1 or E2 can be used as the data input when the 74LS138 IC is being used as a de-multiplexer.*

(b) If output Y7 is to be selected, what are the logic levels required at the Enable and Select inputs?

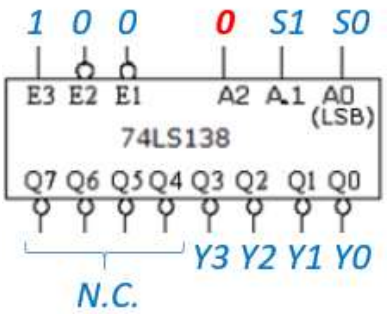
(2 marks)

All enable inputs must be active: E1, E2, E3 = 0, 0, 1.

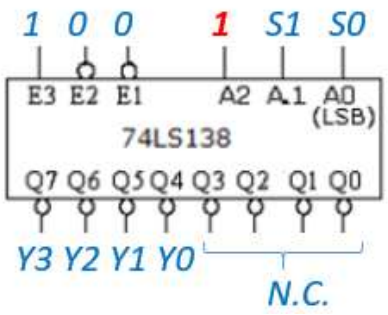
Select inputs A2, A1, A0 must be: 1, 1, 1 (i.e. 7_{10}).

(c) Using one 74LS138 IC, show how the the IC can be connected as a 2-to-4 decoder. Your circuit diagram, to be drawn in your answer booklet, must be clearly labelled, showing all required inputs and outputs. The select inputs required should be labelled as S1, S0 and the four outputs should be labelled respectively as Q3 to Q0, where Q3 is the MSB, and Q0 is the LSB.

(4 marks)



Alternatively:



B3(a) Briefly explain what is the main difference between an BCD ordinary encoder and a BCD priority encoder?

(3 marks)

An ordinary encoder assumes only 1 of the inputs is ON, otherwise it may give a wrong BCD output.

A priority encoder will give a BCD output representing the highest input which is ON.

(b) Determine the outputs (in the order Q3 Q2 Q1 Q0) of the BCD encoder circuit shown in Figure B3 when:

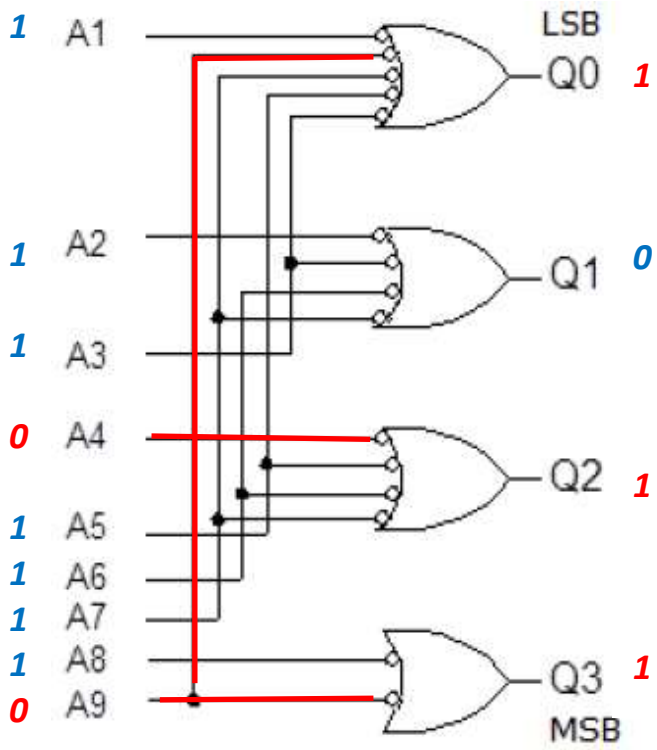
i) All inputs are logic HIGH *All inputs are OFF: Q3,Q2,Q1,Q0 =0000 (0_{10})*

ii) All inputs HIGH except input A4. *Only A4 is ON: Q3,Q2,Q1,Q0 =0100 (4_{10})*

iii) All inputs HIGH except input A9. *Only A9 is ON: Q3,Q2,Q1,Q0 =1001 (9_{10})*

iv) All inputs HIGH except inputs A4 and A9. *Only A4 & A9 are ON - see below:*

(4 marks)



(c) Is the circuit shown in Figure B3 a priority encoder? If it is not, briefly explain why? Hint: Illustrate your answer with an example of the code generated when 2 or more inputs are activated. (3 marks)

No, a priority encoder will give a BCD output representing the highest input which is ON (0).

When both A9 & A4 are ON, the output should be =1001 (9_{10}).

B4 The sum-of-products expression for output Z of a logic circuit is given as:

$$Z = \overline{C}\,\overline{B}\,\overline{A} + \overline{C}\,B\,\overline{A} + C\,\overline{B}\,\overline{A} + C\,B\,\overline{A} + C\,B\,A$$

0 0 0 *0 1 0* *1 0 0* *1 1 0* *1 1 1*

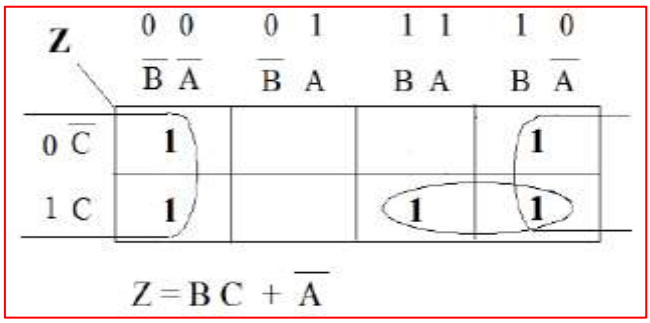
(a) Determine the truth-table for output Z of the logic circuit.

(2 marks)

	C	B	A	Z
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1
3	0	1	1	0
4	1	0	0	1
5	1	0	1	0
6	1	1	0	1
7	1	1	1	1

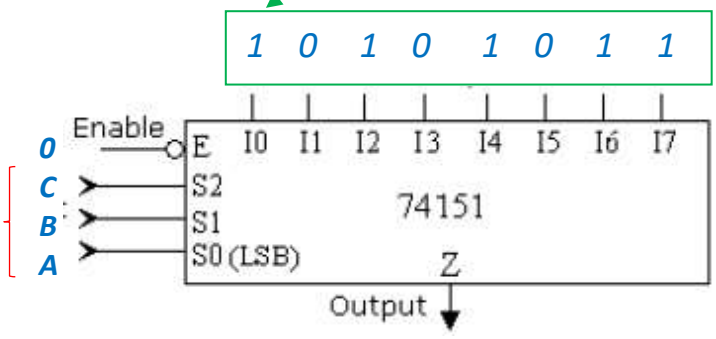
(b) Using the k-map, simplify the Boolean expression of output Z.

(3 marks)



(c) Given the logic symbol of 74151 as shown in Figure B4, show how you would connect the multiplexer to generate the expression for output Z. Your circuit must be clearly labelled or marks will be deducted. (*Hint: assume variable A to be the LSB and assign it to S0.*)

(5 marks)



Match MSB of truth-table inputs with MSB of select inputs

B5 The symbol and internal circuit of the 7493, a 4-bit binary counter IC, is shown in figure B5.

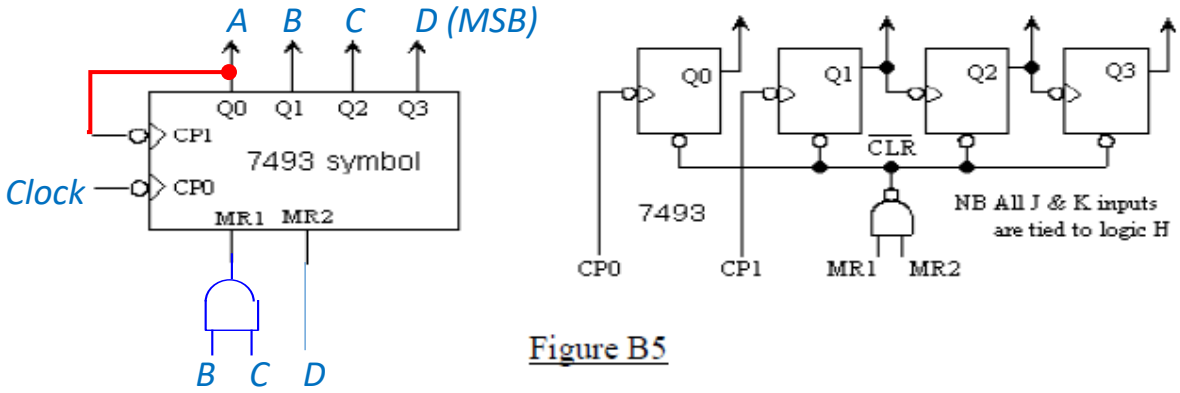


Figure B5

(a) Using one 7493 counter IC, and any other gates as necessary, show how you would connect a mod-14_{10} up-counter. Indicate and label clearly all the connections made to the IC, in particular the CLK input, the LSB and MSB outputs. What is the maximum count in binary for this mod-14_{10} counter?

(6 marks)

Mod-14 = 1110_2

reset when D,C,B,A=1,1,1,0

or D=1, C=1 & B=1.

(b) If the signal frequency at the MSB output of the mod-14_{10} counter is 14 kHz, what is the signal frequency of the clock signal applied at its CLK input?

(2 marks)

Freq at MSB = Freq at CLK ÷ Mod.

Hence, Freq at CLK = 14 kHz x Mod = 14 kHz x 14 = 196 kHz.

(c) Determine the duty cycle of the signal at the MSB output given that the CLK signal is a perfect square wave.

(2 marks)

Dec	DCBA
0	0000
1	0001
2	0010
3	0011
4	0100
5	0101
6	0110
7	0111
8	1000
9	1001
10	1010
11	1011
12	1100
13	1101

At the MSB (D), there are 6 '1's in a counter cycle of 14 clock pulses.

Hence, duty-cycle = 6 / 14 x 100% = 42.9%

B6 The **7402** IC is described as a **Quad 2-input NOR gate IC.**

Table B6 list some of the electrical parameters of the **7402 IC**.

Symbol	Parameters	Max	Min
V_{CC}	Supply voltage (V)	5	
V_{IH}	High level input voltage (V)		2
V_{IL}	Low level input voltage (V)	0.8	
V_{OH}	High level output voltage (V)		2.4
V_{OL}	Low level output voltage (V)	0.4	
$I_{CC(H)}$	Supply current (mA), outputs High	10	
$I_{CC(L)}$	Supply current (mA), outputs Low	22	
t_{pLH}	Propagation delay (nS)	20	
t_{pHL}	Propagation delay (nS)	15	

Table B6

(a) From the description given, how many NOR gates are there in the 7402 IC?

'Quad' means 4 – there are 4 gates in it.

(1 mark)

(b) What is the guaranteed maximum value of the output voltage when the output is at logic Low?

V_{OL} : 0.4V

(2 marks)

(c) Calculate the power dissipation for the whole IC and hence, for each gate.

(4 marks)

Average P = V_{CC} x Average I_{CC}

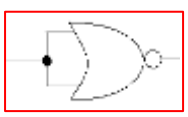
Average I_{CC} = ($I_{CC(H)}$ + $I_{CC(L)}$) / 2 = (10 + 22)/2 = 16 mA

Average P = 5V x 16 mA = 80 mW for the IC

Average P per gate: 80 mW / 4 = 20 mW

(d) Using one NOR gate, show how it can be connected as an inverter. Hence, determine the time taken for the **output** to respond to an input signal changing from Low to High?

(3 marks)



Input changing from low to high

→ output changing from high to low → t_{pHL} = 15 ns

(t_{pHL} and t_{pLH} always refer to the output.)

C1. A **BCD number** detector circuit is required to be designed (see figure C1.1). This combinational circuit has an output **Z**, and responds to BCD numbers as follows:

- **Z = 1** whenever the BCD inputs are 1_{10}, 3_{10}, 8_{10} and, 9_{10}.

You are to assume that **only BCD** numbers are applied to the inputs of this circuit, i.e. there are don't care conditions.

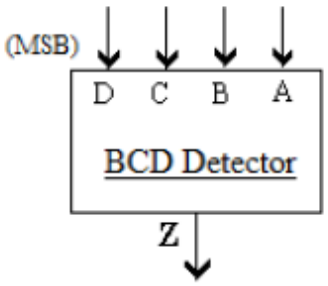


Figure C1.1

(a) Determine the truth-table for this circuit using a table format as shown in Table C1. You are reminded that input D is the MSB and input A is the LSB and all '**don't care**' conditions should be denoted as 'X's.

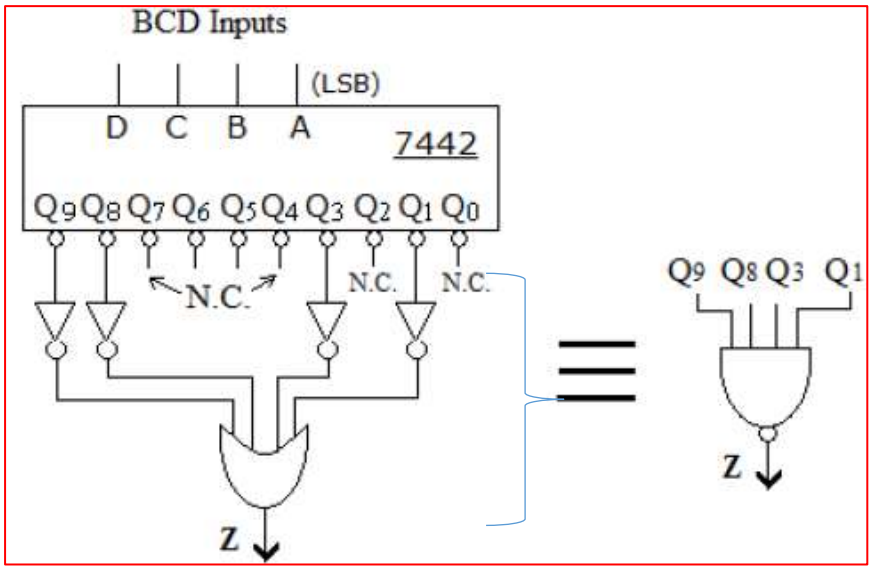
(8 marks)

	BCD Inputs				Output
	D	**C**	**B**	**A**	**Z**
0	0	0	0	0	0
1	0	0	0	1	1
2	0	0	1	0	0
3	0	0	1	1	1
4	0	1	0	0	0
5	0	1	0	1	0
6	0	1	1	0	0
7	0	1	1	1	0
8	1	0	0	0	1
9	1	0	0	1	1
10	1	0	1	0	X
11	1	0	1	1	X
12	1	1	0	0	X
13	1	1	0	1	X
14	1	1	1	0	X
15	1	1	1	1	X

4-bit BCD is from 0-9 only, hence don't care the output for 10-15

(b) Using the 7442 BCD decoder (symbol is as shown in Figure C1.2) and, any other logic gates as necessary, implement the BCD number detector circuit as specified in the question

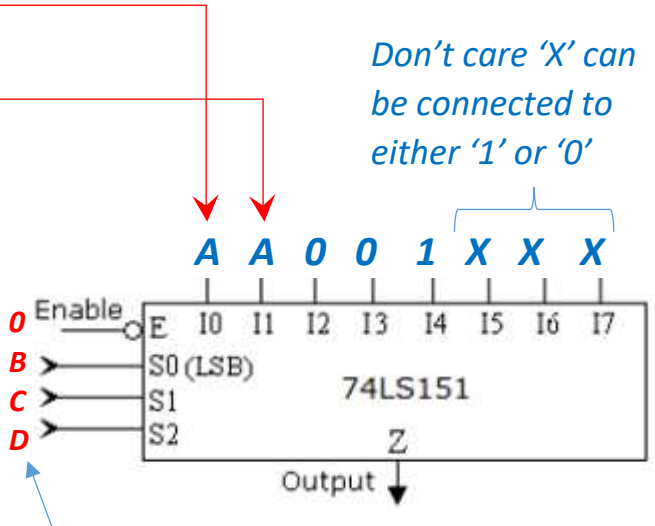
(6 marks)



(c) Using one 74151 multiplexer IC, the symbol of which is shown in Figure B4, show how you would implement the logic circuit for output Z using the truth-table derived in part (a). The 74151 symbol given in Figure B4 on page 6 is to be used, and input variables D, C, and B should preferably be assigned to multiplexer select inputs S2, S1, and S0, respectively. Your completed circuit must be clearly labelled or marks will be deducted.

(6 marks)

	BCD Inputs				Output	
	D	C	B	A	Z	
0	0	0	0	0	0	Z=A
	0	0	0	1	1	
1	0	0	1	0	0	Z=A
	0	0	1	1	1	
2	0	1	0	0	0	Z=0
	0	1	0	1	0	
3	0	1	1	0	0	Z=0
	0	1	1	1	0	
4	1	0	0	0	1	Z=1
	1	0	0	1	1	
5	1	0	1	0	X	Z=X
	1	0	1	1	X	
6	1	1	0	0	X	Z=X
	1	1	0	1	X	
7	1	1	1	0	X	Z=X
	1	1	1	1	X	



Don't care 'X' can be connected to either '1' or '0'

Match MSB of truth-table inputs with MSB of select inputs