SINGAPORE POLYTECHNIC ET1003

SEMESTER EXAMINATION (SAMPLE)

SAS code: **EXAM**

Diploma in Electrical and Electronic Engineering DEEE 1st Year FT /EO

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Clean Energy DCEG 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

DIGITAL ELECTRONICS 1

Time Allowed : 2 hours

Instructions to Candidates

1. The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2. This paper consists of **THREE** sections:
   Section A - 10 Multiple Choice Questions, 2 marks each.
   Section B - 6 Short Questions, 10 marks each.
   Section C - 1 Long Question of 20 marks.

3. Answer **ALL** questions in the accompanying Answer Booklet, unless otherwise indicated. Start each question in Sections B and C on a new page.

4. This Examination Paper consists of 9 pages.

5. Your admission number and module class must be entered in the box provided on the cover page of your Answer Booklet.

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A Multiple Choice Questions (20 Marks)

1. How many (bits) binary digits are required to count up to a maximum of decimal 9999?

(a) 12 bits
(b) 13 bits
(c) 14 bit
(d) 15 bits

2. What is the equivalent function of the circuit shown in figure A2?

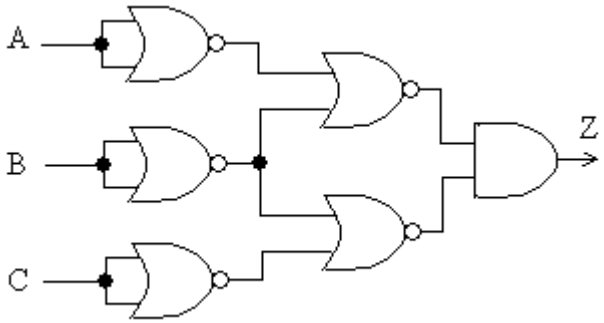

Figure A2

(a) 3-input NAND
(b) 3-input AND
(c) 3-input NOR
(d) 3-input OR

3. What is the minimum number of D flip-flops required to store an 8-digit decimal number expressed in BCD format?

(a) 4_{10}
(b) 8_{10}
(c) 32_{10}
(d) 256_{10}

4. Which of the following statements is a result of simplifying a Boolean expression?

(a) More gates are added to the design.
(b) Only NAND gates are used to implement the design.
(c) Unnecessary logic gates are removed.
(d) Inverter gates are removed, as they are not necessary to the design

5. In the circuit shown in figure A5, a logic HIGH output would be produced if:

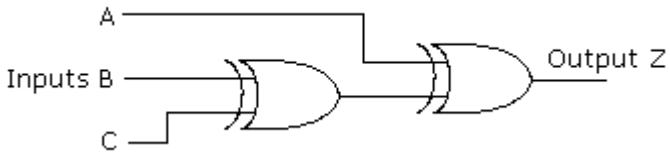

Figure A5

(a) inputs A = B = C = 0.
(b) inputs A = 0, and B = C = 1.
(c) inputs A = B = 1, and C = 0.
(d) inputs A = B = C = 1.

6. In using a JK flip-flop, if the output is to **Toggle** on application of the clock signal, the required settings for the JK flip-flop should be:

(a) J = 1, K = 1
(b) J = 0, K = 0
(c) J shorted to K
(d) K = NOT J

7. In using a D flip-flop, if the output is to **Toggle** on application of the clock signal, the required settings/connections for the D flip-flop should be:

(a) D = Not Q
(b) D = 1
(c) D = Q
(d) Impossible to toggle

8. Given the Boolean expression:

$$Y = [\overline{(A+B)} + \overline{(C \cdot D + \overline{F} + G)} + (E \cdot \overline{F} + G + \overline{H})] + K$$

If A = 0, B = 1, C = 1, D = 0, E = 1, F = 1, G = 0 , H = 1, what is Y?

(a) Y = Not K
(b) Y = 0
(c) Y =1
(d) Y = K

9. How many different sets of input combinations will produce a Low from a 4-input AND gate?

(a) 1_{10}
(b) 4_{10}
(c) 15_{10}
(d) 1

10. If the numbering system used is base-7, which one of the following numbers would be invalid?

(a) 2475_7
(b) 2315_7
(c) 1001001_7
(d) 236.43_7

Section B Short Questions (60 marks)

B1 (a) Convert the Decimal number 7788_{10} to Binary and Hexadecimal

(4 marks)

(b) Convert the following numbers to decimal or base 10.

(6 marks)

(i) 10110011_2

(ii) 56271_8

(iii) $3FAD_{16}$

NB: All workings in question B1 must be shown or marks will not be awarded.

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B2. Table B2 shows the truth table of a logic circuit with 3 inputs A B C and an output Y.

A	B	C	Y
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	0
1	0	0	1
1	0	1	1
1	1	0	1
1	1	1	0

Table B2

(a) Derive the unsimplified Boolean expression for output Y.

(2 marks)

(b) Using Boolean theorems or the K-map, simplify the Boolean expression obtained in part (a).

(5 marks)

(c) Implement the simplified Boolean expression of part (b) using only NAND gates.

(3 marks)

B3 Study the circuit shown in figure B3 carefully and hence, determine the logic states at outputs Q1 and Q2 of the two flip-flops for input logic values as specified in Table B3. You are to assume that the initial values of Q1 and Q2 are logic H.

(10 marks)

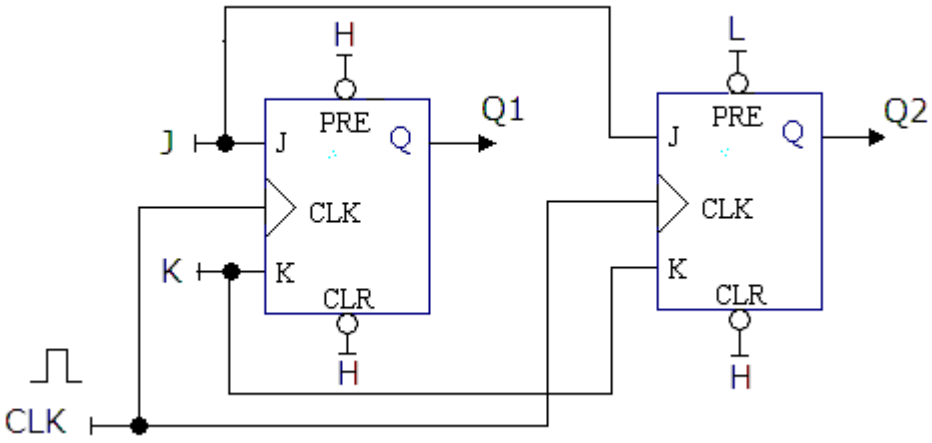

Figure B3

CLK	J	K	Q1	Q2
L	L	L	H	H
↓	L	L	?	?
↑	L	H	?	?
↑	H	L	?	?
↓	H	H	?	?
↑	H	H	?	?

Table B3

NB: The truth table shown in Table B3 must be completed and entered in your Answer Booklet or marks will not be awarded.

B4 (a) Refer to the circuit of Figure B4.1

(i) Write the Boolean expression for the output Z.

(3 marks)

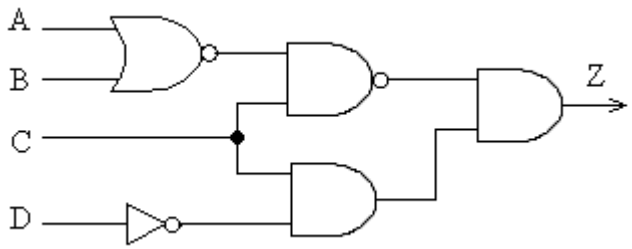

Figure B4.1

(ii) Use Boolean theorems to simplify the expression obtained in (i) above.

(3 marks)

(b) Derive the simplest possible Boolean expression from the K-Map of figure B4.2

(4 marks)

Z	$\overline{C}\,\overline{D}$	$\overline{C}D$	CD	$C\overline{D}$
$\overline{A}\,\overline{B}$	1	1	1	1
$\overline{A}B$	1	0	0	1
AB	1	0	0	1
$A\overline{B}$	1	1	1	1

Figure B4.2

B5(a) For the Clock signal shown in Figure B2.1, determine the frequency and duty cycle of the signal. If the duty cycle of the clock signal is to be changed to 70% without its frequency being changed, what circuit or device can be used to achieve this? You need not draw the circuit or device. Just state what is required.

(6 marks)

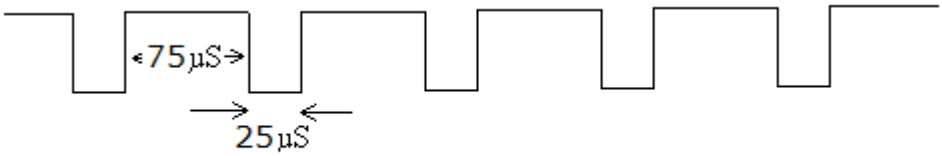

Figure B5.1

B5(b) Calculate the value of resistor *R* in the Astable circuit shown in figure B5.2, given that the frequency at its output is: $F = \frac{0.8}{R\,C}$ = 80 kHz, and R, the value of the capacitor is 0.1 uF..

(4 marks)

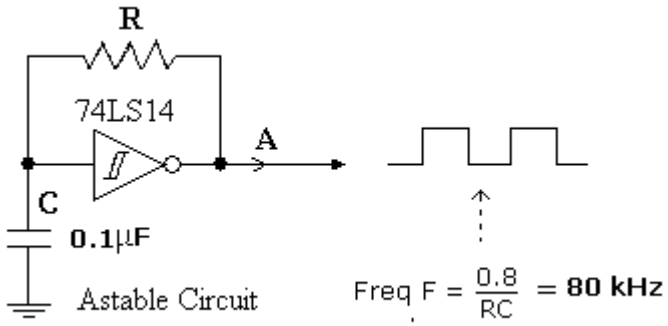

Figure B5.2

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B6 Refer to Figure B3. Draw the output waveforms at A, B, and C given the CLK and $\overline{PRE}$ waveforms as shown. Assume all outputs of the Flip-Flops are zero initially and all propagation delays are negligible. You may enter the answer on the question paper.
(10 marks)

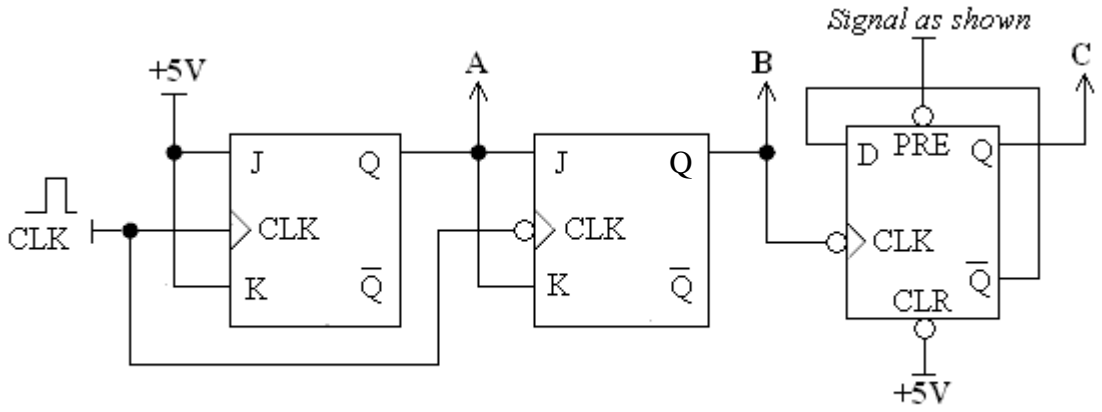
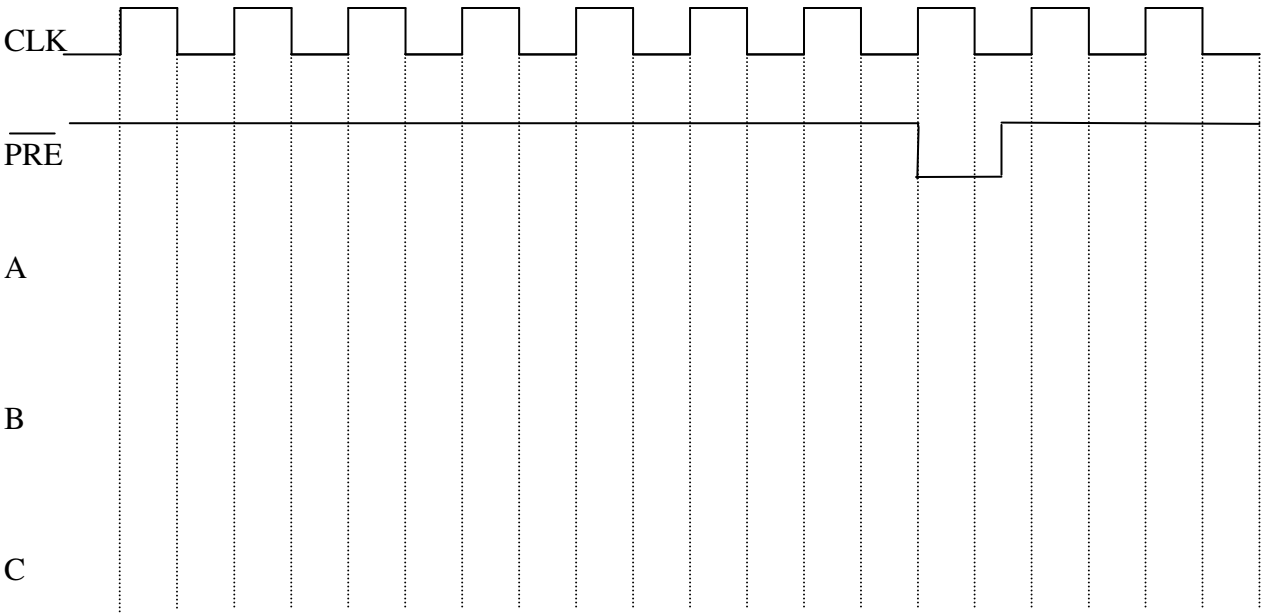


Figure B3



Section C Long Question (20 marks)

C1 A hexadecimal number detector with 4-bit inputs D, C, B and A, and a single output Z, is required to be designed (figure C1). The detector output Z goes high whenever the 4-bit inputs are hexadecimal digits: $\mathbf{0}_H$, $\mathbf{2}_H$, $\mathbf{5}_H$, $\mathbf{7}_H$, $\mathbf{8}_H$, $\mathbf{A}_H$, $\mathbf{D}_H$ and $\mathbf{F}_H$.

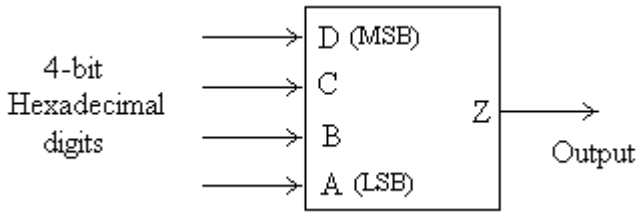


Figure C1: block diagram of Hex number detector circuit

Inputs				Output
D	**C**	**B**	**A**	**Z**
0	0	0	0	1
0	0	0	1	0
:	:	:	:	?
:	:	:	:	?
1	1	1	0	0
1	1	1	1	1

Table C1

(a) Complete the truth table for the hexadecimal number detector using a table format as shown in Table C1, where 4 input combinations and their expected output values are given as examples. Hence state the Boolean expression for output Z in a sum-of-products form.

(8 marks)

(b) Use the Karnaugh Map **or** Boolean theorems to simplify the Boolean expression obtainedin part (a).

(5 marks)

(c) Implement the simplified expression obtained in (b) using the **least** possible number of gate(s).

(3 marks)

(d) Implement the simplified Boolean expression obtained in part (b) using only NAND gates.

(4 marks)

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