SINGAPORE POLYTECHNIC   ET1004

2015/2016 SEMESTER 2 EXAMINATION

Diploma in Electrical & Electronic Engineering DEEE 1st Year FT

Diploma in Computer Engineering DCPE 1st Year FT

Diploma in Aerospace Electronics DASE 1st Year FT

Diploma in Energy Systems Management DESM 1st Year FT

Diploma in Common Engineering DCEP 1st Year FT

SAS code:
EXAM

DIGITAL ELECTRONICS II   Time Allowed : 2 hours

Instructions to Candidates

1.   The attention of candidates is drawn to the Rules of Conduct of Examination found on the back of the Answer Booklet.

2.   This paper consists of **THREE** sections:

   Section A   -   10 Multiple Choice Questions, 2 marks each.

   Section B   -   6 Short Questions, 10 marks each.

   Section C   -   1 Long Question of 20 marks.

3.   Answer **ALL** questions in the accompanying Answer Booklet. Start each question in Sections B and C on a new page.

4.   This Examination Paper consists of 8 pages

5.   Your admission number and module class must be entered in the box provided on the cover page of your Answer Booklet.

Multiple choice question answer procedure

Please tick the correct answer in the box provided at the back of the cover page in the answer booklet. No marks will be deducted for incorrect answers.

Section A   Multiple Choice Questions (20 Marks)

1.   The range of decimal values for a 2's complement signed numbering system is defined as from $+1023_{10}$ to -1024_{10}. How many bits (including the sign bit) are used in this 2's complement signed numbering system?

   (a) 12_{10} bits   (b) 11_{10} bits   (c) 10_{10} bits   (d) 9_{10} bits

2.   The outcome of a BCD arithmetic addition operation is: 0001 0010. Which one of the following sets of decimal numbers could have been added?

   (a) $+9_{10}$ and $+9_{10}$ (b) $+8_{10}$ and $+5_{10}$
   (c) $+8_{10}$ and $+4_{10}$ (d) $+1_{10}$ and $+2_{10}$

3.   To construct a 32-bit parallel adder using the 7483, a 4-bit parallel adder IC, how many 7483 ICs are required?

   (a) $+4_{10}$ (b) $+6_{10}$ (c) $+8_{10}$ (d) $+10_{10}$

4.   A **Mod-10_{10} BCD up-counter** starts with the output state of 0101_2. What will be the value at its outputs after the application of 103_{10} clock cycles to its clock input?

   (a) 0110_2 (b) 0111_2
   (c) 1000_2 (d) 1001_2

5.   Binary data is to be transferred from the W, X, Y and Z outputs of a combinational logic circuit to a single input digital device. Which one of the following shift registers can be used for this purpose?

   (a)   Serial-input, serial-output shift register

   (b)   Parallel-input, parallel-output shift register

   (c)   Serial-input, parallel-output shift register

   (d)   Parallel-input, serial-output shift register

6. The symbol of a 74147 BCD priority encoder is as shown in figure A6. Which one of the following sets of input conditions is necessary for the outputs Y_3 to Y_0 to be 1000_2?
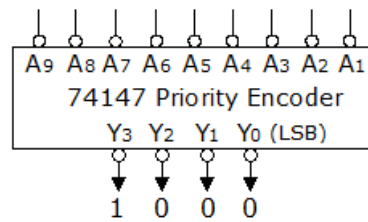

Figure A6

(a) All inputs are Low, except A_8 = High

(b) All inputs are High, except A_8 = Low

(c) Inputs A_7, A_8, A_9 = Low; Inputs A_1 to A_6 = High

(d) Input A_7 = Low; Inputs A_8, A_9 = High; Inputs A_1 to A_6 = don't care

7. Which one of the following application examples cannot be implemented using the Multiplexer?

(a) Combining bit streams from several digital sources into a single bit stream.

(b) Serial-to-parallel conversion of binary data.

(c) Implementation of combinational logic functions.

(d) Parallel-to-serial conversion of binary data.

8. How many select lines are there in a 1-of-16 decoder/demultiplexer?

(a) 16_{10} (b) 5_{10} (c) 4_{10} (d) 1_{10}

9. The correct mathematical expression to calculate the average power consumed by a TTL digital IC is:

(a) $(I_{CCH} + I_{OH})/2 \ast V_{CC}$

(b) $(I_{IH} + I_{IL})/2 \ast V_{CC}$

(c) $(I_{OL} + I_{CCL})/2 \ast V_{CC}$

(d) $(I_{CCH} + I_{CCL})/2 \ast V_{CC}$

10. The parameter that defines how much electrical noise a digital IC can tolerate is:

(a) Noise Margin

(b) Speed-power product

(c) Standard unit load

(d) Fan-out

Section B   Short Questions (60 marks)

B1   Use the 8 bits (including the sign bit) 2's complement signed numbering system to perform the following additions:

   (a)   Add $+26_{10}$ to $+53_{10}$

   (b)   Subtract $+34_{10}$ from $+75_{10}$

(10 marks)

   NB: **All workings** for question B1 must be **shown or marks** will **not** be awarded.

B2   The 7442, as shown in figure B2, is a BCD-to-Decimal decoder.
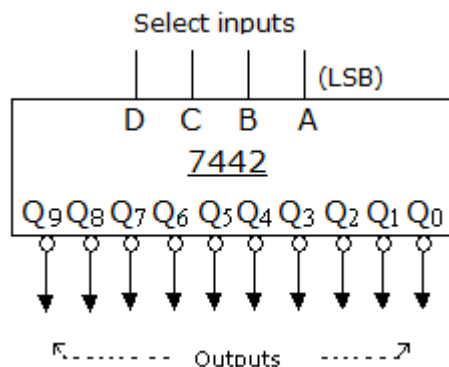

Figure B2

   (a) If the data to the select inputs DCBA is 1000_2, what will be the output states at each output Q_0 to Q_9?

(2 marks)

   (b) If output Q_6 is to be selected, what must be the combination applied to the select inputs DCBA (in this order)? And what happens to output Q_6 when it is selected?

(2 marks)

   (c) Briefly described what is a 1-of-4 decoder? What is another common name for this 1-of-4 decoder?

(2 marks)

   (d) Using one 7442 IC, show how this IC can be connected as a 1-of-4 decoder. Ensure you labelled your circuit clearly or marks will be deducted. Any input(s) that needs logic Low or High must be clearly indicated as such and any unused outputs must be labelled as N.C. (abbreviation for No connections).

(4 marks)

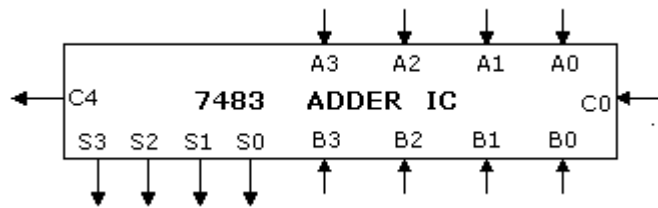B3.   The 7483 as shown in figure B3 is described as a 4-bit parallel adder IC.

Figure B3

(a) Briefly explain what is a 4-bit parallel adder? If the full adder unit is used to construct this 4-bit parallel adder IC, how many full adder units are required?

(3 marks)

(b) If $C_4 S_3 S_2 S_1 S_0 = 1\ 0\ 1\ 1\ 0$ and, $B_3 B_2 B_1 B_0 = 1\ 1\ 1\ 0$, respectively, what will be the binary value at the inputs A_3, A_2, A_1, A_0 if $C_0 = 1$?

(3 marks)

(c) If a **4-bit** (including the sign bit) **2's complement** signed numbering system is used, what are the equivalent decimal numbers being added and the equivalent decimal sum result in part(b)? How should the carry-out bit C_4 be treated in this case?

(4 marks)

B4   The Boolean expression: $X = \overline{C} B A + C \overline{B} A + C B \overline{A}$ is to be implemented using an 8-input multiplexer .

(a) From the given Boolean expression, determine the truth table for output X. Note that in your truth-table input variable C should be designated as the MSB.

(4 marks)

(b) Using one 74151 multiplexer IC, show how you would implement the output X using the truth-table derived in part(a). The 74151 symbol given in figure B4 is to be used and input C should be assigned to the multiplexer select input S_2. Your completed circuit must be clearly labelled or marks will be deducted
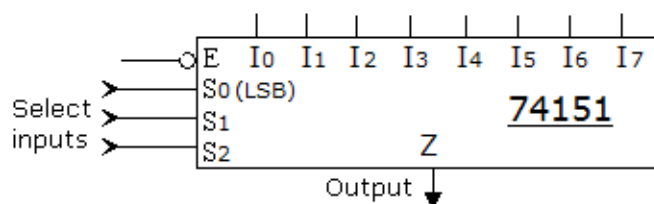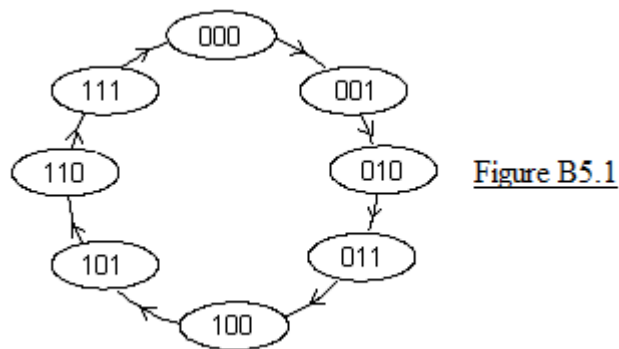
(6 marks)

Figure B4

B5   A counter has a state transition diagram as shown in figure B5.1.

Figure B5.1

(a) What is the mod-number of this counter?

(3 marks)

(b) If a clock signal of frequency 1000 Hz is applied to the clock input of this counter, what is the signal frequency and duty cycle at its MSB output?

(3 marks)

(c) Using one 7493 IC, the symbol and internal circuit of which is as given in figure B5.2, show how you would connect the IC to implement the counter of part (a). Draw your circuit in your answer booklet using only the 7493 symbol. You must ensure that all the inputs and outputs of your circuit diagram are labelled clearly or marks will be deducted.

(4 marks)
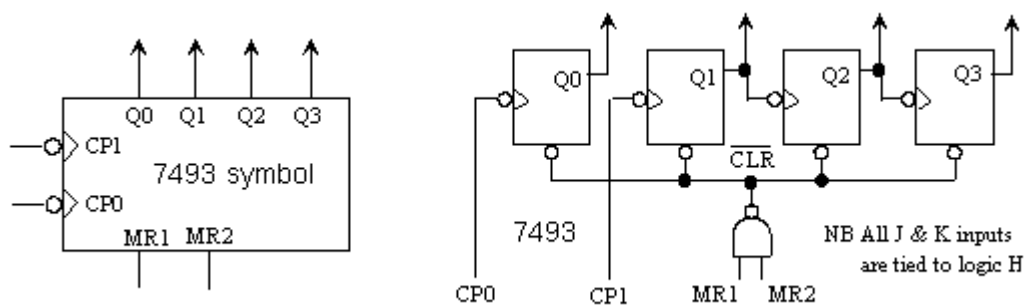
Figure B5.2

B6 Typical performance ratings and voltage parameters for five series of the TTL family of logic devices are given in the table B6. The values shown in the table are on **a per gate basis.**

|	**74**	**74S**	**74LS**	**74AS**	**74ALS**
*Performance ratings **per gate***					
Propagation delay (nS)	9	3	9.5	1.7	4
Power dissipation (mW)	10	20	2	8	1.2
Speed-power product (pJ)	90	60	19	13.6	4.8
Max. clock rate (MHz)	35	125	45	200	70
Fan-out (same series)	10	20	20	40	20
Voltage parameters in Volts					
VOH (min)	2.4	2.7	2.7	2.5	2.5
VOL (max)	0.4	0.5	0.5	0.5	0.4
VIH (min)	2	2	2	2	2
VIL (max)	0.8	0.8	0.8	0.8	0.8

Table B6

(a) Which TTL series has the lowest guaranteed output voltage for logic High and what is the value of this voltage?

(2 marks)

(b) If chargeable batteries (e.g. Lithium Ion) are to be used to power the circuit to be built, which TTL series would you use and why?

(2 marks)

(c) Determine the Low-level noise margin V_{NL} for the 74LS series?

(3 marks)

(d) A simple digital circuit consisting of **12 NOR** gates constructed from **three 7402** ICs (74 standard series) is connected to a dc supply voltage of **5V**. Calculate the average supply current drawn from this 5V power supply.

(3 marks)

Section C

C1.   A **decoder** for a mod-10, BCD up-counter (i.e. a counter that counts in the BCD sequence) is required (see figure C1). The decoder has an output Z, which responds in the following manner:

- **Z = H** when the BCD counter output is **greater than 7_{10}** .
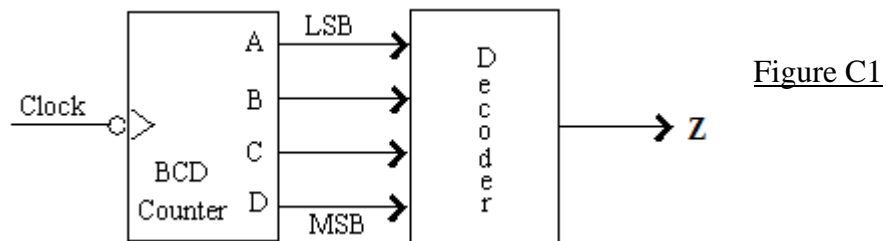
Figure C1

Your task in this question is to design this BCD up-counter and the decoder using two different methods.

(a) Using the 7493 counter IC (symbol as shown in figure B5.2 on page 6), implement the BCD up-counter. Ensure that your circuit diagram is clearly labelled or marks will be deducted.

(5 marks)

(b) Determine the truth-table for this decoder, showing all the possible input combinations and expected responses for output **Z**. Use a table format as shown in Table C1. You are reminded that A is the LSB and D is the MSB and all don't care conditions should be indicated as 'X's.

(5 marks)

MSB	**Inputs**		LSB	**Output**
D	**C**	**B**	**A**	**Z**
0	0	0	0	0
:	:	:	:	
1	1	1	1	X

Table C1

(c) Given one 74151 multiplexer IC, show how you would implement the decoder logic circuit for output **Z** using the truth-table derived in part (b). The 74151 symbol shown in figure B4 on page 5 is to be used and decoder input D should be assigned to multiplexer select input S2. Your completed circuit must be clearly labelled or marks will be deducted.

(6 marks)

(d) Using one 7442 BCD decoder IC as shown in figure B2 on page 4, and one other 2-input logic gate, implement the decoder for the BCD counter as specified in the question.

(4 marks)

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