KHOI PHAM

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EDUCATION

Purdue University West Lafayette, IN
Bachelor of Science in Computer Engineering GPA: 3.85/4.0 May 2025
Enrolled in Purdue ECE 4+1 BS/MS Program
Relevant Coursework: Data Structures and Algorithms, Digital System, ASIC Design, Microprocessor, Computer Architecture

SKILLS

Software: C/C++, Python, Java, JavaScript, Bash, LaTeX, SQL
Hardware: SystemVerilog, RISCV/MIPS ISA, KiCad, Arduino, QuestaSim, Innovus, Oscilloscope, Multimeter, Soldering
Professional Organization: Purdue IEEE (Chair of Social Events 2022-2023), Purdue Eta Kappa Nu

EXPERIENCE

BorgWarner Drive Systems Kokomo, IN
PRODUCT ENGINEERING INTERN May – Aug 2024

- Validated test boards to model statistical performance of ASIC chips under the presence of electromagnetic fields.
- Programmed the Zynq™ 7000 SoC using C and SystemVerilog to emulate digital system designs.
- Developed an ASIC test program in Python and C to communicate with the test board via serial ports and SPI.

Dr. Jung Research Group, Department of Physics and Astronomy, Purdue University West Lafayette, IN
RESEARCH ASSISTANT Jan 2023 – Present

- Designed graphing algorithms for quantum annealing on the D-Wave's Pegasus architectures, saving qubit resources.
- Generated 3D visualizations of qubits in a quantum computer's architecture, providing a comprehensive graphical representation for future lab members.

Dr. Shalaev Research Group, Birck Nanotechnology Center, Purdue University West Lafayette, IN
SOFTWARE DEVELOPER May 2023 – Present

- Contributed to the open-source code of Thorlabs devices (gitlab.com/ptapping/thorlabs-apt-device).
- Developed a Python software suite and hardware packages to control and automate a single photon counter and confocal microscopy experiment setup, utilizing multi-threading and object-oriented programming.

Elmore Family School of Electrical and Computer Engineering, Purdue University West Lafayette, IN
UNDERGRADUATE TEACHING ASSISTANT Jan 2023– Aug 2023

- Assisted students in building and troubleshoot digital system design with physical circuits and SystemVerilog.
- Developed and tested auto-grading scripts using Python and C++, significantly cutting down labor work.
- Managed and sustained the infrastructure of the course, which encompassed maintaining the students' database and course website by leveraging expertise in bash shell scripting and JavaScript.

DESIGN PROJECTS

Purdue System-on-Chip Extension Technologies (SoCET) West Lafayette, IN
DIGITAL HARDWARE DESIGNER June 2022 – Present

- Designed and tested a Floating Point Unit (FPU), SPI module, and a pipelined activation function module for an AI accelerator hardware with SystemVerilog.
- Worked with the architecture team to write C++ microservices that benchmarked a full-stack open-source RISC-V GPU (Vortex), supporting critical product development decisions, and confirming the design to have a speedup of 60%.

ECE 43700: Computer Design and Prototyping Jan – May 2024

- Implemented and tested a 5-stage pipelined, dual-core, MIPS-based CPU using SystemVerilog and QuestaSim.
- Designed L1 caches featuring a coherence control unit to support the Multiple Instruction Single Data paradigm.
- Wrote a MIPS assembly test, implementing threading and locking procedures to ensure concurrent execution.
- Achieved frequency of 53.6 MHz and a speedup of 200% compared to a single-core design.

ECE 36200: Microprocessor Systems and Interfacing Aug – Dec 2023

- Implemented ADC, DAC, PWM, SPI, and USART processes using STM32F0 advanced ARM-based MCU's peripherals and Direct Memory Access (DMA), including software emulation and configuration.
- Developed recursive algorithms, using memory allocations and control flow instructions, and translating complex C programs into Assembly code for RISC-V architecture.