KHOI PHAM

West Lafayette, IN | vphamkha@purdue.edu | (765) 701-9452

EDUCATION

Purdue University West Lafayette, IN
Bachelor of Science in Computer Engineering May 2025
GPA: 3.85 / 4.0
Coursework: Fundamental of Electrical Engineering I + II, Introduction to Digital System Design, ASIC Design Laboratory

SKILLS

Programming Languages: C, Python, C++, Java, HTML/CSS, JavaScript, Bash
Hardware Tools: SystemVerilog, KiCad, Arduino, Oscilloscope, Soldering
Professional Organization: Purdue ECE Student Society (2021-2022), Purdue IEEE (Social Chair 2022-2023)

DESIGN PROJECTS

ASIC Design Laboratory Jan - May 2023

- Designed and verified various System-on-Chip (SoC) modules, including a UART receiver, APB-slave UART receiver, and AHB-Lite FIR filter.
- Implemented and verified a USB TX module and a data buffer to handle data packet payloads in a FIFO queue fashion for a USB full-speed bulk-transfer endpoint within an AHB-Lite SoC module.
- Enhanced the USB TX module by incorporating a bit-stuffer mechanism and integrated a 16-bit cyclic redundancy check (CRC) generator.

Purdue System-on-Chip Extension Technologies (SoCET)
DIGITAL HARDWARE DEVELOPER & PCB DESIGNER June 2022 – May 2023

- Designed and tested thoroughly a Floating Point Unit with SystemVerilog, specifically catering to arithmetic operations (addition, subtraction, multiplication) of half-precision floating point units.
- Developed an activation function digital module for AI accelerator hardware, employing a pipeline design to significantly enhance computational speed and efficiency.
- Added different features to PCBs test platforms to extensively test SoCET's latest fabricated chip, including FTDI communication and on-chip memory, and adapted to the multiple-signal pins characteristics of the chip.
- Redesigned and improved old platforms to implement better communication with the chip through the use of on-board elements such as ring oscillator, serial-to-USB interface, and multiplexed DIP switches.

EXPERIENCE

Elmore Family School of Electrical and Computer Engineering, Purdue University
UNDERGRADUATE TEACHING ASSISTANT Jan 2023 – Present

- Assisted ECE 27000 students (Introduction to Digital System Design) build and troubleshoot basic digital design with physical circuits and SystemVerilog.
- Managed and sustained the infrastructure of the course, which encompassed maintaining the students' database and course website by leveraging expertise in bash shell scripting and JavaScript.
- Developed and tested auto-grading scripts using Python and C++, significantly cut down labor work.

Dr. Shalaev Research Group, Birck Nanotechnology center, Purdue University
FIRMWARE DEVELOPER May 2023 – Aug 2023

- Contributed to the open-source code of ThorLabs devices based on the APT communications protocol (gitlab.com/ptapping/thorlabs-apt-device)
- Implemented the Python software suite Qudi to remotely control and automate a time-correlated single photon counting and confocal microscopy experiment setup through hardware abstractions.
- Built Python hardware packages for various experimental devices, including mirror galvanometer, laser, linear actuator with proportional–integral–derivative (PID) controller, live camera.