**AL3201BG**
**Digital Reverb Engine**
**Complies with RoHS Directive**

DRE Digital Reverb Engine AL3201BG

## General Description

The AL3201BG Digital Reverb Engine provides all of the signal processing power required to implement a compact, easy to use, high quality reverb solution at an extremely affordable price. Built-in DRAM eliminates the need for wide bus connections to external RAM, while its 16 built-in programs and user programmable RAM allows instant usability or custom program design.

## Applications

- Guitar and Instrument Amps
- Digital Mixing Boards
- Karaoke Systems
- Digital Effects Boxes
- Computer Sound Cards
- Car Audio Systems
- Personal Stereo Products

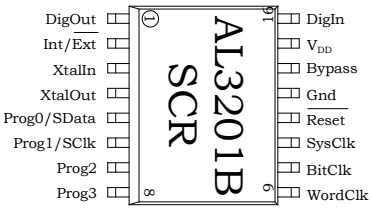
## Features

- 16 internal ROM programs consisting of halls, rooms, plates, delays, chorus, flange, vocal cancel, and rotary speaker emulation.
- Serially programmable SRAM for program development or dynamically changing programs
- 128 instructions per wordclock. (6 MIPS @ 48kHz.)
- 32k location DRAM provides over 0.68s of delay at 48kHz sampling frequency.
- Internal crystal oscillator circuit eliminates need for discrete external passive components.
- Internal voltage regulators allow operation from 5.5V down to 3.0V $V_{DD}$.
- Internal 1000pF bypass capacitor to reduce voltage swings at the rails.
- **Lead Free and RoHS Compliant**

## Program List and Package

| Prog[3:0] | Name | Description |
|---|---|---|
| 0110 | Hall 1 | Bright hall reverb for drums, guitars, and vocals. |
| 0010 | Hall 2 | Warm hall for acoustic guitars, pianos, and vocals. |
| 1010 | Room 1 | Hardwood studio for acoustic instruments. |
| 1110 | Room 2 | Ambience for acoustic mixes and synth sounds. |
| 1111 | Room 3 | Warm room for guitars and rhythm instruments. |
| 1011 | Plate 1 | Classic plate reverb for lead vocals and instruments. |
| 1001 | Plate 2 | Sizzling bright plate reverb for vocals and drums. |
| 1101 | Plate 3 | Short vintage plate reverb for snares and guitars. |
| 1100 | Chorus | Stereo chorus for guitars and pianos. |
| 1000 | Flange | Stereo flanger for jet wash effects. |
| 0000 | Delay 1 | 125ms slapback delay for vocals and guitars. |
| 0100 | Delay 2 | 190ms delay for percussive arpeggios. |
| 0101 | Chorus/Room 1 | Chorus with reverb for guitars, synths, and pianos. |
| 0001 | Chorus/Room 2 | Auto-wah guitar effect with reverb for lead instruments. |
| 0011 | Vocal Cancel | Removes lead vocals from many stereo recordings. |
| 0111 | Rotary Speaker | Rotary speaker emulation for organs and guitars. |

Note: The unusual ordering of the programs allows a 16-position rotary switch's Gray code output to be connected to the program pins.



16 pin SOIC
300 mils wide

Wavefront Semiconductor ∴ 200 Scenic View Drive ∴ Cumberland, RI 02864 ∴ U.S.A.
Tel: +1 401 658-3670 ∴ Fax: +1 401 658-3680 ∴ Email: info@wavefrontsemi.com
On the web at www.wavefrontsemi.com

## Table of Contents

## Pin Descriptions

(*: Pullup to $V_{DD}$ via nominal internal 5.3kΩ resistor.)

| Pin# | Name | Pin Type | Description |
|---|---|---|---|
| 1 | DigOut | Out | Digital serial output for stereo DAC. |
| 2 | Int/$\overline{\text{Ext}}$ | In* | Internal/external program selection. 1:Internal, 0:External. |
| 3 | XtalIn | In | 12.288MHz crystal input. [1] |
| 4 | XtalOut | Out | 12.288MHz crystal output. [1] |
| 5 | Prog0/SData | I/O* | Internal program select 0 / serial interface data line. |
| 6 | Prog1/SClk | In* | Internal program select 1 / serial interface clock line. |
| 7 | Prog2 | In* | Internal program select 2. |
| 8 | Prog3 | In* | Internal program select 3. |
| 9 | WordClk | Out | Word clock output, XtalIn/256 (48kHz with 12.288MHz crystal). |
| 10 | BitClk | Out | Bit clock output, XtalIn/4 (3.072MHz with 12.288MHz crystal). |
| 11 | SysClk | Out | System clock output, internal 12.288MHz clock. |
| 12 | $\overline{\text{Reset}}$ | In | Active low reset. |
| 13 | Gnd | Ground | Ground connection. |
| 14 | Bypass | I/O | Connect 0.1μF bypass capacitor to Gnd for internal regulator. [2] |
| 15 | $V_{DD}$ | Power | $V_{DD}$ power pin. Connect 0.1μF capacitor to Gnd. |
| 16 | DigIn | In | Digital serial input from stereo ADC. |

Note 1: Internal 18pF capacitor to ground. Internal 120kΩ resistor between Xtal pads.

Note 2: If $V_{DD}$ will always be below 3.6V (including the effects of ripple, spikes, etc.) then $V_{DD}$ should be connected to BYPASS.

## Electrical Characteristics

| Symbol | Description | Condition | Min | Typ | Max | Units |
|---|---|---|---|---|---|---|
| **Recommended Operating Conditions** | | | | | | |
| $V_{DD}$ | Supply Voltage | Note 1 | 3.0 | 5.0 | 5.5 | V |
| $I_{DD}$ | Supply Current | | 9 | 10 | 11 | mA |
| Gnd | Ground | | - | 0.0 | - | V |
| $F_S$ | Sample rate | Note 2 | 24 | 48 | 50 | kHz |
| Temp | Temperature | | 0 | 25 | 70 | °C |
| **Outputs** (DigOut, SysClk, BitClk, WordClk) | | | | | | |
| $V_{OH}$ | Logical "1" output voltage | Unloaded | 0.9 $V_{DD}$ | $V_{DD}$ | - | V |
| $V_{OL}$ | Logical "0" output voltage | Unloaded | - | 0 | 0.05 $V_{DD}$ | V |
| $I_{OH}$ | Logical "1" output current | $V_{DD}$=5V $V_O$=4.5V | - | - | -8.0 | mA |
| $I_{OL}$ | Logical "0" output current | $V_{DD}$=5V $V_O$=0.4V | - | - | 8.0 | mA |
| **Inputs** (DigIn, Int/Ext, Prog0/Sdata, Prog1/SClk, Prog2, Prog3, Reset) Note 3. | | | | | | |
| $V_{IH}$ | Logical "1" input voltage | | 2.5 | - | $V_{DD}$ | V |
| $V_{IL}$ | Logical "0" input voltage | | 0 | - | 0.5 | V |
| $I_{IH}$ | Logical "1" input current | $V_{DD}$=$V_{IH}$=5V | - | - | 2 | μA |
| $I_{IL}$ | Logical "0" input current | No pullup pin | - | - | 2 | μA |
| $I_{ILP}$ | Logical "0" input current | Pullup pin, Vin=0 | 83 | 167 | 333 | μA |
| $C_{IN}$ | Input Capacitance | | - | 2.0 | - | pF |

Note 1: If $V_{DD}$ will always be below 3.6V (including the effects of ripple, spikes, etc.) then $V_{DD}$ should be connected to BYPASS.

Note 2: Changing the sample rate (by changing the crystal frequency) will change the maximum delay available through the Data RAM proportionally. Low sample rates require more refresh instructions.

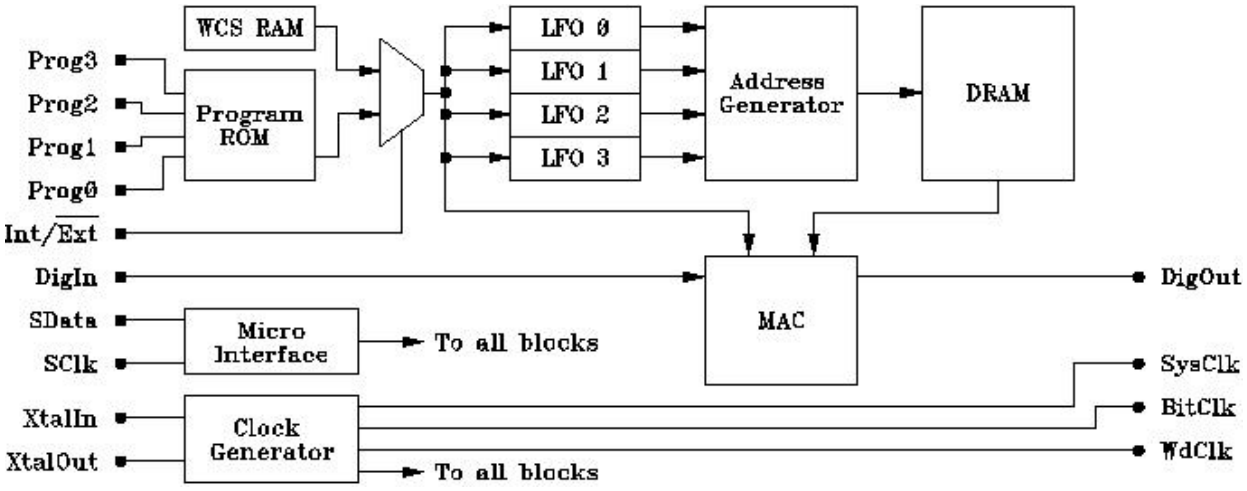
Note 3: XtalIn, XtalOut are special pins designed to be connected to a crystal. XtalOut is a relatively weak pin (about 0.2mA) and should not be used to drive external circuits. Instead of using a crystal, XtalIn may be driven by a standard $V_{DD}$ to Gnd logic signal, but the logic levels are **not specified.**

## Architecture Overview

The DRE contains the following major blocks:

- DigIn/DigOut Interface
- 16 x 128 location Program ROM
- 128 location Instruction (Writable Control Store - WCS) RAM
- 32768 location Data RAM
- Data RAM address generator
- 4 independent Low Frequency Oscillators (LFOs)
- Multiply/Accumulate (MAC) unit
- Instruction decoding and program control unit
- Microprocessor interface
- Clock generator

### Architecture Block Diagram

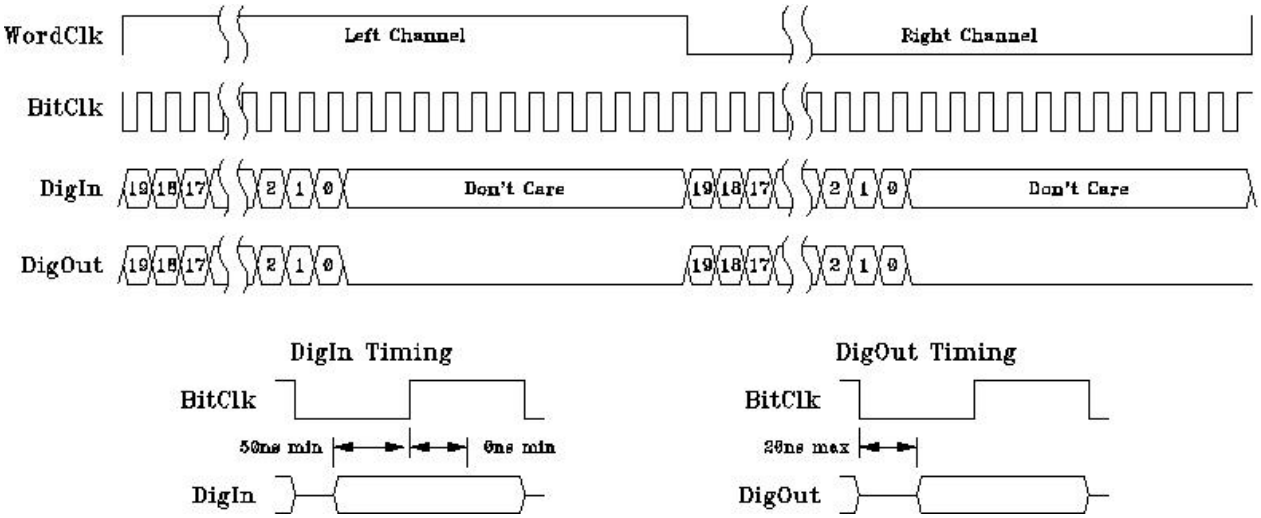


## Architecture Details

### DigIn/DigOut Interface

The DigIn/DigOut bitclock rate is 1/4th the XtalIn frequency, at a nominal 3.072MHz with a 12.288MHz crystal, reading or writing 20 bits of data from the start of each frame.

**DigIn/DigOut Format Timing**




The data is read into the 20-bit internal datapaths as two's complement numbers in S.23 notation, with the most significant bit indicating the sign, and the remaining bits as a factional immediately after the binary point, resulting in an effective range of ±1.0. The data is outputted in the same format.

---

### Instruction RAM

Alongside the 16 internal programs in the Program ROM is an externally programmable SRAM that is easily accessible through the serial clock and data pins. By setting the chip to external mode, the SClk and SData pins (pins 6 and 5) become available for serial communication. Except for its external programmability, there is no functional difference between using the Instruction RAM and the Program ROMs.

The Instruction RAM consists of 128 address locations continuously cycled through on every wordclock period, starting with instruction 0 at the beginning of the period and completing the execution of instruction 127 by the end. This is synchronized with the DigIn inputs and DigOut outputs such that a new sample is received after the execution of instruction 1023 and before instruction 0. This type of cycling is advantageous for processing streaming data such as audio, where the same program is applied to each sample as it is received.

Programs may be written for the Instruction RAM as a binary file, or in assembly code using software available from Wavefront Semiconductor. For a detailed description of the assembly instructions and their usage, please refer to the DRE Assembler Manual IM3101-01 in the Development System software package. For the instructions executing in the Instruction RAM, the internal program memory map is explained in the following table.

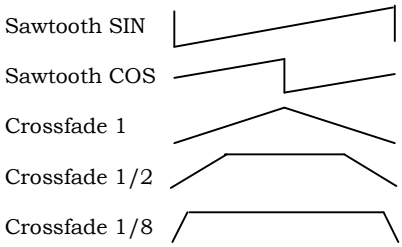
**Instruction RAM Memory Map**

| Addr | Name |
|---|---|
| 0:3 | LFO Coefficients |
| 4:127 | MAC Instructions |

**LFO Coefficient Word**

| Bit# | Description | | |
|---|---|---|---|
| 31 | P: Pitch shift mode select (S must be set). [1] | | |
| 30 | S: Sine/triangle select. 1:Triangle; 0: Sine. | | |
| 29:28 | X[1:0]: Crossfade coefficient select. Value indicates the fraction of a half sawtooth period used in crossfading. | X[1:0] | Xfade |
| | | 11 | 1/16 |
| | | 10 | 1/8 |
| | | 01 | 1/2 |
| | | 00 | 1 |
| 27:15 | F[12:0]: Frequency coefficient, unsigned. | | |
| 14:0 | A[14:0]: Amplitude coefficient, unsigned. | | |

Note 1: If set, the output waveform is a sawtooth with double the triangle wave's frequency.




The first four instructions in the Instruction RAM set the parameters for the four Low Frequency Oscillators (LFOs). The sinusoid generated by the LFOs is of the formula A*sin(nF/M) or A*cos(nF/M), where n is the time index, F/M = 2πf/Fs, M = 262143 (0x3FFFF, internal maximum 18-bit value), f is the selected frequency, and Fs is the sampling frequency. Solving for the selected frequency f:

$f = (F/M)*Fs/(2\pi) = 0.029142*F$ @ sampling frequency Fs = 48kHz

$f_{min} = f(F=1) = 0.029142Hz$
$f_{max} = f(F=8191) = 238.7Hz$

Triangle waves are generated by incrementally adding or subtracting C*F/M, where $C = 2^{22}$, an internal constant, from the maximum internal negative or positive value H respectively (H = 0x7FFFFF for maximum positive). One quarter of the waveform is traversed in H/(C*F/M). The equation for selected frequency f is then:

$f = Fs*C*(F/M)/(4*H) = 0.022888*F$ @ sampling frequency Fs = 48kHz

$f_{min} = f(F=1) = 0.022888Hz$
$f_{max} = f(F=8191) = 187.5Hz$

Sawtooths are triangle waves which roll over from one maximum to another without changing the sign of the increment, and thus the equation for selected frequency f is simply double that of the triangle wave:

$f = Fs*C*(F/M)/(2*H) = 0.045777*F$ @ sampling frequency Fs = 48kHz

$f_{min} = f(F=1) = 0.045777Hz$
$f_{max} = f(F=8191) = 375.0Hz$

When chorus instructions are used, addresses are offset by the output of an LFO. The range of this offset is ±A/8 samples (or ±4096 maximum), or A/4 samples total (8192 samples maximum).

By judiciously choosing the LFO frequency and waveform with which to sweep through the Data RAM, it is possible to generate pitch shifts, flanges, choruses, reverbs, and other effects. Please see the various application notes for descriptions and examples.

Following the 4 LFO coefficient words are 124 MAC Instruction Words. These instructions allow the manipulation of the Data RAM and the waveforms generated by the LFOs.

A good NOP instruction is 0x00030000. This instruction preserves the value in all registers, and is the NOP executed in the MAC during the first four ticks of every sample period while the LFO coefficients are loaded.

**MAC Instruction Word**

<table>
<tr><th>Bit#</th><th colspan="3">Description</th></tr>
<tr><td>31</td><td colspan="3">S: Sign bit for multiplier coefficient.</td></tr>
<tr><td rowspan="10">30:23</td><td colspan="3">C[7:1]: Multiplier coefficient, sign-magnitude.<br>C[7:0]: Chorus instruction. Only the 7 MSBs are used as multiplier coefficients. The LSB is used in chorus mode. If I[5] is set, C[7:0] is:</td></tr>
<tr><td>C</td><td colspan="2">Description</td></tr>
<tr><td>7</td><td colspan="2">Chorus/Xfade select:<br>1: Pass LFO address to address generator & select chorus coefficient.<br>0: Mask LFO address to address generator & select crossfade coefficient.</td></tr>
<tr><td>6</td><td colspan="2">1's complement the LFO address sign bit. [1]</td></tr>
<tr><td>5</td><td colspan="2">1's complement the LFO coefficient.</td></tr>
<tr><td>4</td><td colspan="2">1's complement the LFO address.</td></tr>
<tr><td>3</td><td colspan="2">LFO latch. 1: Latch in new LFO data;<br>0: Hold last LFO data. [2]</td></tr>
<tr><td>2:1</td><td colspan="2">LFO select.</td></tr>
<tr><td>0</td><td colspan="2">LFO sine/cosine select. 1: Cos; 0: Sin.</td></tr>
<tr><td>22</td><td colspan="3">W: Write select. [3, 4]</td></tr>
<tr><td rowspan="9">21:16</td><td colspan="3">I[5:0]: Instruction field.</td></tr>
<tr><td>I</td><td colspan="2">Description</td></tr>
<tr><td>5</td><td colspan="2">Chorus select (When set, MAC coefficient is LFO block output, LFO address offset added to Data RAM address).</td></tr>
<tr><td>4</td><td colspan="2">Clock register C. [3]</td></tr>
<tr><td>3</td><td colspan="2">Clock register B. [5]</td></tr>
<tr><td>2</td><td colspan="2">Reserved – set to zero.</td></tr>
<tr><td rowspan="4">1:0</td><td rowspan="4">MAC product instruction.</td><td>I[1:0]</td><td>Instruction</td></tr>
<tr><td>11</td><td>Acc = Prod + Acc [6]</td></tr>
<tr><td>10</td><td>Acc = Prod + C [3]</td></tr>
<tr><td>01</td><td>Acc = Prod + B [5]</td></tr>
<tr><td>15:0</td><td colspan="3">A[15:0]: Multiplicand address. [7, 8] (Currently only lower 15 bits used; reserve MSB for future expansion.)<br>Address 0x0000 = LeftIn/Out;<br>Address 0x0001 = RightIn/Out.</td></tr>
</table>

Note 1: This complement is only for the MSB, and sign-extension bits are not affected.

Note 2: Upon latching new data, the LFO registers will store the lower or upper LFO pairs' sinusoid/triangle waves, and the lower or upper LFO pairs' crossfade coefficient. I.e. there are two pairs of registers; LFO 0/1's sinusoid /triangle/crossfade will be latched together, and LFO 2/3's sinusoid/triangle/crossfade will be latched together.

Note 3: The LeftOut, RightOut, and C registers are in parallel with the accumulator, and will contain the same value as the accumulator if clocked at the end of the tick. Thus, a write to LeftOut or RightOut will store the current tick's results.

Note 4: A write to Data RAM stores the last tick's results into address A. During writes, the multiplicand is set to be the Acc, since A[15:0] is used for the destination address. Writes to LeftOut or RightOut can use the Acc = Product + Acc instruction with the multiplier coefficient set to 0 to pass all bits unaltered.

Note 5: Register B, if clocked at the end of the tick, will store the value of the current tick's multiplicand. When a read is executed, B latches LeftIn, RightIn, or Data RAM. When a write is executed, B latches the accumulator from the last tick.

Note 6: The accumulator contains the result from the last instruction tick, and is updated at the end of the current instruction tick.

Note 7: The internal Data RAM address offset automatically decrements by 1 every wordclock period.

Note 8: Because addresses 0x0000 and 0x0001 are being used to access the left and right channels, those DATA RAM memory locations may not be directly written to or read from.

## Program ROM

The DRE comes with 16 proven, high-quality ROM programs. By setting the chip to internal mode, the four program pins may be used to select between the different algorithms. Each program change automatically initiates a Data RAM zero cycle, thus ensuring that no residual data from a previous program is present when the new program begins execution. The ROMs may not be read due to the serial interface becoming the program select interface when in internal mode.

**Program List**

| Prog[3:0] (Pins 8-5) | Name | Description |
|---|---|---|
| 0110 | Hall 1 | Bright hall reverb for drums, guitars, and vocals. |
| 0010 | Hall 2 | Warm hall for acoustic guitars, pianos, and vocals. |
| 1010 | Room 1 | Hardwood studio for acoustic instruments. |
| 1110 | Room 2 | Ambience for acoustic mixes and synth sounds. |
| 1111 | Room 3 | Warm room for guitars and rhythm instruments. |
| 1011 | Plate 1 | Classic plate reverb for lead vocals and instruments. |
| 1001 | Plate 2 | Sizzling bright plate reverb for vocals and drums. |
| 1101 | Plate 3 | Short vintage plate reverb for snares and guitars. |
| 1100 | Chorus | Stereo chorus for guitars and pianos. |
| 1000 | Flange | Stereo flanger for jet wash effects. |
| 0000 | Delay 1 | 125ms slapback delay for vocals and guitars. |
| 0100 | Delay 2 | 190ms delay for percussive arpeggios. |
| 0101 | Chorus/Room 1 | Chorus with reverb for guitars, synths, and pianos. |
| 0001 | Chorus/Room 2 | Auto-wah guitar effect with reverb for lead instruments. |
| 0011 | Vocal Cancel | Removes lead vocals from many stereo recordings. |
| 0111 | Rotary Speaker | Rotary speaker emulation for organs and guitars. |

Note: The unusual ordering of the programs allows a 16-position rotary switch's Gray code output to be connected to the program pins.

---

## Data RAM

The Data RAM is a DRAM consists of 32768 storage locations, and stores values in a floating point format. The format used is: E[2:0].S.F[9:0], where E is the exponent, S is the sign bit, and F is the fractional portion. The expansion of the floating point into fixed point is as follows:

If E<7, S E*S !S FFFFFFFFFF (8-E)*0 (where E*S means S repeated E times).
If E=7, S SSSSSSS FFFFFFFFFF 00.

This method encodes one extra bit for sign extensions less than 7 bits.

To automatically implement circular addressing, the effective address of a Data RAM memory location is calculated by adding the address portion of the instruction to a counter which decrements once per sample period. This counter is synchronized with the DigIn input, DigOut output, and the program counter such that the decrement occurs after the execution of instruction 1023 and before the execution of instruction 0. As the value of the offset counter cannot be accessed, the exact physical address where values are stored cannot be determined (only the relative addresses used in the program are effective in accessing determinate locations).

In order to clear the Data RAM of residual values, changing the selected Internal ROM program via the Prog[3:0] pins or toggling the /Reset pin both initiate a Data Ram Zero Cycle, where a value equal to a fixed-point zero is written to every location. For manual programming of the Instruction RAM, it is up to the user to clear the Data RAM as appropriate.

As typical for all DRAMs, the Data RAM requires refreshing in order to retain data. Below 70°C, each address modulo 1024 needs to be accessed every 1.34ms. If the program in the Instruction RAM does not achieve this, then the program needs to be padded with refresh instructions. An adequate set of refresh instructions for a 12.288MHz input at XtalIn is the reading of 16 Data RAM locations spaced 64 addresses apart (addresses 0x0000, 0x0040, ..., 0x03C0).

---

## Multiply/Accumulate Unit

The MAC performs all the arithmetic operations on the data in the DRE. All instructions are executed in one clock cycle. It uses a 20-bit-wide datapath. The multiplier in the MAC truncates the resulting value to 20 bits, and the overflow unit reports overflows of any multiply-accumulation in Control/Status Word 0 bit 10, as well as set the result to the maximum positive or negative value (±1.0), depending on the sign bit. The MAC consists of:

- A 20-bit x 8-bit multiplier producing a 20-bit result.
- A 20-bit accumulator (A)
- A 20-bit register (B) in S3.24 format that the multiplicand may be copied to
- A 20-bit register (C) in S3.24 format that the accumulator may be copied to
- DigIn input registers
- DigOut output registers

---

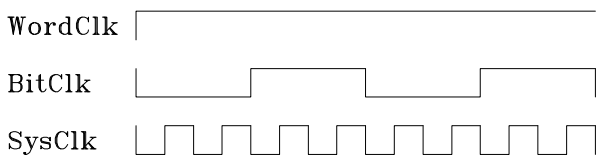
## Reset Circuitry

The DRE may be asynchronously reset using the /Reset pin, with a minimum pulse width of 163ns. This will start a Data RAM zero cycle, and set/reset certain bits of the Control/Status Words as noted; it does not alter the contents of the Instruction RAM. After reset, all internal counters and state registers have been zeroed, and multiple DREs may be synchronized. The use of Reset upon power-up is mandatory to obtain proper operation of the AL3201.

---

## Clock Generator

The clock generation logic inside the DRE takes the signal presented on the XtalIn/XtalOut pins and buffers it as SysClk for internal use, as well as output it on pin 11. SysClk is divided down by 4 to generate a BitClk for receiving and transmitting data on DigOut and DigIn, and is outputted on pin 10. SysClk is also divided down by 256 to generate a WordClk, presented on pin 9. Thus, the three output clock signals are edge-aligned, with SysClk and BitClk falling on WordClk's rising edge.



## Serial Microprocessor Interface

The DRE allows read and write access to the internal Instruction RAM and two Control/Status Word registers, as well as the Data RAM through a Control/Status Word. The host microprocessor communicates to the DSP-1K in a special serial format.

The serial microcontroller interface contains a one-stage pipeline for accessing the internal memories in order to synchronize accesses. This means that it is possible to have a write access waiting in the pipeline while another is being inputted, as long as the write access is complete before the second access starts the internal machinery, which for writes is the Attention-Deselect sequence, and for reads it is the end of the address. This also means that the Control/Status Words can be accessed independent of any pending writes in the pipeline, without worries of the completion of the pending write.

### Serial Microprocessor Interface Format and Access Timing

The basic format for the micro serial interface is:

Attn Sel R/W A7 A6 A5 A4 A3 A2 A1 A0 DN DN-1 DN-2 … D2 D1 D0 Attn Desel

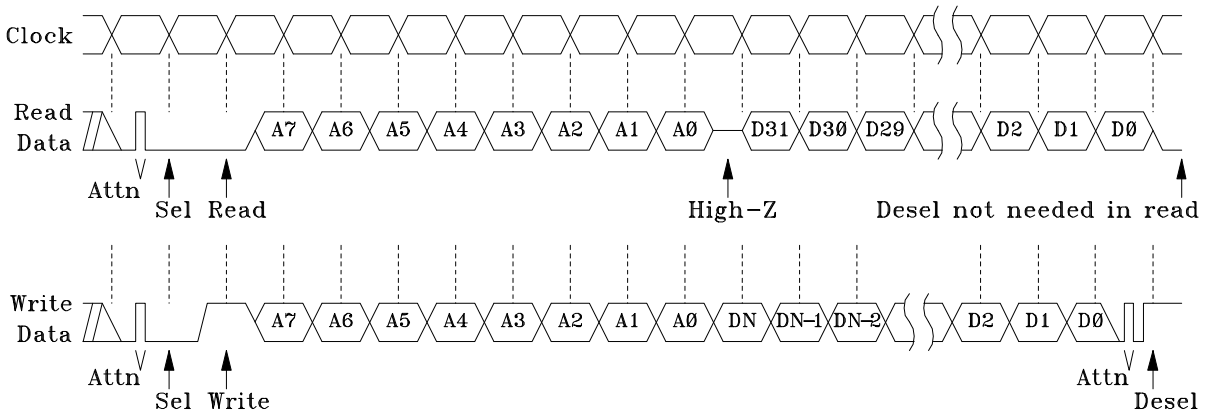
⇑ ⇑ Write mode only

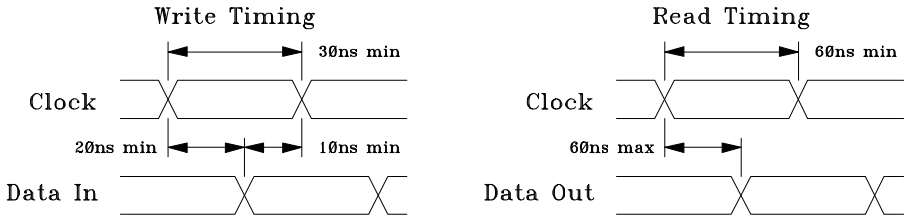
| | | | |
|---|---|---|---|
| Attn: | A 0-1-0 is used to signal attention/start. | | |
| Sel/Desel: | 0:Select; 1:Deselect. | A7 - A0: | Address |
| R/W: | 0:Read; 1:Write | DN - D0: | Data |

Note 1: There is a short period of High-Z during a read between A0 and the first data bit shifted out. This period must be at least 5 SysClks long, 1 WordClk long if not in direct mode (CS0[3]).

Note 2: As long as data is being sent during a write, the address will be automatically incremented. Therefore only a start address need be sent.

Note 3: The phase of the clock is unimportant.




### Serial Microprocessor Interface Memory Map

| Addr | Name | | |
|---|---|---|---|
| 0:127 | Instruction RAM | Addr | Name |
| | | 0:3 | LFO Coefficients |
| | | 4:127 | MAC Instructions |
| 128 | Control/Status 0 | | |
| 129 | Control/Status 1 | | |

### The 4 Word Formats

| | |
|---|---|
| LFO | PSXXFFFF FFFFFFFF FAAAAAAA AAAAAAAA |
| MAC | SCCCCCCC CWIIIIII AAAAAAAA AAAAAAAA |
| CS0 | --BBBBBB BBBBBBBB -----OPR MZXLI-SS |
| CS1 | RWDDDDDD DDDDDDDD AAAAAAAA AAAAAAAA |

**Control/Status Word 0**

| Bit# | Description |
|---|---|
| 31:30 | Reserved. Set to zero. |
| 29:16 | B[13:0]: Data RAM read data. [1] |
| 15:11 | Reserved. Set to zero. |
| 10 | O: MAC overflow. Self-clears after read. Read only. |
| 9 | P: Self test pass. Read only. |
| 8 | R: Ready indication. Read/write/test/clear complete. |
| 7 | M: DigOut mute in external mode. Resets to 1. |
| 6 | Z: Data RAM zero. Initiates zeroing cycles until set to 0. Resets to 0. [2, 3, 4, 5] |
| 5 | X: Data RAM zero cancel. Prevents zeroing circuitry from running until set to 0. Overrides Z. Resets to 0. [3] |
| 4 | L: LFO reset pulse. Resets LFO internal status registers and clears overflow flag. Self clearing. Resets to 0. |
| 3 | I: Instruction RAM direct mode. Resets to 1.<br>1: Instructions are written/read as soon as received; 0: Instructions are written/read when the address counter rolls around to matching address. [6] |
| 2 | Reserved. Set to zero. |
| 1 | S[1]: Data RAM self test pattern select.<br>1: Load Data RAM with 0x2AAA/0x1555 checkerboard pattern;<br>0: Load Data RAM with 0x1555/0x2AAA checkerboard pattern. |
| 0 | S[0]: Data RAM self test initiate. Self-clears after test completion. Resets to 0. [2, 3, 5, 7] |

Note 1: See Data RAM section for data format.

Note 2: The Data RAM zeroing circuitry and Data RAM self test circuitry share gates; do not turn more than one on at a time.

Note 3: The Data RAM zeroing cycle will run to completion even if Z is set to 0. Only the X bit may cancel it mid-cycle. Until the cycle ends, self test results will be inaccurate. Thus do not set Z=0 and S[0]=1 at the same time. Rather, set X and S[0] to 1 at the same time. Z does not self-clear, and will affect both internal and external mode.

Note 4: A Data RAM zeroing cycle takes approximately 5.33ms to complete with a 12MHz crystal. After a zeroing cycle has completed, do not start another for one wordclock period.

Note 5: During Data RAM zeroing and test cycles, reads and writes to the Data RAM are ignored.

Note 6: For dynamically changing programs, set I=0 so that changing the program does not interrupt its execution. Otherwise reads and writes to the Instruction RAM will usurp the address bus to the RAM and cause address jumps in the instruction sequence. With I=0, reads and writes to each address may take up to one wordclock period to complete. Thus during continuous writes, the start of each instruction word should be at least one wordclock period apart, and during reads the serial clock should wait 1 wordclock after the address before continuing.

Note 7: A Data RAM self test cycle takes approximately 10.66ms to complete with a 12MHz crystal. The cycle will run to completion even if S[0] is set to 0. It may not be cancelled.

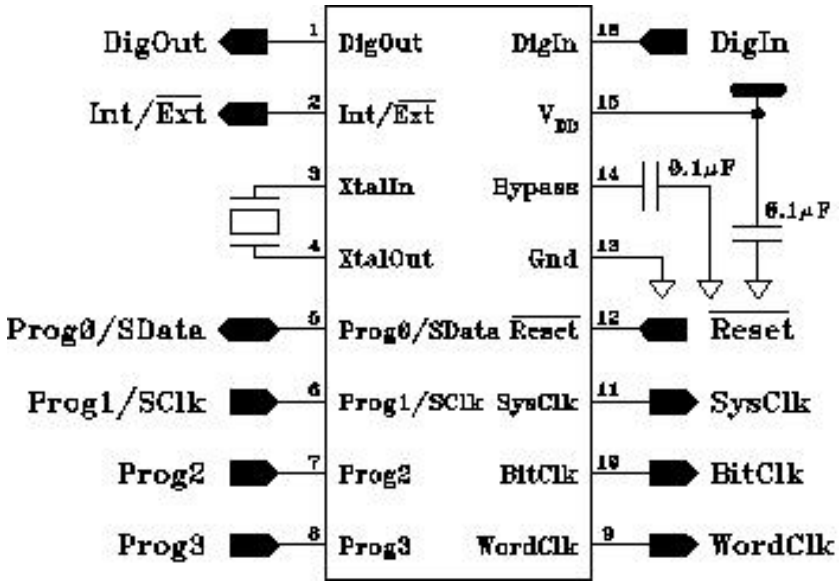
**Control/Status Word 1**

| Bit# | Description |
|---|---|
| 31 | R: Read select. Read data from Data RAM address A[15:0] and put data in B of control/status word 0. Self-clears after completion. [2] |
| 30 | W: Write select. Write data D[13:0] to Data RAM address A[15:0]. Self-clears after completion. [2] |
| 29:16 | D[13:0]: Data RAM write data. [1] |
| 15:0 | A[15:0]: Data RAM address. The MSB is unused and reserved for future expansion. |

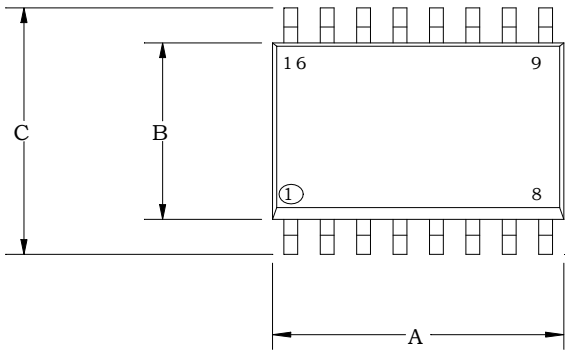
Note 1: See Data RAM section for data format.

Note 2: Reading and writing Data RAM will usurp Data RAM access for one cycle, possibly disrupting proper code execution.

## Suggested Connections

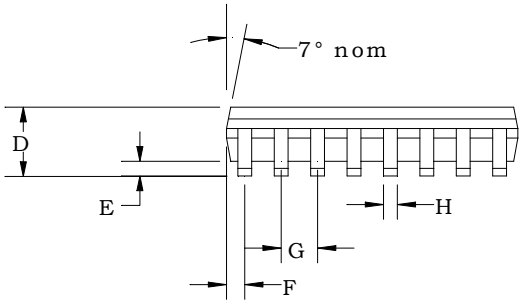


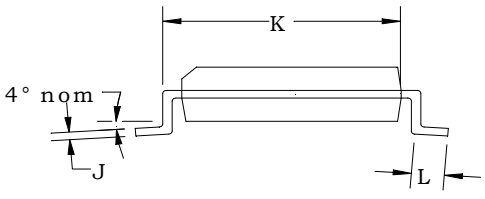

## Package Dimensions




| Dimensions (Typical) | | |
|---|---|---|
| | Inches | Millimeters |
| A | 0.406" | 10.31 |
| B | 0.295" | 7.49 |
| C | 0.407" | 10.34 |
| D | 0.100" | 2.50 |
| E | 0.008" | 0.20 |
| F | 0.025" | 0.64 |
| G | 0.050" | 1.27 |
| H | 0.017" | 0.42 |
| J | 0.011" | 0.27 |
| K | 0.340" | 8.66 |
| L | 0.033" | 0.83 |

Note: Dimension "A" does not include mold flash, protrusions, or gate burrs.



NOTICE

Wavefront Semiconductor reserves the right to make changes to their products or to discontinue any product or service without notice. All products are sold subject to terms and conditions of sale supplied at the time of order acknowledgement. Wavefront Semiconductor assumes no responsibility for the use of any circuits described herein, conveys no license under any patent or other right, and makes no representation that the circuits are free of patent infringement. Information contained herein is only for illustration purposes and may vary depending upon a user's specific application. While the information in this publication has been carefully checked, no responsibility is assumed for inaccuracies.

Wavefront Semiconductor products are not designed for use in applications which involve potential risks of death, personal injury, or severe property or environmental damage or life support applications where the failure or malfunction of the product can reasonably be expected to cause failure of the life support system or to significantly affect its safety or effectiveness.

All trademarks and registered trademarks are property of their respective owners.

**Contact Information:**

Wavefront Semiconductor
200 Scenic View Drive
Cumberland, RI 02864 U.S.A.
Tel: +1 401 658-3670
Fax: +1 401 658-3680
On the web at www.wavefrontsemi.com
Email: info@wavefrontsemi.com



Application note revised September, 2005