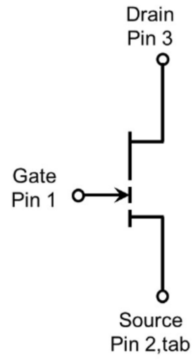
General description

HINN700TK190B is a 725V GaN-on-Si enhancement-mode power transistor in TO-252-2L package. The properties of GaN allow for high current, high breakdown voltage and high switching frequency. The TO-252-2L package offers low parasitic inductance, strong heat dissipation capability and high solderability, which make GaN better apply to consumer and industrial applications.

TO-252-2L



Features

- 725V GaN enhancement-mode power switch
- $R_{DS(on),\,max}$ 200mΩ
- Gate recommend drive voltage 0V - 6V
- Ultra-low FOM
- Ultra-high switching frequency
- Reverse current capability
- Zero reverse recovery loss Monolithic
- integrated ESD protection
- RoHS, Pb-free, REACH-compliant

Gate	1
Source	2, tab
Drain	3

Applications

- AC-DC converters
- DC-DC converters
- Totem pole PFC
- Fast charging
- Power adapters
- LED lighting drivers
- Wireless power transfer
- Laser drivers
- TV display

Maximum ratings

at T_j = 25 °C unless otherwise specified. Continuous application of maximum ratings can deteriorate transistor lifetime. For further information, contact CloudSemi sales office.

Table 3 Maximum rating

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Drain-source voltage	$V_{DS, max}$	-	-	725	V	V_{GS} = 0 V, I_D = 10 μA
Drain-source voltage transient [1]	$V_{DS, transient}$	-	-	850	V	V_{GS} = 0 V, V_{DS} = 850 V
Continuous current, drain-source	I_D	-	-	10	A	T_c = 25 °C
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	18	A	T_c = 25 °C; V_G = 6 V
Pulsed current, drain-source [2]	$I_{D, pulse}$	-	-	10	A	T_c = 125 °C; V_G = 6 V
Gate-source voltage, continuous	V_{GS}	-1.4	-	+7	V	T_j = -55 °C to 150 °C
Gate-source voltage, pulsed	$V_{GS, pulse}$	-	-	+10	V	T_j = -55 °C to 150 °C; t_{Pulse} = 50 ns, f = 100 kHz; open drain
Power dissipation	P_{tot}	-	-	73	W	T_c = 25 °C
Operating temperature	T_j	-55	-	+150	°C	
Storage temperature	T_{stg}	-55	-	+150	°C	

1. $V_{DS, transient}$ is intended for surge rating during non-repetitive events, t_{Pulse} < 1 μs.
2. Pulse width = 10 μs.

Thermal characteristics

Table 4 Thermal characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Thermal resistance, junction-case	R_{thJC}	-	-	1.7	°C/W	
Reflow soldering temperature	T_{sold}	-	-	260	°C	MSL3

Electrical characteristics

at T_j = 25 °C, unless specified otherwise.

Table 5 Static characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate threshold voltage	$V_{GS(TH)}$	1.2	1.6	2.5	V	I_D = 11 mA; V_{DS} = V_{GS}; T_j = 25 °C
		-	1.6	-		I_D = 11 mA; V_{DS} = V_{GS}; T_j = 125 °C
Drain-source leakage current	I_{DSS}	-	4	50	μA	V_{DS} = 725 V; V_{GS} = 0 V; T_j = 25 °C
		-	10	-		V_{DS} = 725 V; V_{GS} = 0 V; T_j = 125 °C
Gate-source leakage current	I_{GSS}	-	-	200	μA	V_{GS} = 6 V; V_{DS} = 0 V
Drain-source on-state resistance	$R_{DS(on)}$	-	160	200	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 25 °C
		-	330	-	mΩ	V_{GS} = 6 V; I_D = 3 A; T_j = 125 °C
Gate resistance	R_G	-	3.5	-	Ω	f = 5 MHz; open drain

Table 6 Dynamic characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Input capacitance	C_{iss}	-	83	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Output capacitance	C_{oss}	-	27	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Reverse transfer capacitance	C_{rss}	-	0.4	-	pF	V_{GS} = 0 V; V_{DS} = 400 V; f = 1 MHz
Effective output capacitance, energy related [1]	$C_{o(er)}$	-	35	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Effective output capacitance, time related [2]	$C_{o(tr)}$	-	54	-	pF	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Output charge	Q_{OSS}	-	22	-	nC	V_{GS} = 0 V; V_{DS} = 0 to 400 V
Turn-on delay time	$t_{d(on)}$	-	2	-	ns	V_{DS} = 400 V; I_D = 6 A; L = 318 μH; V_{GS} = 6 V; R_{on} = 10 Ω; R_{off} = 2 Ω
Turn-off delay time	$t_{d(off)}$	-	4	-	ns	
Rise time	t_r	-	5	-	ns	
Fall time	t_f	-	6	-	ns	

1. $C_{o(er)}$ is the fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V.
2. $C_{o(tr)}$ is the fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V.

Table 7 Gate charge characteristics

Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Gate charge	Q_G	-	2.3	-	nC	V_{GS} = 0 to 6 V; V_{DS} = 400 V; I_D = 3 A
Gate-source charge	Q_{GS}	-	0.2	-	nC	
Gate-drain charge	Q_{GD}	-	0.9	-	nC	
Gate plateau voltage	V_{plat}	-	2.4	-	V	V_{DS} = 400 V; I_D = 3 A

Table 8 Reverse conduction characteristics

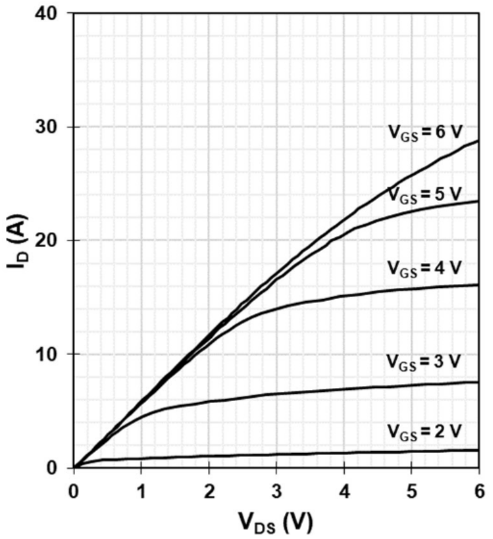
Parameters	Symbols	Values			Units	Notes/Test Conditions
		Min.	Typ.	Max.		
Source-drain reverse voltage	V_{SD}	-	2.5	-	V	V_{GS} = 0 V; I_{SD} = 3 A
Pulsed current, reverse	$I_{S,\ pulse}$	-	20	-	A	V_{GS} = 6 V
Reverse recovery charge [1]	Q_{rr}	-	0	-	nC	I_{SD} = 3 A; V_{DS} = 400 V
Reverse recovery time	t_{rr}	-	0	-	ns	
Peak reverse recovery current	I_{rrm}	-	0	-	A	

1. Excluding Q_{OSS}

Electrical characteristics diagrams

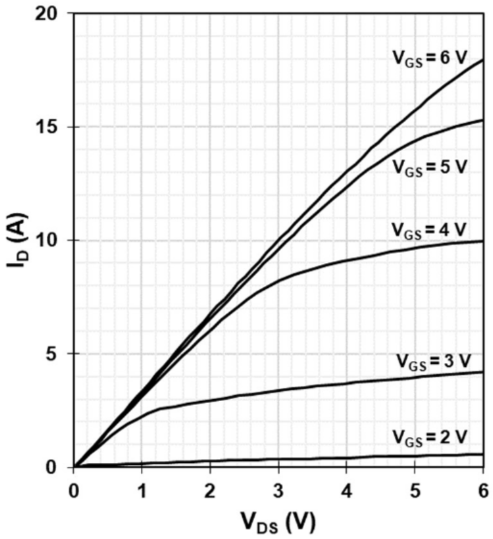
at T_j = 25 °C, unless specified otherwise.

Figure 1 Typ. output characteristics



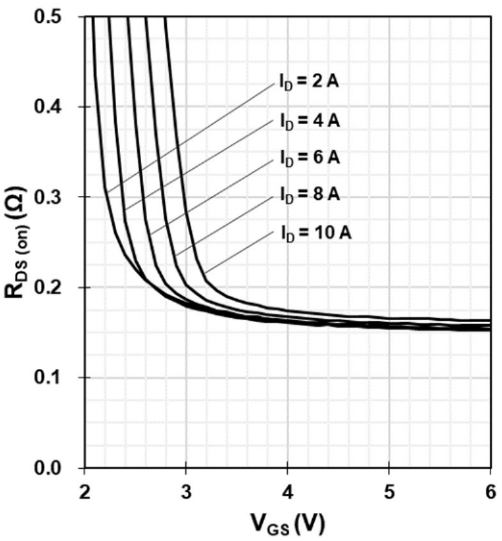
$I_D = f(V_{DS}, V_{GS})$; T_j = 25 °C

Figure 2 Typ. output characteristics



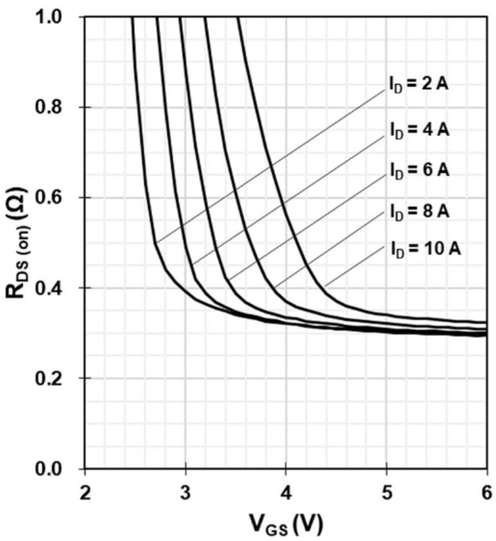
$I_D = f(V_{DS}, V_{GS})$; T_j = 125 °C

Figure 3 Typ. drain-source on-state resistance



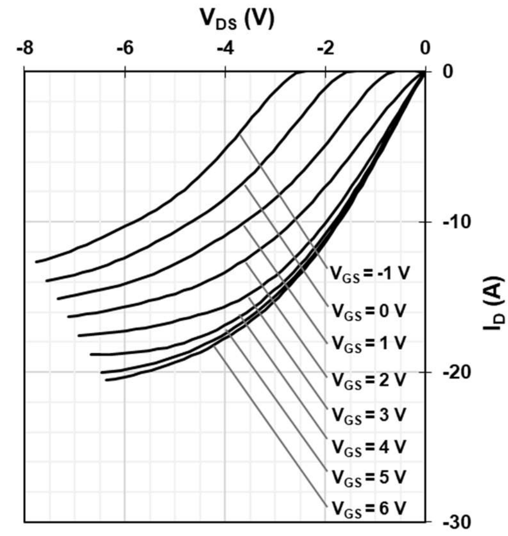
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 25 °C

Figure 4 Typ. drain-source on-state resistance



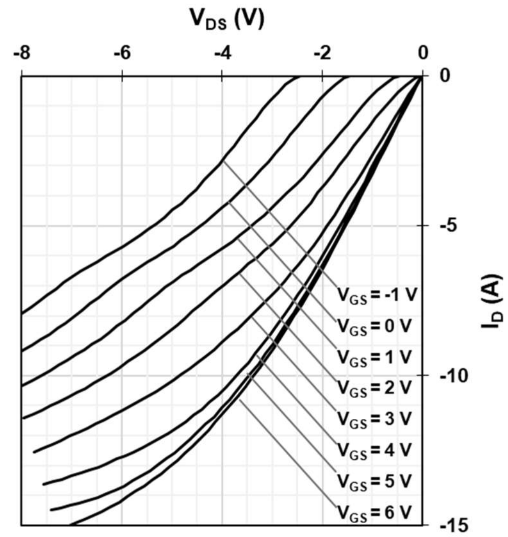
$R_{DS(on)} = f(I_D, V_{GS})$; T_j = 125 °C

Figure 5 Typ. channel reverse characteristics



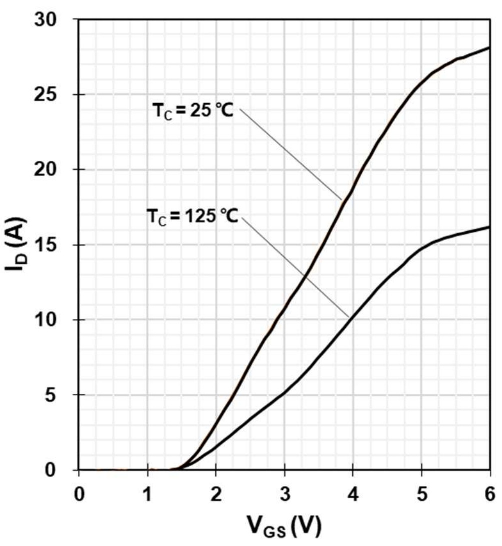
$I_D = f(V_{DS}, V_{GS})$; $T_j = 25$ °C

Figure 6 Typ. channel reverse characteristics



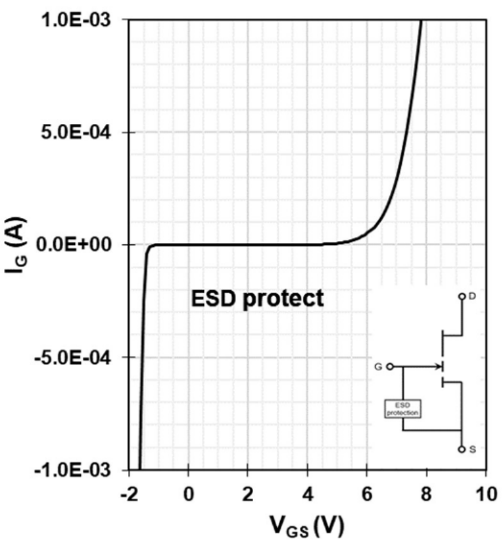
$I_D = f(V_{DS}, V_{GS})$; $T_j = 125$ °C

Figure 7 Typ. transfer characteristics



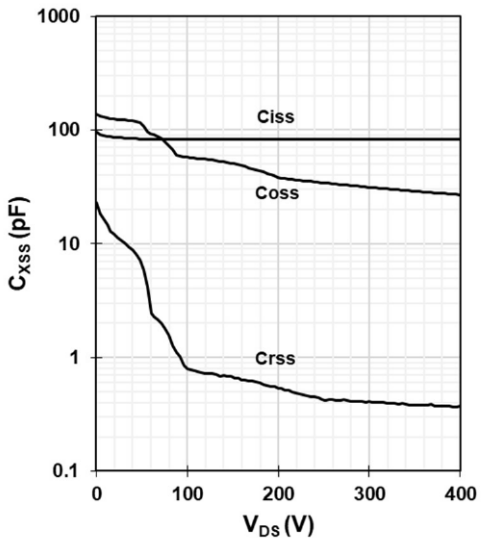
$I_D = f(V_{GS})$; $V_{DS} = 5$ V

Figure 8 Typ. gate-to-source leakage



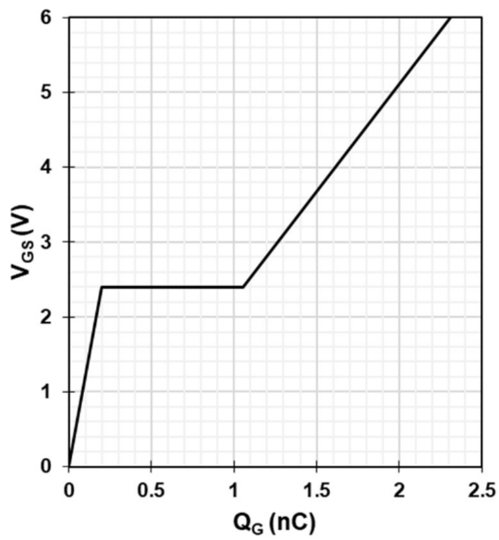
$I_G = f(V_{GS})$; V_D = open

Figure 9 Typ. capacitances



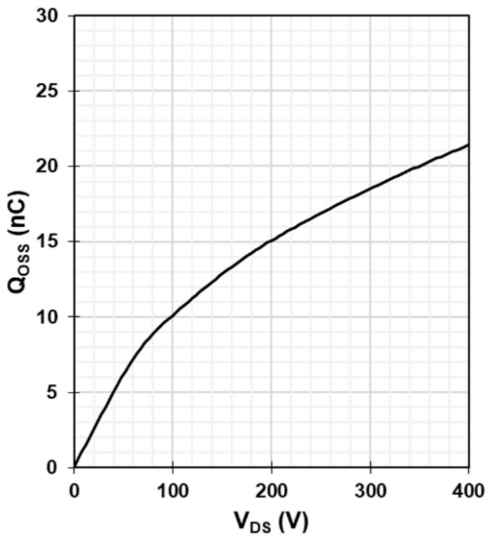
$C_{XSS} = f(V_{DS})$; Freq. = 1 MHz

Figure 10 Typ. gate charge



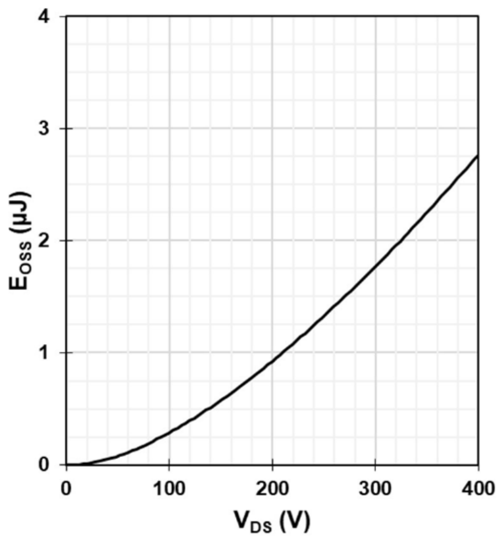
$V_{GS} = f(Q_G)$; V_{DS} = 400 V; I_D = 3 A

Figure 11 Typ. output charge



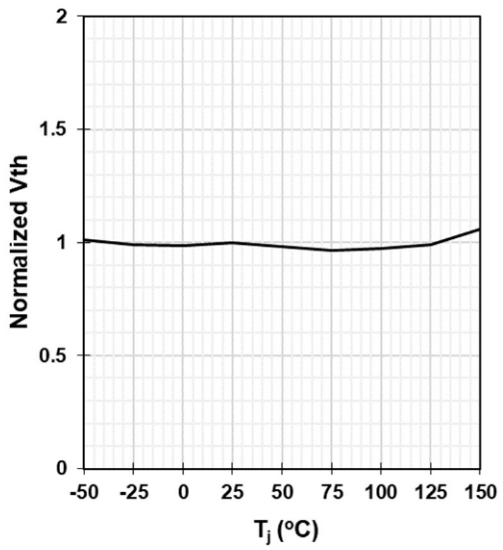
$Q_{OSS} = f(V_{DS})$; Freq. = 1 MHz

Figure 12 Typ. C_{OSS} stored energy



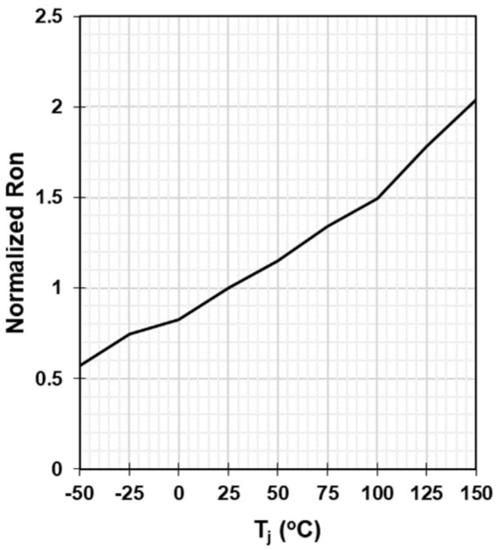
$E_{OSS} = f(V_{DS})$; Freq. = 1 MHz

Figure 13 Gate threshold voltage



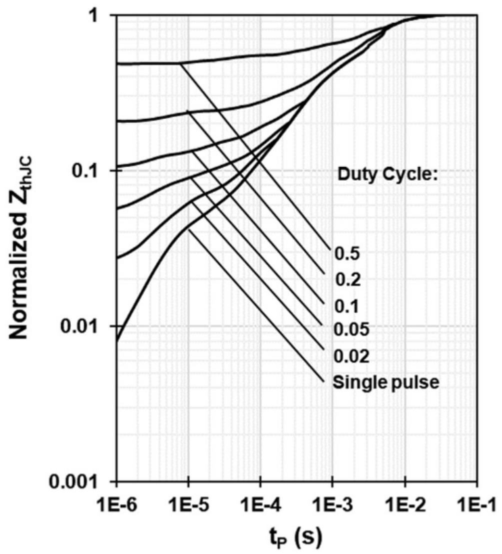
$V_{GS(TH)} = f(T_j)$; $V_{GS} = V_{DS}$; $I_D = 11$ mA

Figure 14 Drain-source on-state resistance



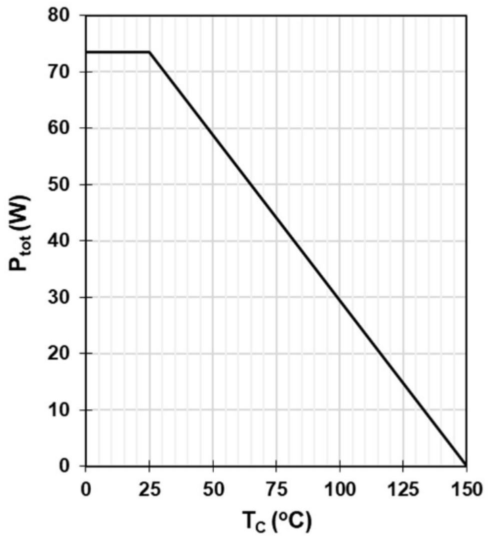
$R_{DS(on)} = f(T_j)$; $I_D = 3$ A; $V_{GS} = 6$ V

Figure 15 Max. transient thermal impedance



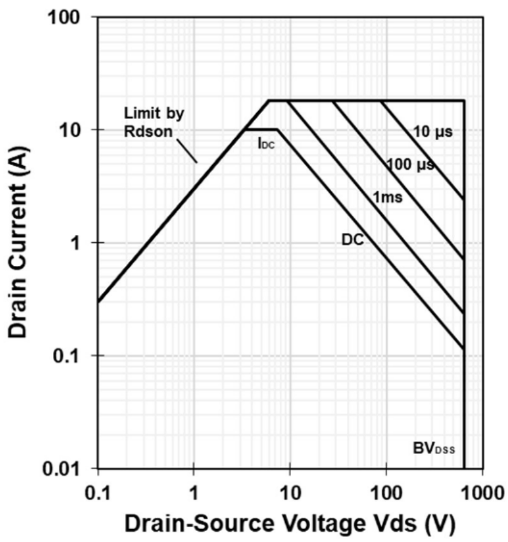
$Z_{thJC} = f(t_P, D)$

Figure 16 Power dissipation



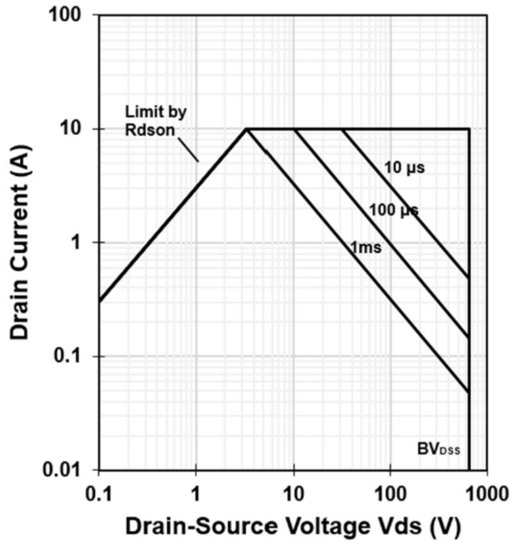
$P_{tot} = f(T_C)$

Figure 17 Safe operating area



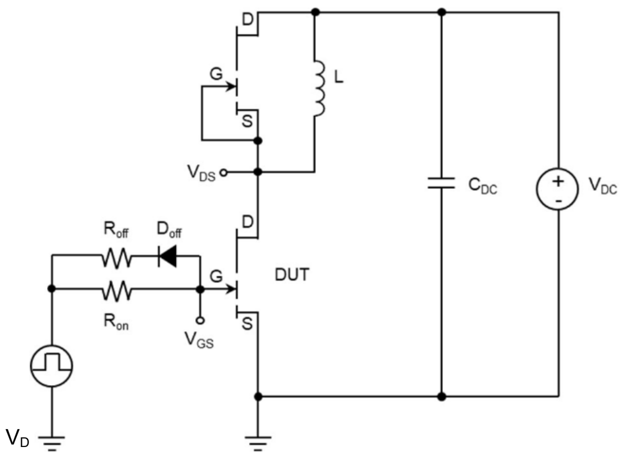
$I_D = f(V_{DS})$; T_C = 25 °C

Figure 18 Safe operating area



$I_D = f(V_{DS})$; T_C = 125 °C

Figure 19 Switching time test circuit

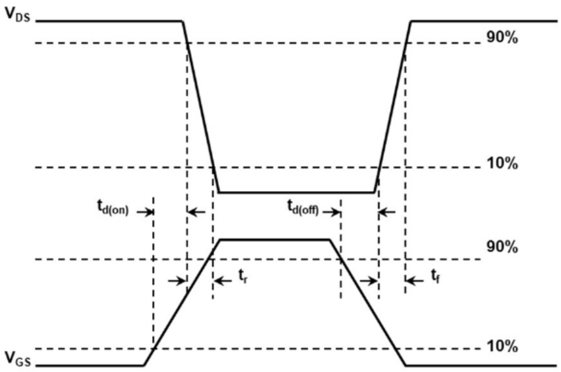


R_{on} = 10 Ω, R_{off} = 2 Ω

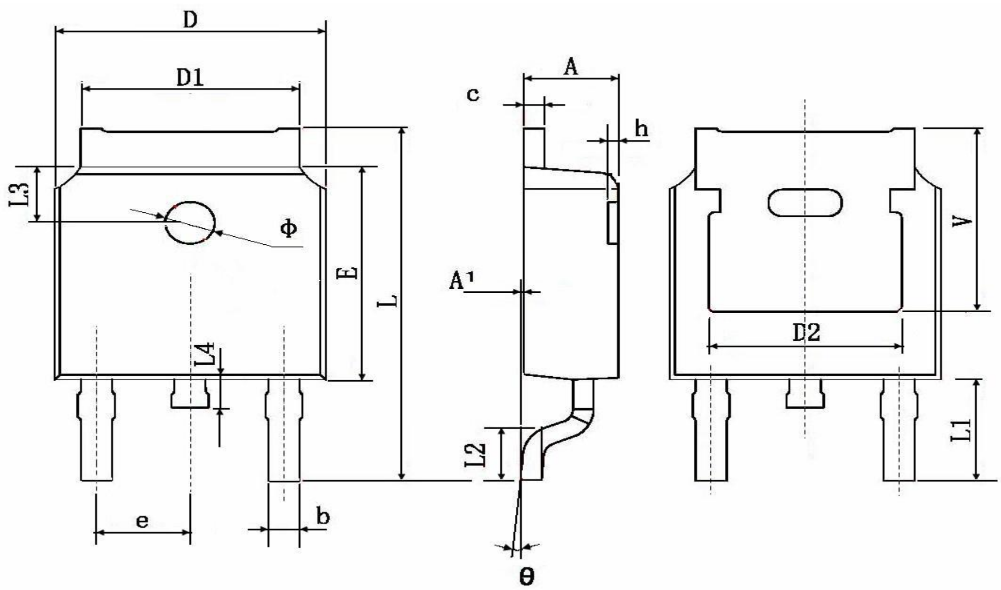
V_{DS} = 400 V, I_D = 6 A, L = 318 µH, V_{GS} = 6 V,

R_{on} = 10 Ω, R_{off} = 2 Ω

Figure 20 Typ. switching time waveforms

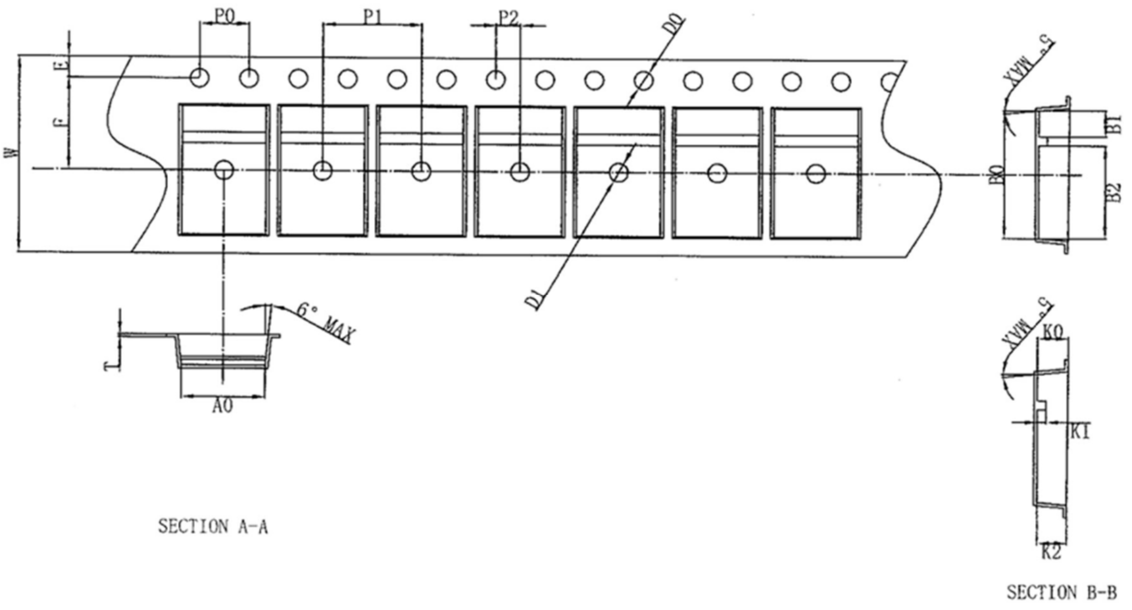


Package outlines
TO-252-2L

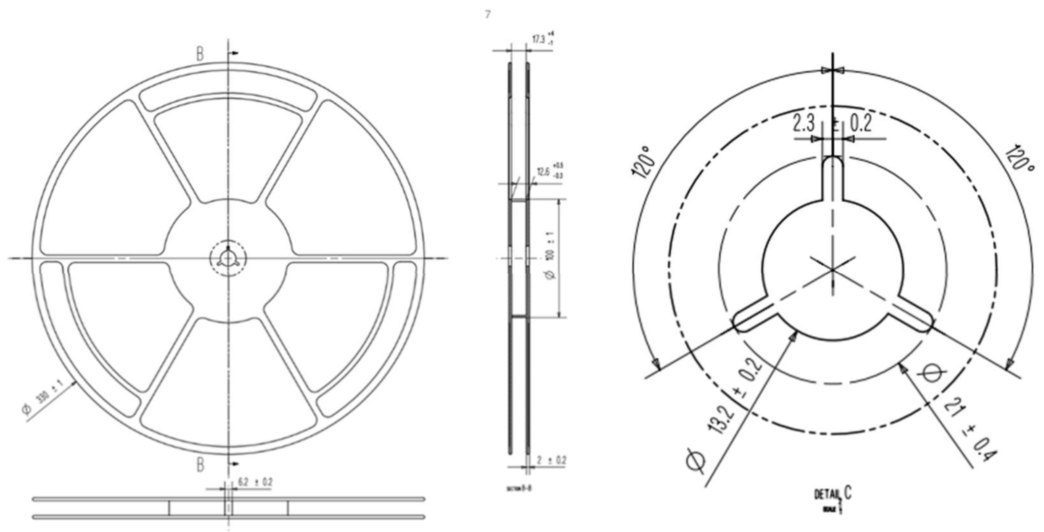


Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	2.200	2.400	0.087	0.094
A1	0.000	0.127	0.000	0.005
b	0.660	0.860	0.026	0.034
c	0.460	0.580	0.018	0.023
D	6.500	6.700	0.256	0.264
D1	5.100	5.460	0.201	0.215
D2	4.830 TYP.		0.190 TYP.	
E	6.000	6.200	0.236	0.244
e	2.186	2.386	0.086	0.094
L	9.800	10.400	0.386	0.409
L1	2.900 TYP.		0.114 TYP.	
L2	1.400	1.700	0.055	0.067
L3	1.600 TYP.		0.063 TYP.	
L4	0.600	1.000	0.024	0.039
Φ	1.100	1.300	0.043	0.051
θ	0°	8°	0°	8°
h	0.000	0.300	0.000	0.012
V	5.350 TYP.		0.211 TYP.	

Reel information



SYMBOL	DIMENSION	SYMBOL	DIMENSION
W	16.00±0.30	10P0	40.00±0.20
E	1.75±0.10	P1	8.00±0.10
F	7.50±0.05	A0	6.80±0.10
D0	1.625±0.125	B0	10.40±0.10
D1	1.55±0.05	K0	2.5±0.10
P0	4.00±0.10	T	0.25±0.05
P2	2.00±0.10	K1	0.70±0.05
B1	2.10±0.05	K2	2.40±0.10
B2	7.55±0.05		



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