Katherine Perez

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EXPERIENCE

Microsoft
Program Manager/SW Developer Intern — Redmond, WA | May 2018 - Aug 2018
> Wrote a functional spec for a Windows driver that updates firmware of Surface docks
> Wrote Windows kernel-mode driver code in C++ to interact with user-mode driver and application

Tesla
Autopilot Hardware Intern — Palo Alto, CA | Jan 2018 - May 2018
> Developed software written in Python to enable automated regression testing
> Developed test plans and test cases to ensure coverage for various IPs, including camera and compute

Intel
Solid-State Drive Validation Intern — Folsom, CA | Jun 2017 - Sep 2017
> Worked with Functional Validation team, reproduced issues with failing drives and assisted with debug to root-cause errors
> Developed features for sequential and concurrent workload validation tool: PCIe register and memory-mapped I/O access in Linux

Intel
Solid-State Drive Validation Intern — Folsom, CA | May 2016 - Aug 2016
> Owner of automated SSD validation test suite - PCIe protocol/host level
> Wrote validation tool in Python which increased testing efficiency by 100%
> Enable cross-platform testing compatibility in Windows and Linux

PROJECTS

Dynamic Braille Panel — *Senior Design Capstone* — Fall 2016 - Spring 2017
> Designed a wirelessly connected information panel which features a programmable, refreshable Braille display
> Programmed TI MSP432 (ARM Cortex M4F) to control electromechanical actuators

Hearthstone Learning Agent — *Intro to Artificial Intelligence* — Spring 2017
> Utilized a decision tree and multi-layered neural network to train a learning agent to successfully play Hearthstone, an online strategy card game

Autonomous Maze-Solving Robot — *Embedded Systems* — Spring 2017
> Programmed a TI Tiva-C microcontroller in C to autonomously solve a maze in the least amount of time while utilizing PID control algorithms
> Utilized RTOS functions (HWI/SWI, semaphores and tasks) to interface with ultrasonic sensors, reflectance sensors, Bluetooth and DC motors

Hybrid Branch Prediction in a Pipelined Processor
Computer Architecture — Spring 2017
> Described a five-stage RISC-V ISA processor in Verilog
> Designed a hybrid branch predictor which features static and two-level adaptive branch prediction techniques

Bomb Squad: FPGA-Based Game — *Advanced Digital Design* — Fall 2016
> Created an interactive game in Verilog which requires the user to solve puzzles displayed on an FPGA
> Utilized Altera DE2-115 development board to implement game features

EDUCATION

UNIVERSITY OF CALIFORNIA, IRVINE
M.S. Computer Engineering
Spring 2019

UNIVERSITY OF HOUSTON
B.S. Electrical Engineering
> Computers/Embedded Systems
Spring 2017 | Magna Cum Laude

SKILLS

LANGUAGES

Python, C++/C, Verilog, Java, Assembly, HTML/CSS, Javascript, SQL

TECHNOLOGIES

Linux, Git, Shell/Bash, TI-RTOS, FreeRTOS, TFS, Visual Studio, Jira, Confluence, Code Composer Studio, Arduino, Altera ModelSim, Quartus Prime, OrCad PSpice, AutoDesk

COURSEWORK

> Computer Architecture
> Design & Analysis of Algorithms
> Real-Time Computer Systems
> Multicore Programming
> State Control, ML & AI
> Artificial Intelligence

MEMBERSHIPS

> Tau Beta Pi (Engineering Honor Society)
> Institute of Electrical and Electronics Engineers (IEEE)

LINKS

> github.com/khperez
> linkedin.com/in/khperez