KATHERINE PEREZ

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EDUCATION

University of California, Irvine - Samueli School of Engineering September 2017-May 2019 (expected)
- M.S. Computer Engineering
- Research Interests: Embedded Systems and Computer Architecture

University of Houston - Cullen College of Engineering August 2012-May 2017
- B.S. Electrical Engineering, Concentration: Computers and Embedded Systems
- Major GPA: 3.655, Magna Cum Laude

TECHNICAL SKILLS

Programming Languages: Python, C, C++, Java, Verilog, Assembly, SQL, Web (HTML, CSS, JavaScript)
Design: Altera ModelSim, Quartus Prime, OrCad PSpice, Autodesk Inventor

WORK EXPERIENCE

Solid-State Drive Validation Intern at Intel Corporation June 2017-September 2017
- Worked with Functional Validation Team, reproduced issues with failing drives and assisted with debug to root-cause errors.
- Developed features for sequential and parallel workload validation tool: PCIe register and memory-mapped I/O access.
- Responsible for overall tool compatibility in Linux.

Solid-State Drive Validation Intern at Intel Corporation May 2016-August 2016
- Owner of automated SSD validation test suite – PCIe protocol/host level.
- Developed a validation tool written in Python which increased testing efficiency by 100%.
- Enabled cross-platform testing compatibility in Windows and Linux.

Senior Design Lab Teaching Assistant at UH Electrical and Computer Engineering Dept. August 2016 – May 2017
- Worked with Omron Robotics Laboratory and Senior Capstone Laboratory.
- Created demonstrations for a programmable logic controller, integrate PLCs and ladder logic in curriculum.

Product Validation Intern at Intel Corporation June 2015-August 2015
- Drove product test plan web-integration project to optimize version control.

PROJECTS

Dynamic Braille Panel – *Senior Design Capstone* Fall 2016 – Spring 2017
- Designed a wirelessly connected information panel which features a programmable, refreshable Braille display.
- Programmed a TI Launchpad to control electromechanical actuators.

Hearthstone Learning Agent – *Introduction to Artificial Intelligence* Spring 2017
- Utilized a decision tree and multi-layered neural network to train a learning agent to successfully play Hearthstone, an online strategy card game.

Autonomous Maze-Solving Robot – *Embedded Systems* Spring 2017
- Programmed a Texas Instruments Tiva-C microcontroller in C to autonomously solve a maze in the least amount of time while utilizing PID control algorithms.
- Utilized RTOS functions (HWI/SWI, semaphores, and tasks) to interface with infrared sensors, reflectance sensors, Bluetooth and DC motors.

Hybrid Branch Prediction in a Pipelined Processor – *Computer Architecture* Spring 2017
- Described a five-stage RISC-V ISA processor in Verilog.
- Designed a hybrid branch predictor which features static and two-level adaptive branch prediction techniques.

Bomb Squad: FPGA-Based Game – *Advanced Digital Design* Fall 2016
- Created an interactive game in Verilog which requires the user to solve puzzles displayed on FPGA.
- Utilized Altera DE2-115 development board to implement the game's hardware features.

MEMBERSHIPS

Tau Beta Pi (Engineering Honors Society) Spring 2016 – Present
Institute of Electrical and Electronics Engineers (Executive Board Officer: Resource Chair) Fall 2013-Spring 2017