Electronic Devices

ECS 321

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Textbook Reading

R. Pierret. *Semiconductor Device Fundamentals.*

Section 1.3: Crystal Growth

Chapter 4: Basics of Device Fabrication

Slides

Experimental

- **Fabrication**
  - Oxidation
  - Diffusion, Ion implantation
  - Etching
  - Lithography (Optical, Electron-beam)
  - Thin film deposition
    - Physical Vapor Deposition (PVD)
      - Evaporation (Thermal, Electron-beam)
      - Sputtering
    - Chemical Vapor Deposition (CVD)
- **Characterization**
  - Electrical characterization - Probe station (IV, CV characteristics)
  - X-Ray Diffraction (XRD)
- **Imaging**
  - Optical Microscope
  - Electron Microscopes
    - Scanning Electron Microscopy (SEM)
    - Transmission Electron Microscopy (TEM)

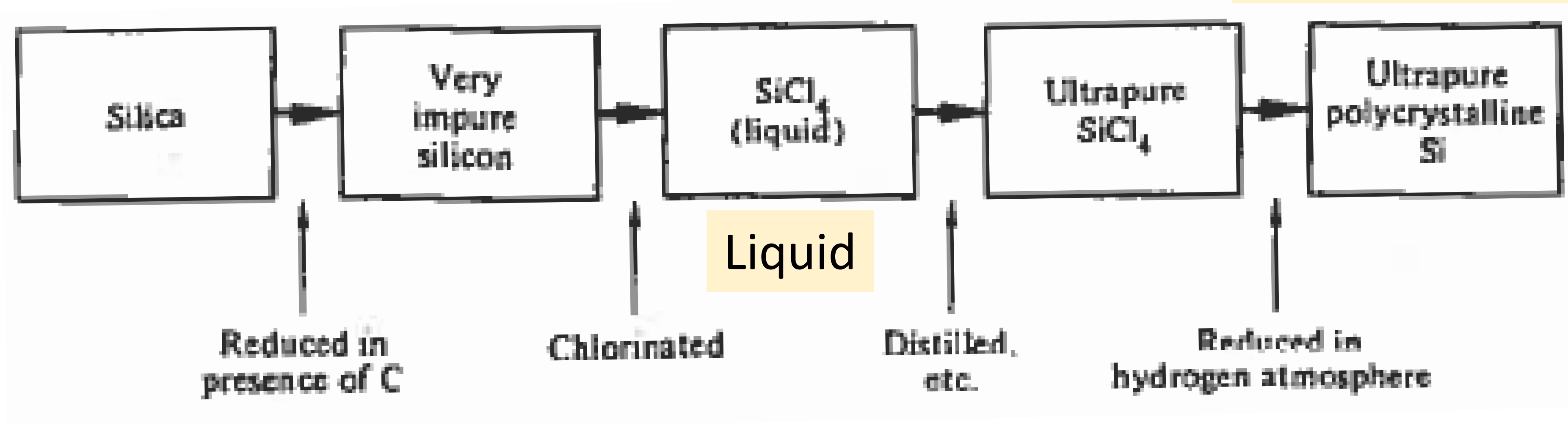
Crystal growth: Obtaining ultrapure Si

(**First** is Oxygen)

- Si is the **second** most abundant element in the Earth's crust
- Si never occurs alone, most of in the forms
  - Silica (impure SiO_2)
  - Silicates ($Si\ +\ O\ +$ another element)

NOT single-crystal

Polycrystalline

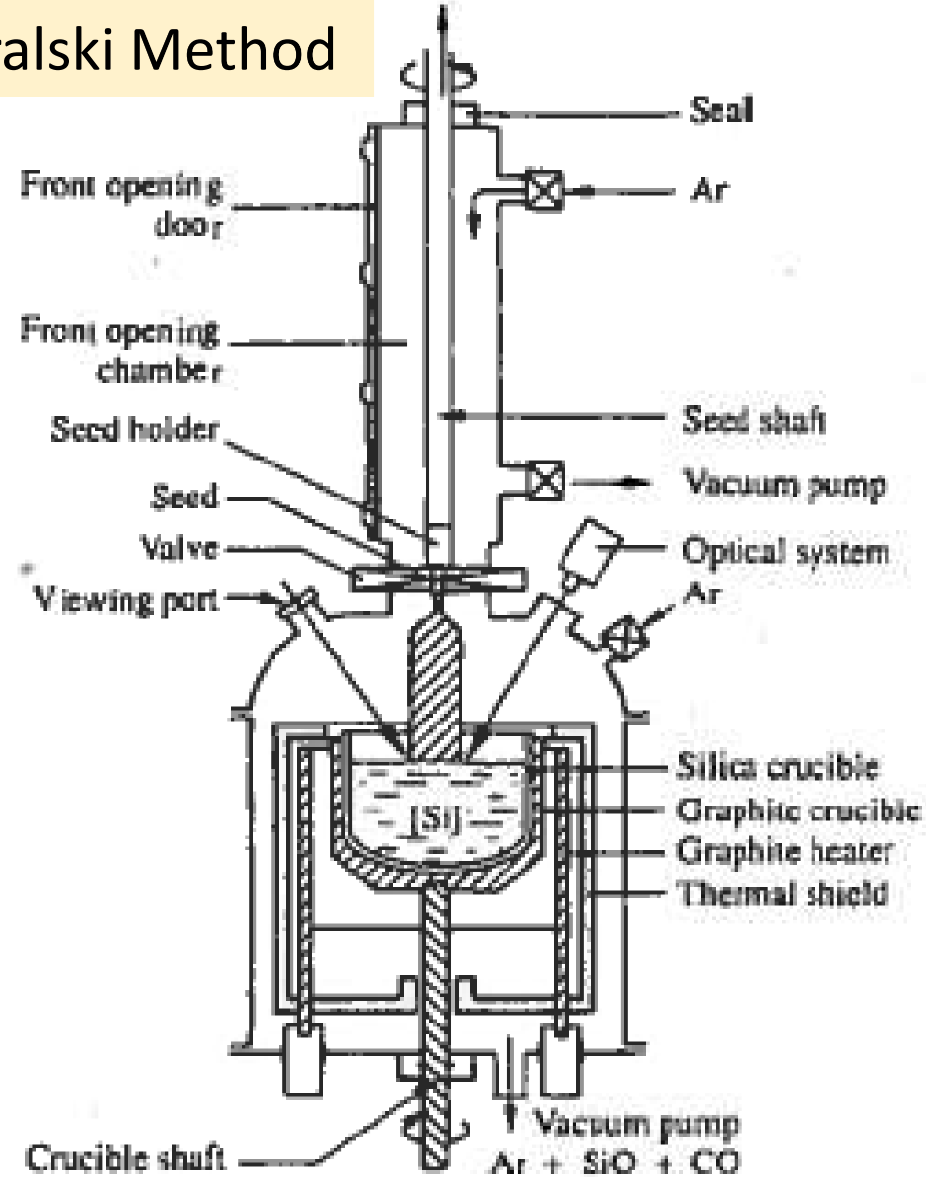


- While solids are very difficult to purify, standard procedures are available for purifying liquids

Crystal growth: Single-crystal formation

Czochralski Method

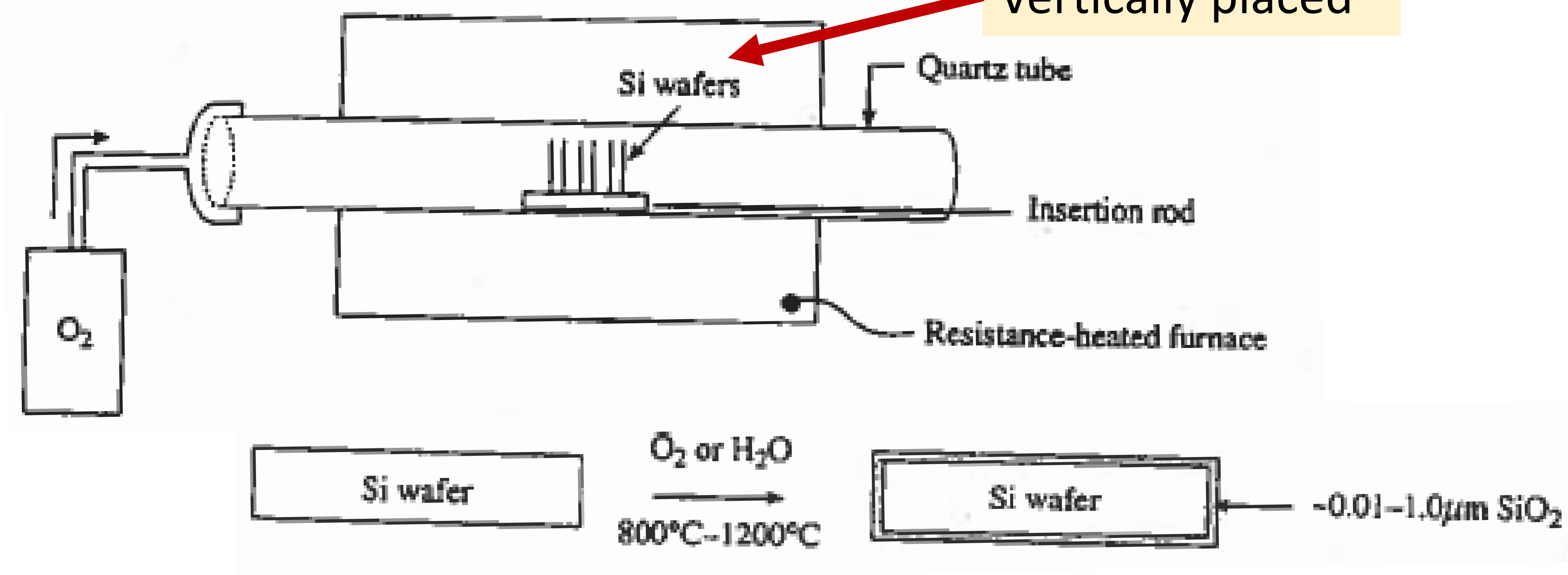
- Poly-Si is heated to form a melt
- A small single-crystal (*seed* crystal) is dipped into the melt
  - ⟨100⟩ or ⟨111⟩
- Seed crystal is slowly rotated and withdrawn from the melt
- Ingots (cylinder of single-crystal)
  - Diameter: 200 m (8 inch)
  - Length 1-2 meters in length
- Cut the cylinders in thin wafers
  - Thickness ~0.5 mm



Oxidation

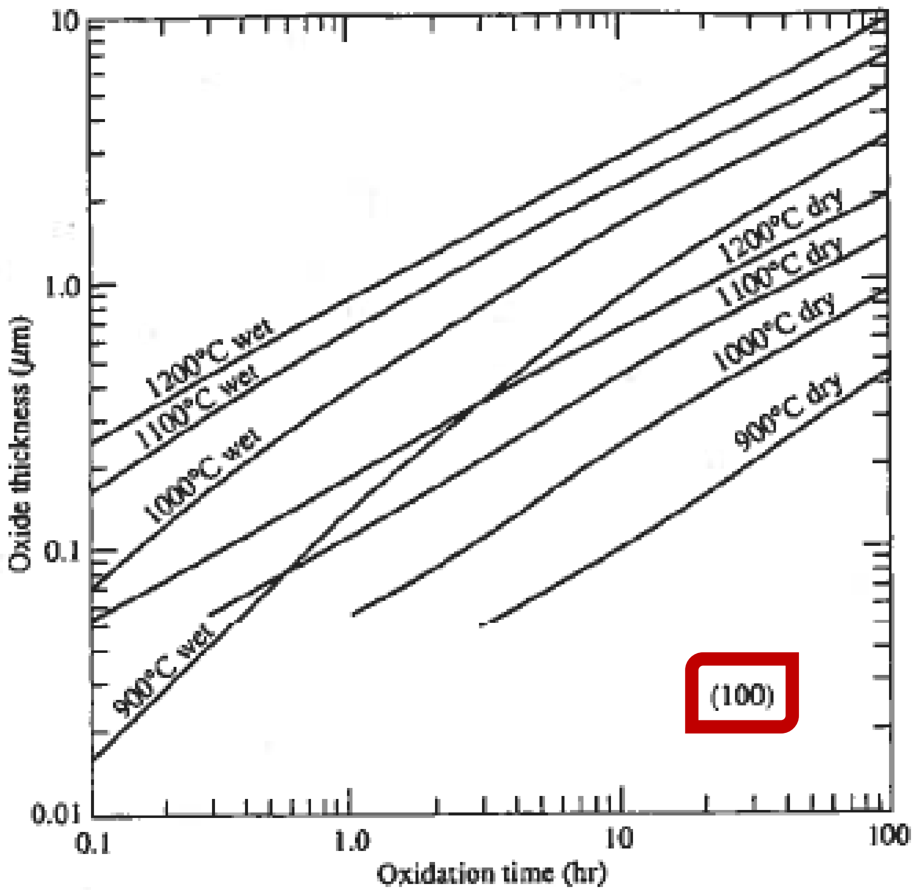
Dry oxidation	$Si + O_2 \rightarrow SiO_2$	Critical insulator regions (gate oxide in MOSFET)
Wet oxidation	$Si + 2H_2O \rightarrow SiO_2 + 2H_2$	Fast (thick barrier oxide)

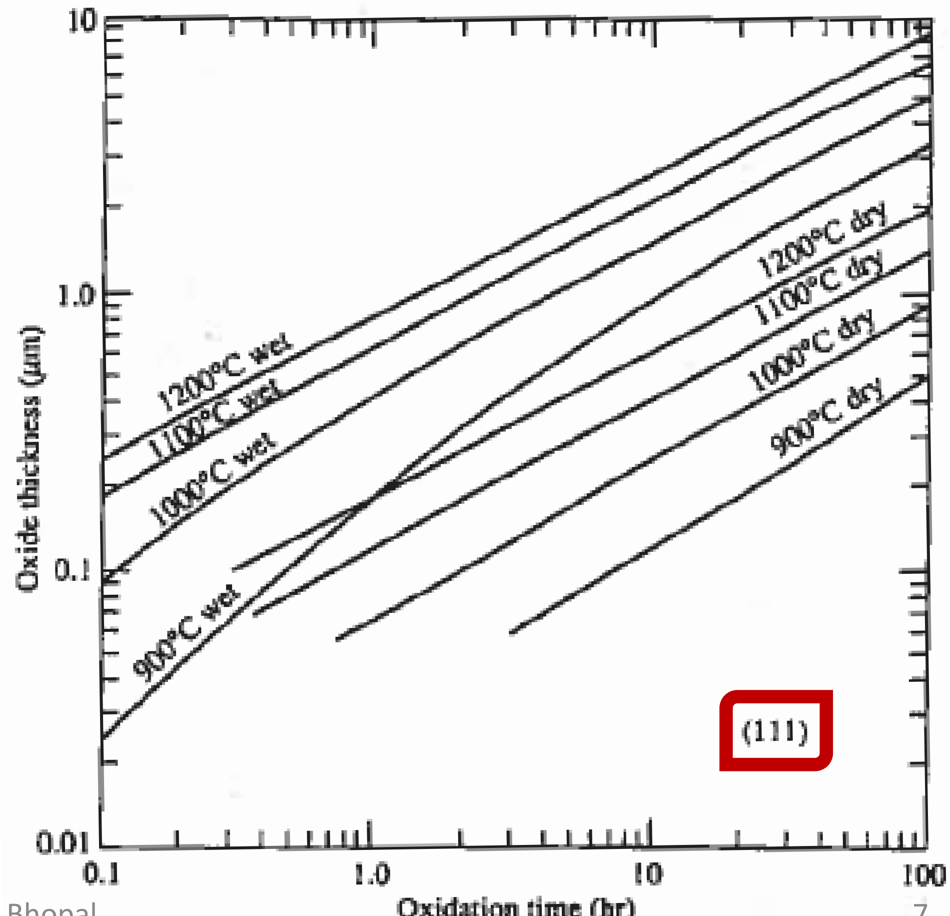
Vertically placed



Wet oxidation: Bubbling a carrier gas (Ar or N_2) through water in a heated flask

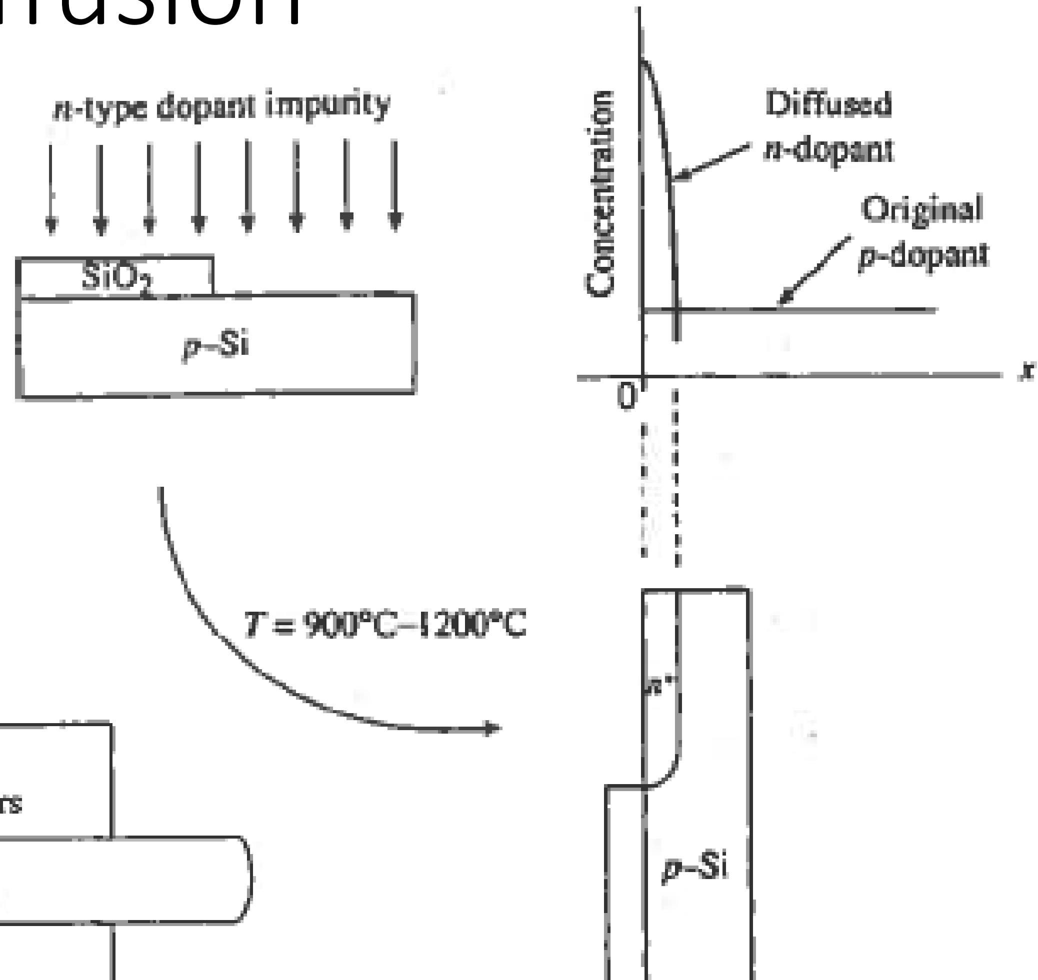
Oxidation: Growth rate



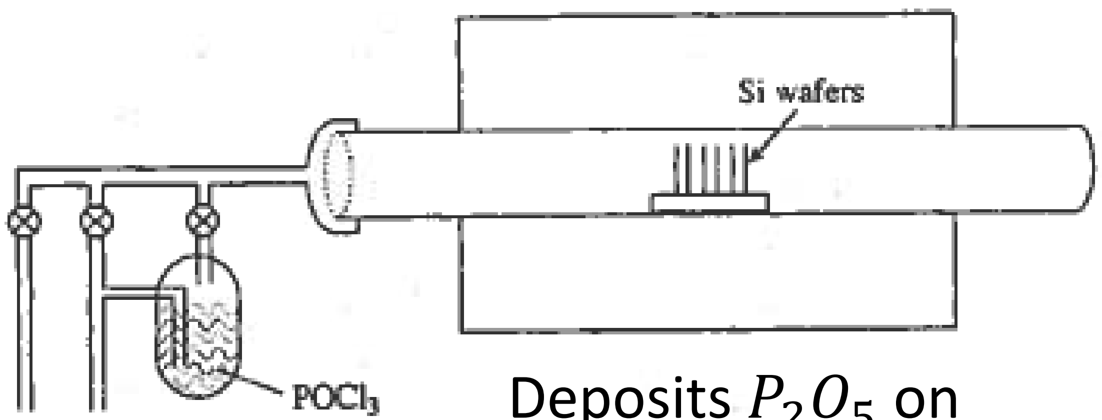


Diffusion

SiO_2 protects the underlying Si for only a limited period of time



Similar tube as in oxidation



Liquid

Deposits P_2O_5 on the Si wafer surface

Predeposition: Source present

Drive-in: Source removed

Diffusion profiles

$$N_1(x, t_1) = N_0 \mathrm{erfc}\left(x/2\sqrt{D_1 t_1}\right)$$

$$N_2(x, t_2) = N_0 \left(\frac{2}{\pi}\sqrt{\frac{D_1 t_1}{D_2 t_2}}\right) e^{-\left(\frac{x}{2\sqrt{D_2 t_2}}\right)^2}$$

1: Predeposition

2: Drive-in

$$D_2 t_2 >> D_1 t_1$$

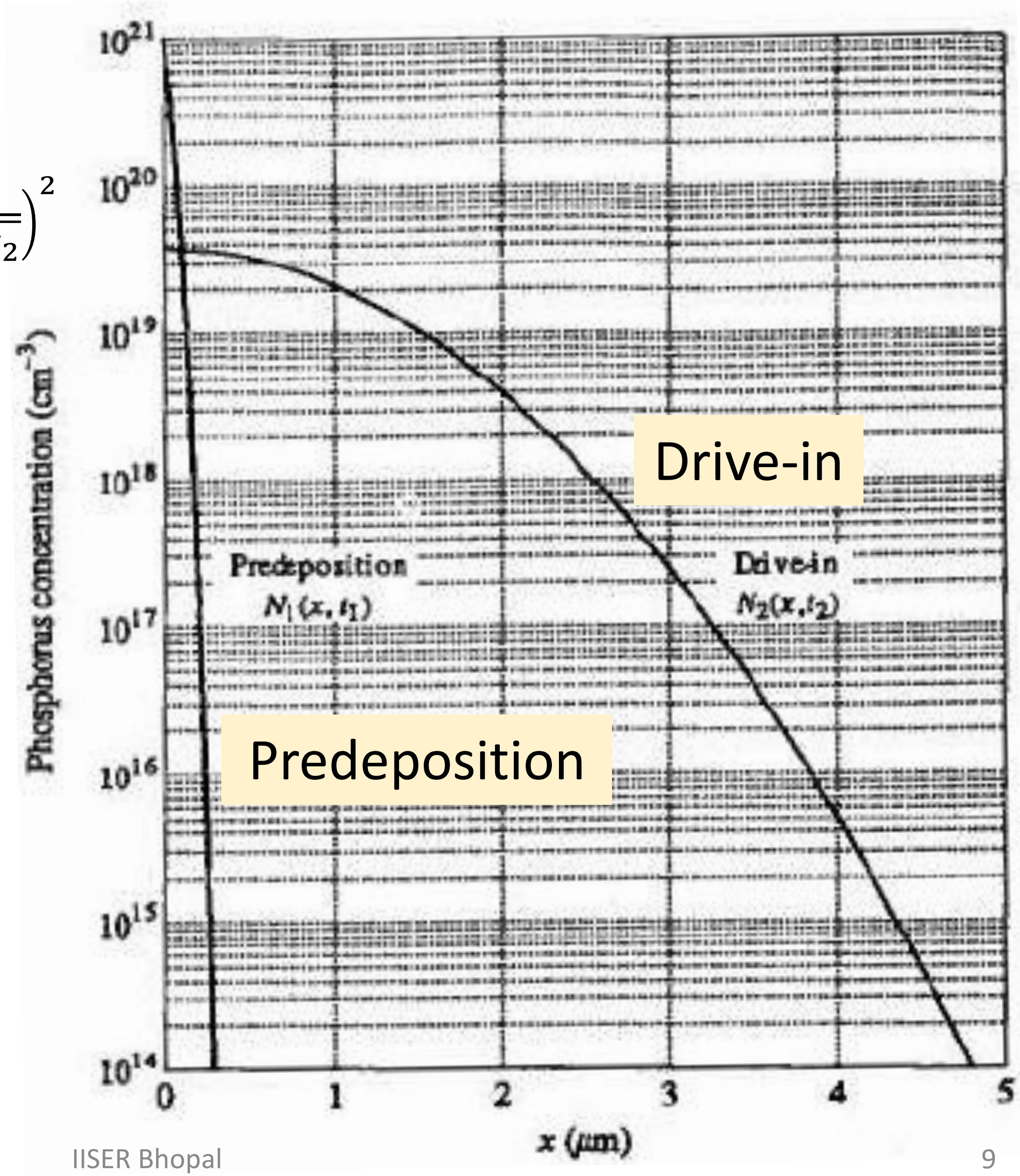
$$N_0 = 10^{21} \ /cm^3$$

$$D_1 = 2.58 \times 10^{-14} \ cm^2/Sec$$

$$D_2 = 2.49 \times 10^{-12} \ cm^2/Sec$$

$$t_1 = 600 \ Sec$$

$$t_2 = 1800 \ Sec$$



Ion Implantation

Alternative means to introducing dopants

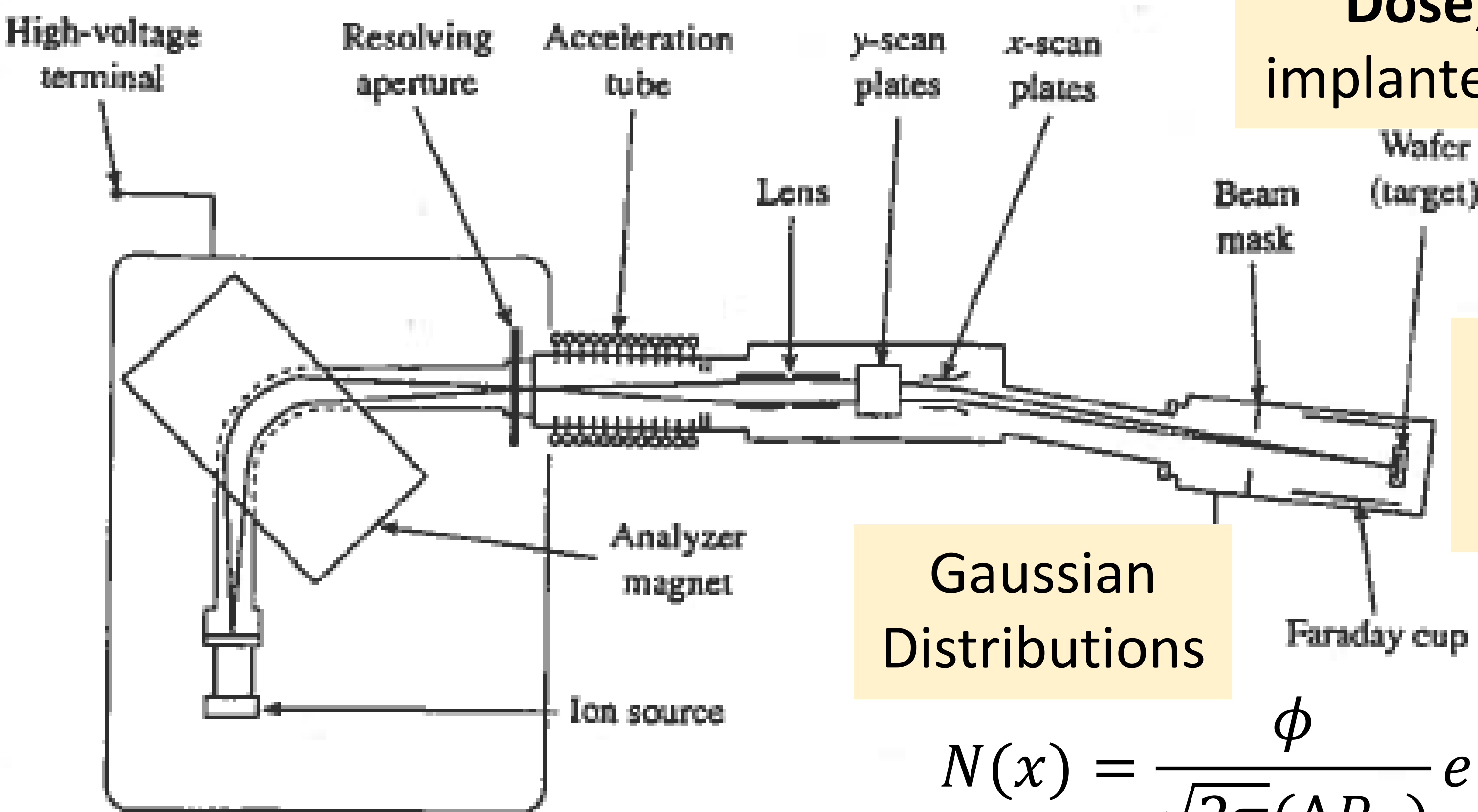
5 keV – 1MeV

Accelerating and shooting the **ions** into the semiconductor

Electrical contact to the wafer allows the flow of electrons to **neutralize**

A follow-up **anneal** to remove crystal damage and activate implants

Dose, ϕ: No. of implanted ions $/cm^2$



R_P : Projected range

ΔR_P: Straggle

Gaussian Distributions

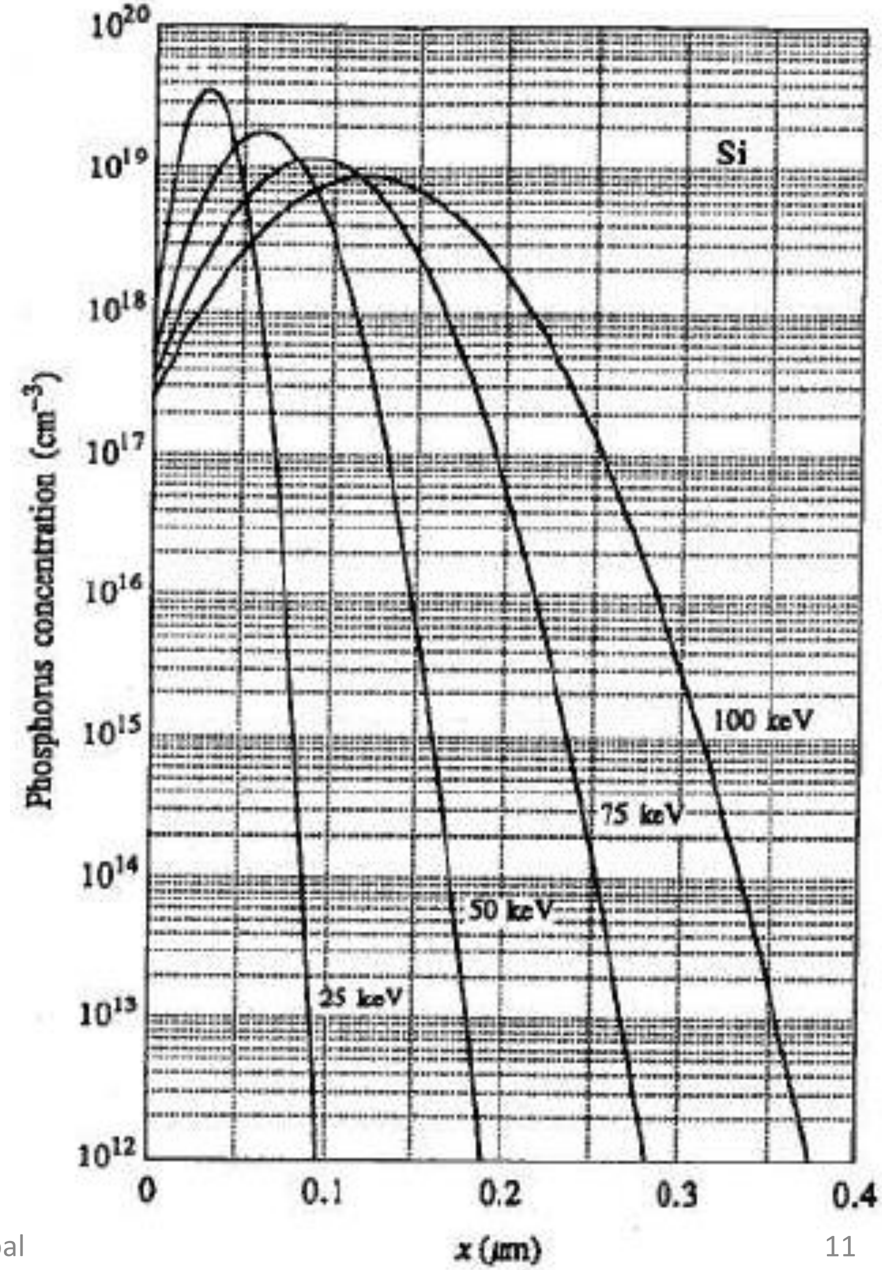
$$N(x) = \frac{\phi}{\sqrt{2\pi}(\Delta R_P)} e^{-\frac{1}{2}\left(\frac{x-R_P}{\Delta R_P}\right)^2}$$

Ion Implantation

$$N(x) = \frac{\phi}{\sqrt{2\pi}(\Delta R_P)} e^{-\frac{1}{2}\left(\frac{x-R_P}{\Delta R_P}\right)^2}$$

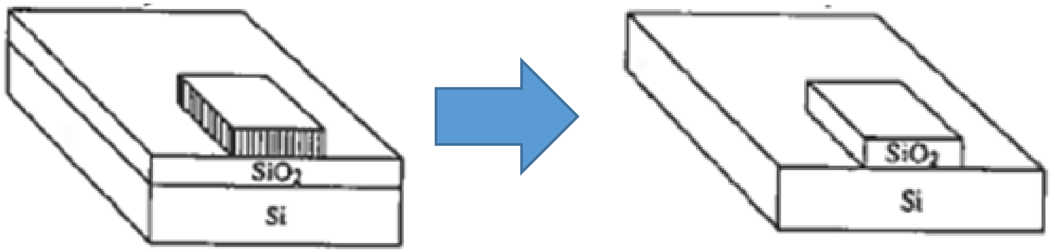
Advantages over diffusion

- Low temperature process
  - ✓ Done at room temperature
- Anneal as low as 600º C
- Precise control, avoids undesirable spread of the concentration
- Very shallow (100 nm) concentration profile
- Buried SiO_2 layer naturally can be formed for SOI structures



Etching

Removal of unprotected parts of a surface to create a pattern



Wet etch: Chemical etching, liquid etching

Dry etch: Plasma etching, gas etching, physical dry etching, chemical dry etching, physical-chemical etching

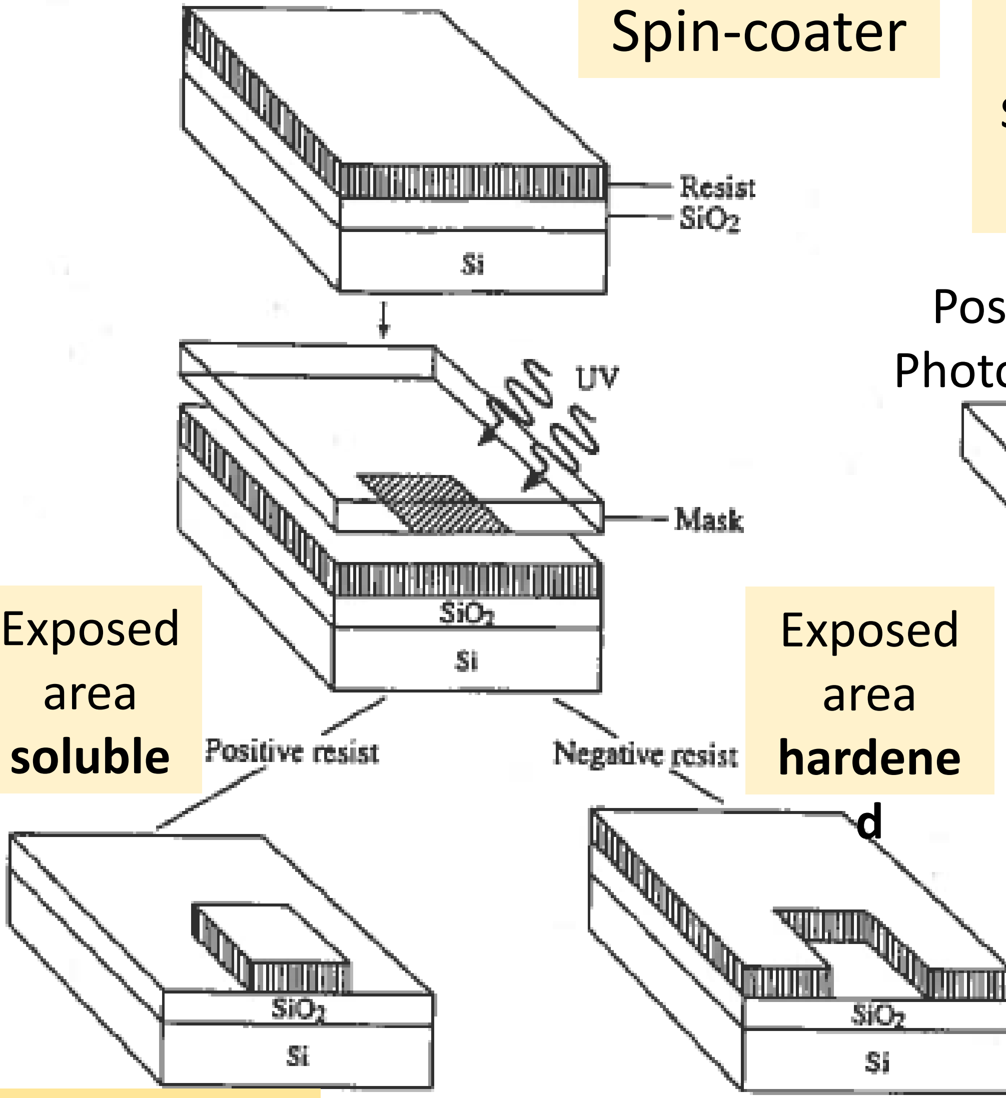
Physical dry etching: High energy kinetic energy (ion, electron, or photon) beams to etch off the substrate atoms

Chemical dry etching: No liquid chemicals or etchants, it involves a chemical reaction between etchant gases to attack the surface

Reactive ion etching (RIE): Uses both physical and chemical mechanisms to achieve high levels of resolution

RIE is the most widely used process in industry and research

Lithography: Pattern generation



Spin-coater

UV-light sensitive material

e.g., AZ1518
Positive Photoresist
3000 rpm, 30 secs

Exposed area **soluble**

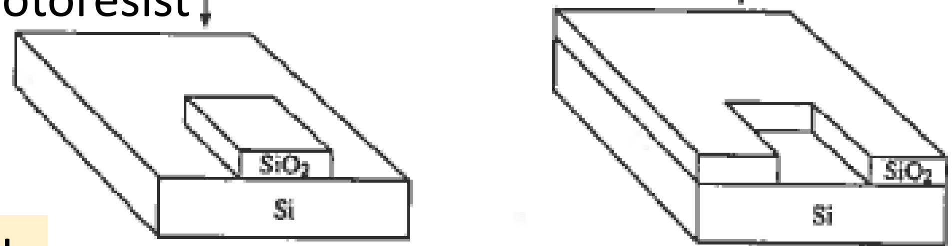
Exposed area **hardened**

e.g., AZ351

After developing

Positive Photoresist

Negative Photoresist



After oxide **etching** and resist removal

HF for SiO_2

Maskless (shutter when the electron beam moves) Lithography
Electron Beam Lithography (EBL)

Evaporation (Thermal/E-Beam)

Older/straightforward method of thin-film deposition

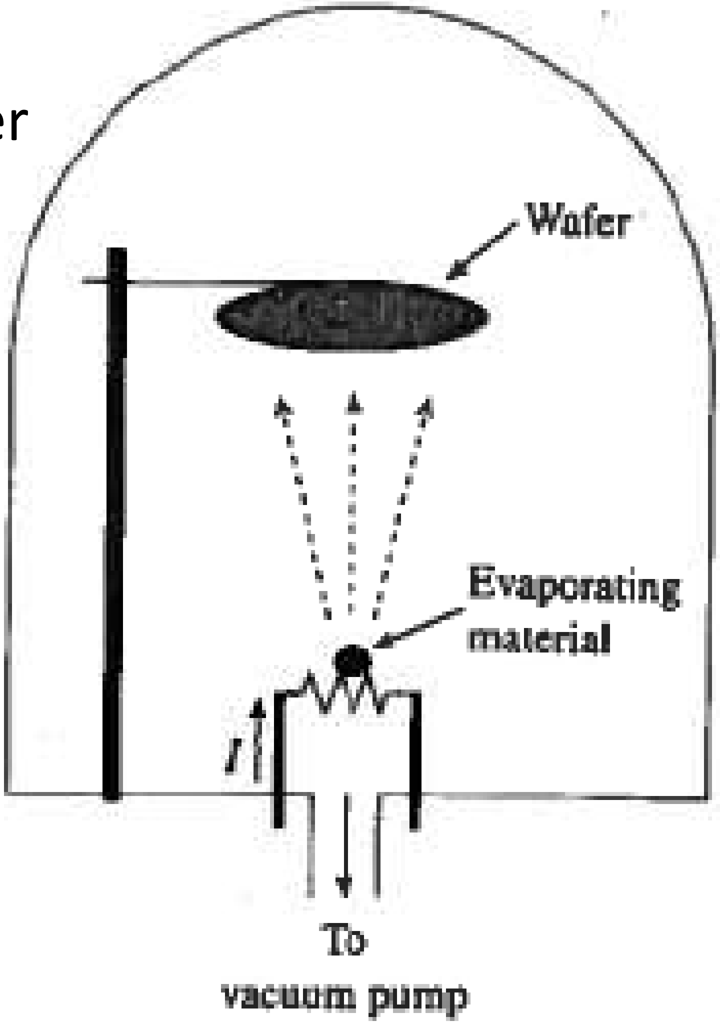
The material is placed on a resistance-heated source holder in a vacuum chamber e.g., Al wire in tungsten filament

Under vacuum, the source material travel unimpeded to the substrate

Thermal evaporation is subject to **high levels of contamination**

Electron-beam evaporation **eliminates contamination**

Aluminum pellets for e-beam evaporation



Sputtering

Sputtering target

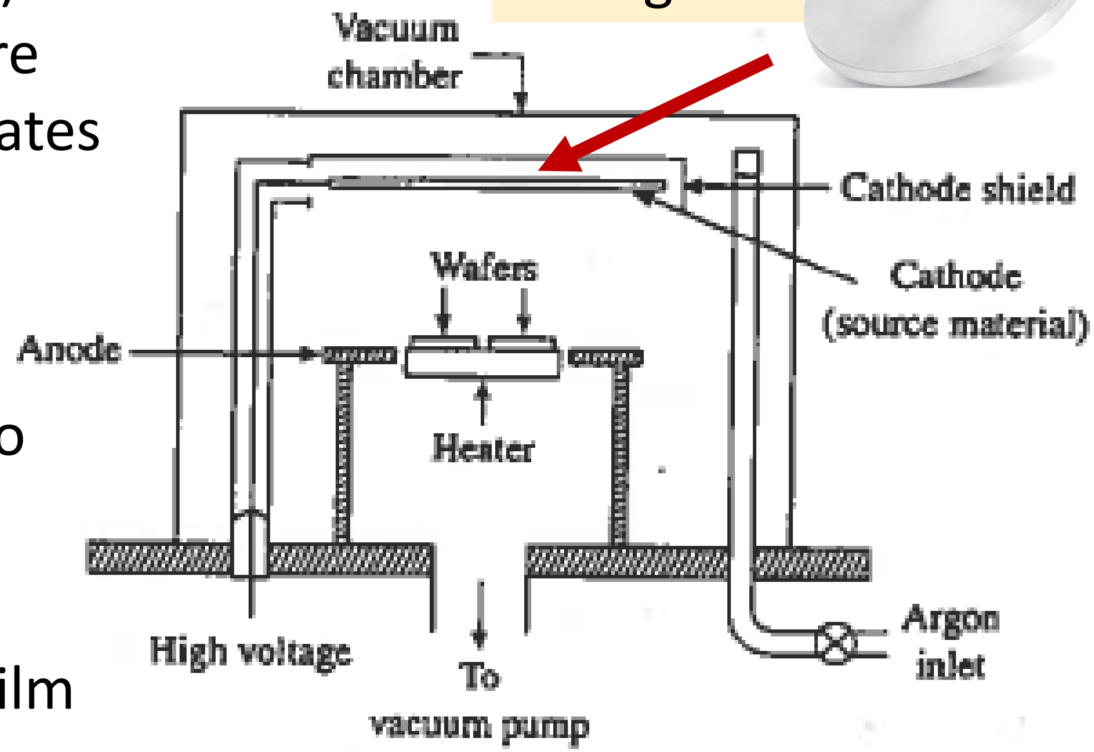
The source material (negative) and the substrate (positive) are placed on opposite parallel plates

A low-pressure amount of sputtering gas (Argon) is put

Ionized Argon is accelerated to the source material

Under vacuum, the source material is deposited as thin film

RF power supply is required for insulator deposition



RF Magnetrons

Sputtering is the commercial method of thin-film deposition
Low-temperature, low-contamination, acceptable surface roughness

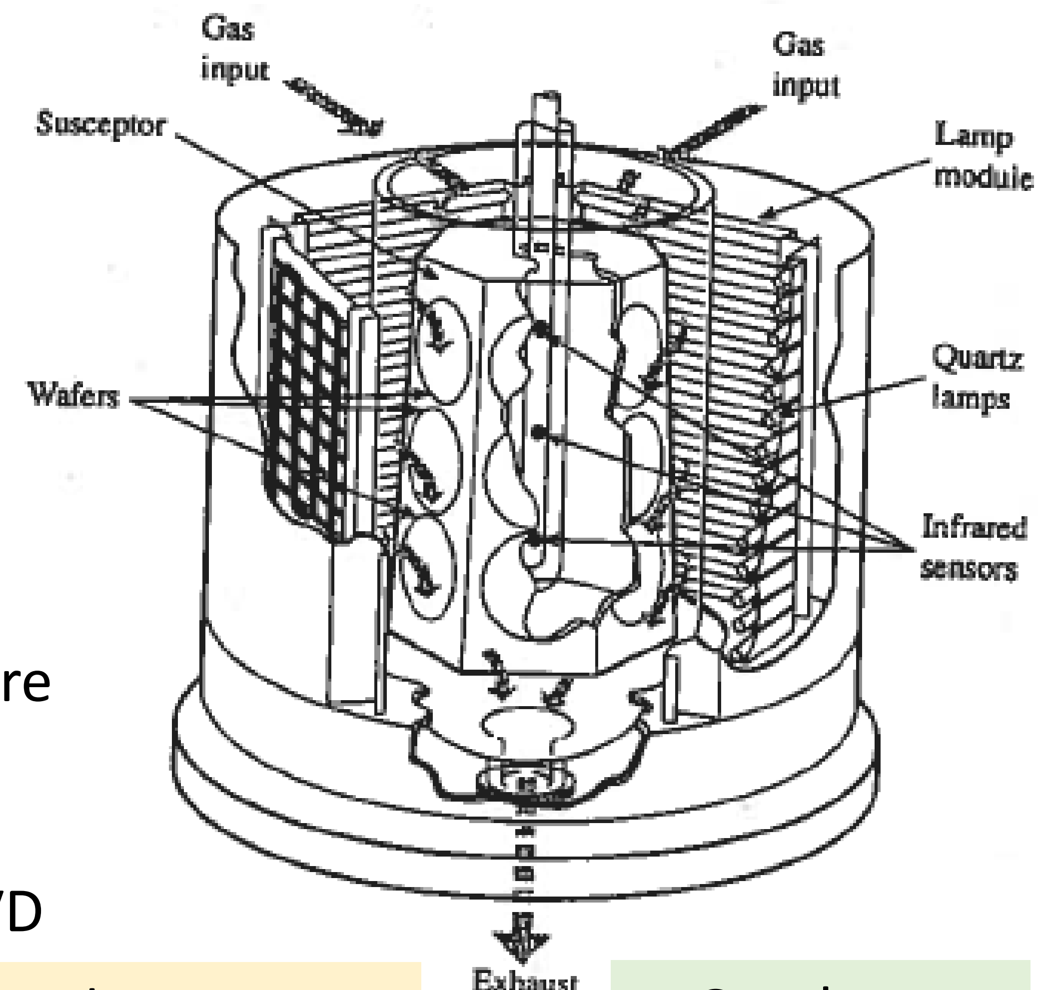
Chemical Vapor Deposition (CVD)

Thin film is formed from one or more gas phase components

- ✓ A gas compound decomposes to form a film
- ✓ A reaction between gas components form a film

Different configurations

- ✓ APCVD : Atmospheric pressure CVD
- ✓ LPCVD: Low-pressure CVD
- ✓ PECVD: Plasma enhanced CVD



PECVD: Plasma impart energy to the reaction gases, enhancing the reactions and permitting low-temperature process

Graphene on Copper foil using CVD

Epitaxy

Epitaxy produces a **crystalline** thin film on the semiconductor lattice

Epitaxy: Greek word meaning "upon-arranged"

The doping of the epi-layer is controlled by introducing a dopant containing gas e.g., phosphine (PH_3)

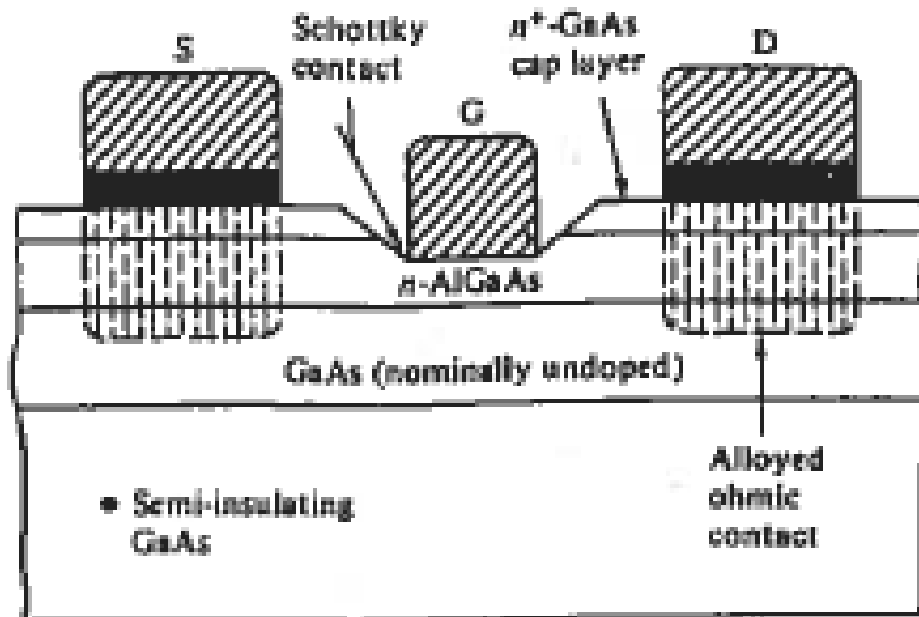
Molecular Beam Epitaxy (MBE)

Heterostructure

MODFET/HEMT

MOdulation Doped FET (MODFET)

High Electron Mobility Transistors (HEMT)



AlGaAs layer is deposited on top of *GaAs*

Probe station: Electrical characteristics

Wafer is put on the vacuum chuck

Vacuum chuck can be moved and rotated

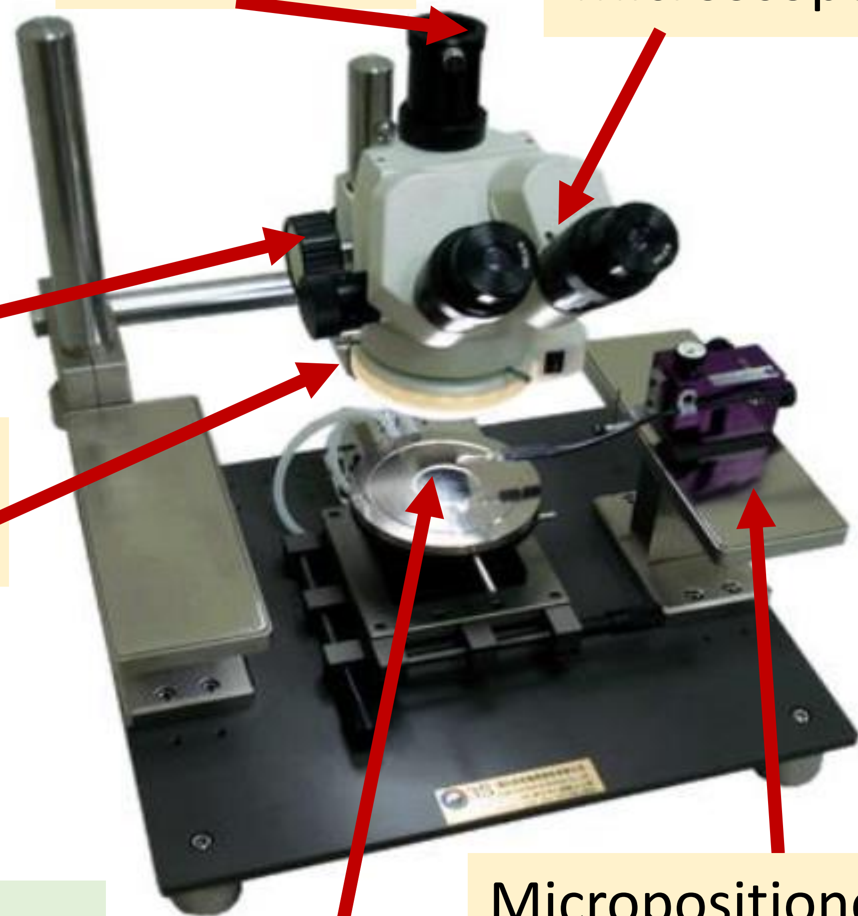
Microscope to view the sample on chuck

Micropositioner to contact the sample with probe

Power supply to be connected to micropositioner

Source & Measure

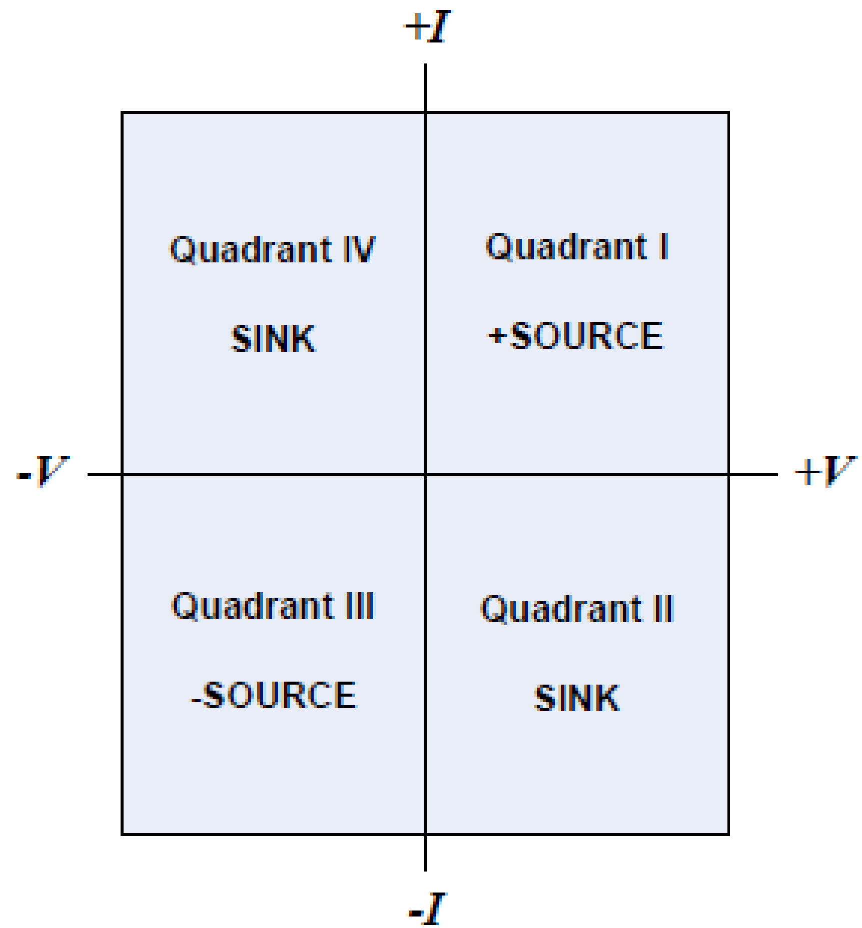
SourceMeter



SourceMeter

Source-Measure Unit (SMU)

SMUs can operate in **four** quadrants
- ➢ Quadrants **I** and **III** are sourcing
  - ✓ I and V have same polarity
  - ✓ Deliver power to load
- ➢ Quadrants **II** and **IV** are sinking
  - ✓ I and V have different polarity
  - ✓ Dissipate power



Input-Output characteristics

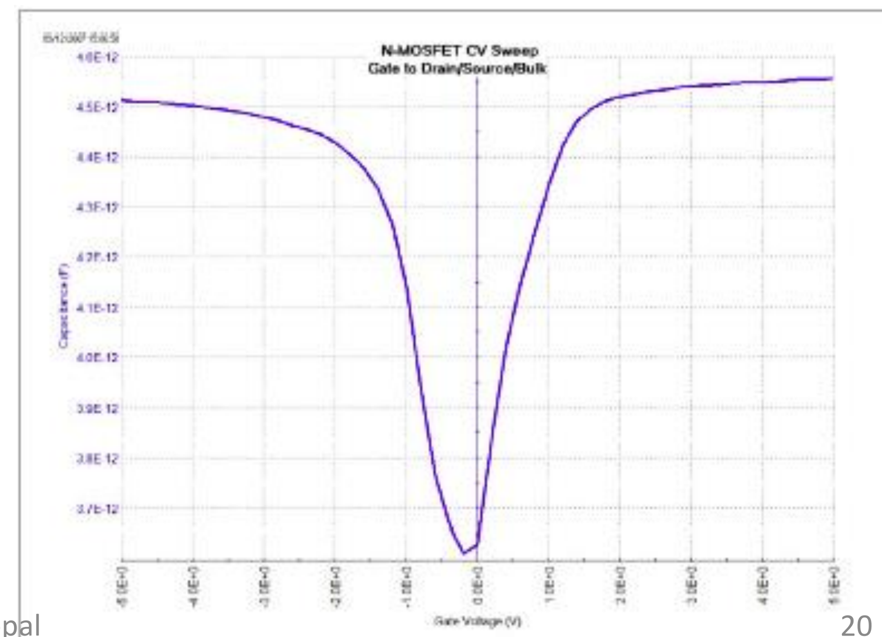
Automatically sweeps input and measure output

Keithley 2450

SourceMeter

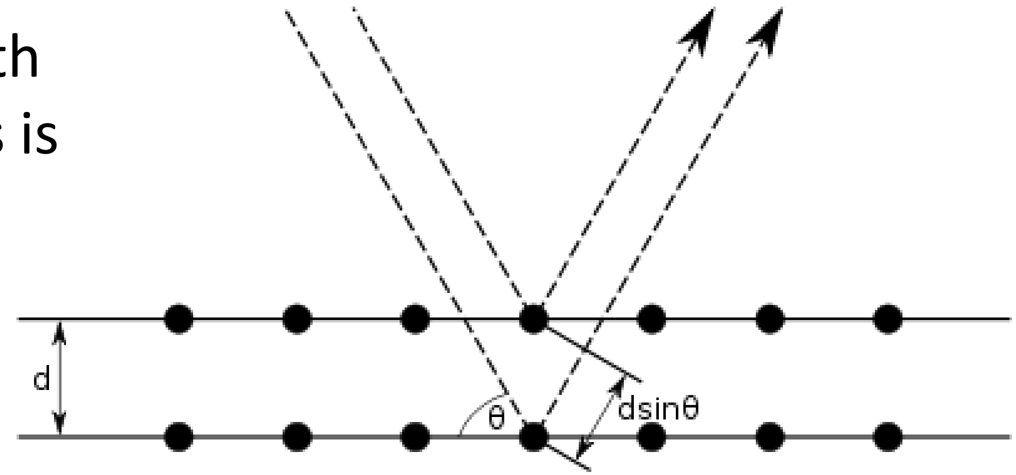
4200A-SCS
Parameter Analyzer

C-V
measurement



X-Ray Diffraction (XRD)

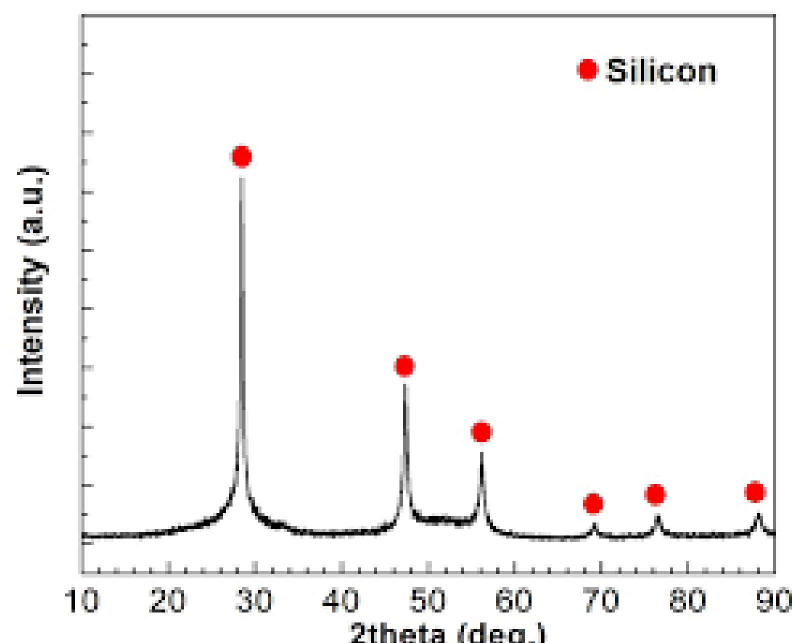
Bragg diffraction: A wavelength comparable to atomic spacings is scattered in by the atoms of a crystalline system



Constructive interference

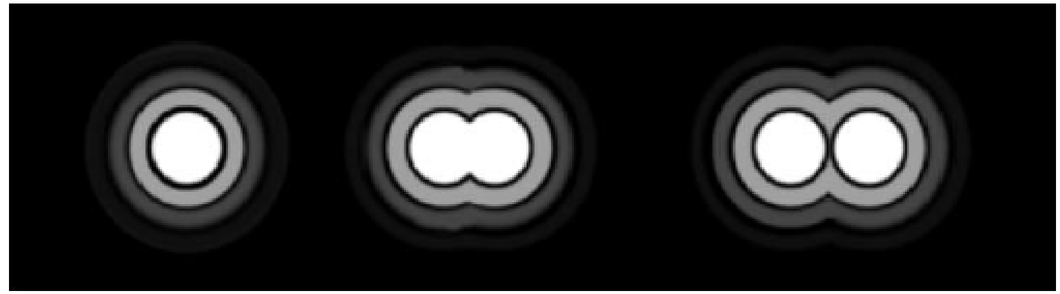
$$2dsin\theta = n\lambda$$

From the location of the peaks, with a known database of materials, we can characterize the deposited materials



Optical and Electron Microscopes

Optical microscope



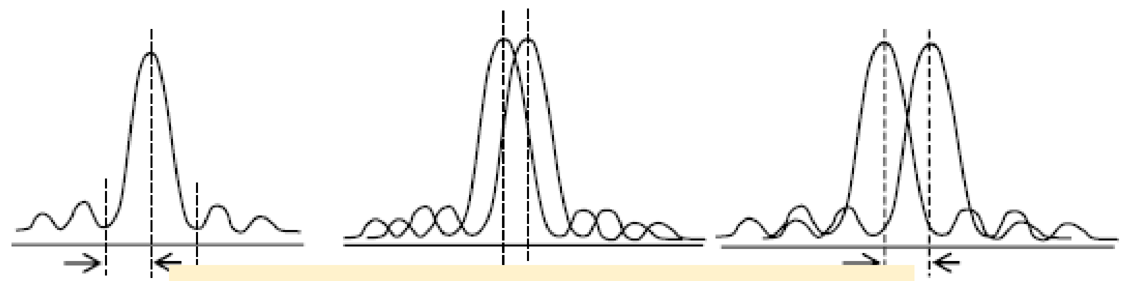


Illustration of resolution

Electron microscopes were proposed due to the **limited image resolution** of optical microscopes

Louis de Broglie (1925): Electron as wave

Scanning Electron Microscope (SEM)

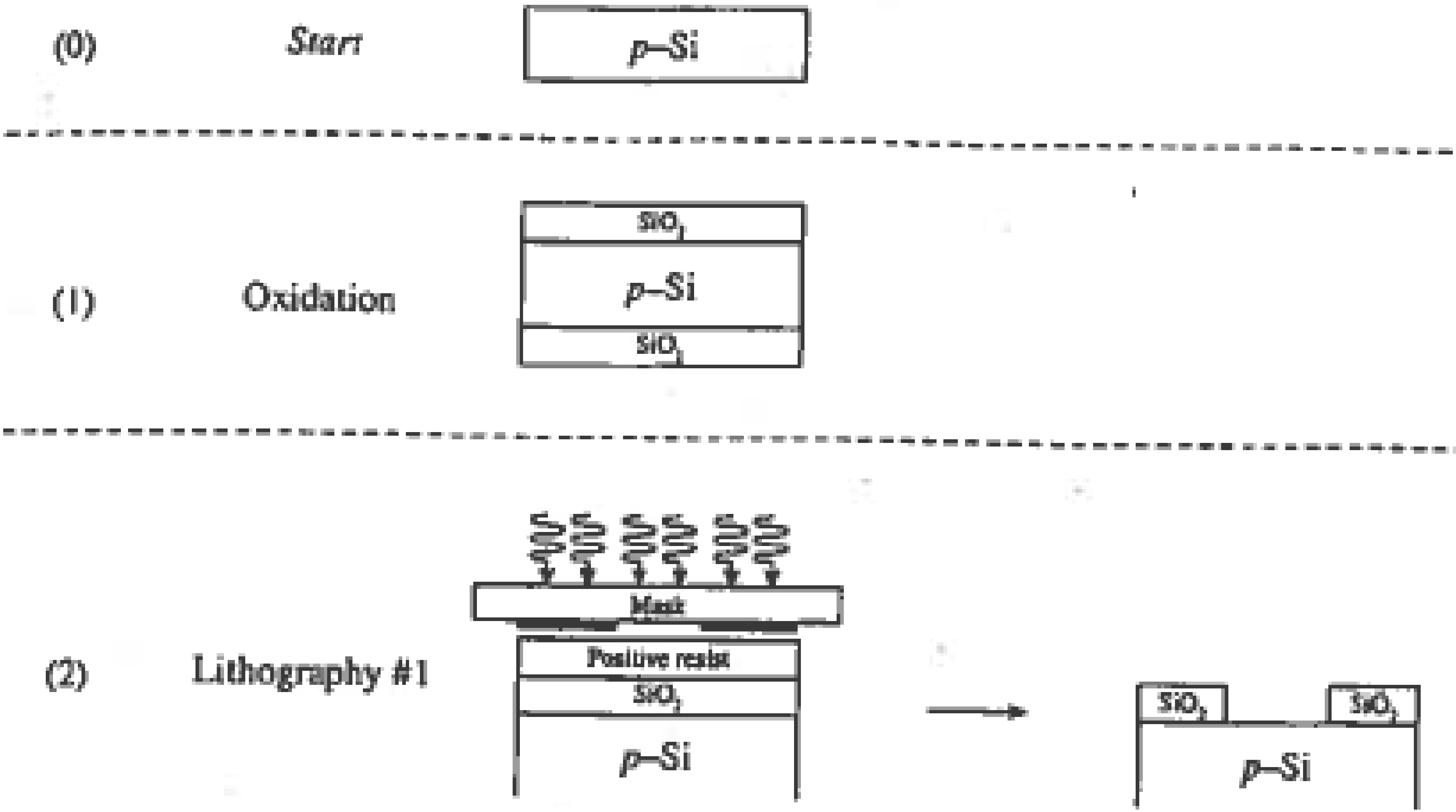
- ✓ Electron beam reflects from the sample

Transmission Electron Microscope (TEM)

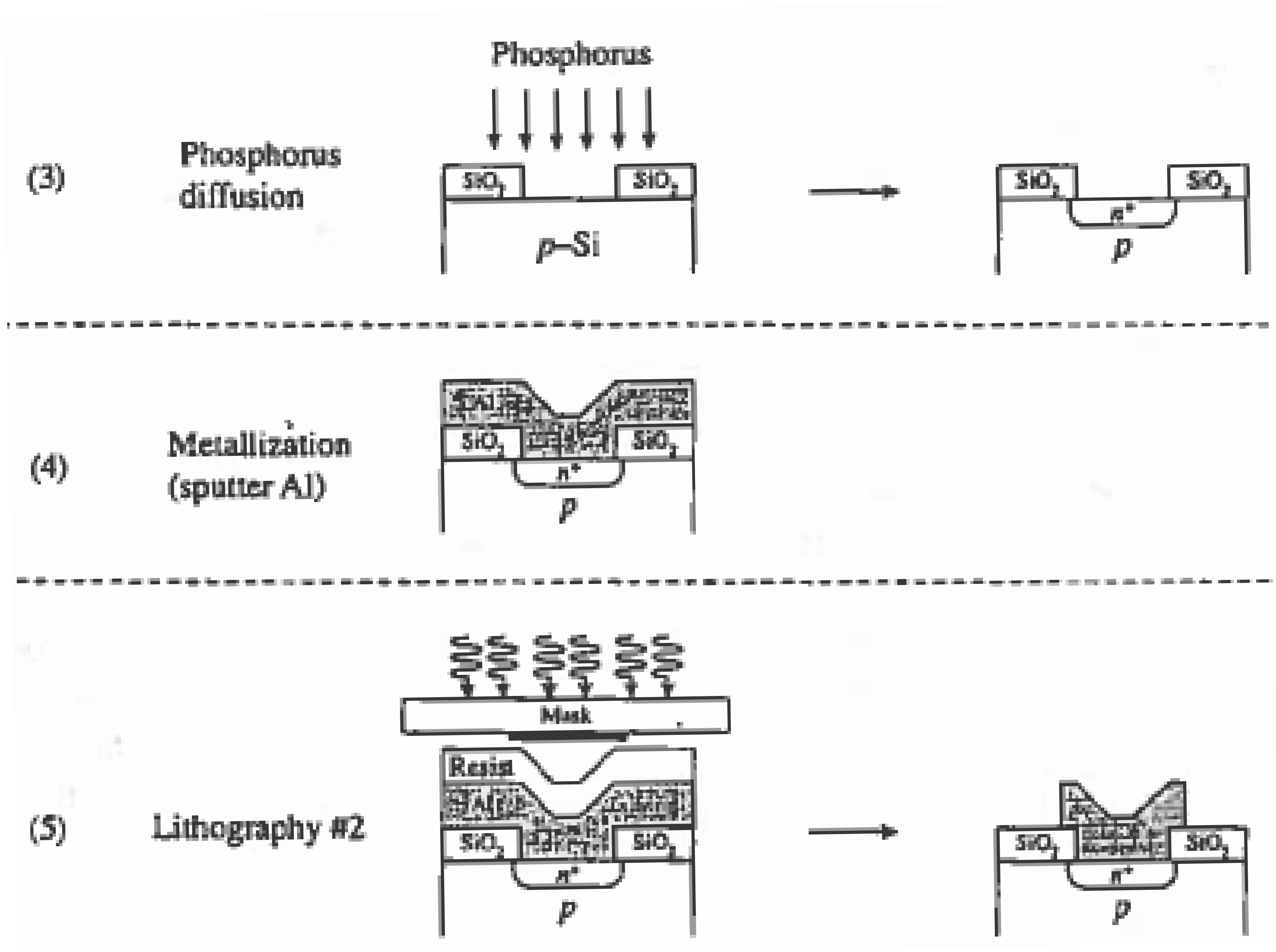
- ✓ The sample has to be thin

Material characterization is also possible

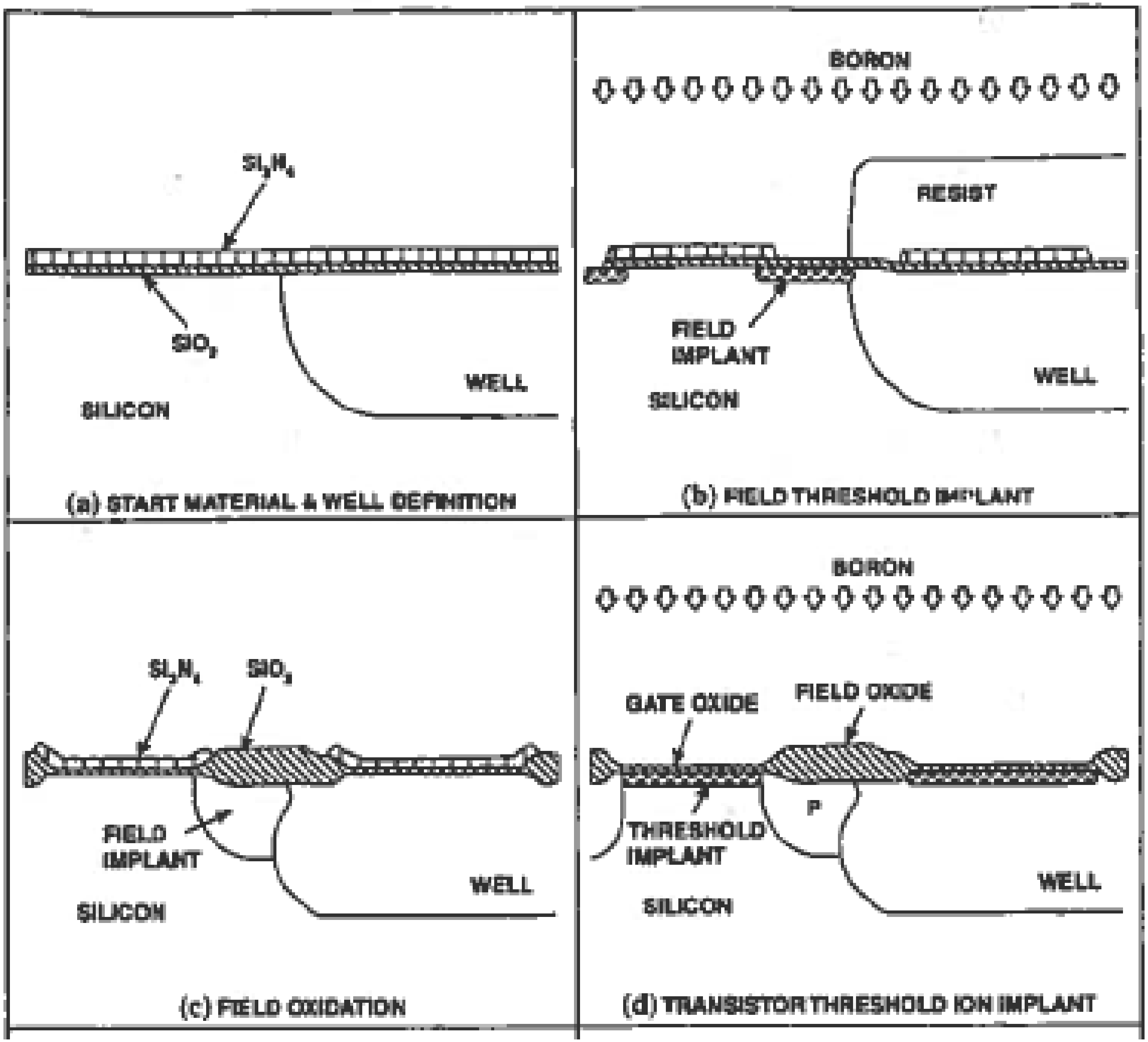
PN junction fabrication



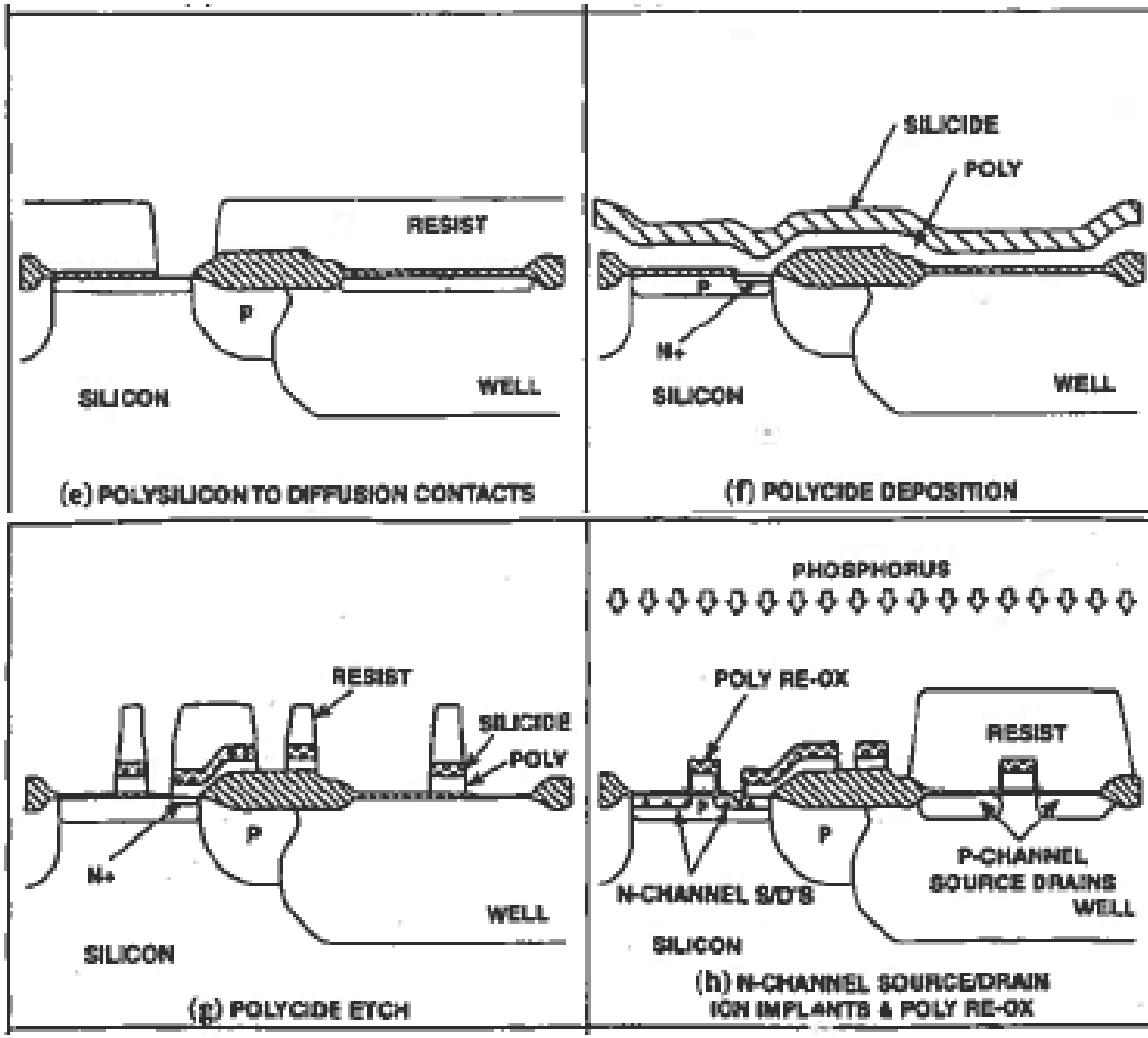
PN junction fabrication



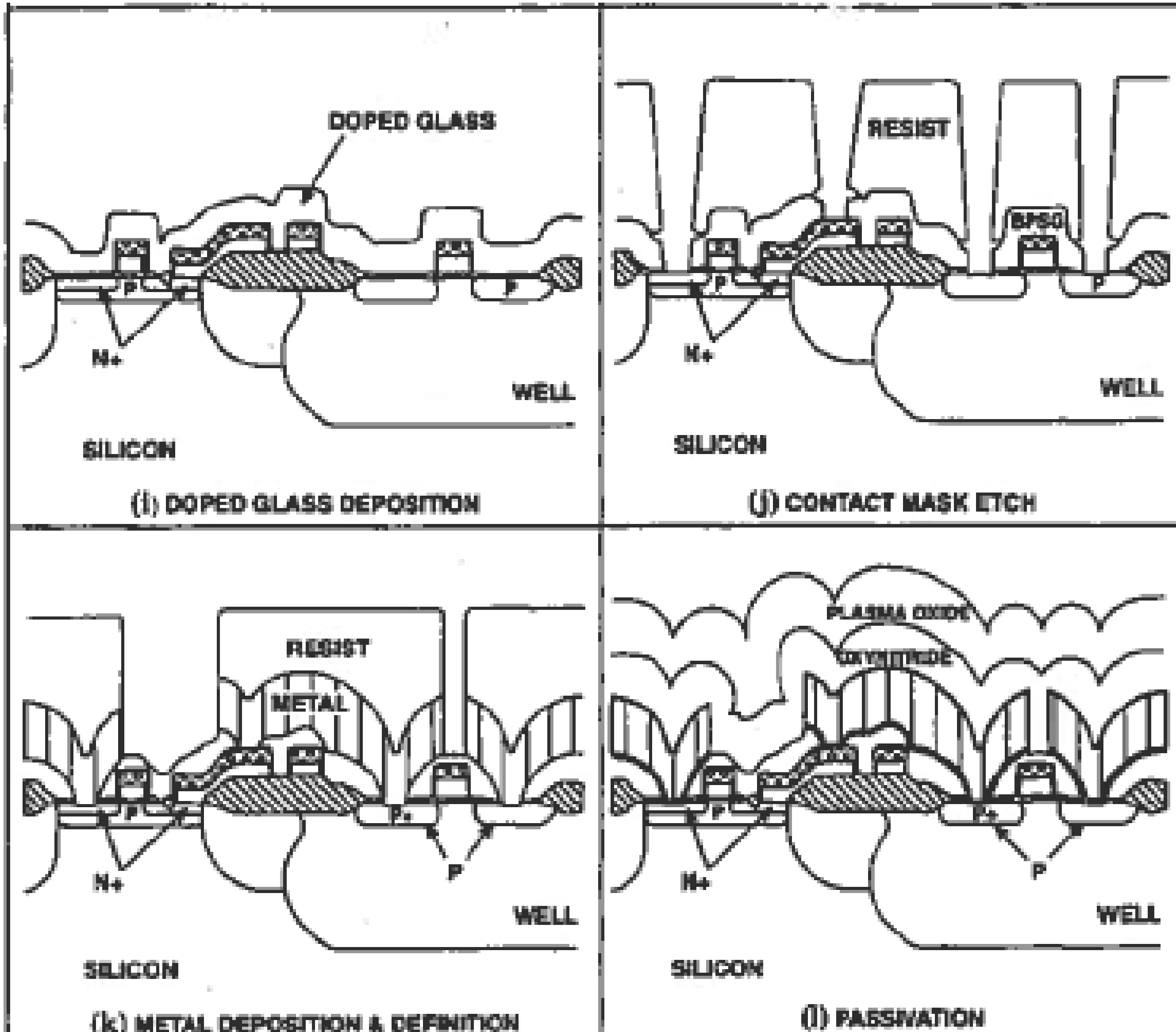
MOSFET fabrication



MOSFET fabrication



MOSFET fabrication



Isolation and Bonding

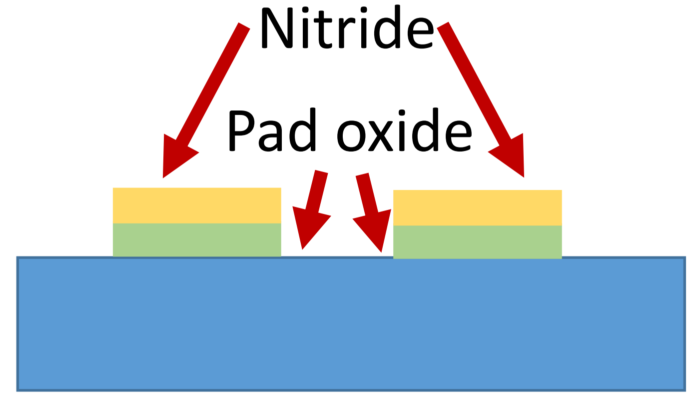
Isolation of neighboring MOS transistors

- Local Oxidation of Silicon

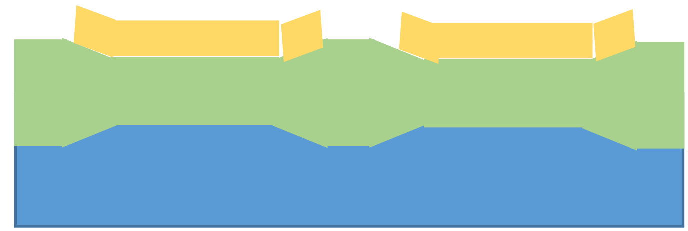
Pad oxide: A very thin silicon oxide layer is grown on the wafer

Silicon nitride is deposited which is used as an oxide barrier

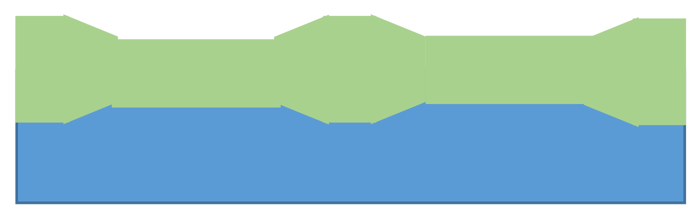
After lithography the pattern is etched into the nitride



Thermal oxidation



Nitride removal



Bonding: An intermediate layer adhesive to connect substrates of different types of materials

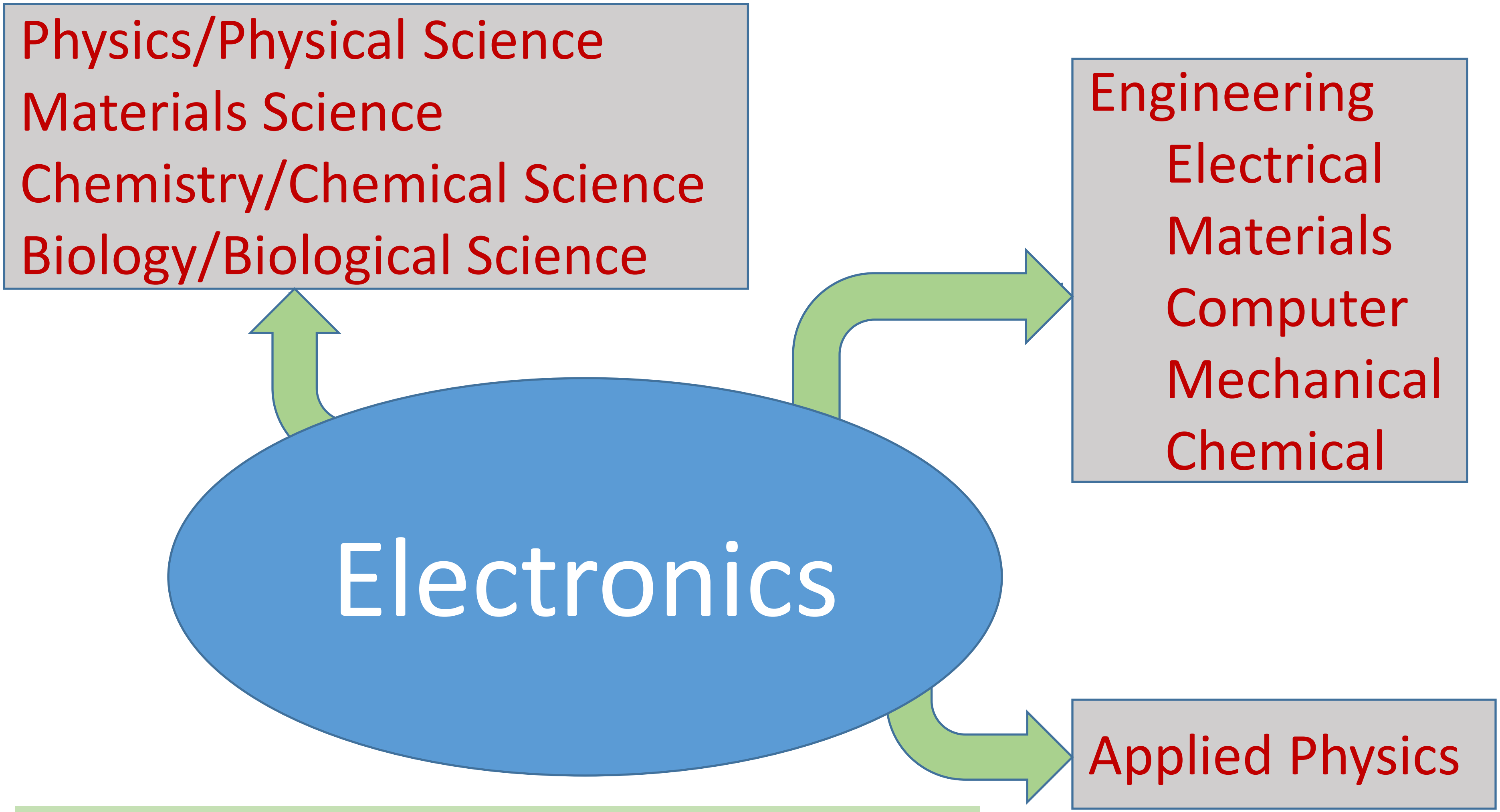
Organic or Inorganic

Theory and Experiment

Theory, Simulation

Experiment

Electronics: Interdisciplinary



Nanosciene and Nanotechnology

GLOBALFOUNDRIES: Sand to Silicon

https://www.youtube.com/watch?v=jTyGFM1M3zs

Intel: The Making of a Microchip

https://www.youtube.com/watch?v=_VMYPLXnd7E

Intel: The Making of a Chip with 22nm/3D Transistors

https://www.youtube.com/watch?v=d9SWNLZvA8g