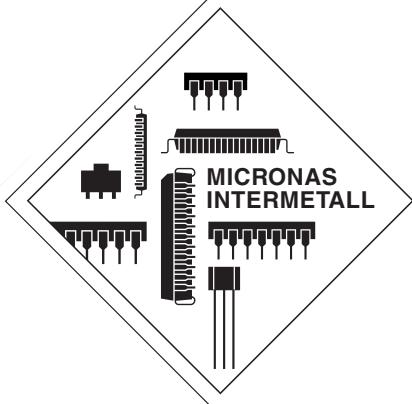


ADVANCE INFORMATION



## DAC 3550A Stereo Audio DAC

Edition Aug. 14, 1998  
6251-467-1AI



**MICRONAS**  
**INTERMETALL**

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## Stereo Audio DAC

### 1. Introduction

The DAC 3550A is single-chip, high-precision, dual digital-to-analog converter designed for audio applications. The employed conversion technique is based on oversampling with noise-shaping.

With INTERMETALL's unique multibit sigma-delta technique, less sensitivity to clock jitter, high linearity, and a superior S/N ratio has been achieved. The DAC 3550A is controlled via I<sup>2</sup>C bus.

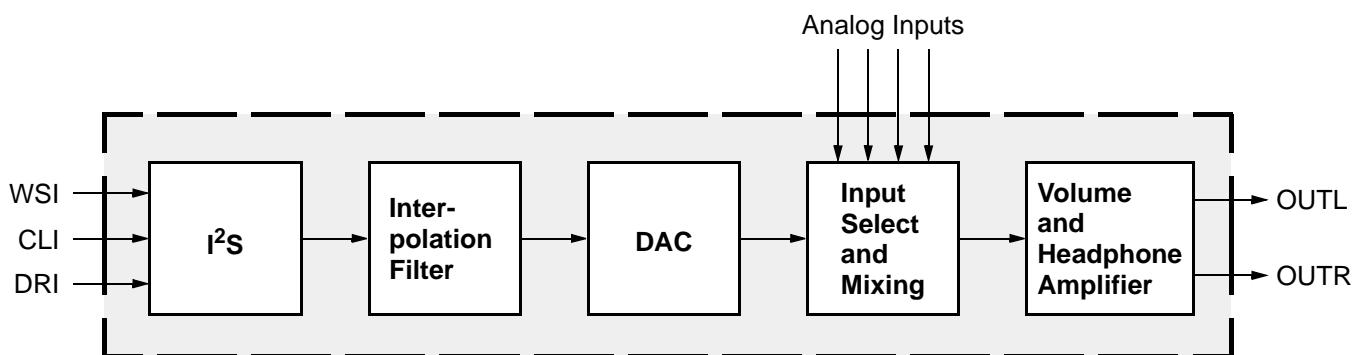
Digital audio input data is received by a versatile I<sup>2</sup>S interface. The analog back-end consists of internal analog filters and op amps for cost-effective additional external sound processing. The DAC 3550A provides line-out, headphone/speaker amplifiers, and volume control. Moreover, mixing additional analog audio sources to the D/A-converted signal is supported.

The DAC 3550A is designed for all kinds of applications in the audio and multimedia field, such as: MPEG players, CD players, DVD players, CD-ROM players, etc.

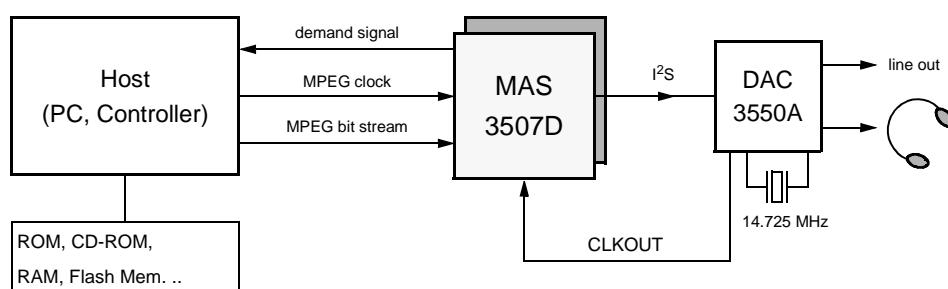
The DAC 3550A ideally complements the MPEG 1/2 layer 2/3 audio decoder MAS 3507D.

### 1.1. Main Features

- no master main input clock required
- integrated stereo headphone amplifier and mono speaker amplifier
- SNR of 100 dB
- 18-bit stereo D/A converter
- I<sup>2</sup>C-bus, I<sup>2</sup>S-bus
- internal clock oscillator
- full-feature mode by I<sup>2</sup>C control (three selectable subaddresses)
- reduced feature mode for non-I<sup>2</sup>C applications
- continuous sample rates from 8 kHz to 50 kHz
- analog deemphasis for 44.1 kHz
- analog volume and balance: +18...-75 dB and mute
- oversample and multibit noise shaping technique
- THD better than 0.01 %
- two additional analog stereo inputs (AUX) with source selection and mixing
- supply range: 2.7 V...5.25 V
- low-power mode
- additional line-out
- on-chip op amps for cost-effective external analog sound processing



**Fig. 1-1:** Block diagram of the DAC 3550A



**Fig. 1-2:** Typical application: MPEG Layer 3 Player

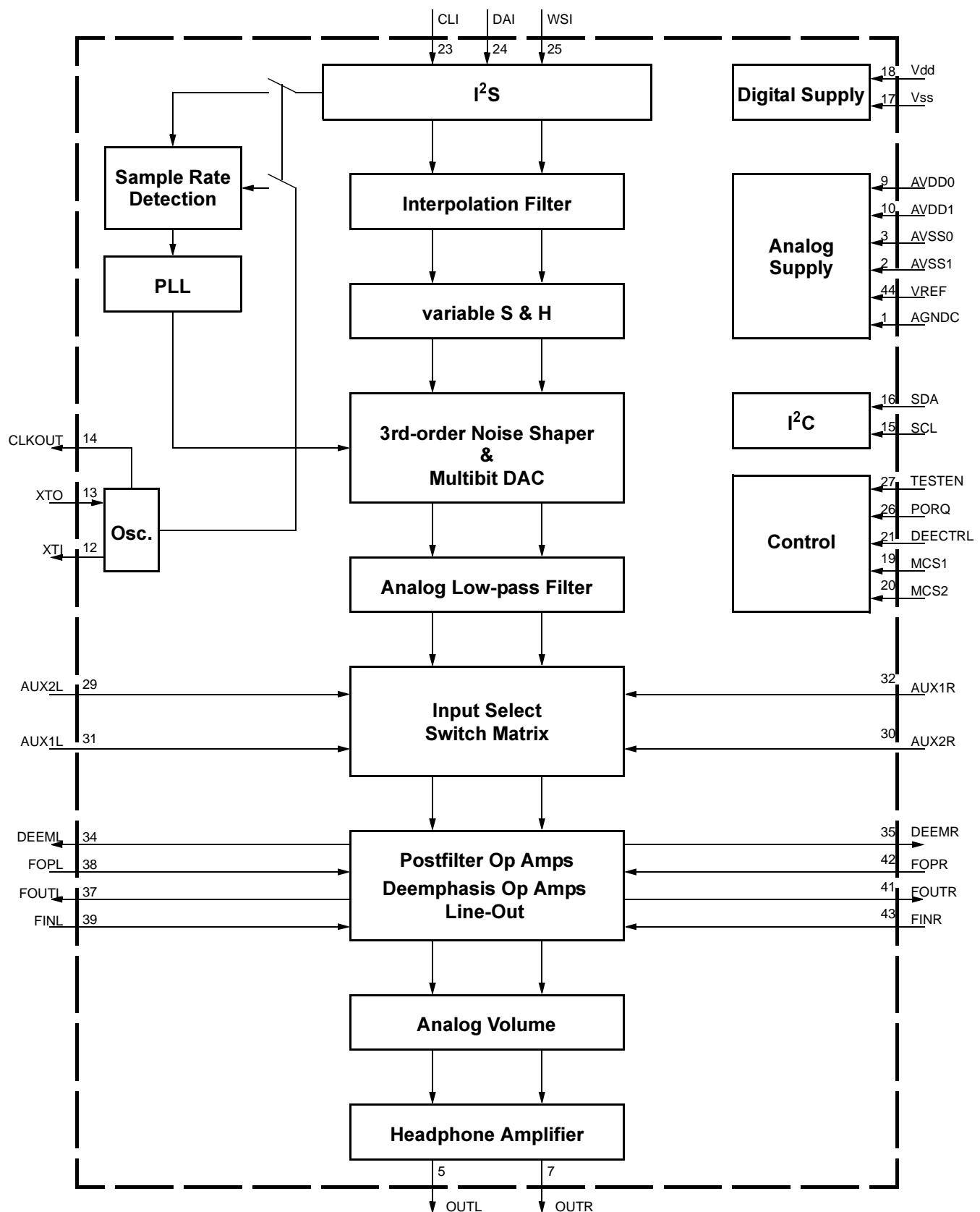


Fig. 1–3: Block diagram of the DAC 3550A

## 2. Functional Description

### 2.1. I<sup>2</sup>S Interface

The I<sup>2</sup>S interface is the digital audio interface between the DAC 3550A and external digital audio sources such as CD/DAT players, MPEG decoders etc. It covers most of the I<sup>2</sup>S-compatible formats.

All modes have in common that the MSB is right justified to an I<sup>2</sup>S frame identification (WSI) transition and that data is valid on the rising edge of the bit clock CLI.

#### 16-bit mode

In this case the bit clock is  $32 \times f_{\text{audio}}$ . Maximum word length is 16 bit.

#### 32-bit mode

In this case the bit clock is  $64 \times f_{\text{audio}}$ . Maximum word length is 32 bit, but maximum 18 MSBs are processed.

#### Automatic Detection

No I<sup>2</sup>C control is required to switch between 16- and 32-bit mode. It is recommended to switch the DAC 3550A in mute position during changing between 16- and 32-bit mode.

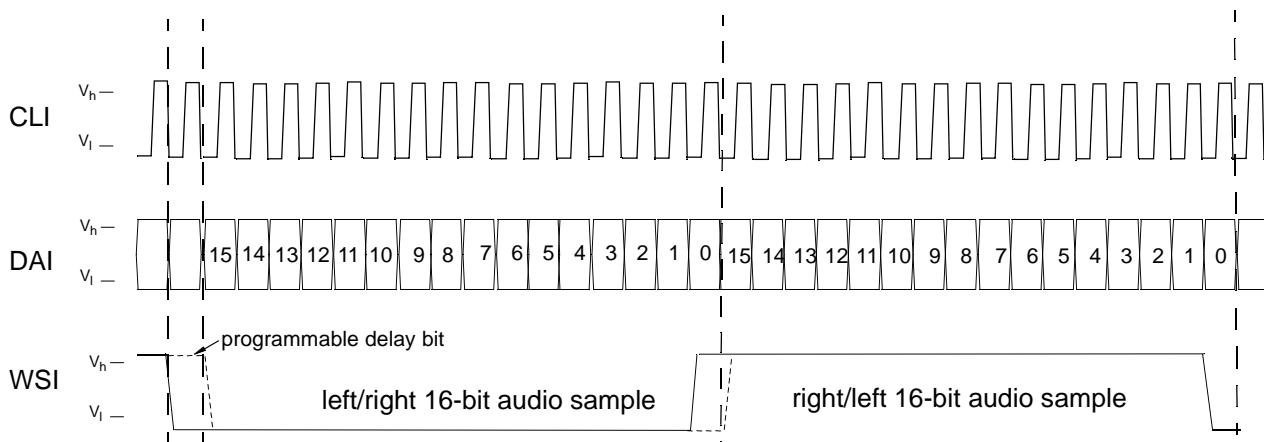
For high-quality audio, it is recommended to use the 32-bit mode of the I<sup>2</sup>S interface to make use of the full dynamic range (if more than 16 bits are available).

#### Left-Right Selection

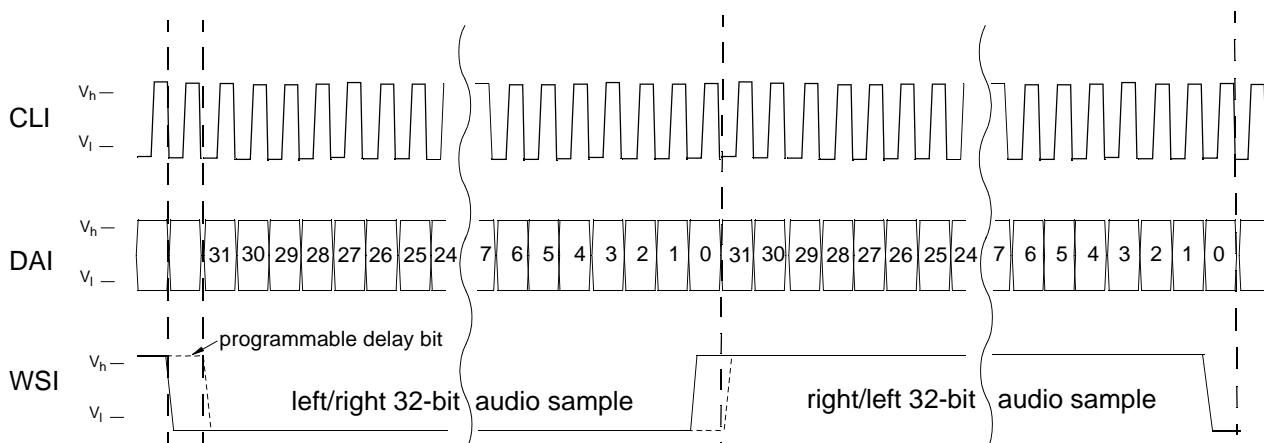
Standard I<sup>2</sup>S format defines an audio frame always starting with left channel and low-state of WSI. However, I<sup>2</sup>C control allows changing the polarity of WSI.

#### Delay Bit

Standard I<sup>2</sup>S format requires a delay of one clock cycle between transitions of WSI and data MSB. In order to fit other formats, however, this characteristic can be switched off and on by I<sup>2</sup>C control.



**Fig. 2-1:** I<sup>2</sup>S 16-bit mode

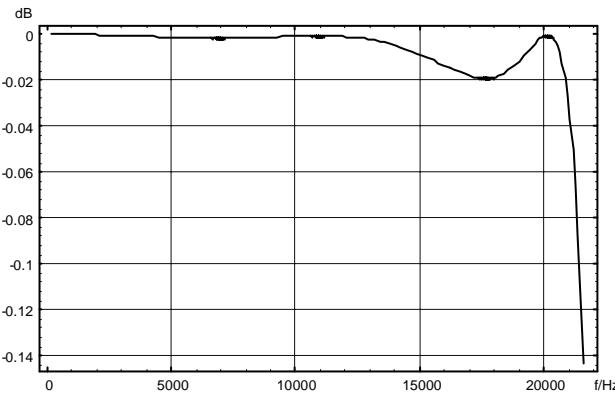


**Fig. 2-2:** I<sup>2</sup>S 32-bit mode

Note: Volume mute should be applied before changing I<sup>2</sup>S mode in order to avoid audible clicks.

## 2.2. Interpolation Filter

The interpolation filter increases the sampling rate by a factor of 8. The characteristic for  $f_{s_{\text{audio}}} = 48 \text{ kHz}$  is shown below.



**Fig. 2-3:** 1→8 Interpolation Filter; Frequency Range 0...22 kHz

## 2.3. Variable Sample & Hold

The advantage of this system is that even at low sample frequencies the out-of-band noise is not scaled down to audible frequencies.

## 2.4. 3rd-order Noise Shaper and Multibit DAC

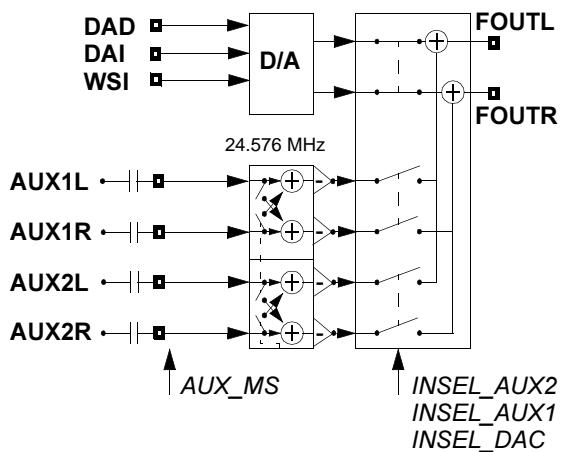
The 3rd-order noise shaper converts the oversampled audio signal into a 5-bit noise-shaping signal at a high sampling rate. This technique results in extremely low quantization noise in the audio band.

## 2.5. Analog Low-pass

The analog low-pass is a first order filter with a cut-off frequency of approximately 1.4 MHz and removes the high frequency components of the noise-shaping signal.

## 2.6. Input Select and Mixing Matrix

This block is used to switch between or mix the auxiliary inputs and the signals coming from the DAC. A switch matrix allows to select between mono and stereo mode as shown in Fig. 2-4.

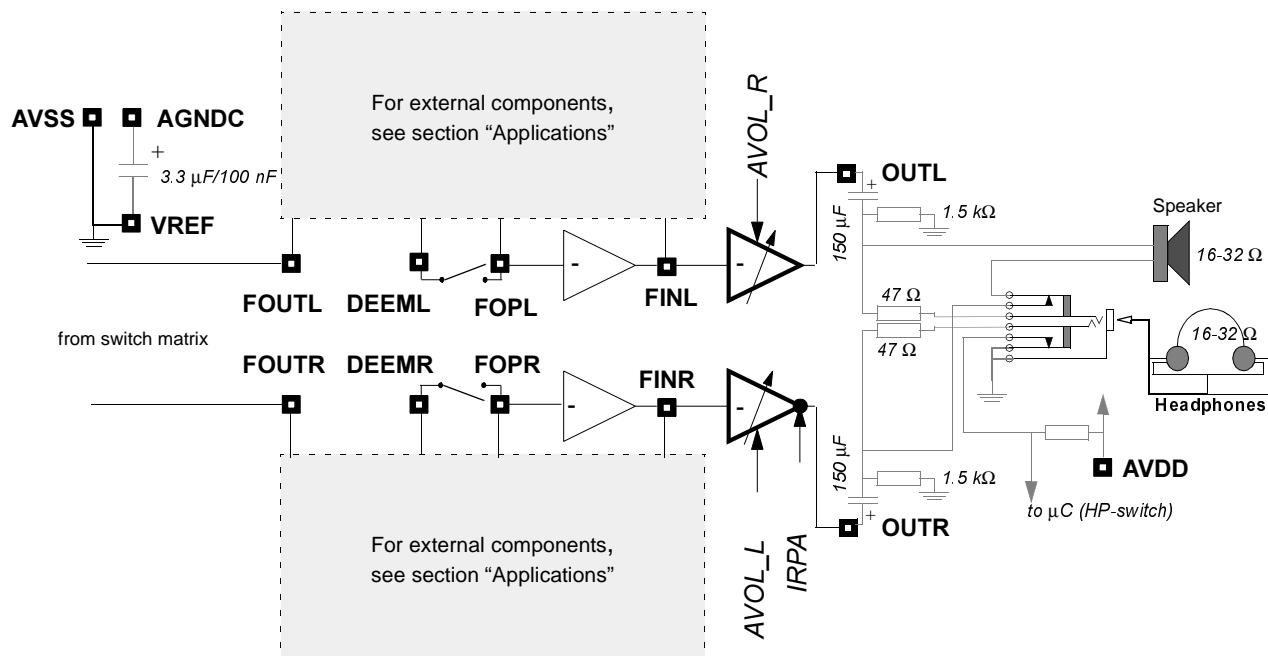


**Fig. 2-4:** Switch Matrix

Mono mode is realized by adding left and right channel.

## 2.7. Postfilter Op Amps, Deemphasis Op Amps, and Line-Out

This block contains the active components for the analog postfilters and the deemphasis network. The op amps and all I/O-pins for this block are shown in Fig. 2-5.

**Fig. 2–5:** Postfilter Op Amps, Deemphasis Op Amps, and Line-Out

## 2.8. Analog Volume

The analog volume control covers a range from +18 dB and –75 dB. The lowest step is the mute position.

Step size is split into a 3-dB and a 1.5-dB range.

–75 dB...–54 dB : 3 dB step size  
–54 dB...+18 dB : 1.5 dB step size

## 2.9. Headphone Amplifier

The headphone amplifier output is provided at the OUTL and OUTR pins connected either to stereo headphones or a mono loudspeaker. The stereo headphones require external  $47\ \Omega$  serial resistors in both channels. If a loudspeaker is connected to these outputs, the power amplifier for the right channel must be switched to inverse polarity. In order to optimize the available power, the source of the two output amplifiers should be identical, i.e. a monaural signal.

Please note, that if a speaker is connected it should strictly be connected as shown in Fig. 2–5. Never use a separate connector for the speaker, because electrostatic discharge could damage the output transistors.

**Table 2–1:** Volume Control

Volume/dB	AVOL_R
18.0	111000
16.5	110111
15.0	110110
13.5	110101
–	–
0.0	101100 (default)
–1.5	101011
–	–
–54.0	001000
–57.0	000111
–	–
–75	000001
Mute	000000

## 2.10. Clock System

The advantage of the DAC 3550A clock system is that no external master clock is needed. Most DACs need  $256 \times f_{\text{audio}}$ ,  $384 \times f_{\text{audio}}$ , or at least an asynchronous clock.

All internal clocks are generated by a PLL circuit, which locks to the I<sup>2</sup>S bit clock (CLI). If no I<sup>2</sup>S clock is present, the PLL is running free and it is guaranteed that there is always a clock to keep the IC controllable by I<sup>2</sup>C.

The device can be set to two different modes:

- Standard mode
- MPEG mode

In the standard mode, I<sup>2</sup>C subaddressing is possible (ADR0, ADR1, ADR2).

MPEG mode always uses ADR0.

To select the modes, the MCS1/MCS2 pins have to be set according to Table 2–2.

**Table 2–2:** Operation Modes

MCS1	MCS2	Mode	Sub-address	Default Sample Rate
0	0	Standard	ADR0	32–48 kHz
0	1	Standard	ADR1	32–48 kHz
1	0	Standard	ADR2	32–48 kHz
1	1	MPEG	ADR0	Automatic

### Standard Mode

- without I<sup>2</sup>C

In standard mode, sample rates from 48 kHz to 32 kHz are handled without I<sup>2</sup>C control automatically. The setting for this range is the default setting. Sample rates below 32 kHz require an I<sup>2</sup>C control to set the PLL divider. This ensures that even at low sample rates the DAC 3550A is running at a high clock rate. This avoids audible effects due to the noise-shaping technique of the DAC 3550A. Sample rate range is continuous from 8 to 50 kHz. The I<sup>2</sup>C setting of low sample rates must follow table Table 2–2.

- with I<sup>2</sup>C

An additional mode allows automatic sample rate detection. In this case, the clock oscillator is required and must run at frequencies between 13.3 MHz to 17 MHz. This mode, however, does not support continuous sample rates. Only the following sample rates are allowed:

8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz,  
24 kHz, 32 kHz, 44.1 kHz, 48 kHz

The sample rate detection allows a tolerance of  $\pm 200$  ppm at WSI.

If the oscillator is not used for automatic sample rate detection, it can be used as general-purpose clock for the application. The frequency range in this case is 10 MHz to 20 MHz

### MPEG Mode

This mode should be used in conjunction with MAS 3507D in MPEG player applications. In this case a 14.725 MHz signal is needed to provide a clock for the MAS 3507D and to allow an automatic sample rate detection in the DAC 3550A. All MPEG sample rates from 8 to 48 kHz can be detected. The internal processing and the DAC itself are automatically adjusted to keep constant performance all over this range. I<sup>2</sup>C control for sample rate adjustment is not needed in this case.

The MPEG sample rates:

8 kHz, 11.025 kHz, 12 kHz, 16 kHz, 22.05 kHz,  
24 kHz, 32 kHz, 44.1 kHz, 48 kHz

As in standard mode, the sample rate detection allows a tolerance of  $\pm 200$  ppm at WSI.

Subaddressing is not possible in MPEG mode; this means, in multi-DAC systems, only one DAC 3550A can run in MPEG mode.

### 2.11. I<sup>2</sup>C Bus Interface

The DAC 3550A is equipped with an I<sup>2</sup>C bus slave interface. The I<sup>2</sup>C bus interface uses one level of sub-addressing: The I<sup>2</sup>C bus address is used to address the IC. The subaddress allows chip select in multi DAC applications and selects one of the three internal registers. The registers are write-only. The I<sup>2</sup>C bus chip address is given below.

dev\_write = \$9A.

The registers of the DAC 3550A have 8- or 16-bit data size; 16-bit registers are accessed by writing two 8-bit data words.

A6	A5	A4	A3	A2	A1	A0	R/W
1	0	0	1	1	0	1	0

S	dev_write	Ack	sub_adr	Ack	1 byte data	Ack	P	8-bit I <sup>2</sup> C write access		
S	dev_write	Ack	sub_adr	Ack	1 byte data	Ack	1 byte data	Ack	P	16-bit I <sup>2</sup> C write access

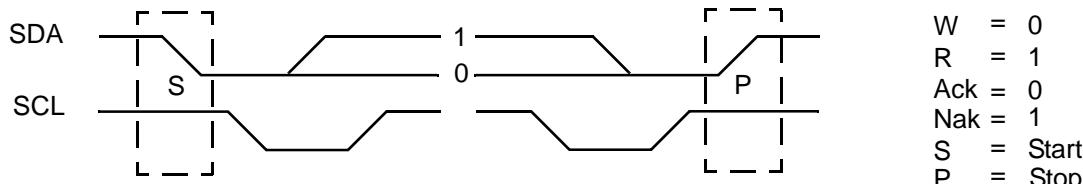


Fig. 2-6: I<sup>2</sup>C bus protocols for write operations

### 2.12. Registers

In Section 3.4. “Control Registers” on page 14, a definition of the DAC 3550A control registers is shown. A hardware reset initializes all control registers to 0. The automatic chip initialization loads a selected set of registers with the default values given in the table.

All registers are write-only.

The register address is coded by 3 bits (RA1, RA0) according to Table 2-3.

Table 2-3: I<sup>2</sup>C Register Address

RA1	RA0	Mnemonics
0	1	SR_REG
1	0	AVOL
1	1	GCFG

The mnemonics used in the INTERMETALL DAC 3550A demo software are given in the last column.

### Chip Select

Chip select allows to connect up to three DAC 3550A to an I<sup>2</sup>C control bus. The chip subaddresses are defined by the MCS1/MCS2 (Mode & Chip Select) pins. Only in standard mode, chip select is possible. MPEG mode always uses chip subaddress 0.

Register address and chip select are mapped into the subaddress field in Table 2-4.

### 2.13. Reduced Feature Mode

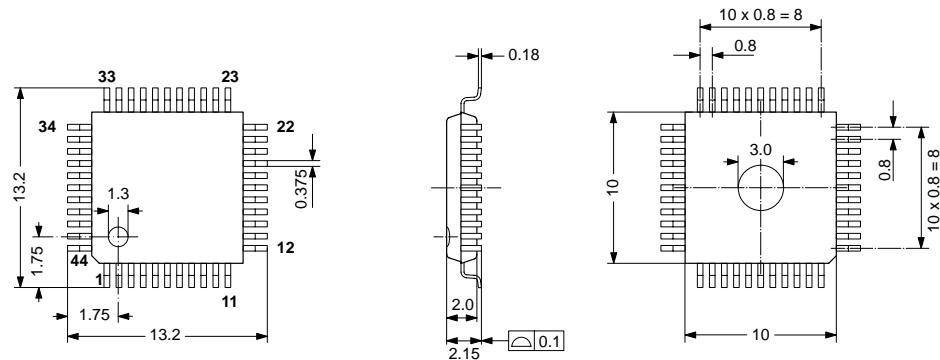
If I<sup>2</sup>C control is not used, the IC is in the default mode (see Section 3.4. “Control Registers” on page 14) after start-up. Default Volume setting is 0 dB and digital audio input is set to standard I<sup>2</sup>S. Sample rates from 32 kHz to 48 kHz are supported in this mode. Applications with no need for volume control or analog input could use this mode.

Table 2-4: I<sup>2</sup>C Subaddress

7	6	5	4	3	2	1	0
MCS2	MCS1					RA1	RA0

### 3. Specifications

#### 3.1. Outline Dimensions



SPGS0006-1/1E

**Fig. 3–1:**  
44-Pin Plastic Quad Flat Package  
**(PQFP44)**

Weight approximately 0.4 g  
Dimensions in mm

#### 3.2. Pin Connections and Short Descriptions

NC = not connected, leave vacant  
 LV = if not used, leave vacant  
 VSS = if not used, connect to VSS  
 X = obligatory; connect as described in application diagram  
 VDD = connect to VDD

Pin No.	Pin Name	Type	Connection (if not used)	Short Description
<b>POWER SUPPLY</b>				
1	AGNDC	BID	X	Analog reference Voltage
2	AVSS1	IN	X	VSS 1 for audio back-end
3	AVSS0	IN	X	VSS 0 for audio output amplifiers
4	NC		LV	Not connected
5	OUTL	OUT	LV	Audio Output: Headphone left or Speaker +
6	NC		LV	Not connected
7	OUTR	OUT	LV	Audio Output: Headphone right or Speaker –
8	NC		LV	Not connected
9	AVDD0	IN	X	VDD 0 for audio output amplifiers
10	AVDD1	IN	X	VDD 1 for audio back-end
11	NC		LV	Not connected
12	XTI	IN	X	Quartz oscillator pin 1
13	XTO	BID	X	Quartz oscillator pin 2

Pin No.	Pin Name	Type	Connection (if not used)	Short Description
14	CLKOUT	OUT	LV	Clock Output
15	SCL	BID	LV	I <sup>2</sup> C clock
16	SDA	BID	LV	I <sup>2</sup> C data
17	VSS	IN	X	Digital VSS
18	VDD	IN	X	Digital VDD
19	MCS1	IN	X	I <sup>2</sup> C Chip Select 1
20	MCS2	IN	X	I <sup>2</sup> C Chip Select 2
21	DEECTRL	IN	VSS	Deemphasis on/off Control
22	NC		LV	Not connected
23	CLI		VSS	I <sup>2</sup> S Bit Clock
24	DAI	IN	VSS	I <sup>2</sup> S Data
25	WSI	IN	VSS	I <sup>2</sup> S Frame Identification
26	PORQ	IN	VDD	Power-On Reset, active-low
27	TESTEN	IN	X	Test Enable
28	NC		LV	Not connected
29	AUX2L	IN	LV	AUX2 left input for external analog signals (e.g. tape)
30	AUX2R	IN	LV	AUX2 right input for external analog signals (e.g. tape)
31	AUX1L	IN	LV	AUX1 left input for external analog signals (e.g. FM)
32	AUX1R	IN	LV	AUX1 right input for external analog signals (e.g. FM)
33	NC		LV	Not connected
34	DEEML	OUT	LV	Deemphasis Network Left
35	DEEMR	OUT	LV	Deemphasis Network Right
36	NC		LV	Not connected
37	FOUTL	OUT	X	Output to left external filter
38	FOPL	BID	X	Filter op amp inverting input, left
39	FINL	IN/OUT	X	Input for FOUTL or filter op amp output (line out)
40	NC		LV	Not connected
41	FOUTR	OUT	X	Output to right external filter
42	FOPR	BID	X	Right Filter op amp inverting input

Pin No.	Pin Name	Type	Connection (if not used)	Short Description
43	FINR	IN/OUT	X	Input for FOUTR or Filter opamp output (line out)
44	VREF	IN	X	Analog reference Ground

### 3.3. Pin Descriptions

#### 3.3.1. Power Supply Pins

The DAC 3550A combines various analog and digital functions which may be used in different modes. For optimized performance, major parts have their own power supply pins. All VSS power supply pins must be connected.

##### **VDD (18)**

##### **VSS (17)**

The VDD and VSS power supply pair are connected internally with all digital parts of the DAC 3550A.

##### **AVDD0 (9)**

##### **AVSS0 (3)**

AVDD0 and AVSS0 are separate power supply pins that are exclusively used for the on-chip headphone/loudspeaker amplifiers.

##### **AVDD1 (10)**

##### **AVSS1 (2)**

The AVDD1 and AVSS1 pins supply the analog audio processing parts, except the headphone/loudspeaker amplifiers.

#### 3.3.2. Analog Audio Pins

##### **AGNDC (1)**

Reference for analog audio signals. This pin is used as reference for the internal op amps. This pin must be blocked against VREF with a 3.3 µF capacitor.

Note: The pin has a typical DC-level of 1.5/2.25 V. It can be used as reference input for external op amps when no current load is applied.

##### **VREF (44)**

Reference ground for the internal band-gap and biasing circuits. This pin should be connected to a clean ground potential. Any external distortions on this pin will affect the analog performance of the DAC 3550A.

##### **AUX1L (31)**

##### **AUX1R (32)**

##### **AUX2L (29)**

##### **AUX2R (30)**

The AUX pins provide two analog stereo inputs. Auxiliary input signals, e.g. the output of a conventional receiver circuit or the output of a tape recorder can be connected with these inputs. The input signals have to be connected by capacitive coupling.

##### **FOUTL (37)**

##### **FOPL (38)**

##### **FINL (39)**

##### **FOUTR (41)**

##### **FOPR (42)**

##### **FINR (43)**

Filter op amps are provided in the analog baseband signal paths. These inverting op amps are freely accessible for external use by these pins.

The FOUTL/R pins are connected with the buffered output of the internal switch matrix. The FOPL/R-pins are directly connected with the inputs of the inverting filter op amps. The FINL/R pins are connected with the outputs of the op amps. The driving capability of the FOUTL/R pins is not sufficient for standard line output signals. Only the FINL/R pins are suitable for line output.

##### **OUTL (5)**

##### **OUTR (7)**

The OUTL/R pins are connected to the internal output amplifiers. They can be used for either stereo headphones or a mono loudspeaker. The signal of the right channel amplifier can be inverted for mono loudspeaker operation.

**Caution:** A short circuit at these pins for more than a momentary period may result in destruction of the internal circuits.

### 3.3.3. Oscillator and Clock Pins

#### **XTI (12)**

#### **XTO (13)**

The XTI pin is connected to the input of the internal crystal oscillator, the XTO pin to its output. Both pins should be directly connected to the crystal and two ground connected capacitors (see application diagram).

#### **CLKOUT (14)**

The CLKOUT pin provides a buffered output of the crystal oscillator.

**Caution:** A short circuit at this pin for more than a momentary period may result in destruction of the internal circuits.

#### **CLI (23)**

#### **DAI (24)**

#### **WSI (25)**

These three pins are inputs for the digital audio data DAI, frame indication signal WSI, and bit clock CLI. The digital audio data is transmitted in an I<sup>2</sup>S-compatible format. Audio word lengths of 16 and 32 bits are supported, as well as SONY and Philips I<sup>2</sup>S protocol.

#### **SCL (15)**

#### **SDA (16)**

SCL (serial clock) and SDA (serial data) provide the connection to the serial control interface (I<sup>2</sup>C).

### 3.3.4. Other Pins

#### **TESTEN (27)**

Test enable. This pin is for test purposes only and must always be connected to VSS.

#### **PORQ (26)**

This pin may be used to reset the chip. If not used, this pin must be connected to VDD.

#### **DEEML (34)**

#### **DEEMR (35)**

These pins connect an external analog deemphasis network to the signal path in the analog back-end. This connection can be switched on and off by an internal switch which is controlled either by I<sup>2</sup>C or the DEECTRL-pin.

#### **DEECTRL (21)**

If no I<sup>2</sup>C-control is used, deemphasis can be switched on and off with this pin.

#### **MCS1 (19)**

#### **MCS2 (20)**

Mode select pins to select MPEG, Standard Mode, and I<sup>2</sup>C subaddress.

### 3.4. Control Registers

I <sup>2</sup> C Sub-address (hex)	Number of Bits	Mode	Function	Default Values (hex)	Name
<b>SAMPLE RATE CONTROL SR_REG</b>					
01	8	w	sample rate control bit[7:5] not used, set to 0 bit[4] L/R-bit 0 WS = 0 → left channel 1 WS = 1 → right channel bit[3] Delay-Bit 0 No Delay 1 1 bit Delay bit[2:0] sample rate control 000 32–48 kHz 001 26–32 kHz 010 20–26 kHz 011 14–20 kHz 100 10–14 kHz 101 8–10 kHz 11x <sup>1)</sup> autoselect	0H	LR_SEL  SP_SEL  SRC_48 SRC_32 SRC_24 SRC_16 SRC_12 SRC_8 SRC_A
<b>ANALOG VOLUME AVOL</b>					
02	16	w	audio volume control bit[15] not used, set to 0 bit[14] deemphasis on/off 0 deemphasis off 1 deemphasis on bit[13:8] analog audio volume level left: 000000 mute 000001 -75 dB 101100 +0 dB (default) 111000 +18 dB bit[7:6] not used, set to 0 bit[5:0] analog audio volume level right 000000 mute 000001 -75 dB 101100 +0 dB (default) 111000 +18 dB	2C2CH	DEEM  AVOL_L  AVOL_R
1) don't care					

I <sup>2</sup> C Sub-address (hex)	Number of Bits	Mode	Function	Default Values (hex)	Name
<b>Global Configuration GCFG</b>					
03	8	w	global configuration bit[7] not used, set to 0 bit[6] select 3V-5 V mode 0 3 V 1 5 V bit[5] power-mode 0 normal 1 low power bit[4] AUX2 select 0 AUX2 off 1 AUX2 on bit[3] AUX1 select 0 AUX1 off 1 AUX1 on bit[2] DAC select 0 DAC off 1 DAC on (default) bit[1] aux-mono/stereo 0 stereo 1 mono bit[0] invert right power amplifier 0 not inverted 1 inverted	4H	SEL_53V PWMD INSEL_AUX2 INSEL_AUX1 INSEL_DAC AUX_MS IRPA

### 3.5. Electrical Characteristics

#### 3.5.1. Absolute Maximum Ratings

Symbol	Parameter	Pin Name	Min.	Max.	Unit
T <sub>A</sub>	Ambient Operating Temperature <sup>1)</sup>		0	70	°C
T <sub>S</sub>	Storage Temperature		-40	125	°C
P <sub>Pmax</sub>	Power Dissipation				mW
V <sub>SUPA</sub>	Analog Supply Voltage <sup>2)</sup>	AVDD0/1	-0.3	6	V
V <sub>SUPD</sub>	Digital Supply Voltage		-0.3	6	V
V <sub>Idig</sub>	Input Voltage, all digital inputs		-0.3	V <sub>SUPD</sub> + 0.3	V
I <sub>Idig</sub>	Input Current, all digital inputs		-5	+0.5	mA
V <sub>Iana</sub>	Input Voltage, all analog inputs		-0.3	V <sub>SUPA</sub> + 0.3	V
I <sub>Iana</sub>	Input Current, all analog inputs		-5	+5	mA
I <sub>Oaudio</sub>	Output Current, audio output <sup>3)</sup>	OUTL/R		0.2	A
I <sub>Oclk</sub>	Output Current	CLKOUT		tbd	A

<sup>1)</sup> =standard temperature range, DAC 3550A tested in extended temperature range (-20 to 85 °C) on request  
<sup>2)</sup> Both have to be connected together!  
<sup>3)</sup> These pins are NOT short-circuit proof!

Stresses beyond those listed in the "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only. Functional operation of the device at these or any other conditions beyond those indicated in the "Recommended Operating Conditions/Characteristics" of this specification is not implied. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.

#### 3.5.2. Recommended Operating Conditions

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Temperature Ranges and Supply Voltages						
T <sub>A</sub>	Ambient Temperature Range <sup>1)</sup>		0		70	°C
V <sub>SUPA1</sub>	Analog Audio Supply Voltage	AVDD0/1	3.0 <sup>2)</sup>	3.3	5.5	V
V <sub>SUPD</sub>	Digital Supply Voltage	VDD	2.7	3.3	5.5	V
Relative Supply Voltages						
V <sub>SUPA</sub>	Analog Audio Supply Voltage in relation to the Digital Supply Voltage	AVDD0/1	V <sub>SUPD</sub> -0.25 V		5.5 V	
Analog Reference						
C <sub>AGNDC1</sub>	Analog Reference Capacitor	AGNDC	1.0	3.3		µF
C <sub>AGNDC2</sub>	Analog Reference Capacitor	AGNDC		10		nF

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit
Analog Audio Inputs						
V <sub>AI</sub>	Analog Input Voltage AC, SEL_53V = 0	AUXnL/R <sup>3)</sup>		0.35	0.7	V <sub>rms</sub>
V <sub>AI</sub>	Analog Input Voltage AC, SEL_53V = 1	AUXnL/R <sup>3)</sup>		0.525	1.05	V <sub>rms</sub>
Analog Filter Input and Output						
Z <sub>AFLO</sub>	Analog Filter Load Output <sup>4)</sup>	FOUTL/R	7.5		6	kΩ pF
Z <sub>AFLI</sub>	Analog Filter Load Input <sup>4)</sup>	FINL/R	5.0		7.5	kΩ pF
Analog Audio Output						
Z <sub>LO</sub>	Audio Line Output <sup>5)</sup>	FINL/R	10		1.0	kΩ nF
Z <sub>AOL_HP</sub>	Analog Output Load HP (47 Ω Series Resistor required)	OUTL/R		32 400		Ω pF
Z <sub>AOL_SP</sub>	Analog Output Load SP (bridged)	OUTL/R	16	32 50		Ω pF
Quartz Characteristics						
T <sub>AC</sub>	Ambient Temperature Range <sup>1)</sup>		0		70	°C
F <sub>P</sub>	Load Resonance Frequency at C <sub>I</sub> = 20 pF		13.3	14.725	17	MHz
ΔF/F <sub>s</sub>	Accuracy of Adjustment		-20		20	ppm
ΔF/F <sub>s</sub>	Frequency Variation versus Temperature		-20		20	ppm
R <sub>EQ</sub>	Equivalent Series Resistance			12	30	Ω
C <sub>0</sub>	Shunt (parallel) Capacitance			3	5	pF
Load at CLKOUT Output						
C <sub>load</sub>	Capacitance	CLKOUT	0		21	pF
1) =standard temperature range, DAC 3550A tested in extended temperature range (-20 to 85 °C) on request						
2) operable down to 2.7 V, but with slightly diminished analog performance						
3) n = 1 or 2						
4) Please refer to Section 4.2. "Recommended Low-Pass Filters for Analog Outputs" on page 22.						
5) Please refer to Section 4.1. "Line Output Details" on page 22.						

### 3.5.3. Characteristics

At  $T_A = 0$  to  $70^\circ\text{C}$ <sup>1)</sup>,  $V_{SUPD} = 2.7$  to  $5.5$  V,  $V_{SUPA} = 3.0$  to  $5.5$  V; typical values at  $T_J = 27^\circ\text{C}$ ,  $V_{SUPD} = V_{SUPA} = 3.3$  V, quartz frequency = 14.725 MHz, duty cycle = 50 %, positive current flows into the IC

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
Digital Supply							
$I_{VDD}$	Current Consumption	VDD		5		mA	$V_{SUPD}=3$ V
$I_{VDD}$	Current Consumption	VDD		8		mA	$V_{SUPD}=5$ V
$I^2S$ Input							
$V_{I2S}$	Input Voltage	CLI,WSI, DAI	0		$V_{SUPA}$	V	
Digital Input Pin – Leakage							
$I_I$	Input Leakage Current	CLI, WSI, DAI, TESTEN, PORQ, DEECTRL, MCS1/2			$\pm 1$	$\mu\text{A}$	$V_{GND} \leq V_I \leq V_{SUP}$
Digital Output Pin – Clock Out							
$V_{OH}$	Output High Voltage	CLKOUT	$V_{SUPD} - 0.3$			V	no load at output
$V_{OL}$	Output Low Voltage				0.3	V	
$I^2C$ Bus							
$R_{on}$	Output Impedance	SCL, SDA			60	$\Omega$	$I_{load} = 5$ mA, $V_{SUPD} = 2.7$ V
Analog Supply							
$I_{AVDD}$	Current Consumption Analog Audio, SEL_53V = 0	AVDD0/1		8 1.5	11	mA mA	PWMD = 0, Mute PWMD = 1, Mute
	SEL_53V = 1			11 2	15	mA mA	PWMD = 0, Mute PWMD = 1, Mute
$PSRR_{AA}$	Power Supply Rejection Ratio for Analog Audio Output	AVDD0/1, OUTL/R		50		dB	1 kHz sine at 100 mV <sub>rms</sub>
				20		dB	$\leq 100$ kHz sine at 100 mV <sub>rms</sub>
$PSRR_{LO}$	Power Supply Rejection Ratio for Line Output	AVDD0/1, FINL/R		50		dB	1 kHz sine at 100 mV <sub>rms</sub>
				40		dB	$\leq 100$ kHz sine at 100 mV <sub>rms</sub>
Reference Frequency Generation							
$V_{DCXTI}$	DC Voltage at Oscillator Pins	XTI/O		$0.5 * V_{SUPA}$		V	
$C_{LI}$	Input Capacitance at Oscillator Pin	XTI		3		pF	

<sup>1)</sup> =standard temperature range, DAC 3550A tested in extended temperature range (-20 to 85 °C) on request

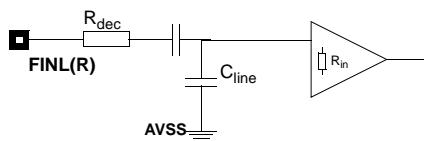
Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$C_{LO}$	Input Capacitance at Oscillator Pin	XTO		7		pF	
Vxtalout	Voltage Swing at Oscillator Pins (peak-peak)	XTI/O	0.6		1.0	pp, $V_{DDA}$	
	Oscillator Start-Up Time				50	ms	$V_{DD}$ slew rate
Analog Audio							
$V_{AGNDC}$	Analog Reference Voltage	AGNDC		1.5		V	$SEL\_53V = 0$ $R_L \gg 10 M\Omega$ , referred to VREF
				2.25		V	$SEL\_53V = 1$ $R_L \gg 10 M\Omega$ , referred to VREF
$R_{IAUX}$	Input Resistance at Input Pins	AUXnL/R	12.1 11.6	15	17.9 19.0	kΩ	$T_J = 27^\circ C$ $T_A = 0$ to $70^\circ C$ <sup>1)</sup> Input selected, $PWMD = 1$ $i = \pm 10 \mu A$ , referred to VREF
			24.2 23.3	30	35.8 37.9	kΩ	$T_J = 27^\circ C$ $T_A = 0$ to $70^\circ C$ <sup>1)</sup> Input not selected $i = \pm 10 \mu A$ , referred to VREF
$R_{OOUT}$	Output Resistance at Output Pins	OUTL/R		700		Ω	$T_J = 27^\circ C$ $PWMD = 0$ $i = \pm 200 \mu A$ , referred to VREF
$R_{OFILT}$	Output Resistance of Filter Pins	FINL		15		kΩ	$PWMD = 0$ , Mute $i = \pm 10 \mu A$ , referred to VREF
		FINR		11,25		kΩ	
$V_{OffI}$	Offset Voltage at Input Pins	AUXnL/R	-20		20	mV	$PWMD = 1$ , referred to AGNDC
$V_{OffO}$	Offset Voltage at Output Pins	OUTL/R	-10		10	mV	$PWMD = 1$ , Mute referred to AGNDC
$V_{OffFI}$	Offset Voltage at Filter Output Pins	FOUTL/R	-20		20	mV	$PWMD = 1$ , referred to AGNDC
$V_{OffFO}$	Offset Voltage at Filter Input Pins	FINL/R	-20		20	mV	$PWMD = 1$ , referred to AGNDC
$dV_{DCPD}$	Difference of DC Voltage at Output Pins after Back-end Low Power Sequence	OUTL/R	-10		10	mV	Analog Gain = Mute, $PWMD$ switched from 0 to 1
$R_{D/A}$	D/A Pass Band Ripple	OUTL/R, FOUTL/R		-0.1		dB	0...0.446 fs (no external filters used)
$A_{D/A}$	D/A Stop Band Attenuation			40		dB	0.55...7.533 fs (no external filters used)
$BW_{AUX}$	Bandwidth for Auxiliary Inputs	AUXnL/R, FINL/R		760		kHz	

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
THD <sub>ALO</sub>	Total Harmonic Distortion from Auxiliary Inputs to Line Outputs	AUXnL/R, FINL/R			0.01	%	BW = 20 Hz...22 kHz, unweighted, $R_L > 5 \text{ k}\Omega$ , Input 1 kHz at 0.5 V <sub>rms</sub> , $R_{dec} \geq 612 \Omega$
THD <sub>DLO</sub>	Total Harmonic Distortion (D/A converter to Line Output)	FINL/R			0.01	%	BW = 20 Hz...0.5 fs, unweighted, $R_L > 5 \text{ k}\Omega$ , Input 1 kHz at -3 dBFS, $R_{dec} \geq 612 \Omega$
THD <sub>HP</sub>	Total Harmonic Distortion (Headphone)	OUTL/R			0.05	%	BW = 20 Hz...0.5 fs, unweighted, $R_L \geq 32 \Omega$ (47 Ω series resistor required), Analog Gain = 0 dB, Input 1 kHz at -3 dBFS
THD <sub>SP</sub>	Total Harmonic Distortion (Speaker)	OUTL/R			0.5	%	BW = 20 Hz...0.5 fs, unweighted, $R_L \geq 32 \Omega$ (speaker bridged), Analog Gain = 0 dB, Input 1 kHz at -3 dBFS
SNR <sub>AUX</sub>	Signal-to-Noise Ratio from Analog Input to Line Output	AUXn, FINL/R		98		dB	SEL_53V = 0: input -40 dB below 0.7 V <sub>rms</sub> , SEL_53V = 1: input -40 dB below 1.05 V <sub>rms</sub>
	Signal-to-Noise Ratio from Analog Input to Headphone Output	AUXn, OUTn		96		dB	
SNR <sub>1</sub>	Signal-to-Noise Ratio	OUTL/R	89	91		dB	$R_L \geq 32 \Omega$ (external 47 Ω series resistor required), BW = 20 Hz...0.5 fs unweighted, Analog Gain = 0 dB, Input = -20 dBFS
		FINL/R	90	92		dB	$R_L \geq 5 \text{ k}\Omega$ , $R_{dec} \geq 612 \Omega$ , BW etc. as above, 16 bit I <sup>2</sup> S, SEL_53V = 0
			94			dB	32 bit I <sup>2</sup> S, SEL_53V = 0
			96			dB	16 bit I <sup>2</sup> S, SEL_53V = 1
			98			dB	32 bit I <sup>2</sup> S, SEL_53V = 1
SNR <sub>2</sub>	Signal-to-Noise Ratio	OUTL/R	58	62		dB	$R_L \geq 32 \Omega$ (external 47 Ω series resistor required), BW = 20 Hz..0.5 fs unweighted, Analog Gain = -40.5 dB, Input = -3 dBFS
Lev <sub>Mute</sub>	Mute Level	OUTL/R		-110		dBV	BW = 20 Hz...22 kHz unweighted, no digital input signal, Analog Gain = Mute

Symbol	Parameter	Pin Name	Min.	Typ.	Max.	Unit	Test Conditions
$V_{AO}$	Analog Output Voltage AC	OUTL/R, FOUTL/R, FINL/R	0.65	0.7	0.75	$V_{rms}$	SEL_53V = 0, $R_L > 5 \text{ k}\Omega$ , Analog Gain = 0 dB Input = 0 dBFS digital
			1.0	1.05	1.1	$V_{rms}$	SEL_53V = 1
$G_{AUX}$	Gain from Auxiliary Inputs to Line Outputs	AUXnL/R, FINL/R	-0.5	0	0.5	dB	$f = 1 \text{ kHz}$ , sine wave, $R_L > 5 \text{ k}\Omega$ 0.5 $V_{rms}$ to AUXnL/R
$P_{HP}$	Output Power (Headphone)	OUTL/R		5		mW	SEL_53V = 0, $R_L = 32 \Omega$ , Analog Gain = +2 dB, distortion < 1%, external 47 $\Omega$ series resistor required
				12		mW	SEL_53V = 1
$P_{SP}$	Output Power (Speaker)	OUTL/R		120		mW	$R_L = 32 \Omega$ (bridged), Analog Gain = +2 dB, distortion < 10%, SEL_53V = 0, IRPA = 1
				280		mW	SEL_53V = 1
$G_{AO}$	Analog Output Gain Setting Range	OUTL/R	-75		18	dB	
$dG_{AO1}$	Analog Output Gain Step Size	OUTL/R		3.0		dB	Analog Gain: -75 dB...54 dB
$dG_{AO2}$	Analog Output Gain Step Size	OUTL/R		1.5		dB	Analog Gain: -54 dB...18 dB
$E_{GA1}$	Analog Output Gain Error	OUTL/R	-2		2	dB	Analog Gain = -54 dB
$E_{GA2}$	Analog Output Gain Error	OUTL/R	-1		1	dB	Analog Gain = -45 dB
$E_{GA3}$	Analog Output Gain Error	OUTL/R	-0.5		0.5	dB	Analog Gain = -39 dB
$E_{dGA}$	Analog Output Gain Step Size Error	OUTL/R	-0.5		0.5	dB	Analog Gain = -48 dB
$XTALK_{LO}$	Cross-Talk Left/Right Channel (Line Output)	AUXnL/R, FOUTL/R, FINL/R	-70	-80		dB	$f = 1 \text{ kHz}$ , sine wave, $R_L > 7.5 \text{ k}\Omega$ Analog Gain = 0 dB, Input = -3 dBFS or 0.5 $V_{rms}$ to AUXnL/R
$XTALK_{HP}$	Crosstalk Left/Right Channel (Headphone)	OUTL/R	-70	-80		dB	$f = 1 \text{ kHz}$ , sine wave, OUTL/R: $R_L \geq 32 \Omega$ (47 $\Omega$ series resistor required) Analog Gain = 0 dB, Input = -3 dBFS or 0.5 $V_{rms}$ to AUXnL/R
$XTALK_2$	Crosstalk between Input Signal Pairs	AUXnL/R	-70	-80		dB	$f = 1 \text{ kHz}$ , sine wave, FOUTL/R: $R_L > 7.5 \text{ k}\Omega$ OUTL/R: $R_L \geq 32 \Omega$ (47 $\Omega$ series resistor required) Analog Gain = 0 dB, Input = -3 dBFS and 0.5 $V_{rms}$ to AUXnL/R

## 4. Applications

### 4.1. Line Output Details



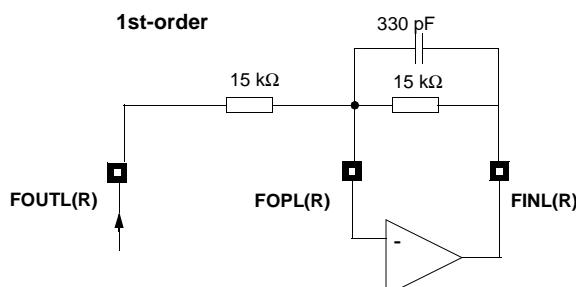
**Fig. 4–1:** Use of FINL/R as Line Outputs

**Table 4–1:** Load at FINL/R when used as Line Output for external amplifier

Filter Order	R <sub>dec</sub>	R <sub>in</sub>
1st	680 Ω	> 10 kΩ
2nd	680 Ω	> 10 kΩ
3rd	680 Ω	> 10 kΩ

R<sub>dec</sub>: Resistor used for decoupling C<sub>line</sub> from FINL(R) to achieve stability  
 C<sub>line</sub>: Capacitive load according to e.g. cable, amplifier  
 R<sub>in</sub>: Input resistance of amplifier

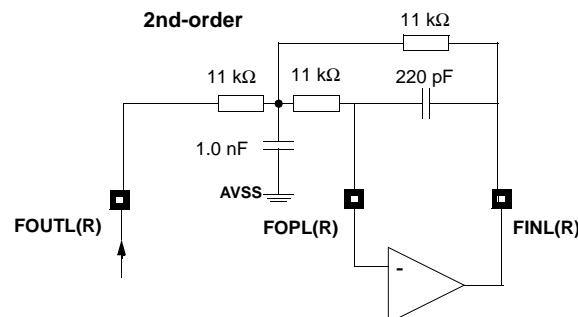
### 4.2. Recommended Low-Pass Filters for Analog Outputs<sup>1)</sup>



**Fig. 4–2:** 1st order low-pass filter

**Table 4–2:** Attenuation of 1st order low-pass filter

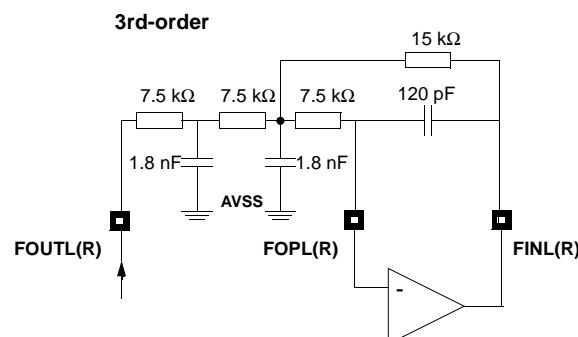
Frequency	Gain
24 kHz	-2.2 dB
30 kHz	-3.0 dB



**Fig. 4–3:** 2nd order low-pass filter

**Table 4–3:** Attenuation of 2nd order low-pass filter

Frequency	Gain
24 kHz	-1.5 dB
30 kHz	-3.0 dB

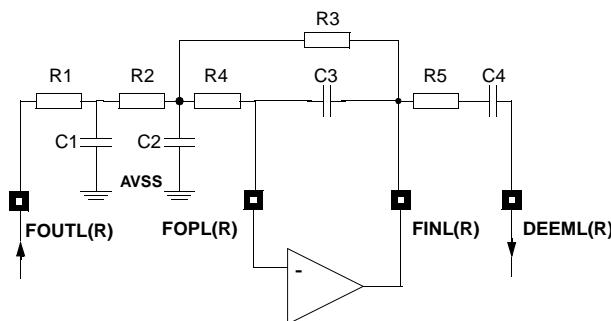
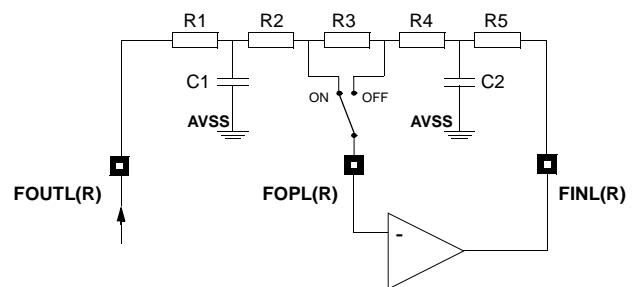


**Fig. 4–4:** 3rd order low-pass filter

**Table 4–4:** Attenuation of 3rd order low-pass filter

Frequency	Gain
18 kHz	0.17 dB
24 kHz	-0.23 dB
30 kHz	-3.00 dB

<sup>1)</sup> without deemphasis circuit

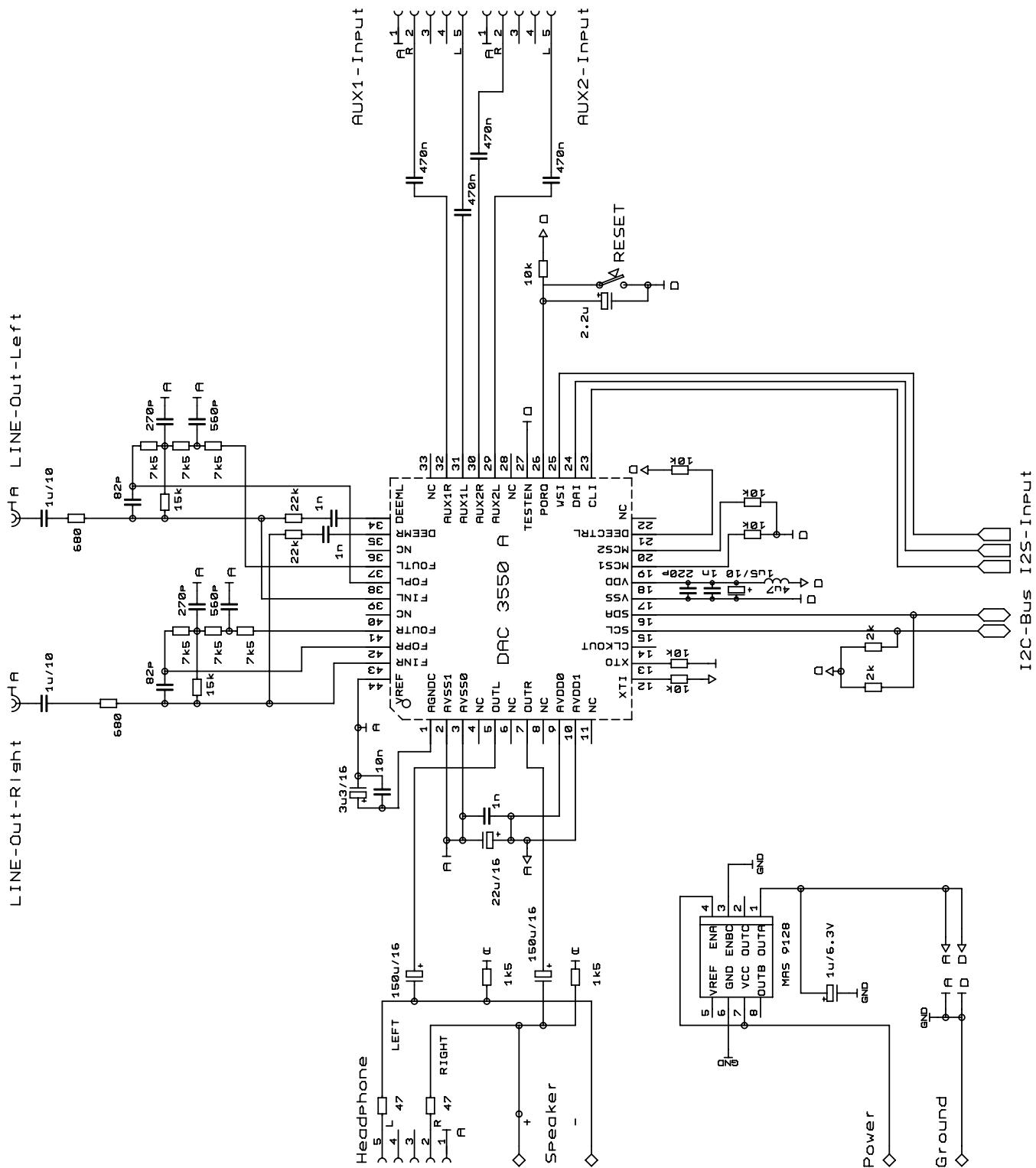
**4.3. Recommendations for Filters and Deemphasis****Fig. 4–5:** General circuit schematic**4.4. Recommendations for MegaBass Filter without Deemphasis****Fig. 4–6:** General circuit schematic**Table 4–5:** Resistor and Capacitor values

	<b>1st order</b>	<b>2nd order</b>	<b>3rd order</b>
R1 ( $k\Omega$ )	0		7.5
C1 (pF)	open		560
R2 ( $k\Omega$ )	18	11	7.5
C2 (pF)	open	1000	270
R3 ( $k\Omega$ )	18	11	15
C3 (pF)	180	180	82
R4 ( $k\Omega$ )	0	11	7.5
R5 ( $k\Omega$ )	18	22	22
C4 (nF)	1.8	1.0	1.0

**Table 4–6:** Resistor and Capacitor values

	<b>DC-Gain = 10 dB</b> <b>fc1 = 100 Hz</b> <b>fc2 = 330 Hz</b>
R1 ( $k\Omega$ )	13
C1 (nF)	47
R2 ( $k\Omega$ )	0
R3 ( $k\Omega$ )	15
R4 ( $k\Omega$ )	15
R5 ( $k\Omega$ )	13
C2 (nF)	47

#### **4.5. Typical Applications**



**Fig. 4–7:** Application circuit schematic 1

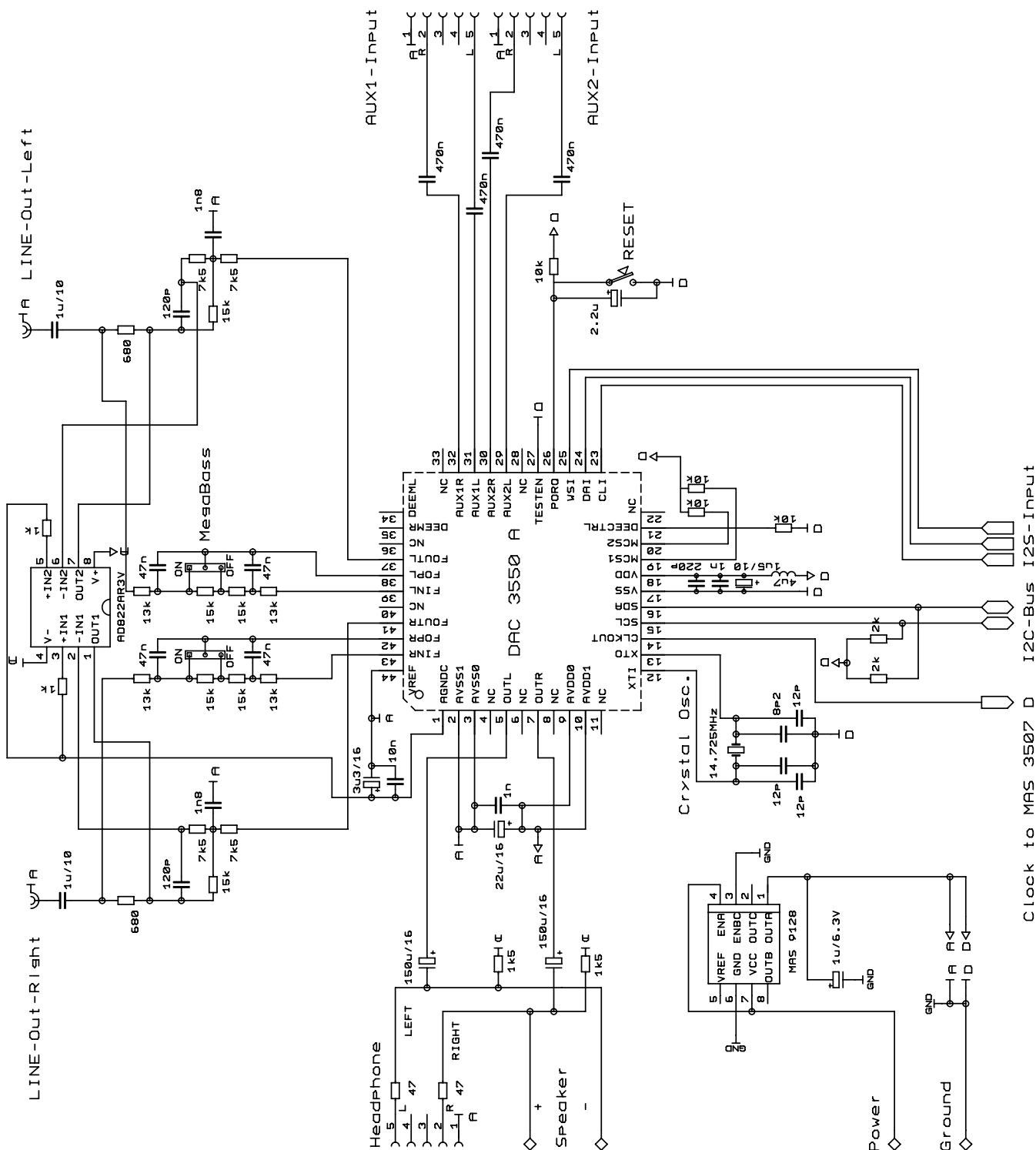
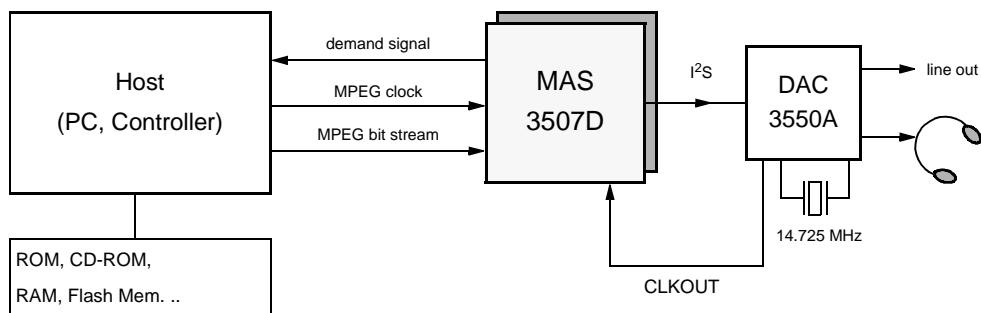
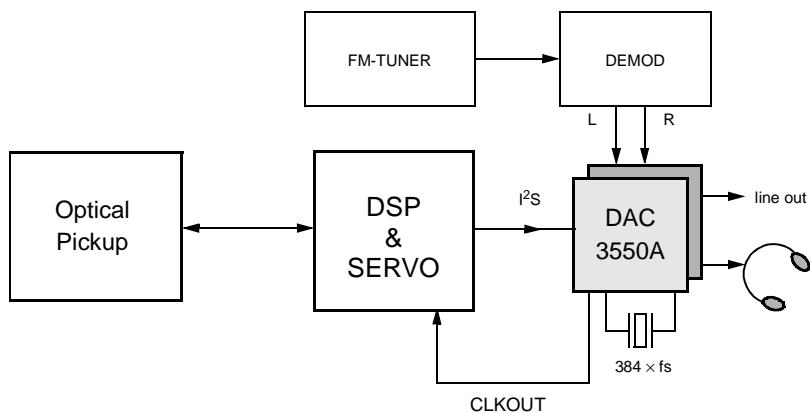


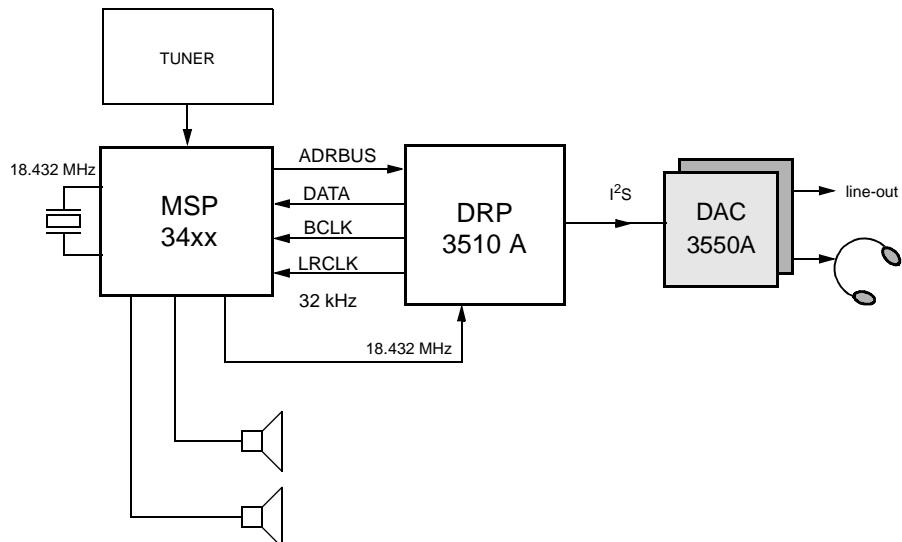
Fig. 4-8: Application circuit schematic 2



**Fig. 4–9: MPEG Layer 3 Player**



**Fig. 4–10: CD-Player with FM-Radio**



**Fig. 4–11: ADR Receiver**



### 5. Data Sheet History

1. Advance Information: "DAC 3550A Stereo Audio DAC", Edition Aug. 14, 1998, 6251-467-1AI. First release of the advance information.

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Printed in Germany  
Order No. 6251-467-1AI

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