Working Draft **X3T13 1153D**

Revision 9
10 February 1997

Information Technology - AT Attachment with Packet Interface Extension (ATA/ATAPI-4)

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Reference number
ANSI X3.*** - 199x
Printed February, 10, 1997 4:57PM

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DOCUMENT STATUS

Revision 0 - 5 February 1996

Document created from ATA3-r6 (X3T10/2008Dr6) with new frontmatter and the content of AT Attachment Packet Interface (X3T10/1120Dr2) added.

Revision 1 - 18 March 1996

Per 2/21-23/96 working group meeting:

- Changed document name
- Removed term ATA from text of document
- Added output table to each command, moved table 6, and equivanlent ATAPI table to Annex E
- Filled in na (not applicable) in command input and output tables
- Added PACKET bit descriptions in register descriptions clause 6.
- Added new clause 7.1 and rearranged clause 7.
- Made other text changes requested during page by page review.

Revision 2 - 5 April 1996

Per 3/27-29/96 working group meeting:

- Eliminated phrase “not used”/”not to be used”.
- Added “signature” the definitions and Protocol clause.
- Added SFF8020 reference and in bibliography.
- Swapped clauses 6 and 7.
- Reworded new clause 7, Register definitions to contains only material common to all commands.
- Added subclauses to clause 8, Commands.
- Made text changes requested during page-by-page review.

Revision 3 - 3 May 1996

Per 4/24-25/96 working group meeting:

- Modified PACKET protocol flowcharts as requested
- Added proposal D96102R2, Pins A-D on 44-pin connector
- Made text changes requested during review
- Added ATA3 letter ballot comment resolution

Revision 4 - 10 June 1996

Added revisions per page-by-page review at 5/22-24/96 working group meeting

Revision 5 - 28 June 1996

Added proposals:

- D96125R5 Vendor specific and optional commands
- D96137R0 Protected area proposal
- D96131R1 SMART change proposal

Added register transfer timing.
Added revisions per page-by-page review at 6/19-21/96 working group meeting.

Revision 6 - 6 September 1996

Added editorial changes from the ATA-3 ANSI pre-edit.
Added proposal D96106r1, FLUSH CACHE, as modified at the 7/31/96 working group meeting.
Added ATA/ATAPI-4 revision 6 to revisions list in IDENTIFY DEVICE response.
IORDY description in clause 5.2.11 changed to allow only tristate drivers.
Added description of invalid register address in Interface register definitions and descriptions clause.
Made “a” power management feature mandatory in the Power Management Feature set.
Moved timing conventions to Conventions clause.

Revision 7 - 3 October 1996

Per September 25-26 working group meeting:
Added Feature Status Reporting, D96103R2 with revisions.
Added PACKET feature set queuing from D96104R8.
Added Removing Redundant Information proposal, D96114R1, except for timing diagram changes.
Added unitized connectors, D96126R1 and D96149R0.
Added modified reset protocol, D96142R6.
Added changes per page-by-page review.

Revision 8 - 3 December 1996

Per October 23-24 and November 13-15 working group meetings:
Added READ/WRITE DMA O/Q commands (D96104R9).
Added new timing diagrams (D96114R2).
Added reset changes (D96157R0).
Added changes per page by page reviews.

Revision 9 - 10 February 1997

Added register access restrictions proposal (D97102R0)
Added SET MAX ADDRESS addition (D97106R1)
Added enhanced security erase proposal (D96156R2)
Added Ultra DMA proposal (D96153R3)
Made changes requested by page by page review through clause 8.9.

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X3.**-199x**

American National Standard
for Information Systems—

AT Attachment with Packet Interface Extension— (ATA/ATAPI-4)

Secretariat
Information Technology Industry Council

Approved mm dd yy

American National Standards Institute, Inc.

Abstract

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices. It includes the Packet Command feature set implemented by devices commonly known as ATAPI devices.

This standard maintains a high degree of compatibility with the AT Attachment-3 Interface (ATA-3), X3.298-1997, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

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American National Standards Institute
11 West 42nd Street, New York, New York 10036

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Foreword

(This foreward is not part of American National Standard X3.***-199*.)

This AT Attachment with Packet Interface Extension (ATA/ATAPI-4) standard is designed to maintain a high degree of compatibility with the AT Attachment-3 Interface (ATA-3) standard and the packet command feature set implemented by devices commonly known as ATAPI devices while providing the advantages of additional features and functions.

This standard was developed by the ATA ad hoc working group of Accredited Standards Committee X3 during 1995-97. The standards approval process started in 199x. This document includes annexes which are informative and are not considered part of the standard.

Requests for interpretation, suggestions for improvement and addenda, or defect reports are welcome. They should be sent to the X3 Secretariat, Information Technology Industry Council, 1250 Eye Street, NW, Suite 200, Washington, DC 20005-3922.

This standard was processed and approved for submittal to ANSI by Accredited Standards Committee on Information Processing Systems, X3. Committee approval of the standard does not necessarily imply that all committee members voted for approval. At the time it approved this standard, the X3 Committee had the following members:

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Gene Milligan, Chairman

Pete McLean, Vice-Chairman

Larry Lamers, Secretary

ATA/ATAPI ad hoc Working Group, which developed this standard, had the following members:

Introduction

This standard encompasses the following:

Clause 1 describes the scope.

Clause 2 provides definitions, abbreviations, and conventions used within this document.

Clause 3 provides normative references.

Clause 4 contains the electrical and mechanical characteristics; covering the interface cabling requirements of the interface and DC cables and connectors.

Clause 5 contains the signal descriptions of the AT Attachment Interface.

Clause 6 describes the general operating requirements of the AT Attachment Interface.

Clause 7 contains descriptions of the registers of the AT Attachment Interface.

Clause 8 contains descriptions of the commands of the AT Attachment Interface.

Clause 9 contains the protocol of the AT Attachment Interface.

Clause 10 contains the interface timing diagrams.

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AMERICAN NATIONAL STANDARD **X3.****-199n**

American National Standard
for Information Systems —

Information Technology—
AT Attachment with Packet Interface Extension—(ATA/ATAPI-4)

1 Scope

This standard specifies the AT Attachment Interface between host systems and storage devices. It provides a common attachment interface for systems manufacturers, system integrators, software suppliers, and suppliers of intelligent storage devices.

The application environment for the AT Attachment Interface is any host system that has storage devices contained within the processor enclosure.

This standard defines the connectors and cables for physical interconnection between host and storage device, as well as, the electrical and logical characteristics of the interconnecting signals. It also defines the operational registers within the storage device, and the commands and protocols for the operation of the storage device.

This standard maintains a high degree of compatibility with the AT Attachment-3 Interface standard (ATA-3), X3.298-1997, and while providing additional functions, is not intended to require changes to presently installed devices or existing software.

2 Normative References

The following standards contain provisions which, through reference in the text, constitute provisions of this standard. At the time of publication, the editions indicated were valid. All standards are subject to revision, and parties to agreements based on this standard are encouraged to investigate the possibility of applying the most recent editions of the standards listed below.

Copies of the following documents can be obtained from ANSI: Approved ANSI standards, approved and draft international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), and approved and draft foreign standards (including BSI, JIS, and DIN). For further information, contact ANSI Customer Service Department at 212-642-4900 (phone), 212-302-1286 (fax) or via the World Wide Web at http://www.ansi.org.

Additional availability contact information is provided below as needed.

2.1 Approved references

The following approved ANSI standards, approved international and regional standards (ISO, IEC, CEN/CENELEC, ITUT), may be obtained from the international and regional organizations who control them.

2.2 References under development

At the time of publication, the following referenced standards were still under development. For information on the current status of the document, or regarding availability, contact the relevant standards body or other organization as indicated.

SCSI-3 Primary Coommands (SPC) [X3T10/0995-D]
SCSI-3 Multimedia Commands (MMC) [X3T10/1048-D]

For more information on the current status of the above documents, contact (Secretariat). To obtain copies of these documents, contact Global Engineering or (Secretariat).

2.3 Other references

The following standards and specification were also consulted.

3 Definitions, abbreviations, and conventions

3.1 Definitions and abbreviations

For the purposes of this American National Standard, the following definitions apply:

3.1.1 ATA (AT Attachment): ATA defines the physical, electrical, transport, and command protocols for the internal attachment of storage devices.

3.1.2 ATAPI (AT Attachment Packet Interface): A device implementing the Packet Command feature set.

3.1.3 ATA-1 device: A device which complies with ANSI X3.221-1994, the AT Attachment Interface for Disk Drives.

3.1.4 ATA-2 device: A device which complies with ANSI X3.279-1996, the AT Attachment Interface with Extensions.

3.1.5 ATA-3 device: A device which complies with ANSI X3.298-1997, the AT Attachment-3 Interface.

3.1.6 check condition: For devices implementing the PACKET Command feature set, this indicates an exception condition has occurred that needs to be reported to the host.

3.1.7 command acceptance: A command is considered accepted whenever the host writes to the Command Register and the device currently selected has its BSY bit equal to zero. An exception exists for the EXECUTE DEVICE DIAGNOSTIC and DEVICE RESET command (see 8.4).

3.1.8 Command Block registers: Interface registers used for delivering commands to the device or posting status from the device.

3.1.9 command packet: A command packet is a data structure transmitted to the device by a PACKET command that includes the command and command parameters.

3.1.10 Control Block registers: Interface registers used for device control and to post alternate status.

3.1.11 CRC: Cyclical Redundancy Check used for the Ultra DMA protocol to check the validity of the data that has been transferred during the last Ultra DMA burst.

3.1.12 CHS (cylinder-head-sector): This term defines the addressing of the device as being by cylinder number, head number, and sector number.

3.1.13 data block: This term describes a unit of data words transferred using PIO data transfer. A data block is transferred between the host and the device as a complete unit. A data block is a sector, except for data blocks of a READ MULTIPLE and WRITE MULTIPLE commands. In the cases of READ MULTIPLE and WRITE MULTIPLE commands, the size of the data block may be changed in multiples of sectors by the SET MULTIPLE MODE command.

3.1.14 device: Device is a storage peripheral. Traditionally, a device on the interface has been a hard disk drive, but any form of storage device may be placed on the interface provided it adheres to this standard.

3.1.15 device selection: A device is selected when the DEV bit of the Drive/Head register is equal to the device number assigned to the device by means of a Device 0/Device 1 jumper or switch, or use of the CSEL signal.

3.1.16 DMA (direct memory access): A means of data transfer between device and host memory without processor intervention.

3.1.17 LBA (logical block address): This term defines the addressing of the device as being by the linear mapping of sectors.

3.1.18 master: In ATA-1, Device 0 has also been referred to as the master. Throughout this document the term Device 0 is used.

3.1.19 packet delivered command: A command that is delivered to the device using the PACKET command via a command packet that contains the command and the command parameters.

3.1.20 PIO (programmed input/output): A means of accessing device registers. PIO is also used to describe one form of data transfers. PIO data transfers are performed by the host processor utilizing PIO register accesses to the Data register.

3.1.21 register delivered command: A command that is delivered to the device by placing the command and all of the parameters for the command in the device Command Block registers.

3.1.22 released: Indicates that a signal is not being driven. For tri-state drivers, this means that the driver is in the high impedance state. For open-collector drivers, the driver is not asserted.

3.1.23 sector: A uniquely addressable set of 256 words (512 bytes).

3.1.24 signature: A unique set of values placed in the Command Block registers by the device to allow the host to distinguish between register delivered command devices and packet delivered command devices.

3.1.25 slave: In ATA-1, Device 1 has also been referred to as the slave. Throughout this document the term Device 1 is used.

3.1.26 SMART: Self-Monitoring, Analysis, and Reporting Technology for prediction of device degradation and/or faults. Throughout this document this is noted as SMART.

3.1.27 Ultra DMA burst: An Ultra DMA burst is defined as the period from an assertion of DMACK- to the subsequent negation of DMACK- when Ultra DMA has been enabled by the host.

3.1.28 unit attention condition: A state that a device implementing the PACKET Command feature set maintains while it has asynchronous status information to report to the host.

3.1.29 unrecoverable error: An unrecoverable error is defined as having occurred at any point when the device sets either the ERR bit or the DF bit to one and the BSY bit to zero in the Status register when processing a command.

3.1.30 VS (vendor specific): This term is used to describe bits, bytes, fields, and code values which are reserved for vendor specific purposes. These bits, bytes, fields, and code values are not described in this standard, and may vary among vendors. This term is also applied to levels of functionality whose definition is left to the vendor.

NOTE – Industry practice could result in conversion of a Vendor Specific bit, byte, field, or code value into a defined standard value in a future standard.

3.2 Conventions

Lowercase is used for words having the normal English meaning. Certain words and terms used in this American National Standard have a specific meaning beyond the normal English meaning. These words and terms are defined either in clause 3 or in the text where they first appear.

The names of abbreviations, commands, fields, and acronyms used as signal names are in all uppercase (e.g., IDENTIFY DEVICE). Fields containing only one bit are usually referred to as the "name" bit instead of the "name" field. (See 3.2.5 for the naming convention used for naming bits.)

Names of device registers begin with a capital letter (e.g., Cylinder Low register).

3.2.1 Precedence

If there is a conflict between text, figures, and tables, the precedence shall be tables, figures, then text.

3.2.2 Keywords

Several keywords are used to differentiate between different levels of requirements and optionality.

3.2.2.1 expected

A keyword used to describe the behavior of the hardware or software in the design models assumed by this standard. Other hardware and software design models may also be implemented.

3.2.2.2 mandatory

A keyword indicating items to be implemented as defined by this standard.

3.2.2.3 may

A keyword that indicates flexibility of choice with no implied preference.

3.2.2.4 obsolete

A keyword used to describe bits, bytes, fields and code values which no longer have consistent meaning or functionality from one implementation to another. However, some degree of functionality may be required for items designated as “obsolete” to provide for backward compatibility. An obsolete bit, byte, field or command shall never be reclaimed for any other use in any future standard. Bits, bytes, fields and code values that had been designated as “obsolete” in previous standards may have been reclassified as “retired” in this standard based on the definitions herein for “obsolete” and “retired”.

Obsolete commands should not be used by the host. Commands defined as obsolete in previous standards may be aborted by devices conforming to this standard. However, if a device does not abort an obsolete command but performs no operation in response to that command, the minimum that is required by the device in response to the command is clearing the BSY bit to zero, setting the DRDY bit to one, clearing the DRQ, CORR and ERR bits to zero and asserting INTRQ.

3.2.2.5 optional

A keyword that describes features that are not required by this standard. However, if any optional feature defined by the standard is implemented, it shall be done in the way defined by the standard. Describing a feature as optional in the text is done to assist the reader.

3.2.2.6 retired

A keyword indicating that the designated bits, bytes, fields and code values that had been defined in previous standards are not defined in this standard and may be reclaimed for other uses in future standards.

If retired bits, bytes, fields or code values are utilized before they are reclaimed, they shall have the meaning or functionality as described in previous standards.

3.2.2.7 reserved

A keyword indicating reserved bits, bytes, words, fields, and code values that are set aside for future standardization. Their use and interpretation may be specified by future extensions to this or other standards. A reserved bit, byte, word, or field shall be set to zero, or in accordance with a future extension to this standard. The recipient shall not check reserved bits, bytes, words, or fields. Receipt of reserved code values in defined fields shall be treated as an error.

3.2.2.8 shall

A keyword indicating a mandatory requirement. Designers are required to implement all such mandatory requirements to ensure interoperability with other standard conformant products.

3.2.2.9 should

A keyword indicating flexibility of choice with a strongly preferred alternative. Equivalent to the phrase “it is recommended”.

3.2.3 Numbering

Numbers that are not immediately followed by a lowercase "b" or "h" are decimal values. Numbers that are immediately followed by a lowercase "b" (e.g., 01b) are binary values. Numbers that are immediately followed by a lowercase "h" (e.g., 3Ah) are hexadecimal values.

3.2.4 Signal conventions

Signal names are shown in all uppercase letters.

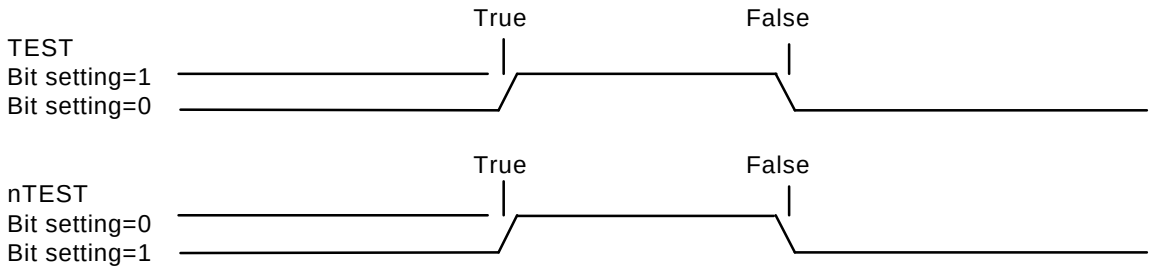
All signals are either high active or low active signals. A dash character (-) at the end of a signal name indicates it is a low active signal. A low active signal is true when it is below V_{iL}, and is false when it is above V_{iH}. No dash at the end of a signal name indicates it is a high active signal. A high active signal is true when it is above V_{iH}, and is false when it is below V_{iL}.

Asserted means that the signal is driven by an active circuit to its true state. Negated means that the signal is driven by an active circuit to its false state. Released means that the signal is not actively driven to any state (see 4.3.1). Some signals have bias circuitry that pull the signal to either a true state or false state when no signal driver is actively asserting or negating the signal.

Control signals that may be used for more than one mutually exclusive functions are identified with their function names separated by a colon.

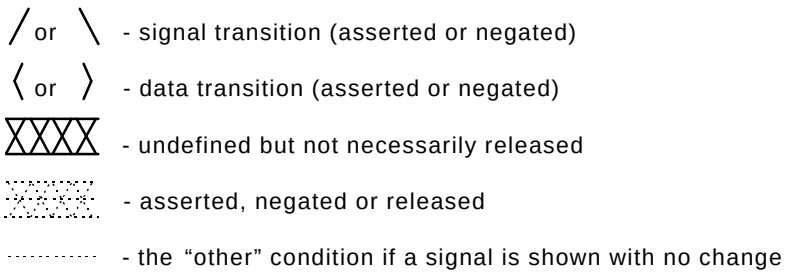
3.2.5 Bit conventions

Bit names are shown in all uppercase letters except where a lowercase n precedes a bit name. If there is no preceding n, then when BIT is set to one the meaning of the bit is true, and when BIT is cleared to zero the meaning of the bit is false. If there is a preceding n, then when nBIT is cleared to zero the meaning of the bit is true and when nBIT is set to one the meaning of the bit is false.



3.2.6 Timing conventions

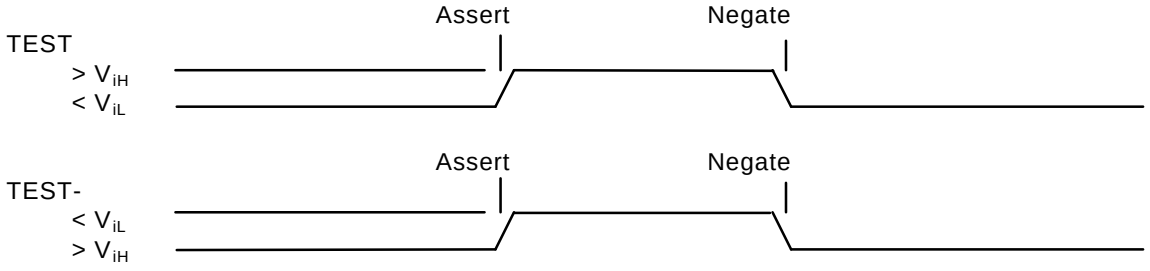
Certain symbols are used in the timing diagrams. These symbols and their respective definitions are listed below.



All signals are shown with the asserted condition facing to the top of the page. The negated condition is shown towards the bottom of the page relative to the asserted condition.

The interface uses a mixture of negative and positive signals for control and data. The terms asserted and negated are used for consistency and are independent of electrical characteristics.

In all timing diagrams, the lower line indicates negated, and the upper line indicates asserted e.g., the following illustrates the representation of a signal named TEST going from negated to asserted and back to negated, based on the polarity of the signal.



3.2.7 Byte ordering for data transfers

Assuming a block of data contains "n" bytes of information, the bytes are labeled Byte(0) through Byte(n-1), where Byte(0) is first byte of the block, and Byte(n-1) is the last byte of the block. Table 1 shows the order the bytes shall be presented in when such a block of data is transferred on the interface.

Table 1 – Byte order

	DD15	DD14	DD13	DD12	DD11	DD10	DD9	DD8	DD7	DD6	DD5	DD4	DD3	DD2	DD1	DD0
First transfer	Byte (1)								Byte (0)							
Second transfer	Byte (3)								Byte (2)							
.....																
Last transfer	Byte (n-1)								Byte (n-2)							

NOTE – The above description is for data on the interface. Host systems and/or host adapters may cause the order of data, as seen in the memory of the host, to be different.

4 Interface physical and electrical requirements

Connectors are documented in annex A.

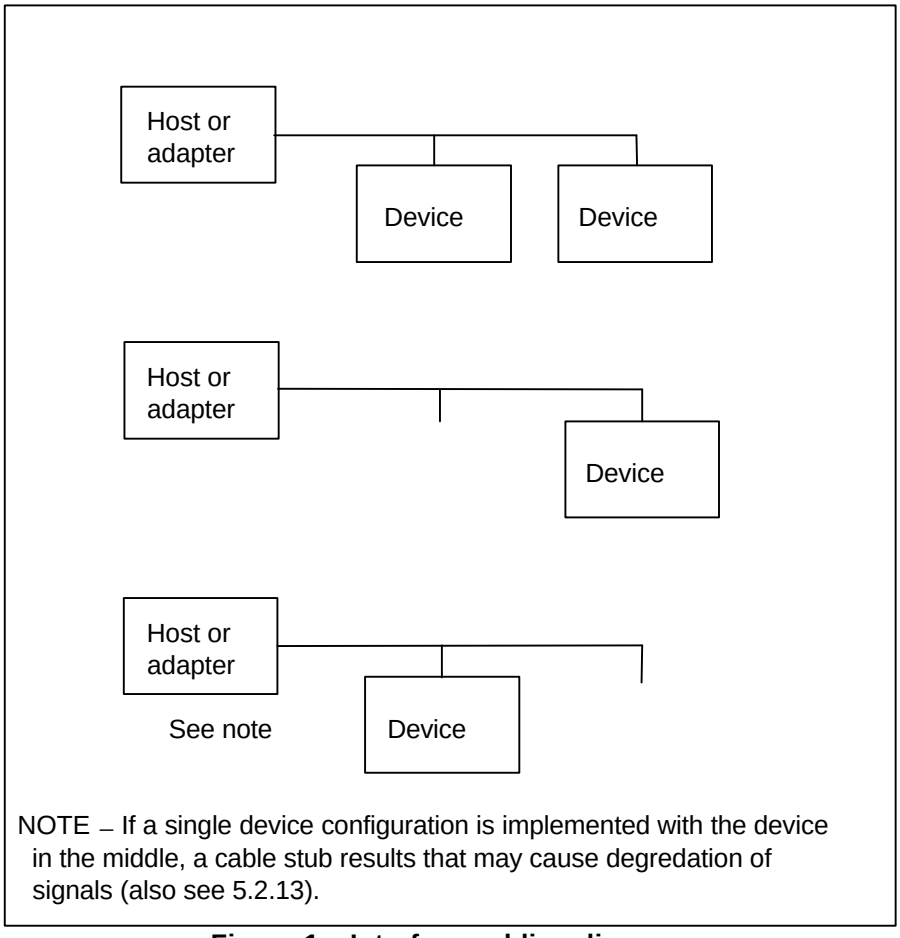
4.1 Cable configuration

This standard defines an interface containing a single host or host adapter and one or two devices. If two devices are connected to the interface, they are connected in a daisychained configuration. One device is configured as Device 0 and the other device as Device 1.

The designation of a device as Device 0 or Device 1 may be made in a number of ways including but not limited to:

- a switch or a jumper on the device;
- use of the Cable Select (CSEL) pin.

The host shall be placed at one end of the cable.



NOTE – If a single device configuration is implemented with the device in the middle, a cable stub results that may cause degredation of signals (also see 5.2.13).

Figure 1 – Interface cabling diagram

4.2 I/O cable

The cable specification affects system integrity and the maximum length that shall be supported in any application.

Cable total length shall not exceed 0.46 m (18 in).

Cable capacitance shall not exceed 35 pf.

4.3 Electrical characteristics

Table 2 defines the DC characteristics of the interface signals. Table 3 defines the AC characteristics.

Table 2 – DC characteristics

Description		Min	Max
I_{oL}	Driver sink current (see note 1)	4 mA	
I_{oH}	Driver source current (see note 2)	400 µA	
V_{iH}	Voltage input high	2.0 VDC	
V_{iL}	Voltage input low		0.8 VDC
V_{oH}	Voltage output high (I_{oH} = -400 µA)	2.4 VDC	
V_{oL}	Voltage output low (I_{oL} = 12 ma)		0.5 VDC

NOTES –
1 I_{oL} for DASP shall be 12 mA minimum to meet legacy timing and signal integrity.
2 I_{oH} value at 400 µA is insufficient in the case of DMARQ which is typically pulled low by a 5.6 kΩ resistor.

Table 3 – AC characteristics

Description		Min	Max
t_{RISE}	Rise time for any signal on AT interface (see note)	5 ns	
t_{FALL}	Fall time for any signal on AT interface (see note)	5 ns	
C_{in}	Host input capacitance		25 pf
C_{out}	Host output capacitance		25 pf
C_{in}	Device input capacitance		20 pf
C_{out}	Device output capacitance		20 pf

NOTE – t_{RISE} and t_{FALL} are measured from 10-90% of full signal amplitude with a total capacitive load of 40 pf.

4.3.1 Driver types and required termination

Table 4 – Driver types and required termination

Signal	Source	Driver type (see note 1)	Host (see note 2)	Device (see note 2)	Notes
Reset	Host	TP			
DD (15:0)	Bidir	TS			3
DMARQ	Device	TS	5.6 kΩ PD		4
DIOR-:HDMARDY-:HSTROBE	Host	TS			
DIOW-:STOP	Host	TS			
IORDY:DDMARDY-:DSTROBE	Device	TS	1.0 kΩ PU		7
CSEL	Host		Ground	10 kΩ PU	5, 7
DMACK-	Host	TP			
INTRQ	Device	TS			6
DA (2:0)	Host	TP			
PDIAG-	Device	TS		10 kΩ PU	7,8
CS0- CS1-	Host	TP			
DASP-	Device	OC		10 kΩ PU	7,9

NOTES –
1 TS=Tri-state; OC=Open Collector; TP=Totem-pole; PU=Pull-up; PD=Pull-down.
2 All resistor values are minimum (lowest) allowed.
3 Devices shall not have a pull-up resistor on DD7. It is recommended that a host have a 10 kΩ pull-down resistor and not a pull-up resistor on DD7 to allow a host to recognize the absence of a device at power-up. It is intended that this recommendation become mandatory in a future revision of this standard.
4 DMARQ shall be driven from its first assertion at the beginning of a DMA transfer until it is negated after the last word is transferred. This signal shall be tri-stated at all other times.
5 When used as CSEL, this line is grounded at the Host and a 10 kΩ pull-up is required at both devices.
6 If the host uses a level sensitive interrupt controller a 10kΩ pull-down or pull-up, depending upon the level sensed, may be required at the host.
7 Pull-up values are based on +5 v Vcc.
8 The host shall not drive PDIAG-. If the host connects to the PDIAG- , the host shall ensure that the signal level detected on the interface for PDIAG- shall maintain V_{oH} and V_{oL} compatibility, given the I_{oH} and I_{oL} requirements of the PDIAG- device drivers.
9 The host shall not drive DASP-. If the host connects to DASP- for any purpose, the host shall ensure that the signal level detected on the interface for DASP- shall maintain V_{oH} and V_{oL} compatibility, given the I_{oH} and I_{oL} requirements of the DASP- device drivers.

4.3.2 Electrical characteristics for Ultra DMA

4.3.2.1 Cable configuration

In a dual cable configuration (shared primary and secondary ports), DMACK- shall not be shared. It is recommended that DIOR-, DIOW-, and IORDY not be shared.

4.3.2.2 Series termination required for Ultra DMA

Series termination resistors are required at both the host and the device for operation in any of the Ultra DMA Modes. The following table describes recommended values for series termination at the host and the device.

Table 5 - Recommended series termination for Ultra DMA

Signal	Host Termination	Device Termination
DIOR-:HDMARDY-:HSTROBE	33 ohm	82 ohm
DIOW-:STOP	33 ohm	82 ohm
CS0-, CS1-	33 ohm	82 ohm
DA0, DA1, DA2	33 ohm	82 ohm
DMACK-	33 ohm	82 ohm
DD15 through DD0	33 ohm	33 ohm
DMARQ	82 ohm	33 ohm
INTRQ	82 ohm	33 ohm
IORDY:DDMARDY-:DSTROBE	82 ohm	22 ohm
Note: Only those signals requiring termination are listed in this table. If a signal is not listed, series termination is not required for operation in an Ultra DMA Mode.		

5 Interface signal assignments and descriptions

5.1 Signal summary

The physical interface consists of receivers and drivers communicating through a set of conductors using an asynchronous interface protocol. Table 6 defines the signal names. For connector descriptions see annex A. For driver and termination definition see 4.3.1. For signal protocol and timing see clause 9 and clause 10.

Table 6 – Interface signal name assignments

Description	Host	Dir	Dev	Acronym
Cable select		(see note)		CSEL
Chip select 0			→	CS0-
Chip select 1			→	CS1-
Data bus bit 0		↔		DD0
Data bus bit 1		↔		DD1
Data bus bit 2		↔		DD2
Data bus bit 3		↔		DD3
Data bus bit 4		↔		DD4
Data bus bit 5		↔		DD5
Data bus bit 6		↔		DD6
Data bus bit 7		↔		DD7
Data bus bit 8		↔		DD8
Data bus bit 9		↔		DD9
Data bus bit 10		↔		DD10
Data bus bit 11		↔		DD11
Data bus bit 12		↔		DD12
Data bus bit 13		↔		DD13
Data bus bit 14		↔		DD14
Data bus bit 15		↔		DD15
Device active or slave (Device 1) present		(see note)		DASP-
Device address bit 0			→	DA0
Device address bit 1			→	DA1
Device address bit 2			→	DA2
DMA acknowledge			→	DMACK-
DMA request	←			DMARQ
Interrupt request	←			INTRQ
I/O read DMA ready during Ultra DMA data in bursts Data strobe during Ultra DMA data out bursts			→ → →	DIOR- HDMARDY- HSTROBE
I/O ready DMA ready during Ultra DMA data out bursts Data strobe during Ultra DMA data in bursts	← ← ←			IORDY DDMARDY- DSTROBE
I/O write Stop during Ultra DMA data bursts			→ →	DIOW- STOP
Passed diagnostics		(see note)		PDIAG-
Reset			→	RESET-
NOTE – See signal descriptions for information on source of these signals				

5.2 Signal descriptions

5.2.1 CS (1:0)- (CHIP SELECT)

These are the chip select signals from the host used to select the Command Block registers, see 7.2. When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16-bits wide.

7.2**DA (2:0) (DEVICE ADDRESS)**

This is the 3-bit binary coded address asserted by the host to access a register or data port in the device, see 7.2.

5.2.3 DASP- (Device active, device 1 present)

This is a time-multiplexed signal which indicates that a device is active, or that Device 1 is present.

> NOTE – The indication that the device is active may be unsynchronized with the execution of the command.

5.2.4 DD (15:0) (Device data)

This is an 8- or 16-bit bi-directional data interface between the host and the device. The lower 8 bits are used for 8-bit register transfers. Data transfers are 16-bits wide.

5.2.5 DIOR-:HDMARDY-:HSTROBE (Device I/O read:Ultra DMA ready:Ultra DMA data strobe)

DIOR- is the strobe signal asserted by the host to read device registers or the data port.

HDMARDY- is a flow control signal for Ultra DMA data in bursts. This signal is asserted by the host to indicate to the device that the host is ready to receive Ultra DMA data in bursts. The host may negate HDMARDY- to pause an Ultra DMA data in burst.

HSTROBE is the data out strobe signal from the host for an Ultra DMA data out burst. Both the rising and falling edge of HSTROBE latch the data from DD(15:0) into the device. The host may stop generating HSTROBE edges to pause an Ultra DMA data out burst.

5.2.6 DIOW-:STOP (Device I/O write:Stop Ultra DMA burst)

DIOW- is the strobe signal asserted by the host to write device registers or the data port

DIOW- shall be negated by the host prior to initiation of an Ultra DMA burst. STOP shall be negated by the host before data is transferred in an Ultra DMA burst. Assertion of STOP by the host during an Ultra DMA burst signals the termination of the Ultra DMA burst.

5.2.7 DMACK- (DMA acknowledge)

This signal shall be used by the host in response to DMARQ to initiate DMA transfers.

5.2.8 DMARQ (DMA request)

This signal, used for DMA data transfers between host and device, shall be asserted by the device when it is ready to transfer data to or from the host. The direction of data transfer is controlled by DIOR- and DIOW-. This signal is used in a handshake manner with DMACK- i.e., the device shall wait until the host asserts DMACK- before negating DMARQ, and re-asserting DMARQ if there is more data to transfer.

When a DMA operation is enabled, CS0- and CS1- shall not be asserted and transfers shall be 16-bits wide.

5.2.9 INTRQ (Device interrupt)

This signal is used by the selected device to interrupt the host system. When the nIEN bit is cleared to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is set to one, or the device is not selected, the INTRQ signal shall be in a high impedance state.

5.2.10 IORDY:DDMARDY-:DSTROBE (I/O channel ready:Ultra DMA ready:Ultra DMA data strobe)

This signal is negated to extend the host transfer cycle of any host register access (Read or Write) when the device is not ready to respond to a data transfer request.

This signal is negated to extend the host transfer cycle of any register read or write when the device is not able to complete the transfer.

If the device requires extending the host transfer cycle time at PIO Modes 3 and above, the device shall utilize IORDY. Hosts that use PIO Modes 3 and above shall support IORDY.

DDMARDY- is a flow control signal for Ultra DMA data out bursts. This signal is asserted by the device to indicate to the host that the device is ready to receive Ultra DMA data out bursts. The device may negate DDMARDY- to pause an Ultra DMA data out burst.

DSTROBE is the data in strobe signal from the device for an Ultra DMA data in burst. Both the rising and falling edge of DSTROBE latch the data from DD(15:0) into the host. The device may stop generating DSTROBE edges to pause an Ultra DMA data in burst.

5.2.11 PDIAG- (Passed diagnostics)

This signal shall be asserted by Device 1 to indicate to Device 0 that it has completed diagnostics.

5.2.12 RESET- (Device reset)

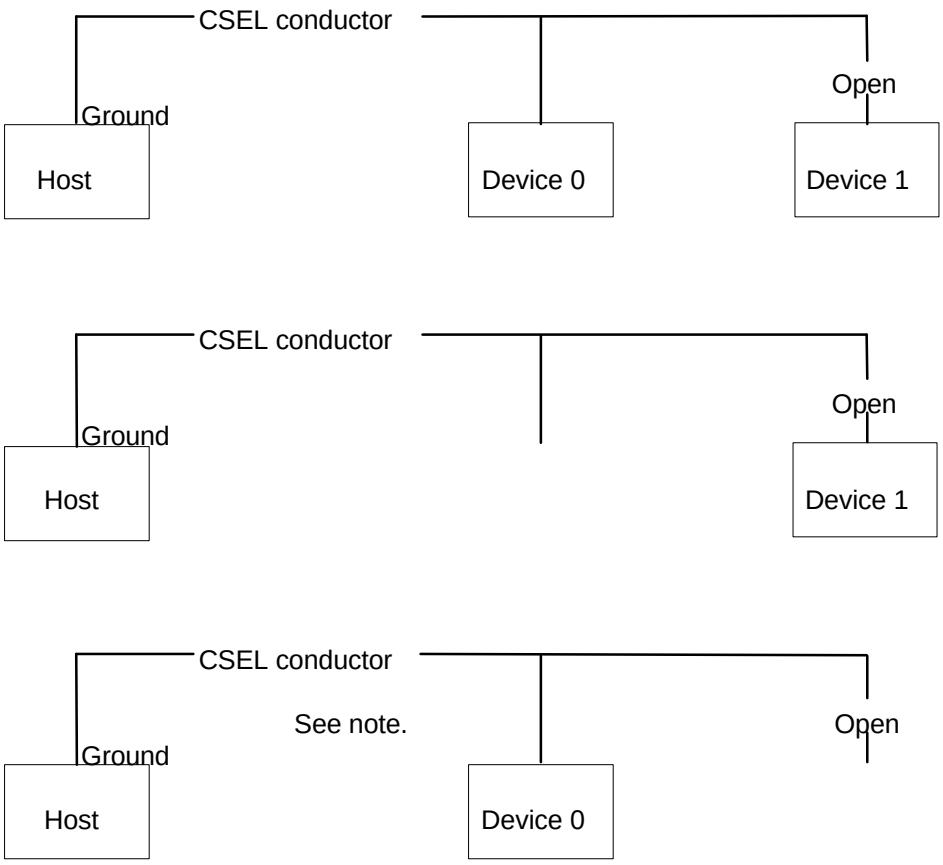
This signal, referred to as hardware reset, shall be used by the host to reset the device (see 6.7 and 9.2).

5.2.13 CSEL (Cable select)

The device is configured as either Device 0 or Device 1 depending upon the value of CSEL:

- If CSEL is negated then the device address is 0;
- If CSEL is asserted then the device address is 1.

NOTE – Special cabling may be used to selectively ground CSEL e.g., CSEL of Device 0 is connected to the CSEL conductor in the cable, and is grounded, thus allowing the device to recognize itself as Device 0. CSEL of Device 1 is not connected to CSEL because the conductor is removed, thus the device recognizes itself as Device 1. It should be recognized that if a single device is configured at the end of the cable using CSEL, a device 1 only configuration results.



NOTE – If a single device configuration is implemented with the device in the middle, a cable Stub results that may cause degredation of signals.

Figure 2 – Cable select example

6 General operational requirements

6.1 Command delivery

Commands may be delivered in two forms. For devices that do not implement the PACKET Command feature set, all commands and command parameters are delivered by writing the device Command Block registers. Such commands are defined as register delivered commands.

Devices that implement the PACKET Command feature set utilize packet delivered commands as well as some register delivered commands.

All register delivered commands and the PACKET command are described in clause 8.

NOTE – The content of command packets delivered by the PACKET command are not described in this specification.

6.2 Register delivered data transfer command sector addressing

For register delivered data transfer commands all addressing of data sectors recorded on the device's media is by a logical sector address. There is no implied relationship between logical sector addresses and the actual physical location of the data sector on the media.

A device shall support at least one logical CHS translation known as the default translation if the device capacity is less than 16,515,072 sectors. The device shall enter this translation following a power-on reset. A device shall support LBA translation regardless of capacity. If the device capacity is equal to or greater than 16,515,072 sectors, the LBA translation shall be the default translation and the device shall enter this translation following a power-on reset. A device may support other logical translations if the device capacity is less than 16,515,072 sectors and the host may use the INITIALIZE DEVICE PARAMETERS command to select the translation. The default translation is described in the IDENTIFY DEVICE information. The current translation may also be described in the IDENTIFY DEVICE information.

A CHS address is made up of three fields: the sector address, the head number and the cylinder number. Sectors are numbered from 1 to the maximum value allowed by the current CHS translation but shall not exceed 255. Heads are numbered from 0 to the maximum value allowed by the current CHS translation but shall not exceed 15. Cylinders are numbered from 0 to the maximum value allowed by the current CHS translation but cannot exceed 65,535.

When the host selects a CHS translation using the INITIALIZE DEVICE PARAMETERS command, the host requests the number of sectors per logical track and the number of heads per logical cylinder. The device then computes the number of logical cylinders available in requested translation.

A device shall not change the addressing method specified by the command and shall return status information utilizing the addressing method specified for the command.

a) The host may select either the currently selected CHS translation addressing or LBA addressing on a command-by-command basis by using the LBA bit in the Device/Head register;

b) The device shall support LBA addressing for all media access commands. The LBA bit of the Device/Head register shall be ignored for commands that do not access the media;

c) Logical sectors on the device shall be linearly mapped with the first LBA addressed sector (sector 0) being the same sector as the first logical CHS addressed sector (cylinder 0, head 0, sector 1). Irrespective of the logical CHS translation currently in effect, the LBA address of a given logical sector does not change. The following is always true:

LBA = ((cylinder * heads_per_cylinder + heads) * sectors_per_track) + sector - 1

where heads_per_cylinder and sectors_per_track are the current translation values.

6.3 Ultra DMA

6.3.1 Overview

Ultra DMA is a data transfer protocol used with the READ DMA, WRITE DMA, READ DMA O/Q, WRITE DMA O/Q, and PACKET commands. When this protocol is enabled it shall be used instead of the Multiword DMA protocol when these commands are issued by the host. This protocol applies to the Ultra DMA data burst only. When this protocol is used there are no changes to other elements of the ATA protocol (e.g.: Command Block Register access).

Several signal lines are redefined to provide new functions during an Ultra DMA burst. These lines assume these definitions when 1) an Ultra DMA Mode is selected, and 2) a host issues a READ DMA, WRITE DMA, READ DMA O/Q, WRITE DMA O/Q or a PACKET command requiring data transfer, and 3) the host asserts DMACK-. These signal lines revert back to the definitions used for non-Ultra DMA transfers upon the negation of DMACK- by the host at the termination of an Ultra DMA burst. All of the control signals are unidirectional. DMARQ and DMACK- retain their standard definitions.

With the Ultra DMA protocol, the control signal (STROBE) that latches data from DD(15:0) is generated by the same agent (either host or device) which drives the data onto the bus. Ownership of DD(15:0) and this data strobe signal are given either to the device during an Ultra DMA data in burst or to the host for an Ultra DMA data out burst.

During an Ultra DMA burst a sender shall always drive data onto the bus, and, after a sufficient time to allow for propagation delay, cable settling, and setup time, the sender shall generate a STROBE edge to latch the data. Both edges of STROBE are used for data transfers so that the frequency of STROBE is limited to the same frequency as the data. The highest fundamental frequency on the cable shall be 16.67 million transitions per second or 8.33 MHz (the same as the maximum frequency for PIO Mode 4 and DMA Mode 2).

Words in the IDENTIFY DEVICE data indicate support of the Ultra DMA feature and the Ultra DMA Modes the device is capable of supporting. The Set transfer mode subcommand in the SET FEATURES command shall be used by a host to select the Ultra DMA Mode at which the system operates. The Ultra DMA Mode selected by a host shall be less than or equal to the fastest mode of which the device is capable. Only one Ultra DMA Mode shall be selected at any given time. All timing requirements for a selected Ultra DMA Mode shall be satisfied. Devices supporting Ultra DMA Mode 2 shall also support Ultra DMA Modes 0 and 1. Devices supporting Ultra DMA Mode 1 shall also support Ultra DMA Mode 0.

An Ultra DMA capable device shall retain its previously selected Ultra DMA Mode after executing a Software reset sequence or the sequence caused by receipt of a DEVICE RESET command. An Ultra DMA capable device shall clear any previously selected Ultra DMA Mode and revert to its default non-Ultra DMA Modes after executing a Power on or hardware reset.

Both the host and device perform a CRC function during an Ultra DMA burst. At the end of an Ultra DMA burst the host sends the its CRC data to the device. The device compares its CRC data to the data sent from the host. If the two values do not match the device reports an error in the error register at the end of the command.

6.3.2 Phases of operation

An Ultra DMA data transfer is accomplished through a series of Ultra DMA data in or data out bursts. Each Ultra DMA burst has three mandatory phases of operation: the initiation phase, the data transfer phase, and the Ultra DMA burst termination phase. In addition, an Ultra DMA burst may be paused during the data transfer phase (see 9.12 and 9.13 for the detailed protocol descriptions for each of these phases, 10.2.4 defines the specific timing requirements). In the following rules DMARDY- is used in cases that could apply to either DDMARDY- or HDMARDY-, and STROBE is used in cases that could apply to either DSTROBE or HSTROBE. The following are general Ultra DMA rules.

a) An Ultra DMA burst is defined as the period from an assertion of DMACK- by the host to the subsequent negation of DMACK-.
b) A recipient shall be prepared to receive at least two data words whenever it enters or resumes an Ultra DMA burst.

6.3.2.1 Ultra DMA burst initiation phase rules

a) An Ultra DMA burst initiation phase begins with the assertion of DMARQ by a device and ends when the sender generates a STROBE edge to transfer the first data word.
b) An Ultra DMA burst shall always be requested by a device asserting DMARQ.
c) A host indicates it is ready to initiate the requested Ultra DMA burst by asserting DMACK-.
d) A host shall never assert DMACK- without first detecting that DMARQ is asserted.
e) For Ultra DMA data in bursts: a device may begin driving DD(15:0) after detecting that DMACK- is asserted, STOP negated, and HDMARDY- is asserted.
f) After asserting DMARQ or asserting DDMARDY- for an Ultra DMA data out burst, a device shall not negate either signal until the first STROBE edge is generated.
g) After negating STOP or asserting HDMARDY- for an Ultra DMA data in burst, a host shall not change the state of either signal until the first STROBE edge is generated.

6.3.2.2 Data transfer phase rules

a) The data transfer phase is in effect from after Ultra DMA burst initiation until Ultra DMA burst termination. b) A recipient pauses an Ultra DMA burst by negating DMARDY- and resumes an Ultra DMA burst by reasserting DMARDY-.
c) A sender pauses an Ultra DMA burst by not generating STROBE edges and resumes by generating STROBE edges.
d) A recipient shall not signal a termination request when the sender stops generating STROBE edges. In the absence of a termination from the sender the recipient shall always negate DMARDY- and wait the required period before signaling a termination request.
e) A sender may generate STROBE edges at greater than the minimum period specified by the enabled Ultra DMA Mode. The sender shall not generate STROBE edges at less than the minimum period specified by the enabled Ultra DMA Mode. A recipient shall be able to receive data at the minimum period specified by the enabled Ultra DMA Mode.

6.3.2.3 Ultra DMA burst termination phase rules

a) Either a sender or a recipient may terminate an Ultra DMA burst.
b) Ultra DMA burst termination is not the same as command termination or completion. If an Ultra DMA burst termination occurs before the command is complete, the command shall be completed by initiation of a new Ultra DMA burst at some later time or aborted by the host issuing a reset to the device.
c) An Ultra DMA burst shall be paused before a recipient requests a termination.
d) A host requests a termination by asserting STOP. A device acknowledges a termination request by negating DMARQ.
e) A device requests a termination by negating DMARQ. A host acknowledges a termination request by asserting STOP.
f) Once a sender requests a termination, it shall not change the state of STROBE until the recipient acknowledges the request. Then, if STROBE is not in the asserted state, the sender shall return STROBE to the asserted state. No data shall be transferred on this transition of STROBE.
g) A sender shall return STROBE to the asserted state whenever it detects a termination request from the recipient. No data shall be transferred nor CRC calculated on this edge of DSTROBE.

h) Once a recipient requests a termination, it shall not change DMARDY from the negated state for the remainder of an Ultra DMA burst.
k) A recipient shall ignore a STROBE edge when DMARQ is negated or STOP is asserted.

6.4 PACKET Command feature set

The PACKET Command feature set provides for devices that require command parameters that are too extensive to be expressed in the Command Block registers. Devices implementing the PACKET Command feature set exhibit responses different from that exhibited by devices not implementing this feature set.

The commands unique to the PACKET Command feature set are:

- PACKET
- IDENTIFY PACKET DEVICE

6.4.1 Identification of PACKET Command feature set devices

When executing a power on, hardware, DEVICE RESET, or software reset, a device implementing the PACKET Command feature set performs the same reset protocol as other devices but leaves the registers with a signature unique to PACKET Command feature set devices (see 9.1).

In addition, the IDENTIFY DEVICE command shall not be executed but aborts and returns a signature unique to devices implementing the PACKET Command feature set. IDENTIFY DEVICE is replaced by the IDENTIFY PACKET DEVICE command that provides information unique to devices using this feature set.

6.4.2 PACKET Command feature set resets

Devices implementing the PACKET Command feature set respond to power-on, hardware, and software resets as any other device except for the resulting contents in the device registers as decribed above. However, it is recommended that software reset not be issued while a PACKET command is in progress. PACKET commands utilized by some devices do not terminate if a software reset is issued.

The DEVICE RESET command is provided to allow the device to be reset without effecting the other device on the bus.

6.4.3 The PACKET command

The PACKET command allows a host to send a command to the device via a command packet. The command packet contains the command and command parameters that the device is to execute.

Upon receipt of the PACKET command the device sets BSY to one and prepares to receive the command packet. When ready, the device sets DRQ to one and clears BSY to zero. The command packet is then transferred to the device by PIO transfer. When the last word of the command packet is transferred, the device sets BSY to one, and clears DRQ to zero (see 8.12 and 9.10).

6.5 Overlapped commands

Overlap allows devices that require extended time to prepare for command execution to release the bus so that the other device on the bus may be used while the overlap device is preparing for the command execution. The act of releasing the bus involves clearing both the DRQ and BSY bits to zero just as at the end of a non-overlapped command.

Commands utilized by the Overlap feature set are:

- PACKET
- READ DMA QUEUED
- SERVICE

- WRITE DMA QUEUED

For the PACKET command, overlap is indicated by the OVL bit in the features register when the PACKET command is issued.

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been enabled via the SET FEATURES command, the device must release when the command packet has been received. This allows the host to select the other device to execute commands if desired. When the device is ready to continue the command, the device sets SERV to one, and asserts INTRQ if selected and interrupts are enabled. The host then issues the SERVICE command to continue the execution of the command

If the device supports PACKET command overlap, the OVL bit is set to one in the Features register and the Release interrupt has been disabled via the SET FEATURES command, the device may or may not release. If the device is to complete execution of the command, it may complete the command immediately as described in the non-overlap case. If the device is not ready to complete execution of the command, the device may release and complete the command as described in the previous paragraph.

For the READ DMA QUEUED and WRITE DMA QUEUED commands, the device may or may not release. If the device is to complete execution of the command, it may complete the command immediately. If the device is not ready to complete execution of the command, the device may release and complete the command via a service request.

6.6 Queued commands

Command queuing allows the host to issue concurrent commands to the same device. Only overlapped commands may be queued. If a queued command is outstanding when a non-queued command is received both commands and the queue will be aborted. The ending status shall be ABORT command and the results are indeterminant.

The maximum queue depth supported by a device shall be indicated in word 73 of the IDENTIFY DEVICE or IDENTIFY PACKET DEVICE response.

A queued command shall have a tag provided by the host in the Sector Count register to uniquely identify the command. When the device restores register parameters during the execution of the SERVICE command, this tag shall be restored so that the host may identify the command for which status is being presented. If a queued command is issued with a tag value that is identical to the tag value for a command already in the queue, the entire queue shall be aborted including the new command. The ending status shall be ABORT command and the results are indeterminant. If any error occurs, the command queue shall be aborted.

6.7 Reset response

There are four types of resets. The following is a suggested method of classifying reset actions:

- Power On Reset: Executed at power on, the device executes a series of electrical circuitry diagnostics, spins up the HDA, tests speed and other mechanical parametrics, and sets default values (see 9.2).
- Hardware Reset: Executed in response to the assertion of the RESET- signal the device executes a series of electrical circuitry diagnostics, and resets to default values (see 9.2).
- Software Reset: Executed in response to the setting of the SRST bit in the Device Control register the device resets the interface circuitry (see 9.3).
- Device Reset: Executed in response to the DEVICE RESET command the device resets the interface circuitry (see 8.2).

6.8 Power Management feature set

A device shall implement power management. A device implementing the PACKET Command feature set may implement the power management as defined by the packet command set implemented by the device. Otherwise, the device shall implement the Power Management feature set as described in this standard.

The Power Management feature set permits a host to modify the behavior of a device in a manner which reduces the power required to operate. The Power Management feature set provides a set of commands and a timer that enable a device to implement low power consumption modes. A register delivered command device that implements the Power Management feature set shall implement the following minimum set of functions:

a) A Standby timer;
b) CHECK POWER MODE command;
c) IDLE command;
d) IDLE IMMEDIATE command;
e) SLEEP command;
f) STANDBY command;
g) STANDBY IMMEDIATE command.

A device that implements the PACKET Command feature set and implements the Power Management feature set shall implement the following minimum set of functions:

a) A Standby timer;
b) CHECK POWER MODE command;
c) IDLE IMMEDIATE command;
d) SLEEP command;
e) STANDBY IMMEDIATE command.

6.8.1 Power modes

In Active mode the device is capable of responding to commands. During the execution of a media access command a device shall be in Active mode. Power consumption is greatest in this mode.

In Idle mode the device is capable of responding to commands but the device may take longer to complete commands than when in the Active mode. Power consumption may be reduced from that of Active mode.

In Standby mode the device is capable of responding to commands but the device may take longer to complete commands than in the Idle mode. The time to respond could be as long as 30 s. Power consumption may be reduced from that of Idle mode.

In Sleep mode the device requires a reset to be activated. The time to respond could be as long as 30 s. Sleep mode provides the lowest power consumption of any mode.

6.8.2 Power management commands

The CHECK POWER MODE command allows a host to determine if a device is currently in, going to or leaving Standby or Idle mode. The CHECK POWER MODE command shall not change the power mode or reset the Standby timer.

The IDLE and IDLE IMMEDIATE commands move a device to Idle mode immediately from the Active or Standby modes. The IDLE command also sets the Standby timer count and enables or disables the Standby timer.

The SLEEP command moves a device to Sleep mode. The device's interface becomes inactive at the completion of the SLEEP command. A reset is required to move a device out of Sleep mode.

It is recommended that a device shall return to the mode it was in before receiving the reset, unless the device was in the Sleep mode. If the device was in the Sleep mode when receiving a reset, the device should return to the Standby mode (This may be made a mandatory requirement in a future standard).

The STANDBY and STANDBY IMMEDIATE commands move a device to Standby mode immediately from the Active or Idle modes. The STANDBY command also sets the Standby timer count and enables or disables the Standby timer.

6.8.3 Standby timer

The Standby timer provides a method for the device to automatically enter Standby mode from either Active or Idle mode following a host programmed period of inactivity. If the Standby timer is enabled and if the device is in the Active or Idle mode, the device waits for the specified time period and if no command is received, the device automatically enters the Standby mode.

If the Standby timer is disabled, the device may not automatically enter Standby mode.

6.8.4 Idle mode transition

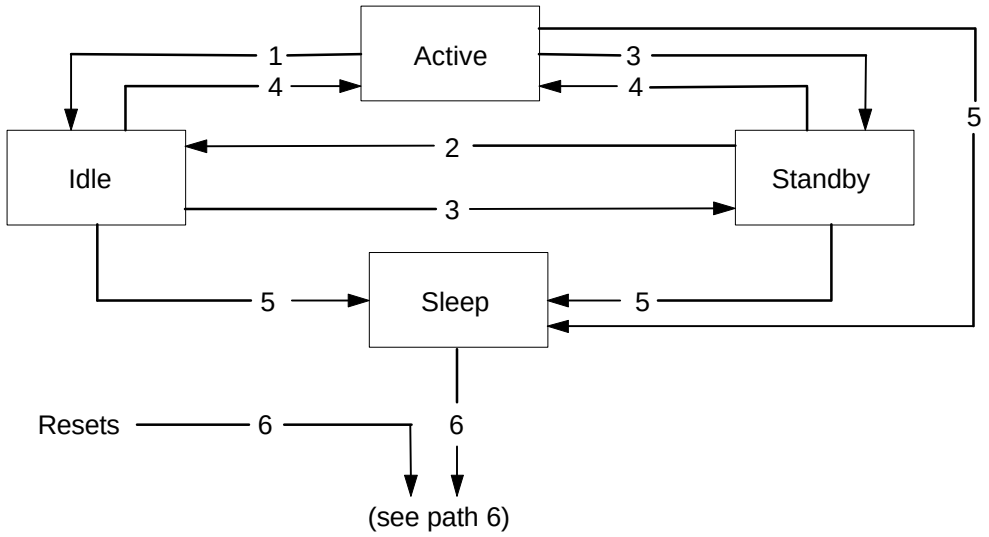
If a device accepts the IDLE IMMEDIATE command, the device shall transition to the Idle mode after receipt of the command. If the device accepts the IDLE command it shall transition to the Idle mode as described in 8.8.7. Some devices may perform internal power management and transition to the Idle mode without host intervention.

6.8.5 Status

In Sleep mode, the device's interface is not active. The content of the Status register is invalid in this mode.

6.8.6 Power mode transitions

Figure 3 shows the minimum set of mode transitions that shall be implemented.



Path 1: An IDLE command, IDLE IMMEDIATE command, or vendor specific implementation moves the device to Idle mode.
Path 2: An IDLE command or IDLE IMMEDIATE command moves the device to Idle mode.
Path 3: A STANDBY command, STANDBY IMMEDIATE command, vendor specific implementation, or Standby timer expiration moves the device to Standby mode.
Path 4: A Media access command moves the device to Active mode.
Path 5: A SLEEP command moves the device to Sleep mode.
Path 6: A reset, either hardware or software, moves the device to Active, Idle or Standby as specified by the device vendor.

Figure 3 – Power management modes

6.9 Security Mode feature set

The Security Mode feature set allows a host to implement a security password system to prevent unauthorized access to the internal disk drive.

A device that implements the Security Mode feature set shall implement the following minimum set of commands:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY ERASE PREPARE
- SECURITY ERASE UNIT
- SECURITY FREEZE LOCK
- SECURITY DISABLE PASSWORD

Support of the Security Mode feature set is indicated in IDENTIFY DEVICE response Word 128.

6.9.1 Security mode default setting

The Master password shall be set to a vendor specific value during manufactuing and the Lock mode disabled.

The system manufacturer/dealer may set a new Master password using the SECURITY SET PASSWORD command, without enabling or disabling the Lock mode.

6.9.2 Intial setting of the User password

When a User password is set, the device shall automatically enter Lock mode the next time the device is powered-on or hardware reset.

6.9.3 Security mode operation from power-on or hardware reset

When Lock is enabled, the device rejects media access commands until a SECURITY UNLOCK command is successfully completed.

6.9.4 Frozen mode

The SECURITY FREEZE LOCK command places the device in Frozen mode. This prevents accidental or malicious password activation or setting. Table 7 lists the commands that the device shall execute when in Frozen mode. The device shall exit Frozen mode on power off. It is recommended that all devices that support the Security Mode feature set be issued a SECURITY FREEZE LOCK command during system initialization.

6.9.5 User password lost

If the User password does not match and High level security is set, the device shall not allow the user to access data. The device shall be unlocked using the Master password.

If the User password is lost and Maximum security level is set, data access shall not be allowed. However, the SECURITY ERASE UNIT command shall unlock the device with the Master password and shall erase all user data.

6.9.6 Attempt limit for SECURITY UNLOCK command

The device shall have an attempt limit counter. The purpose of this counter is to defeat repeated trial attacks. After each failed User or Master password SECURITY UNLOCK command, the counter is decremented. When the counter value reaches zero the EXPIRE bit (bit 4) of word 128 in the IDENTIFY DEVICE information is set, and the SECURITY UNLOCK and SECURITY UNIT ERASE commands are aborted until the drive is powered off or hardware reset. The EXPIRE bit shall be cleared to zero after power on or hardware reset. The counter shall be set to five after a power on or reset.

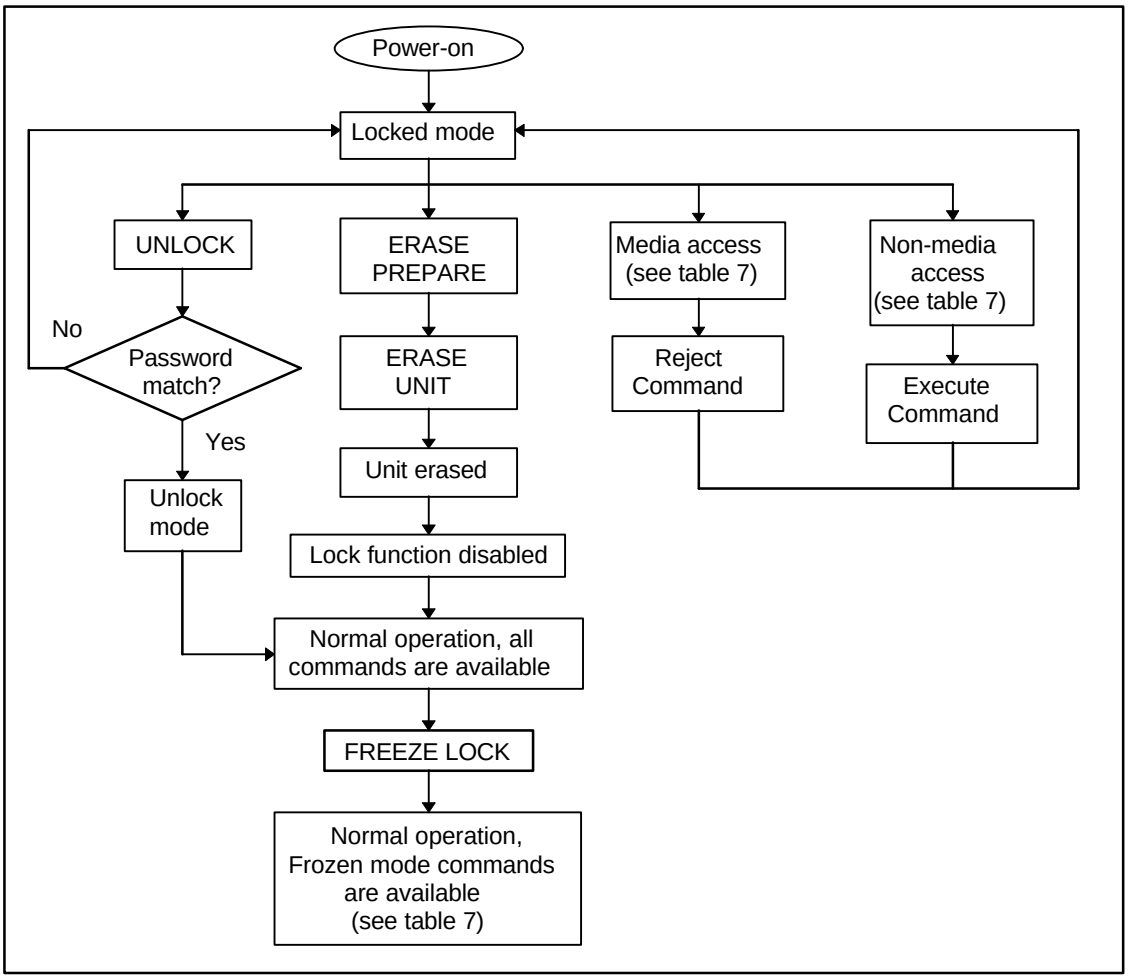


Figure 4 – Password set security mode power-on flow

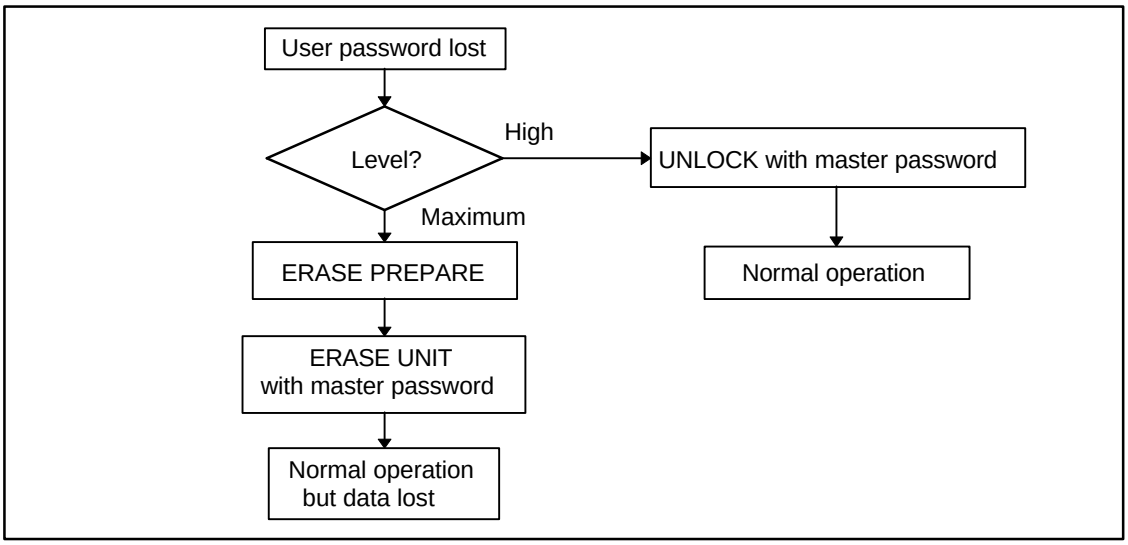


Figure 5 – User password lost

Table 7 – Security mode command actions

Command	Locked mode	Unlocked mode	Frozen mode
CHECK POWER MODE	Executable	Executable	Executable
DEVICE RESET	Executable	Executable	Executable
DOOR LOCK	Executable	Executable	Executable
DOOR UNLOCK	Executable	Executable	Executable
DOWNLOAD MICROCODE	Executable	Executable	Executable
EXECUTE DEVICE DIAGNOSTIC	Executable	Executable	Executable
FORMAT TRACK	Aborted	Executable	Executable
IDENTIFY DEVICE	Executable	Executable	Executable
IDENTIFY DEVICE DMA	Executable	Executable	Executable
IDENTIFY PACKET DEVICE	Executable	Executable	Executable
IDLE	Executable	Executable	Executable
IDLE IMMEDIATE	Executable	Executable	Executable
INITIALIZE DEVICE PARAMETERS	Executable	Executable	Executable
MEDIA EJECT	Executable	Executable	Executable
NOP	Executable	Executable	Executable
PACKET	Aborted	Executable	Executable
READ BUFFER	Executable	Executable	Executable
READ DMA	Aborted	Executable	Executable
READ LONG	Aborted	Executable	Executable
READ MULTIPLE	Aborted	Executable	Executable
READ NATIVE MAX ADDRESS	Executable	Executable	Executable
READ SECTORS	Aborted	Executable	Executable
READ VERIFY SECTORS	Aborted	Executable	Executable
RECALIBRATE	Executable	Executable	Executable
SECURITY DISABLE PASSWORD	Aborted	Executable	Aborted
SECURITY ERASE PREPARE	Executable	Executable	Executable
SECURITY ERASE UNIT	Executable	Executable	Aborted
SECURITY FREEZE LOCK	Aborted	Executable	Executable
SECURITY SET PASSWORD	Aborted	Executable	Aborted
SECURITY UNLOCK	Executable	Executable	Aborted
SEEK	Executable	Executable	Executable
SERVICE	Aborted	Executable	Executable
SET FEATURES	Executable	Executable	Executable
SET MAX ADDRESS	Executable	Executable	Executable
SET MULTIPLE MODE	Executable	Executable	Executable
SLEEP	Executable	Executable	Executable
SMART DISABLE OPERATIONS	Executable	Executable	Executable
SMART ENABLE/DISABLE AUTOSAVE	Executable	Executable	Executable
SMART ENABLE OPERATIONS	Executable	Executable	Executable
SMART READ THRESHOLDS	Executable	Executable	Executable
SMART READ VALUES	Executable	Executable	Executable
SMART RETURN STATUS	Executable	Executable	Executable
SMART SAVE VALUES	Executable	Executable	Executable
STANDBY	Executable	Executable	Executable
STANDBY IMMEDIATE	Executable	Executable	Executable
WRITE BUFFER	Executable	Executable	Executable
WRITE DMA	Aborted	Executable	Executable
WRITE LONG	Aborted	Executable	Executable
WRITE MULTIPLE	Aborted	Executable	Executable
WRITE SECTORS	Aborted	Executable	Executable
WRITE VERIFY	Aborted	Executable	Executable

6.10 Self-monitoring, analysis, and reporting technology feature set

The intent of self-monitoring, analysis, and reporting technology (the SMART feature set) is to protect user data and minimize the liklihood of unscheduled system downtime that may be caused by predictable degradation and/or fault of the device. By monitoring and storing critical performance and calibration parameters, SMART feature set devices attempt to predict the likelihood of near-term degradation or fault condition. Providing the host system the knowledge of a negative reliability condition, allows the host system to warn the user of the impending risk of a data loss and advise the user of appropriate action. Support of this feature set is indicated in bit 0 of word 82 of the IDENTIFY DEVICE response.

Devices that implement the PACKET Command feature set shall not implement the SMART feature set as described in this subclause. Devices that implement the PACKET Command feature set and SMART shall implement as defined by the command packet set implemented by the device.

6.10.1 Device SMART data structure

SMART feature set capability and status information for the device are stored in the device SMART data structure. The off-line data collection capability and status data stored herein may be useful to the host if the SMART EXECUTE OFF-LINE IMMEDIATE command is implemented (see clause 8.35.5).

6.10.2 On-line data collection

Collection of SMART data in an “on-line” mode shall have no impact on device performance. The SMART data which is collected or the methods by which data is collected in this mode may be different than those in the off-line data collection mode for any particular device and may vary from one device to another.

6.10.3 Off-line data collection

The device shall use its off-line mode for data collection routines that have an impact on performance if the device is required to respond to commands from the host while performing that data collection. This impact on performance may vary from device to device. The data which is collected or the methods by which the data is collected in this mode may be different than those in the on-line data collection mode for any particular device and may vary from one device to another.

6.10.4 Threshold exceeded condition

This condition occurs when the device’s SMART reliability status indicates an impending degrading or fault condition.

6.10.5 SMART feature set commands

These commands use a single command code and are differentiated from one another by the value placed in the Features register, see 8.35.

If the SMART feature set is implemented, the following commands shall be implemented.

- SMART DISABLE OPERATIONS
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATIONS
- SMART RETURN STATUS

If the SMART feature set is implemented, the following commands may be implemented.

- SMART EXECUTE OFF-LINE IMMEDIATE
- SMART READ DATA

6.10.6 SMART operation with power management modes

When used with a host that has implemented the Power Management feature set, it is recommended that a SMART enabled device should automatically save its accumulated SMART data upon receipt of an IDLE IMMEDIATE, STANDBY IMMEDIATE or SLEEP command or upon return to an Active or Idle mode from a Standby mode (see the SMART capability bits in the device SMART data structure in 8.35.5).

If a SMART feature set enabled device has been set to utilize its Standby timer, it is recommended that the device automatically save its accumulated SMART data prior to going from an Idle mode to the Standby mode or upon return to an Active or Idle mode from a Standby mode.

A device shall not execute any routine to automatically save its accumulated SMART data while the device is in a Standby or Sleep mode.

6.11 Host Protected Area feature set

A reserved area for data storage outside the normal operating system file system is required for several specialized applications. Systems may wish to store configuration data or save memory to the device in a location that the operating systems cannot change. The Host Protected Area feature set allows a portion of the device to be reserved for such an area when the device is initially configured. A device that implements the Host Protected Area feature set shall implement the following minimum set of commands:

a) READ NATIVE MAX ADDRESS
b) SET MAX ADDRESS

If the Host Protected Area feature set is supported, the device shall indicate so by setting bit 10 of word 82 of the IDENTIFY DEVICE response.

The READ NATIVE MAX ADDRESS command allows the host to determine the maximum native address space of the device even when a protected area has been allocated.

The SET MAX ADDRESS command allows the host to redefine the maximum address of the user accessable address space. That is, when the SET MAX ADDRESS command is issued with a maximum address less than the native maximum address, the device reduces the user accessable address space to the maximum set, providing a protected area above that maximum address. The SET MAX ADDRESS command shall be immediately preceded by a READ NATIVE MAX ADDRESS command. After the SET MAX ADDRESS command has been issued, the device shall report only the reduced user address space in response to an IDENTIFY DEVICE command in words 1, 54, 57, 58, 60, and 61. Any read or write command to an address above the maximum address set shall return an IDNF error for a bad parameter just would be for any address that exceeds the device capacity. A volatility bit in the Sector Count register allows the host to specify if the maximum address set is preserved over power-up or hard reset. If the SET MAX ADDRESS command is issued with a value that exceeds the native maximum address an Aborted command error shall be returned.

Typical use of these commands would be:

On Reset

a) BIOS receives control after a system reset;
b) BIOS issues a Read Native Max Address command to find the max capacity of the device;.
c) BIOS issues a Set Max Address command to the values returned by Read Native Max Address;
d) BIOS reads configuration data from the highest area on the disk;
e) BIOS issues a Read Native Max Address command followed by a Set Max Address command to reset the drive to the size of the file system.

On Save to Disk

a) BIOS receives control prior to shut down;
b) BIOS issues a Read Native Max Address command to find the max capacity of the device;
c) BIOS issues a Set Max Address command to the values returned by Read Native Max Address;
d) Memory is copied to the reserved area;
e) Shut down completes.

These commands are intended for use only by system BIOS or other low level boot time process. Using these commands outside BIOS controlled boot or shutdown may result in damage to file systems on the device.

6.11.1 Host protected area orphan sectors

Issueing a SET MAX ADDRESS command with an LBA value may create orphan sectors just as an INITIALIZE DEVICE PARAMETERS command may create such sectors (see 6.2 and B.3).If the SET MAX ADDRESS LBA value does not correspond to a cylinder boundary, orphan sectors are created. The device shall report the CHS boundary just below the requested LBA value in word 1. Sectors above this cylinder boundary are orphan sectors and the device may or may not allow access to them in CHS translation.

7 Interface register definitions and descriptions

7.1 Device addressing considerations

In traditional controller operation, only the selected device receives commands from the host following selection. In this standard, the register contents go to both devices (and their embedded controllers). The host discriminates between the two by using the DEV bit in the Device/Head register.

Data is transferred in parallel either to or from host memory to the device's buffer under the direction of commands previously transferred from the host. The device performs all of the operations necessary to properly write data to, or read data from, the media. Data read from the media is stored in the device's buffer pending transfer to the host memory and data is transferred from the host memory to the device's buffer to be written to the media.

The devices using this interface shall be programmed by the host computer to perform commands and return status to the host at command completion. When two devices are daisychained on the interface, commands are written in parallel to both devices, and for all except the EXECUTE DEVICE DIAGNOSTIC command, only the selected device executes the command. On an EXECUTE DEVICE DIAGNOSTIC command addressed to Device 0, both devices shall execute the command, and Device 1 shall post its status to Device 0 via PDIAG-.

Devices are selected by the DEV bit in the Device/Head register. see 7.2.8. When the DEV bit is equal to zero, Device 0 is selected. When the DEV bit is equal to one, Device 1 is selected. When devices are daisy chained, one shall be set as Device 0 and the other as Device 1.

For register access protocols and timing see clauses 9 and 10.

7.2 I/O register descriptions

Communication to or from the device is through an I/O Register that routes the input or output data to or from registers addressed by the signals from the host (CS0-, CS1-, DA (2:0), DIOR- and DIOW-). CS0- and CS1- both asserted or negated is an invalid (not used) address except when both are negated during a DMA data transfer. When CS0- and CS1- are both asserted or both negated and a DMA transfer is not in progress, the device shall hold DD (15:00) in the high impedance state and ignore DIOR- and DIOW-. When CS0- is negated and CS1- is asserted only DA (2:0) with a value of 6h is valid. The device shall hold DD (15:00) in the high impedance state and ignore DIOR- and DIOW- when this occurs. All valid register addresses are described in the clause defining the register.

The Command Block Registers are used for sending commands to the device or posting status from the device. The Control Block Registers are used for device control and to post alternate status.

Each register description in the following clauses contain the following format:

ADDRESS - the CS and DA address of the register.

DIRECTION - indicates if the register is read/write, read only, or write only from the host.

ACCESS RESTRICTIONS - indicates when the register may be accessed.

EFFECT - indicates the effect of accessing the register.

FUNCTIONAL DESCRIPTION - describes the function of the register.

FIELD/BIT DESCRIPTION - describes the content of the register.

7.2.1 Alternate Status register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
N	A	A	A	N
A = asserted, N = negated				

DIRECTION - This register is read only. If this address is written to by the host, the Device Control register is written.

ACCESS RESTRICTIONS - When the BSY bit is set to one, the other bits in this register shall not be used. The entire contents of this register are not valid while the device is in Sleep mode.

EFFECT - Reading this register shall not perform an interrupt acknowledge or clear a pending interrupt.

FUNCTIONAL DESCRIPTION - This register contains the same information as the Status register in the command block.

See 7.2.13 for definitions of the bits in this register.

7.2.2 Command register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	A	A	A
A = asserted, N = negated				

DIRECTION - This register is write only. If this address is read by the host, the Status register is read.

ACCESS RESTRICTIONS - For all commands except DEVICE RESET, this register shall only be written when BSY and DRQ are both equal to zero and DMACK- is not asserted. The contents of the this register is not valid while a device is in the Sleep mode.

EFFECT - Command processing begins when this register is written. The content of the Command Block registers become parameters of the command when this register is written. Writing this register clears any pending interrupt condition.

FUNCTIONAL DESCRIPTION - This register contains the command code being sent to the device. Command execution begins immediately after this register is written. The executable commands, the command codes, and the necessary parameters for each command are summarized in0 tables E.3 and E.4.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
Command Code							

7.2.3 Cylinder High register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	A	N	A
A = asserted, N = negated				

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted. The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register are not valid while a device is in the Sleep mode.

EFFECT - The content of this register becomes a command parameter when the Command register is written.

FUNCTIONAL DESCRIPTION - The content of this register is command dependent. See clause0 0.

7.2.4 Cylinder Low register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	A	N	N
A = asserted, N = negated				

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted. The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register are not valid while a device is in the Sleep mode.

EFFECT - The content of this register becomes a command parameter when the Command register is written.

FUNCTIONAL DESCRIPTION - The content of this register is command dependent. See clause0 0.

7.2.5 Data register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	N	N	N
A = asserted, N = negated				

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be accessed for host PIO data only when DRQ is cleared to zero and DMACK- is not asserted. The contents of the this register are not valid while a device is in the Sleep mode.

EFFECT - PIO out data transfers are processed by a series of reads to this register, each read transferring the data that follows the previous read. PIO in data transfers are processed by a series of writes to this

register, each write transferring the data that follows the previous write. The results of a read during a PIO in or a write during a PIO out are indeterminant.

FUNCTIONAL DESCRIPTION - The data register is 16-bits wide.

FIELD/BIT DESCRIPTION -

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

7.2.6 Data port

ADDRESS - When DMACK- is asserted, CS0- and CS1- shall be negated and transfers shall be 16-bits wide.

CS1	CS0	DA2	DA1	DA0
N	N	X	X	X
A = asserted, N = negated, X = don't care				

DIRECTION - This port is read/write.

ACCESS RESTRICTIONS - This port shall be accessed for host DMA data transfers only when DMACK- and DMARQ are asserted.

EFFECT - DMA out data transfers are processed by a series of reads to this port, each read transferring the data that follows the previous read. DMA in data transfers are processed by a series of writes to this port, each write transferring the data that follows the previous write. The results of a read during a DMA in or a write during a DMA out are indeterminant.

FUNCTIONAL DESCRIPTION - The data port is 16-bits in width.

FIELD/BIT DESCRIPTION -

15	14	13	12	11	10	9	8
Data(15:8)							

7	6	5	4	3	2	1	0
Data(7:0)							

7.2.7 Device Control register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
N	A	A	A	N
A = asserted, N = negated				

DIRECTION - This register is write only. If this address is read by the host, the Alternate Status register is read.

ACCESS RESTRICTIONS - This register shall only be written when DMACK- is not asserted.

EFFECTIVENESS - the content of this register shall take effect when written.

FUNCTIONAL DESCRIPTION - This register allows a host to software reset attached devices and enable/disable interrupts.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
r	r	r	r	r	SRST	nIEN	0

- Bits 7 through 3 are reserved;
- SRST is the host software reset bit. See 9.3;
- nIEN is the enable bit for the device interrupt to the host. When the nIEN bit is cleared to zero, and the device is selected, INTRQ shall be enabled through a tri-state buffer. When the nIEN bit is set to one, or the device is not selected, the INTRQ signal shall be in a high impedance state;
- Bit 0 shall be cleared to zero.

7.2.8 Device/Head register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	A	A	N
A = asserted, N = negated				

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are cleared to zero and DMACK- is not asserted. The contents of this register are valid only when BSY is cleared to zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register are not valid while a device is in the Sleep mode.

EFFECT - The DEV bit becomes effective when this register is written by the host or the signature is set by the device. All other bits in this register become a command parameter when the Command register is written.

FUNCTIONAL DESCRIPTION - Bit 4, DEV, in this register selects the device. Other bits in this register are command dependent, see clause 0.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
r			DEV				

- DEV - Device select. Cleared to zero selects Device 0. Set to one selects Device 1.

7.2.9 Error register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	N	N	A
A = asserted, N = negated				

DIRECTION - This register is read only. If this address is written to, the Features register is written.

ACCESS RESTRICTIONS - The contents of this register shall be valid when BSY and DRQ equal zero and ERR equals one. The contents of this register shall be valid upon completion of power on or after a reset. The contents of the this register are not valid while a device is in the Sleep mode.

EFFECT - None.

FUNCTIONAL DESCRIPTION - This register contains status for the current command.

Following a power on, a reset, or completion of an EXECUTE DEVICE DIAGNOSTIC or DEVICE RESET command, this register contains a diagnostic code, see 8.4.

At the completion of any command except EXECUTE DEVICE DIAGNOSTIC, the contents of this register are valid when the ERR bit is equal to one in the Status register.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
#	#	MC	#	MCR	ABRT	#	#

- Bit 5 - MC (Media changed) is used by removable media devices and is set to one to indicate that new media is available to the operating system.
- Bit 3 - MCR (Media change requested) is used by removable media devices and is set to one to indicate that a request for media removal has been detected by the device.
- Bit 2 - ABRT (Aborted command) is set to one to indicate the requested command has been aborted because the command code or a command parameter is invalid or some other error has occurred.
- # -The content of this bit is command dependent, see clause 8.

7.2.10 Features register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	N	N	A
A = asserted, N = negated				

DIRECTION - This register is write only. If this address is read by the host, the Error register is read.

ACCESS RESTRICTIONS - This register shall be written only when BSY and DRQ equal zero and DMACK- is not asserted. If this register is written when BSY or DRQ is set to one, the result is indeterminant.

EFFECT - The content of this register becomes a command parameter when the Command register is written.

FUNCTIONAL DESCRIPTION - The content of this register is command dependent, see clause 8.

7.2.11 Sector Count register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	N	A	N
A = asserted, N = negated				

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register are not valid while a device is in the Sleep mode.

EFFECT - The content of this register becomes a command parameter when the Command register is written.

FUNCTIONAL DESCRIPTION - The content of this register is command dependent, see clause 8.

7.2.12 Sector Number register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	N	A	A
A = asserted, N = negated				

DIRECTION - This register is read/write.

ACCESS RESTRICTIONS - This register shall be written only when both BSY and DRQ are zero and DMACK- is not asserted. The contents of this register are valid only when both BSY and DRQ are zero. If this register is written when BSY or DRQ is set to one, the result is indeterminant. The contents of the this register are not valid while a device is in the Sleep mode.

EFFECT - The content of this register becomes a command parameter when the Command register is written.

FUNCTIONAL DESCRIPTION - The content of this register is command dependent, see clause 8.

7.2.13 Status register

ADDRESS -

CS1	CS0	DA2	DA1	DA0
A	N	A	A	A
A = asserted, N = negated				

DIRECTION - This register is read only. If this address is written to by the host, the Command register is written.

ACCESS RESTRICTIONS - The contents of this register, except for BSY, shall be ignored when BSY is set equal to one. BSY is valid at all times. The contents of this register are not valid while a device is in the Sleep mode.

EFFECT - Reading this register when an interrupt is pending causes the interrupt to be cleared, see 5.2.9.

FUNCTIONAL DESCRIPTION - This register contains the device status. The contents of this register are updated to reflect the current state of the device and the progress of any command being executed by the device.

FIELD/BIT DESCRIPTION -

7	6	5	4	3	2	1	0
BSY	DRDY	#	#	DRQ	CORR	#	ERR

– BSY (Busy) is set to one to indicate that the device is busy. After the host has written the Command register either the BSY bit shall be set to one, or if the BSY bit is cleared to zero, the DRQ bit shall be set to one, until command completion or the bus is released for an overlapped command.

The BSY bit shall be set to one by the device under the following circumstances:

a) after either the negation of RESET- or the setting of the SRST bit to one in the Device Control register;
b) after writing the Command register if the DRQ bit is not set to one;
c) between blocks of a data transfer during PIO data in commands if the DRQ bit is not set to one;
d) after the transfer of a data block during PIO data out commands if the DRQ bit is not set to one;
e) during the data transfer of DMA commands if the DRQ bit is not set to one.

NOTE – The BSY bit is set to one and then cleared to zero so quickly, that host detection of the BSY bit being set to one is not certain.

When BSY is set to one, the device has control of the Command Block Registers:

a) A write to a Command Block register by the host shall be ignored by the device except for writing DEVICE RESET command;
b) A read from a Command Block register by the host will most likely yield invalid contents except for the BSY bit itself.

The BSY bit shall be cleared to zero by the device under the following circumstances:

a) after setting DRQ to one to indicate the device is ready to transfer data;
b) after completion of a command;
c) upon releasing the bus for an overlapped command;
d) when the device is ready to accept commands that do not require DRDY during a power-on, hardware or software reset.

When BSY is cleared to zero, the host has control of the Command Block registers:

a) The device shall not set DRQ to one;
b) The device shall not change ERR bit;
c) The device shall only set BSY to one as described below;
d) The device shall not change the content of any other Command Block register.

NOTE – BIOSs and software device drivers that sample status as soon as the BSY bit is cleared to zero may not detect the assertion of the CORR bit by the device.

– DRDY (Device Ready) indicates the device ready to accept all commands.

The DRDY bit shall be cleared to zero under the following circumstances:

a) at power on;
b) when the SRST bit is asserted.

When the DRDY bit is cleared to zero, the device shall accept and attempt to execute only:

a) the PACKET command;
b) the SERVICE command;

c) the EXECUTE DEVICE DIAGNOSTIC command;
d) the DEVICE RESET command;
e) the INITIALIZE DEVICE PARAMETERS command.

The DRDY bit shall be set to one under the following circumstances. When the state of the DRDY bit changes, it shall not change again until after the host reads the Status register.

a) when the device is capable of accepting all commands.

When the DRDY bit is set to one, the device shall accept and attempt to execute:

a) all commands;
b) devices that implement the Power Management feature set shall maintain the DRDY bit equal to one when they are in the Idle or Standby modes.

– DRQ (Data Request) indicates that the device is ready to transfer a word of data between the host and the device. After the host has written the Command register either the BSY bit shall be set to one, or if the BSY bit is cleared to zero, the DRQ bit shall be set to one, until command completion or the bus is released for an overlapped command.

The DRQ bit shall be set to one under the following circumstances:

a) when BSY is set to one and data is ready for PIO transfer;
b) when BSY is set to one, data is ready for DMA transfer, and BSY is not to be cleared to zero.

When the DRQ bit is set to one, the host may:

a) transfer data via PIO mode;
b) transfer data via DMA mode if DMARQ and DMACK- are asserted.

The DRQ bit shall be cleared to zero under the following circumstances:

a) when the last word of the data transfer occurs.

When the DRQ bit is cleared to one, the host may:

a) transfer data via DMA mode if DMARQ and DMACK- are asserted and BSY is set to one.

– CORR Obsolete.

– ERR (Error) indicates that an error occurred during execution of the previous command. For the PACKET and SERVICE commands, this bit is defined as CHK and indicates that an exception conditions exists.

The ERR bit shall be set to one under the following circumstances:

a) when BSY or DRQ is set to one and an error occurs in the executing command.

When the ERR bit is set to one:

a) the bits in the Error register have additional information regarding the cause of the error;
b) the device shall not change the contents of the following registers until a new command has been accepted, the SRST bit is set to one or RESET- is asserted:
   – Error register;
   – Cylinder High register;
   – Cylinder Low register;
   – Sector Count register;
   – Sector Number register;
   – Device/Head register.

The ERR bit shall be cleared to zero, under the following circumstances:

a) when a new command is written to the Command register;
b) when the SRST bit is set to one;
c) when the RESET- signal is asserted.

When the ERR bit is cleared to zero:

a) the content of the Erreo register shall be ignored by the host.

– # - the content of this bit is command dependent (see clause 8).

8 Command descriptions

Commands are issued to the device by loading the pertinent registers in the command block with the needed parameters, and then writing the command code to the Command register.

Each command description in the following clauses contains the following subclauses:

Command code - Indicates the command code for this command.

Feature set - Indicates Feature set and if the command is:

- Mandatory - Required to be implemented by devices as specified.
- Optional - Implementation is optional but if implemented shall be implemented as specified.

Protocol - Indicates which protocol is used by the command (see clause 9).

Inputs - Describes the Command Block register data that the host shall supply.

Register	7	6	5	4	3	2	1	0
Features								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Command	Command Code							
NOTE – na indicates the content of a bit or field is not applicable to the particular command.								

Normal outputs - Describes the Command Block register data returned by the device at the end of a command.

Register	7	6	5	4	3	2	1	0
Error								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Status								
NOTE – na indicates the content of a bit or field is not applicable to the particular command.								

Error outputs - Describes the Command Block register data that shall be returned by the device at the end of a command which completes with an unrecoverable error.

Register	7	6	5	4	3	2	1	0
Error								
Sector Count								
Sector Number								
Cylinder Low								
Cylinder High								
Device/Head								
Status								
NOTE – na indicates the content of a bit or field is not applicable to the particular command.								

Prerequisites - Any prerequisite commands or conditions that shall be met before the command is issued.

Description - The description of the command function(s).

8.1 CHECK POWER MODE

8.1.1 Command code

E5h

8.1.2 Feature set

Power Management feature set.

- Power Management feature is mandatory if power management is not provided by a PACKET feature set command set.
- Mandatory if the Power Management feature set is implemented.

8.1.2 Protocol

Non-data command, see 9.8.

8.1.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E5h							

8.1.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Result value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

Sector Count result value

00h - device is in Standby mode
80h - device is in Idle mode
FFh - device is in Active mode or Idle mode

8.1.5 Error outputs

Aborted command if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register - ABRT shall be set to one if Power Management feature set not supported.
Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.1.6 Prerequisites

DRDY set equal to one.

8.1.7 Description

The CHECK POWER MODE command allows the host to determine the current power mode of the device. The CHECK POWER MODE command shall not cause the device to change power modes.

8.2 DEVICE RESET

8.2.1 Command code

08h

8.2.2 Feature set

General feature set
- Use prohibited if the PACKET Command feature set or Overlap/queuing feature set are not implemented.
- Mandatory if the PACKET Command feature set is implemented.
- Mandatory if the Overlap or Queued feature set is implemented.

8.2.2 Protocol

Device reset (see 9.4).

8.2.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	08h							

8.2.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	Diagnostic results							
Sector Count	signature							
Sector Number	signature							
Cylinder Low	signature							
Cylinder High	signature							
Device/Head	0	0	0	DEV	0	0	0	0
Status	see 9.4							

Error register - The diagnostic code as described in 8.4 is placed in this register.
Sector Count, Sector Number, Cylinder low, Cylinder High - Signature (see 9.1).
Status register - see 9.4.

8.2.5 Error outputs

If supported, this command cannot end in an error condition. If not supported, the results of this command are indeterminant if the device has BSY set to one when the DEVICE RESET command is written and the device posts an Aborted command error if the device has BSY cleared to zero when the DEVICE RESET command is written.

8.2.6 Prerequisites

In particular, this command shall be accepted when BSY or DRQ is set to one, DRDY is cleared to zero, or DMARQ is asserted. This command shall be accepted when in Sleep mode.

8.2.7 Description

The DEVICE RESET command enables the host to reset an individual device without affecting the other device.

8.3 DOWNLOAD MICROCODE

8.3.1 Command code

92h

8.3.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.3.2 Protocol

PIO data out, see 9.7.

8.3.3 Inputs

The head bits of the Device/Head register shall always be cleared to zero. The Cylinder High and Low registers shall be cleared to zero. The Sector Number and Sector Count registers are used together as a 16-bit sector count value. The Feature register specifies the subcommand code.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Sector count (low order)							
Sector Number	Sector count (high order)							
Cylinder Low	00h							
Cylinder High	00h							
Device/Head	1	na	1	DEV	0	0	0	0
Command	92h							

8.3.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one

ERR shall be cleared to zero

8.3.5 Error outputs

Aborted command if the device does not support this command or did not accept the microcode data. Aborted command if subcommand code is not a supported value.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register - ABRT shall be set to one if the device does not support this command or did not accept the microcode data.
Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.3.6 Prerequisites

DRDY set equal to one.

8.3.7 Description

This command enables the host to alter the device's microcode. The data transferred using the DOWNLOAD MICROCODE command is vendor specific.

All transfers shall be an integer multiple of the sector size. The size of the data transfer is determined by the contents of the Sector Number Register and the Sector Count register. The Sector Number Register shall be used to extend the Sector Count register to create a sixteen bit sector count value. The Sector Number Register shall be the most significant eight bits and the Sector Count register shall be the least significant eight bits. A value of zero in both the Sector Number Register and the Sector Count register shall indicate no data is to be transferred. This allows transfer sizes from 0 bytes to 33,553,920 bytes, in 512 byte increments.

The Features register shall be used to determine the effect of the DOWNLOAD MICROCODE command. The values for the Feature Register are:

- 01h - download is for immediate, temporary use
- 07h - save downloaded code for immediate and future use

Either or both values may be supported. All other values are reserved.

8.4 EXECUTE DEVICE DIAGNOSTIC

8.4.1 Command code

90h

8.4.2 Feature set

General feature set
- Mandatory for all devices.

8.4.2 Protocol

Device diagnostics (see 9.5).

8.4.3 Inputs

None. The device selection bit in the Device/Head register is ignored.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	na	na	na	na	na
Command	90h							

8.4.4 Normal outputs

The diagnostic code written into the Error register is an 8-bit code. Table 8 defines these values. The values are not as defined in 7.2.9.

Register	7	6	5	4	3	2	1	0
Error	Diagnostic code							
Sector Count	Signature							
Sector Number	Signature							
Cylinder Low	Signature							
Cylinder High	Signature							
Device/Head	Signature							
Status	see 9.5							

Error register - Diagnostic code.
Sector Count, Sector number, Cylinder Low, Cylinder High, Device/Head registers - device signature, see 9.1.
Status register - see 9.5.

Table 8 – Diagnostic codes

Code	Description
When this code is in the Device 0 Error register	
01h	Device 0 passed, Device 1 passed or not present
00h, 02h-7Fh	Device 0 failed, Device 1 passed or not present
81h	Device 0 passed, Device 1 failed
80h, 82h-FFh	Device 0 failed, Device 1 failed
When this code is in the Device 1 Error register	
01h	Device 1 passed
00h,02h-7Fh	Device 1 failed
NOTE – Codes other than 01h and 81h may indicate additional information about the failure(s).	

8.4.5 Error outputs

Error information is returned as a diagnostic code in the Error register, see Table 8.

8.4.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

8.4.7 Description

This command shall perform the internal diagnostic tests implemented by the device. See also 7.2.9 and 7.2.13. The DEV bit in the Device/Head register is ignored. Both devices, if present, shall execute this command regardless of which device is selected.

If the host issues an EXECUTE DEVICE DIAGNOSTIC command while a device is in or going to a power management mode except Sleep, then the device shall execute its EXECUTE DEVICE DIAGNOSTIC sequence.

8.5 FLUSH CACHE

8.5.1 Command code

E7h

8.5.2 Feature set

General feature set

- Optional for all devices.

8.5.2 Protocol

Non-data command, see 9.8.

8.5.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E7h							

8.5.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.5.5 Error outputs

If the command is not supported, the device posts an Aborted command error. An unrecoverable error encountered during execution of writing data results in the termination of the command and the Command Block registers contain the sector address of the sector where the first unrecoverable error occurred. The sector is removed from the cache. Subsequent FLUSH CACHE commands continue the process of flushing the cache.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register - ABRT shall be set to one if device does not support this command.
Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of the first unrecoverable error.
Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.5.6 Prerequisites

DRDY set equal to one.

8.5.7 Description

This command is used by the host to request the device to flush the write cache. If the write cache is to be flushed, all data cached shall be written to the media. The BSY bit shall remain set to one until all data has been successfully written or an error occurs. The device should use all error recovery methods available to ensure the data is written successfully. The flushing of write cache may take several seconds to complete depending upon the amount of data to be flushed and the success of the operation.

NOTE – This command may take longer than 30 s to complete.

8.6 IDENTIFY DEVICE

8.6.1 Command code

ECh

8.6.2 Feature set

General feature set

- Mandatory for all devices.
- Devices implementing the PACKET Command feature set see 8.6.4.2.

8.6.2 Protocol

PIO data in, see 9.6.

8.6.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	ECh							

8.6.4 Outputs

8.6.4.1 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.6.4.2 Outputs for PACKET Command feature set devices

In response to this command, devices that implement the PACKET Command feature set shall post an Aborted command error and place the PACKET Command feature set signature in the Command Block registers (see 9.1).

8.6.5 Error outputs

Devices not implementing the PACKET Command feature set shall not report an error.

8.6.6 Prerequisites

DRDY set equal to one.

8.6.7 Description

The IDENTIFY DEVICE command enables the host to receive parameter information from the device.

Some devices may have to read the media in order to complete this command.

When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and generates an

interrupt. The host may then transfer the data by reading the Data register. Table 9 defines the arrangement and meaning of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a sixteen bit value. A word which is defined as a sixteen bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.

Some parameters are defined as 32 bit values (e.g., words 57 and 58). Such fields are transferred using two successive word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD (15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD (15:0) respectively.

Some parameters are defined as a string of ASCII characters. ASCII data fields shall contain only graphic codes (i.e., code values 20h through 7Eh). For the string “Copyright”, the character “C” is the first byte, the character “o” is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character (“C”) is on bits DD (15:8) of the first word
the 2nd character (“o”) is on bits DD (7:0) of the first word
the 3rd character (“p”) is on bits DD (15:8) of the second word
the 4th character (“y”) is on bits DD (7:0) of the second word
etc.

Table 9 – Identify device information

Word	F/V	
0		General configuration bit-significant information:
	F	15 0=ATA device
	F	14-8 retired
	F	7 1=removable media device
	F	6 1=not removable controller and/or device
	F	5-1 retired
	F	0 Reserved
1	F	Number of logical cylinders
2	R	Reserved
3	F	Number of logical heads
4-5	X	retired
6	F	Number of logical sectors per logical track
7-9	X	retired
10-19	F	Serial number (20 ASCII characters)
20-21	X	retired
22	F	obsolete
23-26	F	Firmware revision (8 ASCII characters)
27-46	F	Model number (40 ASCII characters)
47	X	15-8 80h
	R	7-0 00h =Reserved
	F	01h-FFh = Maximum number of sectors that shall be transferred per interrupt on READ/WRITE MULTIPLE commands
48	R	Reserved
49		Capabilities
	R	15-14 Reserved for the IDENTIFY PACKET DEVICE command.
	F	13 1=Standby timer values as specified in this standard are supported
		0=Standby timer values shall be managed by the device
	R	12 Reserved for the IDENTIFY PACKET DEVICE command.
	F	11 1=IORDY supported
		0=IORDY may be supported
	F	10 1=IORDY may be disabled
	R	9 Shall be set to one. Utilized by IDENTIFY PACKET DEVICE command.
	R	8 Shall be set to one. Utilized by IDENTIFY PACKET DEVICE command.
	X	7-0 retired
50	R	Reserved
51	F	15-8 PIO data transfer cycle timing mode
	X	7-0 retired
52	R	retired
53	R	15-3 Reserved
	F	2 1=the fields reported in word 88 are valid
		0=the fields reported in word 88 are not valid
	F	1 1=the fields reported in words 64-70 are valid
	F	0=the fields reported in words 64-70 are not valid
	V	0 1=the fields reported in words 54-58 are valid
	V	0=the fields reported in words 54-58 may be valid

(continued)

Table 9 – Identify device information *(continued)*

Word	F/V	
54	V	Number of current logical cylinders
55	V	Number of current logical heads
56	V	Number of current logical sectors per track
57-58	V	Current capacity in sectors
59	R V V	15-9 Reserved 8 1=Multiple sector setting is valid 7-0 xxh=Current setting for number of sectors that shall be transferred per interrupt on R/W Multiple command
60-61	F	Total number of user addressable sectors (LBA mode only)
62	R	retired
63	V F	15-8 Multiword DMA mode selected 7-0 Multiword DMA modes supported
64	R F	15-8 Reserved 7-0 Advanced PIO modes supported
65	 F	Minimum Multiword DMA transfer cycle time per word 15-0 Cycle time in nanoseconds
66	 F	Manufacturer's recommended Multiword DMA transfer cycle time 15-0 Cycle time in nanoseconds
67	 F	Minimum PIO transfer cycle time without flow control 15-0 Cycle time in nanoseconds
68	 F	Minimum PIO transfer cycle time with IORDY flow control 15-0 Cycle time in nanoseconds
69-72	R	Reserved (for future command overlap and queuing)
73	F	Queue depth 15-5 Reserved 4-0 Maximum queue depth
74-79	R	Reserved
80	F	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 Reserved for ATA/ATAPI-7 6 Reserved for ATA/ATAPI-6 5 Reserved for ATA/ATAPI-5 4 1=supports ATA/ATAPI-4 3 1=supports ATA-3 2 1=supports ATA-2 1 1=supports ATA-1
81	F	Minor version number 0000h or FFFFh=device does not report version 0001h-FFFEh=see 8.6.44

(continued)

Table 9 – Identify device information *(continued)*

Word	F/V	
82	F	Command set supported. If words 82 and 83 =0000h or FFFFh command set notification not supported. 15 1=IDENTIFY DEVICE DMA command supported 14 1=NOP command supported 13 1=READ BUFFER command supported 12 1=WRITE BUFFER command supported 11 1=WRITE VERIFY command supported 10 1=Host Protected Area feature set supported 9 1=DEVICE RESET command supported 8 1=SERVICE interrupt supported 7 1=release interrupt supported 6 1=look-ahead supported 5 1=write cache supported 4 1=supports PACKET Command feature set 3 1=supports Power Management feature set 2 1=supports Removable Media feature set 1 1=supports Security Mode feature set 0 1=supports SMART feature set
83	F	Command sets supported. If words 82 and 83 =0000h or FFFFh command set notification not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-2 Reserved 1 1=READ/WRITE DMA QUEUED supported 0 1=DOWNLOAD MICROCODE command supported
84	F	Command set/feature supported extension. If words 82, 83, and 84 = 0000h or FFFFh command set notification extension is not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-0 Reserved
85	V	Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported. 15 1=IDENTIFY DEVICE DMA command supported 14 1=NOP command supported 13 1=READ BUFFER command supported 12 1=WRITE BUFFER command supported 11 1=WRITE VERIFY command supported 10 1=Host Protected Area feature set supported 9 1=DEVICE RESET command supported 8 1=SERVICE interrupt enabled 7 1=release interrupt enabled 6 1=look-ahead enabled 5 1=write cache enabled 4 1=supports PACKET Command feature set 3 1=supports Power Management feature set 2 1=supports Removable Media feature set 1 1= Security Mode feature set enabled 0 1= SMART feature set enabled

Table 9 – Identify device information *(concluded)*

Word	F/V	
86	V	Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported. 15-2 Reserved 1 1=READ/WRITE DMA QUEUED command supported 0 1=DOWNLOAD MICROCODE command supported
87	V	Command set/feature default. If words 85, 86, and 87 = 0000h or FFFFh command set default notification is not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-0 Reserved
88	R V V V R F F F	15-11 Reserved 10 1=Ultra DMA mode 2 is selected 0=Ultra DMA mode 2 is not selected 9 1=Ultra DMA mode 1 is selected 0=Ultra DMA mode 1 is not selected 8 1=Ultra DMA mode 0 is selected 0=Ultra DMA mode 0 is not selected 7-3 Reserved 2 1=Ultra DMA mode 2 and below are supported 0=Ultra DMA mode 2 is not supported 1 1=Ultra DMA mode 1 and below are supported 0=Ultra DMA mode 1 is not supported 0 1=Ultra DMA mode 0 is supported 0=Ultra DMA is not supported
89	F	Time required for security erase unit completion
90	F	Time required for Enhanced security erase completion
91-127	R	Reserved
128	V	Security status 15-9 Reserved 8 Security level 0=High, 1=Maximum 7-6 Reserved 5 1=Enhanced security erase supported 4 1=Security count expired 3 1=Security frozen 2 1=Security locked 1 1=Security enabled 0 1=Security supported
129-159	X	Vendor specific
160-255	R	Reserved

Key:
F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the word is vendor specific and may be fixed or variable.
R = the content of the word is reserved and shall be zero.

8.6.8 Word 0: General configuration

Devices that conform to this standard shall clear bit 15 to zero.

8.6.9 Word 1: Number of cylinders

The number of user-addressable logical cylinders in the default translation. If the value in Words 60 and 61 exceed 16,515,072, this word shall contain 16,383 (see 6.2).

8.6.10 Word 2: Reserved.

8.6.11 Word 3: Number of logical heads

The number of user-addressable logical heads per logical cylinder in the default translation. If the value in Words 60 and 61 exceeds 16,515,072, this word shall contain the value 16 or less (see 6.2).

8.6.12 Word 4-5: Retired.

8.6.13 Word 6: Number of logical sectors per logical track

The number of user-addressable logical sectors per logical track in the default translation. If the value in Words 60 and 61 exceeds 16,515,072, this word shall contain 63 (see 6.2).

8.6.14 Words 7-9: Retired.

8.6.15 Words 10-19: Serial number

This field contains the serial number of the device. The contents of this field is an ASCII character string of twenty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (Words 10-19) and Model number (Words 27-46) shall be unique for a given manufacturer..

8.6.16 Word 20-21: Retired.

8.6.17 Word 22: Obsolete.

8.6.18 Word 23-26: Firmware revision

This field contains the firmware revision number of the device. The contents of this field is an ASCII character string of eight bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length.

8.6.19 Words 27-46: Model number

This field contains the model number of the device. The contents of this field is an ASCII character string of forty bytes. The device shall pad the character string with spaces (20h), if necessary, to ensure that the string is the proper length. The combination of Serial number (Words 10-19) and Model number (Words 27-46) shall be unique for a given manufacturer.

8.6.20 Word 47: READ/WRITE MULTIPLE support.

Bits 7-0 of this word define the maximum number of sectors per block that the device supports for READ/WRITE MULTIPLE commands.

8.6.21 Word 48: Reserved.

8.6.22 Word 49: Capabilities

Bits 15 and 14 of word 49 are reserved for use in the IDENTIFY PACKET DEVICE command response.

Bit 13 of word 49 is used to determine whether a device utilizes the Standby timer values as defined in this standard. Table 12 specifies the Standby timer values utilized by the device if bit 13 is set to one. If bit 13 is cleared to zero, the timer values shall be vendor specific.

Bit 12 of word 49 is reserved for use in the IDENTIFY PACKET DEVICE command response.

Bit 11 of word 49 is used to determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This ensures backward compatibility. If a device supports PIO Mode 3 or higher, then this bit shall be set to one.

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Disabling and enabling of IORDY is accomplished using the SET FEATURES command.

Bits 9 and 8 of word 49 shall be set to one for backward compatibility. These bits are defined for use in the IDENTIFY PACKET DEVICE command response.

8.6.23 Word 50: Reserved

8.6.24 Word 51: PIO data transfer cycle timing mode

The PIO transfer timing for each device falls into categories which have unique parametric timing specifications. To determine the proper device timing category, compare the cycle time specified in 10.2.2 with the contents of this field. The value returned in Bits 15-8 should fall into one of the mode 0 through mode 2 categories specified in 10.2.2, and if it does not, then Mode 0 shall be used to serve as the default timing.

> NOTE – For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the time corresponding with the highest original PIO mode (i.e., PIO Mode 0, 1, or 2) it supports.

8.6.25 Word 52: Retired

8.6.26 Word 53: Field validity

If bit 0 of word 53 is set to one, the values reported in words 54 through 58 are valid. If this bit is cleared to zero, the values reported in words 54 through 58 may be valid. If bit 1 of word 53 is set to one, the values reported in words 64 through 70 are valid. If this bit is cleared to zero, the values reported in words 64-70 are not valid. Any device which supports PIO Mode 3 or above, or supports Multiword DMA Mode 1 or above, shall set bit 1 of word 53 to one and support the fields contained in words 64 through 70. If the device supports Ultra DMA and the values reported in word 88 are valid, then bit 2 of word 53 shall be set to one. If the device does not support Ultra DMA and the values reported in word 88 are not valid, then this bit is cleared to zero.

8.6.27 Word 54: Number of current logical cylinders

The number of user-addressable logical cylinders in the current translation.

8.6.28 Word 55: Number of current logical heads

The number of user-addressable logical heads per logical cylinder in the current translation.

8.6.29 Word 56: Number of current logical sectors per logical track

The number of user-addressable logical sectors per logical track in the current translation.

8.6.30 Word 57-58: Current capacity in sectors

The current capacity in sectors excludes all sectors used for device-specific purposes. The value reported in this field shall be the product of words 54, 55 and 56.

8.6.31 Word 59: Multiple sector setting

If bit 8 is set to one, bits 7-0 reflect the number of sectors currently set to transfer on a READ/WRITE MULTIPLE command. If word 47 bits 7-0 are zero then word 59 bits 8-0 shall also be zero. This field may default to the preferred value for the device.

8.6.32 Word 60-61: Total number of user addressable sectors

These words reflect the total number of user addressable sectors in LBA translation. This value does not depend on the current device geometry

8.6.33 Word 62: Retired

8.6.34 Word 63: Multiword DMA transfer

The low order byte identifies by bit all of the modes which are supported, e.g., if Mode 0 is supported, bit 0 is set to one. The high order byte contains a single bit set to one to indicate which mode is active, e.g., if Mode 0 is active, bit 0 is set to one. If an Ultra DMA Mode is selected, then the high order byte shall be set to 00h.

8.6.35 Word 64: PIO transfer modes supported

Bits 7 through 0 of word 64 of the Identify Device parameter information is defined as the advanced PIO data transfer supported field. If this field is supported, bit 1 of word 53 shall be set to one. This field is bit significant. Any number of bits may be set to one in this field by the device to indicate which advanced PIO modes it is capable of supporting.

Of these bits, bits 7 through 2 are Reserved for future advanced PIO modes. Bit 0, if set to one, indicates that the device supports PIO Mode 3. Bit 1, if set to one, indicates that the device supports PIO Mode 4.

> NOTE – For backwards compatibility with BIOSs written before Word 64 was defined for advanced modes, a device reports in Word 51 the time corresponding with the highest original PIO mode (i.e., PIO Mode 0, 1, or 2) it supports.

8.6.36 Word 65: Minimum Multiword DMA transfer cycle time per word

Word 65 of the parameter information of the IDENTIFY DEVICE command is defined as the minimum Multiword DMA transfer cycle time per word. This field defines, in nanoseconds, the minimum cycle time that the device supports when performing Multiword DMA transfers on a per word basis.

If this field is supported, bit 1 of word 53 shall be set to one. Any device which supports Multiword DMA mode 1 or above shall support this field, and the value in word 65 shall not be less than the minimum cycle time for the fastest DMA mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.6.37 Word 66: Device recommended Multiword DMA cycle time

Word 66 of the parameter information of the IDENTIFY DEVICE command is defined as the device recommended Multiword DMA transfer cycle time. This field defines, in nanoseconds, the minimum cycle time per word during a single sector host transfer while performing a multiple sector READ DMA or WRITE

DMA command for any location on the media under nominal conditions. If a host runs at a faster cycle rate by operating at a cycle time of less than this value, the device may negate DMARQ for flow control. The rate at which DMARQ is negated could result in reduced throughput despite the faster cycle rate. Transfer at this rate does not ensure that flow control will not be used, but implies that higher performance may result.

If this field is supported, bit 1 of word 53 shall be set to one. Any device which supports Multiword DMA Mode 1 or above shall support this field, and the value in word 66 shall not be less than the value in word 65.

If bit 1 of word 53 is set to one because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.6.38 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 of the parameter information of the IDENTIFY DEVICE command is defined as the minimum PIO transfer without flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that, if used by the host, the device guarantees data integrity during the transfer without utilization of flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 67 shall not be less than the value reported in word 68.

If bit 1 of word 53 is set to one because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.6.39 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 of the parameter information of the IDENTIFY DEVICE command is defined as the minimum PIO transfer with IORDY flow control cycle time. This field defines, in nanoseconds, the minimum cycle time that the device supports while performing data transfers while utilizing IORDY flow control.

If this field is supported, Bit 1 of word 53 shall be set to one.

Any device which supports PIO Mode 3 or above shall support this field, and the value in word 68 shall be the fastest defined PIO mode supported by the device.

If bit 1 of word 53 is set to one because a device supports a field in Words 64-70 other than this field and the device does not support this field, the device shall return a value of zero in this field.

8.6.40 Words 69-72: Reserved

8.6.41 Word 73: Queue depth

Bits 4 through 0 of word 73 indicate the maximum queue depth supported by the device. If bit 1 of word 83 is cleared to zero indicating that the device does not support READ/WRITE DMA QUEUED commands, the value in this field shall be 00h. If bit 1 of word 83 is set to one, bits 4 through 0 indicate the maximum queue depth supported and if this value is zero, queuing of the READ/WRITE DMA QUEUED commands is not supported.

8.6.42 Words 74-79: Reserved

8.6.43 Word 80: Major version number

If not 0000h or FFFFh, the device claims compliance with the major version(s) as indicated by bits 1 through 4 being equal to one. Values other than 0000h and FFFFh are bit significant. Since ATA standards maintain downward compatibility, it is allowed for a device to set more then one bit.

8.6.44 Word 81: Minor version number

If an implementor claims that the revision of the standard they used to guide their implementation does not need to be reported or if the implementation was based upon a standard prior to the ATA-3 standard, Word 81 shall be 0000h or FFFFh.

Table 10 defines the value that may optionally be reported in Word 81 to indicate the revision of the standard which guided the implementation.

Table 10 – Minor version number

Value	Minor revision
0001h	ATA (ATA-1) X3T9.2 781D prior to revision 4
0002h	ATA-1 published, ANSI X3.221-1994
0003h	ATA (ATA-1) X3T9.2 781D revision 4
0004h	ATA-2 published, ANSI X3.279-1996
0005h	ATA-2 X3T10 948D prior to revision 2k
0006h	ATA-3 X3T10 2008D revision 1
0007h	ATA-2 X3T10 948D revision 2k
0008h	ATA-3 X3T10 2008D revision 0
0009h	ATA-2 X3T10 948D revision 3
000Ah	ATA-3 published, ANSI X3.298-199x
000Bh	ATA-3 X3T10 2008D revision 6
000Ch	ATA-3 X3T13 2008D revision 7 and 7a
000Dh	ATA/ATAPI-4 X3T13 1153D revision 6
000Eh	Reserved
000Fh	ATA/ATAPI-4 X3T13 1153D revision 7
0010h-FFFFh	Reserved

8.6.45 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall indicate features/command sets supported. The value 0000h or FFFFh was placed in each of these words by devices prior to ATA-3 and shall be interpreted by the host as meaning that features/command sets supported are not indicated. Bits 1 through 13 of word 83 and bits 0 through 13 of word 84 are reserved. Bit 14 of word 83 and word 84 shall be set to one and bit 15 of word 83 and word 84 shall be cleared to zero to provide indication that the features/command sets supported words are valid.

If bit 0 of word 82 is set to one, the SMART feature set is supported.

If bit 1 of word 82 is set to one, the Security Mode feature set is supported.

If bit 2 of word 82 is set to one, the Removable Media feature set is supported.

If bit 3 of word 82 is set to one, the Power Management feature set is supported.

If bit 4 of word 82 is set to one, the PACKET Command feature set is supported.

If bit 5 of word 82 is set to one, write cache is supported.

If bit 6 of word 82 is set to one, look-ahead is supported.

If bit 7 of word 82 is set to one, release interrupt is supported.

If bit 8 of word 82 is set to one, SERVICE interrupt is supported.

If bit 9 of word 82 is set to one, the DEVICE RESET command is supported.

If bit 10 of word 82 is set to one, the Host Protected Area feature set is supported.

If bit 11 of word 82 is set to one, the device supports the WRITE VERIFY command.

If bit 12 of word 82 is set to one, the device supports the WRITE BUFFER command.

If bit 13 of word 82 is set to one, the device supports the READ BUFFER command.

If bit 14 of word 82 is set to one, the device supports the NOP command.

If bit 15 of word 82 is set to one, the device supports the IDENTIFY DEVICE DMA command.

If bit 0 of word 83 is set to one, the device supports the DOWNLOAD MICROCODE command.

If bit 1 of word 83 is set to one, the device supports the READ DMA QUEUED and WRITE DMA QUEUED commands.

8.6.46 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall indicate features/command sets enabled. The value 0000h or FFFFh was placed in each of these words by devices prior to ATA-4 and shall be interpreted by the host as meaning that features/command sets enabled are not indicated. Bits 1 through 15 of word 86 are reserved. Bits 0-13 of word 87 are reserved. Bit 14 of word 87 shall be set to one and bit 15 of word 87 shall be cleared to zero to provide indication that the features/command sets enabled words are valid.

If bit 0 of word 85 is set to one, the SMART feature set has been enabled via the SMART ENABLE OPERATIONS command.

If bit 1 of word 85 is set to one, the Security Mode feature set has been enabled via the SECURITY SET PASSWORD command.

If bit 2 of word 85 is set to one, the Removable Media feature set is supported.

If bit 3 of word 85 is set to one, the Power Management feature set is supported.

If bit 4 of word 85 is set to one, the PACKET Command feature set is supported.

If bit 5 of word 85 is set to one, write cache has been enabled via the SET FEATURES command (see 8.28.8).

If bit 6 of word 85 is set to one, look-ahead has been enabled via the SET FEATURES command (see 8.28.10).

If bit 7 of word 85 is set to one, release interrupt has been enabled via the SET FEATURES command (see 8.28.11).

If bit 8 of word 85 is set to one, SERVICE interrupt has been enabled via the SET FEATURES command (see 8.28.12).

If bit 9 of word 85 is set to one, the DEVICE RESET command is supported.

If bit 10 of word 85 is set to one, the Host Protected Area feature set is supported.

If bit 11 of word 85 is set to one, the device supports the WRITE VERIFY command.

If bit 12 of word 85 is set to one, the device supports the WRITE BUFFER command.

If bit 13 of word 85 is set to one, the device supports the READ BUFFER command.

If bit 14 of word 85 is set to one, the device supports the NOP command.

If bit 15 of word 85 is set to one, the device supports the IDENTIFY DEVICE DMA command.

If bit 0 of word 86 is set to one, the device supports the DOWNLOAD MICROCODE command.

If bit 1 of word 86 is set to one, the device supports the READ DMA QUEUED and WRITE DMA QUEUED commands.

8.6.47 Word 88: Ultra DMA modes

Only one Ultra DMA mode shall be selected at any time.

8.6.47.1 Reserved

Bits 15 though 11 of word 88 are reserved.

8.6.47.2 Ultra DMA mode 2 selected

If bit 10 of word 88 is set to one, then Ultra DMA mode 2 is selected. If this bit is cleared to zero, then Ultra DMA mode 2 is not selected. If bit 9 is set to one or if bit 8 is set to one, then this bit shall be cleared to zero.

8.6.47.3 Ultra DMA mode 1 selected

If bit 9 of word 88 is set to one, then Ultra DMA mode 1 is selected. If this bit is cleared to zero then Ultra DMA mode 1 is not selected. If bit 10 is set to one or if bit 8 is set to one, then this bit shall be cleared to zero.

8.6.47.4 Ultra DMA mode 0 selected

If bit 8 of word 88 is set to one, then Ultra DMA mode 0 is selected. If this bit is cleared to zero then Ultra DMA mode 0 is not selected. If bit 10 is set to one or if bit 9 is set to one, then this bit shall be cleared to zero.

8.6.47.5 Reserved

Bits 7 through 3 of word 88 are reserved.

8.6.47.6 Ultra DMA mode 2 supported

If bit 2 of word 88 is set to one, then Ultra DMA modes 2 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 2 is not supported. If Ultra DMA mode 2 is supported, then Ultra DMA modes 1 and 0 shall also be supported.

8.6.47.7 Ultra DMA mode 1 supported

If bit 1 of word 88 is set to one, then Ultra DMA modes 1 and below are supported. If this bit is cleared to zero, then Ultra DMA mode 1 is not supported. If Ultra DMA mode 1 is supported, then Ultra DMA mode 0 shall also be supported.

8.6.47.8 Ultra DMA mode 0 supported

If bit 0 of word 88 is set to one, then Ultra DMA mode 0 is supported. If this bit is cleared to zero, then Ultra DMA is not supported.

8.6.48 Word 89: Time required fro Security erase unit completion

Word 89 specifies the time required for the SECURITY ERASE UNIT command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

8.6.49 Word 90: Time required for Enhanced security erase unit completion

Word 89 specifies the time required for the ENHANCED SECURITY ERASE UNIT command to complete.

Value	Time
0	Value not specified
1-254	(Value*2) minutes
255	>508 minutes

8.6.50 Words 01-127: Reserved

8.6.51 Word 128: Security status

8.6.51.1 Security level

Bit 8 of Word 128 indicates the security level. If security mode is enabled and the security level is high, bit 8 shall be cleared to zero. . If security mode is enabled and the security level is maximum, bit 8 shall be set to one. When security mode is disabled, bit 8 shall be cleared to zero.

8.6.51.2 Enhanced security erase unit supported

Bit 5 of Word 128 indicates the Enhanced security erase unit feture is supported

8.6.51.3 Security count expired

Bit 4 of Word 128 indicates that the security count has expired. If bit 4 is set to one, the security count is expired and SECURITY UNLOCK and SECURITY ERASE UNIT are aborted until a power-on reset or hard reset.

8.6.51.4 Security Frozen

Bit 3 of Word 128 indicates security Frozen. If bit 3 is set to one, the security is Frozen.

8.6.51.5 Security locked

Bit 2 of Word 128 indicates security locked. If bit 2 is set to one, the security is locked.

8.6.51.6 Security enabled

Bit 1 of Word 128 indicates security enabled. If bit 1 is set to one, the security is enabled.

8.6.51.7 Security supported

Bit 0 of Word 128 indicates the Security Mode feature set supported. If bit 0 is set to one, security is supported.

8.6.52 Words 129-159: Vendor specific.

8.6.53 Words 160-255: Reserved.

8.7 IDENTIFY PACKET DEVICE

8.7.1 Command code

A1h

8.7.2 Feature set

PACKET Command feature set

- Use prohibited for devices not implementing the PACKET Command feature set.
- Mandatory for devices implementing the PACKET Command feature set.

8.7.2 Protocol

PIO data in, see 9.6.

8.7.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	ba
Command	A1h							

8.7.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.7.5 Error outputs

Aborted command if the device does not implement this command, otherwise, the device shall not report an error.

8.7.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

8.7.7 Description

The IDENTIFY PACKET DEVICE command enables the host to receive parameter information from a device that implements the PACKET Command feature set.

Some devices may have to read the media in order to complete this command.

When the command is issued, the device sets the BSY bit to one, prepares to transfer the 256 words of device identification data to the host, sets the DRQ bit to one, clears the BSY bit to zero, and generates an interrupt. The host may then transfer the data by reading the Data register. Table 11 defines the arrangement and meanings of the parameter words in the buffer. All reserved bits or words shall be zero.

Some parameters are defined as a group of bits. A word which is defined as a set of bits is transmitted with indicated bits on the respective data bus bit (e.g., bit 15 appears on DD15).

Some parameters are defined as a sixteen bit value. A word which is defined as a sixteen bit value places the most significant bit of the value on bit DD15 and the least significant bit on bit DD0.

Some parameters are defined as 32 bit values (e.g., words 57 and 58). Such fields are transferred using two word transfers. The device shall first transfer the least significant bits, bits 15 through 0 of the value, on bits DD (15:0) respectively. After the least significant bits have been transferred, the most significant bits, bits 31 through 16 of the value, shall be transferred on DD (15:0) respectively.

Some parameters are defined as a string of ASCII characters. For the string “Copyright”, the character “C” is the first byte, the character “o” is the 2nd byte, etc. When such fields are transferred, the order of transmission is:

the 1st character (“C”) is on bits DD (15:8) of the first word
the 2nd character (“o”) is on bits DD (7:0) of the first word
the 3rd character (“p”) is on bits DD (15:8) of the second word
the 4th character (“y”) is on bits DD (7:0) of the second word
etc.

Table 11 – Identify packet device information

Word	F/V		
0		General configuration bit-significant information:	
	F	15-14	10=ATAPI device 11=reserved
	R	13	reserved
	F	12-8	Field indicates command packet set used by device
	F	7	1=removable media device
	F	6-5	00=Device shall set DRQ to one within 3 ms of receiving PACKET command. 01=Device shall assert INTRQ when DRQ is set to one after receiving PACKET. 10=Device shall set DRQ to one within 50 µs of receiving PACKET command.
	R	4-2	reserved
	F	1-0	11=reserved 00=12 byte command packet 01=16 byte command packet 1x=reserved
1-9	R	Reserved	
10-19	F	Serial number (20 ASCII characters)	
20-22	R	Reserved	
23-26	F	Firmware revision (8 ASCII characters)	
27-46	F	Model number (40 ASCII characters)	
47-48	R	Reserved	
49		Capabilities	
	F	15	1=interleaved DMA supported
	F	14	1=command queuing supported
	F	13	1=overlap operation supported
	F	12	1=ATA software reset required (obsolete)
	F	11	1=IORDY supported
	F	10	1=IORDY may be disabled
	F	9	1=LBA supported
	F	8	1=DMA supported
	X	7-0	Vendor specific
50	R	Reserved	
51	F	15-8	PIO data transfer cycle timing mode
	X	7-0	Vendor specific
52	R	Reserved	
53	R	15-3	Reserved
	F	2	1=the fields reported in word 88 are valid 0=the fields reported in word 88 are not valid
	F	1	1=the fields reported in words 64-70 are valid 0=the fields reported in words 64-70 are not valid
	V	0	1=the fields reported in words 54-58 are valid 0=the fields reported in words 54-58 may be valid
54-62	R	Reserved	

(continued)

Table 11 – Identify packet device information *(continued)*

Word	F/V	
63	V	15-8 Multiword DMA transfer mode selected
	F	7-0 Multiword DMA transfer modes supported
64	R	15-8 Reserved
	F	7-0 Advanced PIO transfer modes supported
65		Minimum Multiword DMA transfer cycle time per word
	F	15-0 Cycle time in nanoseconds
66		Manufacturer's recommended Multiword DMA transfer cycle time
	F	15-0 Cycle time in nanoseconds
67		Minimum PIO transfer cycle time without flow control
	F	15-0 Cycle time in nanoseconds
68		Minimum PIO transfer cycle time with IORDY flow control
	F	15-0 Cycle time in nanoseconds
69-70	R	Reserved (for future command overlap and queuing)
71	F	Typical time in ns from receipt of PACKET command to release.
72	F	Typical time in ns from receipt of SERVICE command to BSY cleared to zero
73	F	Queue depth 15-5 Reserved 4-0 Maximum queue depth supported
74-79	R	Reserved
80	F	Major version number 0000h or FFFFh = device does not report version 15 Reserved 14 Reserved for ATA/ATAPI-14 13 Reserved for ATA/ATAPI-13 12 Reserved for ATA/ATAPI-12 11 Reserved for ATA/ATAPI-11 10 Reserved for ATA/ATAPI-10 9 Reserved for ATA/ATAPI-9 8 Reserved for ATA/ATAPI-8 7 Reserved for ATA/ATAPI-7 6 Reserved for ATA/ATAPI-6 5 Reserved for ATA/ATAPI-5 4 1=supports ATA/ATAPI-4 3 1=supports ATA-3 2 1=supports ATA-2 1 1=supports ATA-1
81	F	Minor version number 0000h or FFFFh=device does not report version 0001h-FFFEh=see 8.6.44

(continued)

Table 11 – Identify packet device information *(continued)*

Word	F/V	
82	F	Command set supported. If words 82 and 83 =0000h or FFFFh command set notification not supported. 15 1=IDENTIFY DEVICE DMA command supported 14 1=NOP command supported 13 1=READ BUFFER command supported 12 1=WRITE BUFFER command supported 11 1=WRITE VERIFY command supported 10 1=Host Protected Area feature set supported 9 1=DEVICE RESET command supported 8 1=SERVICE interrupt supported 7 1=release interrupt supported 6 1=look-ahead supported 5 1=write cache supported 4 1=supports PACKET Command feature set 3 1=supports Power Management feature set 2 1=supports Removable Media feature set 1 1=supports Security Mode feature set 0 1=supports SMART feature set
83	F	Command sets supported. If words 82 and 83 =0000h or FFFFh command set notification not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-1 Reserved 0 1=DOWNLOAD MICROCODE command supported
84	F	Command set/feature supported extension. If words 82, 83, and 84 = 0000h or FFFFh command set notification extension is not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-0 Reserved
85	V	Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported. 15 1=IDENTIFY DEVICE DMA command supported 14 1=NOP command supported 13 1=READ BUFFER command supported 12 1=WRITE BUFFER command supported 11 1=WRITE VERIFY command supported 10 1=Host Protected Area feature set supported 9 1=DEVICE RESET command supported 8 1=SERVICE interrupt enabled 7 1=release interrupt enabled 6 1=look-ahead enabled 5 1=write cache enabled 4 1=supports PACKET Command feature set 3 1=supports Power Management feature set 2 1=supports Removable Media feature set 1 1= Security Mode feature set enabled 0 1= SMART feature set enabled
86	V	Command set/feature enabled. If words 85, 86, and 87 = 0000h or FFFFh command set enabled notification is not supported. 15-1 Reserved 0 1=DOWNLOAD MICROCODE command supported

Table 11 – Identify packet device information *(concluded)*

Word	F/V	
87	V	Command set/feature default. If words 85, 86, and 87 = 0000h or FFFFh command set default notification is not supported. 15 Shall be cleared to zero 14 Shall be set to one 13-0 Reserved
88	R	15-11 Reserved
	V	10 1=Ultra DMA mode 2 is selected 0=Ultra DMA mode 2 is not selected
	V	9 1=Ultra DMA mode 1 is selected 0=Ultra DMA mode 1 is not selected
	V	8 1=Ultra DMA mode 0 is selected 0=Ultra DMA mode 0 is not selected
	R	7-3 Reserved
	F	2 1=Ultra DMA mode 2 and below are supported 0=Ultra DMA mode 2 is not supported
	F	1 1=Ultra DMA mode 1 and below are supported 0=Ultra DMA mode 1 is not supported
	F	0 1=Ultra DMA mode 0 is supported 0=Ultra DMA is not supported
89-127	R	Reserved
128	V	Security status 15-9 Reserved 8 Security level 0=High, 1=Maximum 7-6 Reserved 5 1=Enhanced security erase supported 4 1=Security count expired 3 1=Security frozen 2 1=Security locked 1 1=Security enabled 0 1=Security supported
129-159	X	Vendor specific
160-255	R	Reserved

Key:
F = the content of the word is fixed and does not change. For removable media devices, these values may change when media is removed or changed.
V = the contents of the word is variable and may change depending on the state of the device or the commands executed by the device.
X = the content of the word is vendor specific and may be fixed or variable.
R = the content of the word is reserved and shall be zero.

8.7.8 Word 0: General configuration

Bits 15 and 14 of word 0 indicate the type of device. If bit 15 is cleared to zero the device does not implement the PACKET Command feature set. If bit 15 is set to one and bit 14 is is cleared to zero, the device implements the PACKET Command feature set. The value bit 15 and bit 14 both set to one is reserved.

Bits 12 through 8 of word 0 indicate the command packet set implemented by the device. This value follows the peripheral device type value as defined in X3T10/995D, SCSI-3 Primary Commands.

Value	Description
00h	Direct-access device
01h	Sequential-access device
02h	Printer device
03h	Processor device
04h	Write-once device
05h	CD-ROM device
06h	Scanner device
07h	Optical memory device
08h	Medium changer device
09h	Communications device
0A-0Bh	Reserved for ACS IT8
0Ch	Array controller device
0D-1Eh	Reserved
1Fh	Unknown or no device type

Bit 7 if set to one indicates that the device has removable media.

Bits 6 and 5 of word 0 indicates the response when a PACKET command is received. A value of 00b indicates a maximum time of 3 ms from receipt of PACKET to the setting of DRQ to one. A value of 01b indicates that INTRQ shall be asserted when DRQ is set to one and that this action will occur within 10ms of the receipt of PACKET. A value of 10b indicates a maximum time of 50 µs from the receipt of PACKET to the setting of DRQ to one. The value 11b is reserved.

Bits 1 and 0 of word 0 indicate the packet size the device supports. A value of 00b indicates that a 12 byte packet is supported; a value of 01b indicates a 16 byte packet. The values 10b and 11b are reserved.

8.7.9 Words 1-9: Reserved

8.7.10 Words 10-19: Serial number

The use of these words is optional. If not implemented, the content shall be zeros. If implemented, the content shall be as described in words 10-19 of the INDENTIFY DEVICE command.

8.7.11 Words 20-22: Reserved

8.7.12 Words 23-26: Firmware revision

Words 23 through 26 shall have the content described for words 23 through 26 of the IDENTIFY DEVICE command.

8.7.13 Words 27-46: Model number

Words 27 through 46 shall have the content described for words 23 through 26 of the IDENTIFY DEVICE command.

8.7.14 Words 47-48: Reserved

8.7.15 Word 49: Capabilities

Bit 15 of word 49 is used to indicated that the device supports interleaved DMA data transfer for overlapped DMA commands.

Bit 14 of word 49 is used to indicated that the device supports command queuing for overlapped commands. If bit 14 is set to one, bit 13 shall be set to one.

Bit 13 of word 49 is used to indicated that the device supports command overlap operation.

Bit 12 of word 49 indicates that the device requires a software reset to reset the device when BSY is set to one. Some devices produced before this standard are unable to process a DEVICE RESET when the BSY bit is set to one. The use of this bit is obsolete.

Bit 11 of word 49 is used to determine whether a device supports IORDY. If this bit is set to one, then the device supports IORDY operation. If this bit is zero, the device may support IORDY. This ensures backward compatibility. If a device supports PIO Mode 3 or higher, then this bit shall be set to one.

Bit 10 of word 49 is used to indicate a device's ability to enable or disable the use of IORDY. If this bit is set to one, then the device supports the disabling of IORDY. Disabling and enabling of IORDY is accomplished using the SET FEATURES command.

Bit 9 of word 49 indicates that an LBA translation is supported

Bits 8 of Word 49 indicates that DMA is supported.

8.7.16 Word 50: Reserved

8.7.17 Word 51: PIO data transfer cycle timing mode

Word 51 shall have the content described for word 51 of the IDENTIFY DEVICE command.

8.7.18 Word 52: Reserved

8.7.19 Word 53: Field validity

Word 53 shall have the content described for word 53 of the IDENTIFY DEVICE command.

8.7.20 Words 54-62: Reserved

8.7.21 Word 63: Multiword data transfer

Word 63 shall have the content described for word 63 of the IDENTIFY DEVICE command.

8.7.22 Word 64: Flow control PIO mode supported

Word 64 shall have the content described for word 64 of the IDENTIFY DEVICE command.

8.7.23 Word 65: Minimum multiword DMA transfer cycle time per word

Word 65 shall have the content described for word 65 of the IDENTIFY DEVICE command.

8.7.24 Word 66: Device recommended multiword DMA cycle time

Word 66 shall have the content described for word 66 of the IDENTIFY DEVICE command.

8.7.25 Word 67: Minimum PIO transfer cycle time without flow control

Word 67 shall have the content described for word 67 of the IDENTIFY DEVICE command.

8.7.26 Word 68: Minimum PIO transfer cycle time with IORDY

Word 68 shall have the content described for word 68 of the IDENTIFY DEVICE command.

8.7.27 Word 69-70: Reserved

8.7.28 Word 71: PACKET to release time

Word 71 shall contain the typical (3 sigma) time in nanoseconds from the receipt of a PACKET command until the device releases the bus.

8.7.29 Word 72: SERVICE to release time

Word 72 shall contain the typical (3 sigma) time in nanoseconds from the receipt of a SERVICE command until the device releases the bus.

8.7.30 Word 73: Queue depth

Bits 4 through 0 of word 73 indicate the maximum queue depth supported by the device. If bit 14 of word 49 is zero indicating that the device does not support command queuing, the value in this field shall be 00h.

8.7.31 Words 74-79: Reserved

8.7.32 Word 80: Major revision number

Word 80 shall have the content described for word 80 of the IDENTIFY DEVICE command.

8.7.33 Word 81: Minor revision number

Word 81 shall have the content described for word 81 of the IDENTIFY DEVICE command.

8.7.34 Words 82-84: Features/command sets supported

Words 82, 83, and 84 shall have the content described for words 82, 83, and 84 of the IDENTIFY DEVICE command.

8.7.35 Words 85-87: Features/command sets enabled

Words 85, 86, and 87 shall have the content described for words 85, 86, and 87 of the IDENTIFY DEVICE command.

8.7.36 Word 88:Ultra DMA modes

Word 88 shall have the content described for word 88 of the IDENTIFY DEVICE command.

8.7.37 Word 89: Time required for Security erase unit completion

Word 89 shall have the content described for word 89 of the IDENTIFY DEVICE command.

8.7.38 Word 90: Time required for Enhanced security erase unit completion

Word 90 shall have the content described for word 90 of the IDENTIFY DEVICE command.

8.7.39 Word 128: Security status

Word 128 shall have the content described for word 128 of the IDENTIFY DEVICE command.

8.7.40 Words 129-255: Reserved

8.8 IDLE

8.8.1 Command code

E3h

8.8.2 Feature set

Power Management feature set.

- Power Management feature is mandatory if power management is not provided by a PACKET feature set command set.
- Mandatory if the Power Management feature set is implemented.

8.8.2 Protocol

Non-data command, see 9.8.

8.8.3 Inputs

Values other than zero in the Sector Count register when the IDLE command is issued shall determine the time period programmed into the Standby timer. Table 12 defines these values.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Timer period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E3h							

Table 12 – Automatic Standby timer periods

Sector Count register contents		Corresponding timeout period
0	(00h)	Timeout disabled
1-240	(01h-F0h)	(value * 5) s
241-251	(F1h-FBh)	((value - 240) * 30) min
252	(FCh)	21 min
253	(FDh)	Period between 8 and 12 hrs
254	(FEh)	Reserved
255	(FFh)	21 min 15 s
NOTE – Times are approximate.		

8.8.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.8.5 Error outputs

Aborted command - The device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register - ABRT shall be set to one if Power Management feature set not supported.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.8.6 Prerequisites

DRDY set equal to one.

8.8.7 Description

The IDLE command allows the host to place the device in the Idle Mode using the Standby timer. INTRQ is asserted even though the device may not have fully transitioned to Idle Mode.

If the Sector Count register is non-zero then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer, see 6.8.

If the Sector Count register is zero then the Standby timer is disabled.

8.9 IDLE IMMEDIATE

8.9.1 Command code

E1h

8.9.2 Feature set

Power Management feature set.
- Power Management feature is mandatory if power management is not provided by a PACKET feature set command set.
- Mandatory if the Power Management feature set is implemented.

8.9.2 Protocol

Non-data command, see 9.8.

8.9.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E1h							

8.9.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.9.5 Error outputs

Aborted command - The device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register - ABRT shall be set to one if Power Management feature set not supported.
Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.9.6 Prerequisites

DRDY set equal to one.

8.9.7 Description

The IDLE IMMEDIATE command allows the host to immediately place the device in the Idle mode. INTRQ is asserted even though the device may not have fully transitioned to Idle mode, see 6.8.

8.10 INITIALIZE DEVICE PARAMETERS

8.10.1 Command code

91h

8.10.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.10.2 Protocol

Non-data, see 9.8.

8.10.3 Inputs

The Sector Count register specifies the number of logical sectors per logical track, and the Device/Head register specifies the maximum head number.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Logical sectors per logical track							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	Max head			
Command	91h							

8.10.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	na	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
ERR shall be cleared to zero

8.10.5 Error outputs

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	na	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the device does not support the requested CHS translation.
IDNF shall be set if the requested CHS translation is not supported.

Status register -

BSY shall be cleared to zero when the command is complete
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.10.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

8.10.7 Description

This command enables the host to set the number of logical sectors per track and the number of logical heads minus 1, per logical cylinder for the current CHS translation mode. A logical sectors per track value zero is illegal .

If the capacity of the device is less than 16,515,072 sectors, a device shall support the CHS translation described in words 1, 3, and 6 of the IDENTIFY DEVICE information. Support of other CHS translations is optional.

If the requested CHS translation is not supported, the device shall set the Error bit to one in the Status register and set the Aborted command bit to one in the Error register before clearing the BSY bit to zero in the Status register.

If the requested CHS translation is not supported, the device shall fail all media access commands with an ID Not Found error until a valid CHS translation is established.

8.11 NOP

8.11.1 Command code

00h

8.11.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Mandatory for devices implementing the PACKET Command feature set.

8.11.2 Protocol

Non-data, see 9.8.

8.11.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	00h							

8.11.4 Normal outputs

This command always fails with an error.

8.11.5 Error outputs

The Command Block registers, other than the Error and Status registers, are not changed by this command. This command always fails with an Aborted command error.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	Initial value							
Sector Number	Initial value							
Cylinder Low	Initial value							
Cylinder High	Initial value							
Device/Head	Initial value							
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register - ABRT shall be set to one if this command not supported.
Sector Count, Sector Number, Cylinder Low, Cylinder High, Device/Head - value set by host is not changed.
Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.11.6 Prerequisites

DRDY set equal to one.

8.11.7 Description

This command enables a host, which only performs 16-bit register accesses, to check device status. The device shall respond, as it does to an unrecognized command, by setting ABRT bit to one in the Error register, Error in the Status register, clearing Busy to zero in the Status register, and asserting INTRQ.

8.12 PACKET

8.12.1 Command code

A0h

8.12.2 Feature set

PACKET Command feature set

- Use prohibited for devices not implemnting the PACKET Command feature set.
- Mandatory for devices implementing the PACKET Command feature set.

8.12.2 Protocol

Packet, see 9.10.

8.12.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na	na	na	na	na	na	OVL	DMA
Sector Count	Tag					na		
Sector Number	na							
Byte count low (Cylinder Low)	Byte count (7-0)							
Byte count high (Cylinder High)	Byte count (15-8)							
Device/Head	1	na	1	DEV	na	na	na	na
Command	A0h							

In the Features register:

OVL - This bit is set to one to inform the device that the PACKET command is to be overlapped.

DMA - This bit is set to one to inform the device that the data transfer (not the command packet transfer) associated with this command is via DMA or Ultra DMA mode.

In the Sector Count register:

Tag - If the device supports command queuing, this field contains the command tag for the command being delivered.

In the Cylinder High and Cylinder Low registers:

These registers are written by the host with the maximum byte count that is to be transferred in any single DRQ assertion for PIO transfers.

8.12.4 Normal outputs

8.12.4.1 Awaiting command

When the device is ready to accept the command packet from the host the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na						OVL	DMA
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	Byte count (7:0)							
Byte count high (Cylinder High)	Byte count (15:8)							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Error register -

OVL - shall reflect the bit value set by the host in the Features register when the command was issued.
DMA - shall reflect the bit value set by the host in the Features register when the command was issued.

Status register -
BSY - Shall be cleared to zero.
DRDY - na.
DMRD - Shall be cleared to zero.
SERV - Shall be cleared to zero.
DRQ - Shall be set to one.
CHK - Shall be cleared to zero

Cylinder High/Low - shall reflect the value set by the host when the command was issued.

Sector Count register -
Tag - If the device supports command queuing, this field contains the command tag for the command being delivered.
REL - Shall be cleared to zero.
I/O - Shall be cleared to zero indicating transfer to the device.
C/D - Shall be set to one indicating the transfer of a command packet.

8.12.4.2 Data transmission

After receiving the command packet, the device sets BSY to one and clears DRQ to zero. If the command packet requires a data transfer and OVL is not set to one, the device prepares for the data transfer and then sets the following register content to initiate the transfer. If the OVL bit is set to one, the device is ready to transfer the data immediately and the Release interrupt has not been enabled, the device sets the following register content to initiate the transfer.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	Byte count (7:0)							
Byte count high (Cylinder High)	Byte count (15:8)							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Status register -
BSY - Shall be cleared to zero.
DRDY - na.
DMRD - Shall be set to one if the transfer is to be a DMA or Ultra DMA transfer.
SERV - Shall be cleared to zero.
DRQ - Shall be set to one.
CHK - Shall be cleared to zero

Cylinder High/Low - If the transfer is to be in PIO mode, the byte count of the data to be transferred for this DRQ assertion shall be presented.

Sector Count register -
Tag - If the device supports command queuing, this field contains the command tag for the command being delivered.
REL - Shall be cleared to zero.

I/O - Shall be cleared to zero if the transfer is to the device. Shall be set to one if the transfer is to the host.
C/D - Shall be cleared to zero indicating the transfer of data.

8.12.4.3 Release

After receiving the command packet, the device sets BSY to one and clears DRQ to zero. If the command packet requires a data transfer, the OVL bit is set to one, and the device is not prepared to immediately transfer data or the Release interrupt is enabled, the device releases the bus by placing the following register content.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	Byte count (7:0)							
Byte count high (Cylinder High)	Byte count (15:8)							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	na	na	CHK

Status register -
BSY - Shall be cleared to zero.
DRDY - na.
DMRD - Shall be cleared to zero.
SERV - Shall be cleared to zero until the device is ready to transfer then set to one when the device is ready to transfer. This bit may be set to one in such a short time that the host may not see the bit in the zero state.
DRQ - Shall cleared to zero.
CHK - Shall be cleared to zero

Cylinder High/Low - na.

Sector Count register -
Tag - If the device supports command queuing, this field contains the command tag for the command being delivered.
REL - Shall be set to one.
I/O - Shall be cleared to zero.
C/D - Shall be cleared to zero.

8.12.4.4 Command completion

When the device has completed the command without error, the device sets the following register content.

Register	7	6	5	4	3	2	1	0
Error	na							
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Byte count low (Cylinder Low)	Byte count (7:0)							
Byte count high (Cylinder High)	Byte count (15:8)							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DMRD	SERV	DRQ	CORR	na	CHK

Status register -

BSY - Shall be cleared to zero.
DRDY - Shall be set to one.
DMRDY - na.
SERV - Shall be cleared to zero.
DRQ - Shall be cleared to zero.
CORR - Shall be set to one if a correctable error was found.
CHK - Shall be cleared to zero.

Cylinder High/Low - Shall be cleared to zero.

Sector Count register -

Tag - If the device supports command queuing, this field contains the command tag for the command being delivered.
REL - Shall be cleared to zero.
I/O - Shall be set to one.
C/D - Shall be set to one.

8.12.5 Error outputs

The device shall not terminate the PACKET command with an error before the last byte of the command packet has been written, see 9.10.

Register	7	6	5	4	3	2	1	0
Error	Sense key				MCR	ABRT	EOM	ILI
Interrupt reason (Sector Count)	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	CHK

Error register -

Sense Key is a command packet set specific error indication.
MCR for removable media devices, shall be set to one to indicate a request for media removal if set to one.
ABRT shall be set to one if the requested command has been aborted because the command code or a command parameter is invalid.
EOM shall be set to one to indicate that the end of the media was detected.
ILI shall be set to one to indicate that an illegal length was encountered.

Sector Count register -

Tag - If the device supports command queuing, this field contains the command tag for the command being delivered.
REL - Shall be cleared to zero.
I/O - Shall be set to one.
C/D - Shall be set to one.

Status register -

BSY shall be cleared to zero indicating the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
CHK shall be set to one if an Error register sense key or code bit is set.

8.12.6 Prerequisites

This command shall be accepted regardless of the state of DRDY.

8.12.7 Description

The PACKET command is used to initiate a device command via a command packet. If the native form of the encapsulated command is shorter than the packet size reported in bits 1 and 0 of word 0 of the IDENTIFY PACKET DEVICE response, the encapsulated command shall begin at byte 0 of the packet. Packet bytes beyond the end of the encapsulated command are reserved.

If the device supports overlap, the OVL bit is set to one in the Features register and the Release interrupt has been disabled via the SET FEATURES command, the device may or may not release. If the device is ready for the data transfer, it may begin the transfer immediately as described in the non-overlap case. If the data is not ready, the device may release and complete the transfer after the execution of a SERVICE command.

For all commands that transfer all of the data requested by the command in a single DRQ transfer, the byte count shall contain the total data length. The maximum number of bytes that may be transferred for a read command with a single assertion of DRQ is 65,535 bytes. If a device requests that more data be transferred than required by the command, the host shall pad the data when sending data to the device. The only permissable time for an odd byte count is for the last DRQ assertion associated with a command. The device is not responsible for padding data, only the amount specified by the command shall be transferred to the host.

8.13 READ BUFFER

8.13.1 Command code

E4h

8.13.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.13.2 Protocol

PIO data in, see 9.6.

8.13.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E4h							

8.13.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.13.5 Error outputs

Aborted command if the command is not supported.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register - ABRT shall be set to one if this command not supported.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.13.6 Prerequisites

DRDY set equal to one. A WRITE BUFFER command shall immediately proceed a READ BUFFER command.

8.13.7 Description

The READ BUFFER command enables the host to read the current contents of the device's sector buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

8.14 READ DMA

8.14.1 Command code

C8h or C9h

8.14.2 Feature set

General feature set
Mandatory for devices not implementing the PACKET Command feature set.
Use prohibited for devices implementing the PACKET Command feature set.

8.14.2 Protocol

DMA or Ultra DMA , see 9.9 or 9.12.

8.14.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	C8h or C9h							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) starting head number or LBA address bits (27:24)

8.14.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.14.5 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	CORR	na	ERR

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA transfers.

UNC shall be set to one if data is uncorrectable

IDNF shall be set to one if sector's ID field could not be found

ABRT shall be set to one if this command not supported or if an error, including an ICRC error, has occured during an Ultra DMA data transfer.

AMNF shall be set to one if the data address mark could not be found after finding correct ID field.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

Status register -

BSY shall be cleared to zero when the command is complete

DRDY shall be set to one

DF shall be set to one if a drive fault has occurred

DRQ shall be cleared to zero

CORR if a correctable data error was found

ERR shall be set to one if an Error register bit is set to one

8.14.6 Prerequisites

DRDY set equal to one. The host shall initialize the DMA channel.

8.14.7 Description

The READ DMA command allows the host to read data using the DMA data transfer protocol.

8.15 READ DMA QUEUED

8.15.1 Command code

C7h

8.15.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET command feature set.

8.15.3 Protocol

DMA QUEUED or Ultra DMA Queued.

8.15.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	Sector Count							
Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C7h							

Features - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector count - if the device supports command queuing, bits (7:3) contain the tag for the command being delivered.
Sector number - starting sector number or LBA address bits (7:0).
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8).
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16).
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address; bits (3:0) starting head number or LBA address bits (27:24).

8.15.5 Normal outputs

8.15.5.1 Release

If the device releases before transferring data for this command, the register content upon release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY		SERV	DRQ	CORR	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.
Bit 2 - REL bit shall be set to one indicating that the device has released an overlap command.
Bit 1 - I/O shall be zero.
Bit 0 - C/D shall be zero.

Status register -

Bit 7 - BSY shall be cleared to zero.
Bit 6 - DRDY shall be set to one.
Bit 4 - SERV shall be cleared to zero when the device releases. This bit shall be set to one when the device is ready to transfer data.
Bit 3 - DRQ bit shall be cleared to zero.
Bit 2 - CORR bit shall be cleared to zero.
Bit 0 - ERR bit shall be cleared to zero.

8.15.5.2 Command complete

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	CORR	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.
Bit 2 - REL shall be cleared to zero.
Bit 1 - I/O shall be set to one.
Bit 0 - C/D shall be set to one.

Status register -

Bit 7 - BSY shall be cleared to zero.
Bit 6 - DRDY shall be set to one..
Bit 4 - SERV shall be cleared to zero.
Bit 3 - DRQ bit shall be cleared to zero.
Bit 2 - CORR shall be set to one if a correctable data error was found.
Bit 0 - ERR bit shall be cleared to zero.

8.15.6 Error outputs

The Sector Count register contains the tag for this command if the device supports command queuing. Aborted command if the command is not supported or if the device has not had overlapped interrupt enabled. Aborted command if the device supports command queuing and the tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort. The device may remain BSY for some time when responding to these errors.

Register	7	6	5	4	3	2	1	0
Error	ICRC	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	Tag					REL	I/O	C/D
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	D	Head number or LBA			
Status	BSY	DRDY	na	SERV	DRQ	CORR	na	ERR

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA data transfers.
UNC shall be set to one if data is uncorrectable.
IDNF shall be set to one if sector's ID field could not be found.
ABRT shall be set to one if this command not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer.

AMNF shall be set to one if the data address mark could not be found after finding the correct ID field.

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.
Bit 2 - REL shall be cleared to zero.
Bit 1 - I/O shall be set to one.
Bit 0 - C/D shall be set to one.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

Status register -

BSY shall be cleared to zero.
DRDY shall be set to one.
DF shall be set to one if a drive fault has occurred.
DRQ shall be cleared to zero.
CORR shall be set to one if a correctable data error was found.
ERR shall be set to one if an Error register bit is set to one.

8.15.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

8.15.8 Description

This command executes in a similar manner to a READ DMA command. The device may release the bus or it may execute the data transfer without release if the data is ready to transfer.

If a release is executed, the host shall reselect the device using the SERVICE command.

See for the protocol utilized for overlapped commands.

8.16 READ MULTIPLE

8.16.1 Command code

C4h

8.16.2 Feature set

General feature set

- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.16.2 Protocol

PIO data in, see 9.6.

8.16.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	C4h							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) starting head number or LBA address bits (27:24)

8.16.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.16.5 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	CORR	na	ERR

Error register -
UNC shall be set to one if data is uncorrectable
IDNF shall be set to one if sector's ID field could not be found
ABRT shall be set to one if this command not supported.
AMNF shall be set to one if the data address mark could not be found after finding correct ID field.
Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
CORR if a correctable data error was found
ERR shall be set to one if an Error register bit is set to one

8.16.6 Prerequisites

DRDY set equal to one. If bit 8 of Word 59 of the IDENTIFY DEVICE response is cleared to zero, a successful SET MULTIPLE MODE command shall precede a READ MULTIPLE command.

8.16.7 Description

The READ MULTIPLE command performs similarly to the READ SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block which contains the number of sectors defined by a SET MULTIPLE MODE command or the default if no intervening SET MULTIPLE command has been issued. Command execution is identical to the READ SECTOR(S) operation except that the number of sectors defined by a SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is programmed by the SET MULTIPLE MODE command, which shall be executed prior to the READ MULTIPLE command. When the READ MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer shall be for n sectors, where n = remainder (sector count/ block count)

If the READ MULTIPLE command is received when READ MULTIPLE commands are disabled, the READ MULTIPLE operation shall be rejected with an Aborted command error.

Device errors encountered during READ MULTIPLE commands are posted at the beginning of the block or partial block transfer, but the DRQ bit is still set to one and the data transfer shall take place, including transfer of corrupted data, if any. The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information.

Subsequent blocks or partial blocks are transferred only if the error was a correctable data error. All other errors cause the command to stop after transfer of the block that contained the error.

8.17 READ NATIVE MAX ADDRESS

8.17.1 Command code

F8h

8.17.2 Feature set

Host Protected Area feature set.

- Mandatory if the Host Protected Area feature set is implemented.

8.17.2 Protocol

Non-data command, see 9.8.

8.17.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	LBA	1	DEV	na			
Command	F8h							

Device/Head - if LBA is set to one, the maximum address shall be reported as an LBA value. If LBA is cleared to zero, the maximum address shall be reported as a CHS value.

8.17.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	Max sector number or LBA							
Cylinder Low	Max cylinder low or LBA							
Cylinder High	Max cylinder high or LBA							
Device/Head	1	na	1	DEV	Max head number or LBA			
Status	BSY	DRDY	na	na	na	na	na	ERR

Sector Number - maximum native sector number or LBA on the device.
Cylinder Low - maximum native cylinder number low or LBA on the device.
Cylinder High - maximum native cylinder number high or LBA on device.
Device/Head - maximum native head number or LBA on the device.
Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.17.5 Error outputs

If this command is not supported an Aborted command error shall be returned.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be set to one if an Error register bit is set to one

8.17.6 Prerequisites

DRDY set equal to one.

8.17.7 Description

This command returns the maximum values valid when using the SET MAX ADDRESS command.

8.18 READ SECTOR(S)

8.18.1 Command code

20h or 21h

8.18.2 Feature set

General feature set
- Mandatory for all devices.
- PACKET Command feature set devices see 8.18.4.2.

8.18.2 Protocol

PIO data in, see 9.6.

8.18.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	20h or 21h							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) starting head number or LBA address bits (27:24)

8.18.4 Outputs

8.18.4.1 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.18.4.2 Outputs for PACKET Command feature set devices

In response to this command, devices that implement the PACKET Command feature set shall post an Aborted command error and place the PACKET Command feature set signature in the Cylinder High and the Cylinder Low register (see 9.1).

8.18.5 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	CORR	na	ERR

Error register -
UNC shall be set to one if data is uncorrectable
IDNF shall be set to one if sector's ID field could not be found
ABRT shall be set to one if this command not supported.
AMNF shall be set to one if the data address mark could not be found after finding correct ID field.
Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
CORR if a correctable data error was found
ERR shall be set to one if an Error register bit is set to one

8.18.6 Prerequisites

DRDY set equal to one.

8.18.7 Description

This command reads from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors. The transfer shall begin at the sector specified in the Sector Number register.

The DRQ bit is always set to one prior to data transfer regardless of the presence or absence of an error condition.

8.19 READ VERIFY SECTOR(S)

8.19.1 Command code

40h or 41h

8.19.2 Feature set

General feature set
- Mandatory for all devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.19.2 Protocol

Non-data, see 9.8.

8.19.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	40h or 41h							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) starting head number or LBA address bits (27:24)

8.19.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.19.5 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	CORR	na	ERR

Error register -

UNC shall be set to one if data is uncorrectable
IDNF shall be set to one if sector's ID field could not be found
ABRT shall be set to one if this command not supported.
AMNF shall be set to one if the data address mark could not be found after finding correct ID field.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
CORR if a correctable data error was found
ERR shall be set to one if an Error register bit is set to one

8.19.6 Prerequisites

DRDY set equal to one.

8.19.7 Description

This command is identical to the READ SECTOR(S) command, except that the DRQ bit is never set to one, and no data is transferred to the host.

8.20 SECURITY DISABLE PASSWORD

8.20.1 Command code

F6h

8.20.2 Feature set

Security Mode feature set.

– Mandatory if the Security Mode feature set is implemented.

8.20.2 Protocol

PIO data out, see 9.7.

8.20.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	F6h							

8.20.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.20.5 Error outputs

Device returns Aborted command error if command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported.

Status register -

BSY shall be cleared to zero when the command is complete

DRDY shall be set to one

DF shall be set to one if a drive fault has occurred

DRQ shall be cleared to zero

ERR shall be set to one if an Error register bit is set to one

8.20.6 Prerequisites

DRDY set equal to one. Device shall be in Unlocked mode.

8.20.7 Description

The SECURITY DISABLE PASSWORD command requests a transfer of a single sector of data from the host. Table 13 defines the content of this sector of information. Then the device checks the transferred password. If the User password or the Master password match, the device disables the Lock mode. This command does not change the Master password that may be reactivated later by setting a User password.

Table 13 – Security password content

Word	Content
0	Control word Bit 0 Identifier 0=compare User password 1=compare Master password Bit 1 Erase mode 0=Normal erase 1=Enhanced erase Bit 2-15 Reserved
1-16	Password (32 bytes)
17-255	Reserved

8.21 SECURITY ERASE PREPARE

8.21.1 Command code

F3h

8.21.2 Feature set

Security Mode feature set.

– Mandatory if the Security Mode feature set is implemented.

8.21.2 Protocol

Non-data, see 9.8.

8.21.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	F3h							

8.21.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.21.5 Error outputs

Device returns Aborted command error if command is not supported or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported or device is in Frozen mode.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.21.6 Prerequisites

DRDY set equal to one.

8.21.7 Description

The SECURITY ERASE PREPARE command shall be issued immediately before the SECURITY ERASE UNIT command to enable device erasing and unlocking. This command prevents accidental erasure of the device.

8.22 SECURITY ERASE UNIT

8.22.1 Command code

F4h

8.22.2 Feature set

Security Mode feature set.

– Mandatory if the Security Mode feature set is implemented.

8.22.2 Protocol

PIO data out, see 9.7.

8.22.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	F4h							

8.22.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete

DRDY shall be set to one

ERR shall be cleared to zero

8.22.5 Error outputs

Device returns Aborted command error if command is not supported, the device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported, device is in Frozen mode, not preceded by a SECURITY ERASE PREPARE command, or if the data area is not successfully overwritten.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.22.6 Prerequisites

DRDY set equal to one. This command shall be immediately preceded by a SECURITY ERASE PREPARE command.

8.22.7 Description

This command requests transfer of a single sector of data from the host. Table 13 defines the content of this sector of information. If the password does not match, the device rejects the command with an Aborted command error.

The SECURITY ERASE PREPARE command shall be completed immediately prior to the SECURITY ERASE UNIT command. If the device receives a SECURITY ERASE UNIT command without an immediately prior SECURITY ERASE PREPARE command, the device aborts the SECURITY ERASE UNIT command

When normal erasure mode is selected, the SECURITY ERASE UNIT command writes binary zeros to all user data areas. When enhanced erasure mode is selected, the SECURITY ERASE UNIT command writes data patterns stored at manufacturing to all user data areas. In enhanced mode, all previously written user data is overwritten, including sectors that are no longer in use due to reallocation.

This command disables the device Lock mode, however, the Master password is still stored internally within the device and may be reactivated later when a new User password is set.

8.23 SECURITY FREEZE LOCK

8.23.1 Command code

F5h

8.23.2 Feature set

Security Mode feature set.

– Mandatory if the Security Mode feature set is implemented.

8.23.2 Protocol

Non-data, see 9.8.

8.23.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	F5h							

8.23.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.23.5 Error outputs

Device returns Aborted command error if command is not supported, or the device is in Locked mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported or device is in locked mode.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred

DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.23.6 Prerequisites

DRDY set equal to one.

8.23.7 Description

The SECURITY FREEZE LOCK command sets the device to Frozen mode. After this command is completed any other commands which update the device Lock mode are rejected. Frozen mode is quit by power off or hardware reset. If SECURITY FREEZE LOCK is issued when the device is in Frozen mode, the command executes and the device remains in Frozen mode.

Commands disabled by SECURITY FREEZE LOCK are:

- SECURITY SET PASSWORD
- SECURITY UNLOCK
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT

8.24 SECURITY SET PASSWORD

8.24.1 Command code

F1h

8.24.2 Feature set

Security Mode feature set.

- Mandatory if the Security Mode feature set is implemented.

8.24.2 Protocol

PIO data out, see 9.7.

8.24.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	F1h							

8.24.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.24.5 Error outputs

Device returns Aborted command error if command is not supported, the device is in Locked mode, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported, if device is in Frozen mode, or if device is in locked mode.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.24.6 Prerequisites

DRDY set equal to one.

8.24.7 Description

This command requests a transfer of a single sector of data from the host. Table 14 defines the content of this sector of information. The data transferred controls the function of this command. Table 15 defines the interaction of the identifier and security level bits.

Table 14 – SECURITY SET PASSWORD data content

Word	Content
0	Control word Bit 0 Identifier 0=set User password 1=set Master password Bits 1-7 Reserved Bit 8 Security level 0=High 1=Maximum Bits 9-15 Reserved
1-16	Password (32 bytes)
17-255	Reserved

Table 15 – Identifier and security level bit interaction

Identifier	Level	Command result
User	High	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by either the User password or the previously set Master password.
User	Maximum	The password supplied with the command shall be saved as the new User password. The Lock mode shall be enabled from the next power-on or hardware reset. The device shall then be unlocked by only the User password. The Master password previously set is still stored in the device but shall not be used to unlock the device.
Master	High or Maximum	This combination shall set a Master password but shall not enable or disable the Lock mode. The security level is not changed.

8.25 SECURITY UNLOCK

8.25.1 Command code

F2h

8.25.2 Feature set

Security Mode feature set.

– Mandatory if the Security Mode feature set is implemented.

8.25.2 Protocol

PIO data out, see 9.7.

8.25.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	F2h							

8.25.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.25.5 Error outputs

Device returns Aborted command error if command is not supported, or the device is in Frozen mode.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported or if device is in Frozen mode.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.25.6 Prerequisites

DRDY set equal to one.

8.25.7 Description

This command requests transfer of a single sector of data from the host. Table 13 defines the content of this sector of information.

If the Identifier bit is set to Master and the device is in high security level, then the password supplied shall be compared with the stored Master password. If the device is in maximum security level then the unlock shall be rejected.

If the Identifier bit is set to user then the device compares the supplied password with the stored User password.

If the password compare fails then the device returns an abort error to the host and decrements the unlock counter. This counter is initially set to five and is decremented for each password mismatch when SECURITY UNLOCK is issued and the device is locked. When this counter reaches zero then SECURITY UNLOCK and SECURITY ERASE UNIT commands are aborted until a power-on reset or a hard reset. SECURITY UNLOCK commands issued when the device is unlocked have no effect on the unlock counter.

8.26 SEEK

8.26.1 Command code

70h

8.26.2 Feature set

General feature set
- Mandatory for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.26.2 Protocol

Non-data, see 9.8.

8.26.3 Inputs

The Cylinder High register, the Cylinder Low register, the head portion of Drive/head register and the Sector Number register contain the address of a sector that the host may request in a subsequent command.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	70h							

Sector Number - sector number or LBA address bits (7:0)
Cylinder Low - cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) head number or LBA address bits (27:24)

8.26.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	DSC	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DSC shall be set to one concurrent with or after the setting of DRDY to one.
ERR shall be cleared to zero

8.26.5 Error outputs

Some devices may not report IDNF because they do not range check the address values requested by the host.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

IDNF shall be set to one if ID not found
ABRT shall be set to one if this command not supported.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.26.6 Prerequisites

DRDY set equal to one.

8.26.7 Description

This command allows the host to provide advanced notification that particular data may be requested by the host in a subsequent command. DSC shall be set to one concurrent with or after the setting of DRDY to one when updating the Status register for this command.

8.27 SERVICE

8.27.1 Command code

A2h

8.27.2 Feature set

Overlap and Queued fetaure sets

– Mandatory if the PACKET, Overlapped or Queued feature sets are implemented.

8.27.2 Protocol

Packet or READ/WRITE DMA QUEUED, see 9.10 and 9.11.

8.27.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	A0h							

8.27.4 Outputs

Outputs as a result of a SERVICE command are descibed in the command description for the command for which SERVICE is being requested.

8.27.4 Prerequisites

The device shall have released a previous overlap PACKET, READ DMA QUEUED, or WRITE DMA QUEUED command and shall have set the SERV bit to one to request the SERVICE command be issued to continue data transfer and/or provide command status(see 8.28.12).

8.27.5 Description

The SERVICE command is used to provide data transfer and/or status of a command that was previously released.

For commands that transfer all of the data requested by the command in a single DRQ transfer, the byte count shall contain the total data length. The maximum number of bytes that may be transferred for a read command with a single assertion of DRQ is 65,535 bytes. If a device requests that more data be transferred than required by the command, the host shall pad when data when sending data to the device. The only permissable time for an odd byte count is for the last DRQ assertion associated with a command. The device is not responsible for padding data, only the amount specified by the command shall be transferred to the host.

8.28 SET FEATURES

8.28.1 Command code

EFh

8.28.2 Feature set

General feature set

- Mandatory for all devices.
- Each subcommand is optional except for enable/disable write cache that is mandatory if write cache is implemented.

8.28.2 Protocol

Non-data, see 9.8.

8.28.3 Inputs

Table 16 defines the value of the subcommand in the Feature register. Some subcommands use other registers, such as the Sector Count register to pass additional information to the device.

Register	7	6	5	4	3	2	1	0
Features	Subcommand code							
Sector Count	Subcommand specific							
Sector Number	Subcommand specific							
Cylinder Low	Subcommand specific							
Cylinder High	Subcommand specific							
Device/Head	1	na	1	DEV	na	na	na	na
Command	EFh							

8.28.4 Normal outputs

See the subcommand descriptions.

8.28.5 Error outputs

If any subcommand input value is not supported or is invalid, the device posts an Aborted command error.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this subcommand not supported or if value is invalid.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.28.6 Prerequisites

DRDY shall be set to one.

8.28.7 Description

This command is used by the host to establish parameters which affect the execution of certain device features. Table 16 defines these features.

At power on, or after a hardware reset, the default setting of the functions specified by the subcommands are vendor specific.

Table 16 – SET FEATURES register definitions

Value (see note)	
01h	Retired
02h	Enable write cache
03h	Set transfer mode based on value in Sector Count register. Table 17 defines values.
04h	Obsolete
33h	Obsolete
44h	Obsolete
54h	Obsolete
55h	Disable read look-ahead feature
5Dh	Enable release interrupt
5Eh	Enable Service interrupt
66h	Disable reverting to power on defaults
77h	Obsolete
81h	Retired
82h	Disable write cache
84h	Obsolete
88h	Obsolete
99h	Obsolete
9Ah	Obsolete
AAh	Enable read look-ahead feature
ABh	Obsolete
BBh	Obsolete
CCh	Enable reverting to power on defaults
DDh	Disable release interrupt
DEh	Disable Service interrupt
NOTE – All values not shown are reserved for future definition.	

8.28.8 Enable/disable write cache

Subcommand codes 02h and 82h allow the host to enable or disable write cache in devices that implement write cache. When the subcommand disable write cache is issued, the device shall initiate the sequence to flush cache to non-volatile memory before posting command complete (see 8.5).

8.28.9 Set transfer mode

A host chooses the transfer mechanism by Set Transfer Mode, subcommand code 03h, and specifying a value in the Sector Count register. The upper 5 bits define the type of transfer and the low order 3 bits encode the mode value.

Table 17 – Transfer mode values

Mode	Bits (7:3)	Bits (2:0)
PIO default mode	00000b	000b
PIO default mode, disable IORDY	00000b	001b
PIO flow control transfer mode	00001b	mode #
Retired	00010b	na
Multiword DMA mode	00100b	mode #
Ultra DMA mode	01000b	mode #
Reserved	10000b	na

If a device supports this standard, and receives a SET FEATURES command with a Set Transfer Mode parameter and a Sector Count register value of “00000000b”, it shall set its default PIO mode. If the value is

“00000001b” and the device supports disabling of IORDY, then the device shall set its default PIO mode and disable IORDY.

See vendor specification for the default mode of the commands which are vendor specific.

Devices reporting support for Multi Word DMA Mode 1 shall also support Multi Word DMA Mode 0. Support of IORDY is mandatory when PIO Mode 3 or above is the current mode of operation.

If an Ultra DMA mode is enabled then no Multiword DMA mode shall be enabled. If a Multiword DMA mode is enabled then no Ultra DMA mode shall be enabled.

8.28.10 Enable/disable read look-ahead

Subcommand codes AAh and 55h allow the host to request the device to enable or disable read look-ahead. Error recovery performed by the device with or without retries is vendor specific.

8.28.11 Enable/disable release interrupt

Subcommand codes 5Dh and DDh allow a host to enable or disable the asserting of an interrupt when a device releases the bus for an overlapped PACKET command.

8.28.12 Enable/disable SERVICE interrupt

Subcommand codes 5Eh and DEh allow a host to enable or disable the asserting of an interrupt when DRQ is set to one in response to a SERVICE command.

8.28.13 Enable/disable reverting to defaults

Subcommand codes CCh and 66h allow the host to enable or disable the device from reverting to power on default values. A setting of 66h allows settings which may have been modified since power on to remain at the same setting after a software reset.

8.29 SET MAX ADDRESS

8.29.1 Command code

F9h

8.29.2 Feature set

Host Protected Area feature set.

- Mandatory if the Host Protected Area feature set is implemented.

8.29.2 Protocol

Non-data command, see 9.8.

8.29.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							VV
Sector Number	Max sector number or LBA							
Cylinder Low	Max cylinder low or LBA							
Cylinder High	Max cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Max head or LBA			
Command	F9h							

Sector Count - Value volatile. If bit 0 is set to one, the device shall preserve the maximum values over power-up or hard reset. If bit 0 is cleared to zero, the device shall revert to its native maximum address value over power-up or hard reset.
Sector Number - contains the maximum sector number or LBA value to be set.
Cylinder Low - contains the maximum cylinder low or LBA value to be set.
Cylinder High - contains the maximum cylinder high or LBA value to be set.
Device/Head - if LBA is set to one, the maximum address value is an LBA value. If LBA is cleared to zero, the maximum address value is a CHS value.

8.29.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	Max sector number or LBA							
Cylinder Low	Max cylinder low or LBA							
Cylinder High	Max cylinder high or LBA							
Device/Head	1	na	1	DEV	Max head number or LBA			
Status	BSY	DRDY	na	na	na	na	na	ERR

Sector Number - maximum sector number or LBA set on the device.
Cylinder Low - maximum cylinder number low or LBA set on the device.
Cylinder High - maximum cylinder number high or LBA set on device.
Device/Head - maximum head number or LBA set on the device.
Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.29.5 Error outputs

If this command is not supported or the maximum value to be set exceeds the capacity of the device an Aborted command error shall be returned.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported or maximum value requested exceeds the device capacity.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be set to one if an Error register bit is set to one

8.29.6 Prerequisites

DRDY set equal to one. A successful READ NATIVE MAX ADDRESS command shall immediately precede a SET MAX ADDRESS command.

8.29.7 Description

After successful completion of this command, all read and write access attempts to LBA or CHS addresses greater than specified in the Sector Count, Cylinder High, Cylinder Low and Drive/Head registers shall be rejected with an IDNF error. Identify command data words 1,3,6,54,55,56,57,58,60, and 61 shall reflect the maximum address set with this command.

8.30 SET MULTIPLE MODE

8.30.1 Command code

C6h

8.30.2 Feature set

General feature set
Mandatory for devices not implementing the PACKET Command feature set.
Use prohibited for devices implementing the PACKET Command feature set.

8.30.2 Protocol

Non-data, see 9.8.

8.30.3 Inputs

The Sector Count register contains number of sectors per block to use on all following READ/WRITE MULTIPLE commands. The host shall set Sector Count values equal to 2, 4, 8, 16, 32, 64, or 128.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sectors per block							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	C6h							

8.30.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.30.5 Error outputs

If a block count is not supported, a Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the block count is not supported.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.30.6 Prerequisites

DRDY set equal to one.

8.30.7 Description

This command establishes the block count for READ MULTIPLE and WRITE MULTIPLE commands.

Devices shall support the block size specified in the IDENTIFY DRIVE parameter word 47, bits 7 through 0, and may also support smaller values.

Upon receipt of the command, the device checks the Sector Count register. If the Sector Count register contains a valid value and the block count is supported, the value is used for all subsequent READ MULTIPLE and WRITE MULTIPLE commands and their execution is enabled.

8.31 SLEEP

8.31.1 Command code

E6h

8.31.2 Feature set

Power Management feature set.

- Power Management feature is mandatory if power management is not provided by a PACKET feature set command set.
- Mandatory if the Power Management feature set is implemented.

8.31.2 Protocol

Non-data command, see 9.8.

8.31.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E6h							

8.31.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.31.5 Error outputs

Aborted command - The device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the device does not support the Power Management feature set.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.31.6 Prerequisites

DRDY set equal to one.

8.31.7 Description

This command is the only way to cause the device to enter Sleep mode.

This command causes the device to set the BSY bit to one, prepare to enter Sleep mode, clear the BSY bit to zero and assert INTRQ. The host shall read the Status register in order to clear the interrupt and allow the device to enter Sleep mode. In Sleep mode the interface becomes inactive without affecting the operation of the interface. The host shall not attempt to access the Command Block registers while the device is in Sleep mode.

Because some host systems may not read the Status register and clear the interrupt, a device may automatically deassert INTRQ and enter Sleep mode after a vendor specific time period of not less than 2 s.

The only way to recover from Sleep mode is with a software reset or a hardware reset.

A device shall not power on in Sleep mode nor remain in Sleep mode following a reset sequence.

8.32 SMART

8.32.1 SMART DISABLE OPERATIONS

8.32.1.1 Command code

B0h with a Feature register value of D9h.

8.32.1.2 Feature set

SMART feature set.

- Mandatory if the SMART feature set is implemented
- Use prohibited if the PACKET Command feature set is implemented

8.32.1.2 Protocol

Non-data command, see 9.8.

8.32.1.3 Inputs

The Features register shall be set to D9h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D9h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	na	1	DEV	na	na	na	na
Command	B0h							

8.32.1.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.32.1.5 Error outputs

If the device does not support this command, if SMART is not enabled or if the values in the Features, Cylinder Low or Cylinder High registers are invalid, an Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported, if SMART is not enabled, or if input register values are invalid.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred

DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.32.1.6 Prerequisites

DRDY set equal to one. SMART enabled.

8.32.1.7 Description

This command disables all SMART capabilities within the device including any and all timer and event count functions related exclusively to this feature. After receipt of this command the device shall disable all SMART operations. SMART data shall no longer be monitored or saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles.

After receipt of this command by the device, all other SMART commands (including SMART DISABLE OPERATIONS commands), with the exception of SMART ENABLE OPERATIONS, are disabled and invalid and shall be aborted by the device, returning the Aborted command error.

8.32.2 SMART ENABLE/DISABLE ATTRIBUTE AUTOSAVE

8.32.2.1 Command code

B0h with a Feature register value of D2h.

8.32.2.2 Feature set

SMART feature set.
- Mandatory if the SMART feature set is implemented
- Use prohibited if the PACKET Command feature set is implemented

8.32.2.2 Protocol

Non-data command, see 9.8.

8.32.2.3 Inputs

The Features register shall be set to D2h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h. The Sector Count register is set to 00h to disable attribute autosave and a value of F1h is set to enable attribute autosave.

Register	7	6	5	4	3	2	1	0
Features	D2h							
Sector Count	00h or F1h							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	na	1	DEV	na	na	na	na
Command	B0h							

8.32.2.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.32.2.5 Error outputs

If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low or Cylinder High registers are invalid, an Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported, if SMART is disabled, or if the input register values are invalid.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.32.2.6 Prerequisites

DRDY set equal to one. SMART enabled.

8.32.2.7 Description

This command enables and disables the optional attribute autosave feature of the device. Depending upon the implementation, this command may either allow the device, after some vendor specified event, to automatically save its updated attribute values to non-volitile memory; or this command may cause the autosave feature to be disabled. The state of the attribute autosave feature (either enabled or disabled) shall be preserved by the device across power cycles.

A value of zero written by the host into the device's Sector Count register before issuing this command shall cause this feature to be disabled. Disabling this feature does not preclude the device from saving SMART data to non-volitile memory during some other normal operation such as during a power-on or power-off sequence or during an error recovery sequence.

A value of F1h written by the host into the device's Sector Count register before issuing this command shall cause this feature to be enabled. Any other meaning of this value or any other non-zero value written by the host into this register before issuing this command may differ from device to device. The meaning of any non-zero value written to this register at this time shall be preserved by the device across power cycles.

If this command is not supported by the device, the device shall abort the command upon receipt from the host, returning the Aborted command error.

During execution of the autosave routine the device shall not set BSY to one nor clear DRDY to zero. If the device receives a command from the host while executing its autosave routine it shall respond to the host within two seconds.

8.32.3 SMART ENABLE OPERATIONS

8.32.3.1 Command code

B0h with a Feature register value of D8h.

8.32.3.2 Feature set

SMART feature set.

- Mandatory if the SMART feature set is implemented
- Use prohibited if the PACKET Command feature set is implemented

8.32.3.2 Protocol

Non-data command, see 9.8.

8.32.3.3 Inputs

The Features register shall be set to D8h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D8h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	na	1	DEV	na	na	na	na
Command	B0h							

8.32.3.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete

DRDY shall be set to one
ERR shall be cleared to zero

8.32.3.5 Error outputs

If the device does not support this command or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, an Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -
ABRT shall be set to one if this command not supported or if the input register values are invalid.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.32.3.6 Prerequisites

DRDY set equal to one.

8.32.3.7 Description

This command enables access to all SMART capabilities within the device. Prior to receipt of this command SMART data are neither monitored nor saved by the device. The state of SMART (either enabled or disabled) shall be preserved by the device across power cycles. Once enabled, the receipt of subsequent SMART ENABLE OPERATIONS commands shall not affect any SMART data or functions.

8.32.4 SMART EXECUTE OFF-LINE IMMEDIATE

8.32.4.1 Command code

B0h with the content of the Features register equal to D4h

8.32.4.2 Feature set

SMART feature set.
- Optional if the SMART feature set is implemented
- Use prohibited if the PACKET Command feature set is implemented

8.32.4.2 Protocol

Non-data command, see 9.8.

8.32.4.3 Inputs

The Features register shall be set to D4h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D4h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	na	1	DEV	na			
Command	B0h							

8.32.4.4 Normal Outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete.
DRDY shall be set to one indicating that the device is capable of receiving any command.
ERR shall be cleared to zero.

8.32.4.5 Error Outputs

If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low or Cylinder High registers are invalid, an Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

IDNF shall be set to one if SMART data sector's ID field could not be found.
ABRT shall be set to one if this command is not supported, if SMART is not enabled, or if register values are invalid.
AMNF shall be set to one if a data structure error occurred.

Status register

BSY shall be cleared to zero when the command is complete.
DRDY shall be set to one indicating that the device is capable of receiving any command.
DF shall be set to one indicating that a drive fault has occurred.
DRQ shall be cleared to zero indicating that there is no data to be transferred.
ERR shall be set to one if any Error register bit is set to one.

8.32.4.6 Prerequisites

DRDY set to one. SMART enabled.

8.32.4.7 Description

This command causes the device to immediately initiate the optional set of activities that collect SMART data in an off-line mode and then save this data to the device's non-volatile memory.

During execution of its off-line activities the device shall not set BSY nor clear DRDY.

If the device is in the process of performing its set of off-line data collection activities as a result of receiving a SMART EXECUTE OFF-LINE IMMEDIATE command from the host and is interrupted by any new command from the host except a SMART DISABLE OPERATIONS, SMART EXECUTE OFF-LINE IMMEDIATE or STANDBY IMMEDIATE command, the device shall suspend or abort its off-line data collection activities and service the host within two seconds after receipt of the new command. After servicing the interrupting command from the host the device may immediately re-initiate or resume its off-line data collection activities without any additional commands from the host (see the definition for Bit 2 in the Off-line data collection capability byte in 8.32.5).

If the device is in the process of performing its off-line data collection activities and is interrupted by a STANDBY IMMEDIATE command from the host, the device shall suspend or abort its off-line data collection activities, and service the host within two seconds after receipt of the command. After receiving a new command that causes the device to exit a power saving mode, the device shall initiate or resume off-line data collection activities without any additional commands from the host unless these activities were aborted by the device (see 8.32.5.7).

If the device is in the process of performing its off-line data collection activities and is interrupted by a SMART DISABLE OPERATIONS command from the host, the device shall suspend or abort its off-line data collection activities and service the host within two seconds after receipt of the command. Upon receipt of the next SMART ENABLE OPERATIONS command the device may, after the next vendor specified event, either re-initiate its off-line data collection activities or resume those activities from where they had been previously suspended.

If the device is in the process of performing its off-line data collection activities and is interrupted by a SMART EXECUTE OFF-LINE IMMEDIATE command from the host, the device shall abort its off-line data collection activities and service the host within two seconds after receipt of the command. The device shall then re-initiate its off-line data collection activities in response to the new EXECUTE OFF-LINE IMMEDIATE command.

8.32.5 SMART READ DATA

8.32.5.1 Command code

B0h with the content of the Features register equal to D0h.

8.32.5.2 Feature set

SMART feature set.

- Optional if the SMART feature set is implemented
- Use prohibited if the PACKET Command feature set is implemented

8.32.5.2 Protocol

PIO data in, see 9.6.

8.32.5.3 Inputs

The Features register shall be set to D0h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0

Features	D0h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	na	1	DEV	na			
Command	B0h							

8.32.5.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete.
DRDY shall be set to one indicating that the device is capable of receiving any command.
ERR shall be cleared to zero.

8.32.5.5 Error outputs

If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low, or Cylinder High registers are invalid, an Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register

UNC shall be set to one if SMART data is uncorrectable.
IDNF shall be set to one if SMART data sector's ID field could not be found or data structure checksum occurred.
ABRT shall be set to one if this command is not supported, if SMART is not enabled, or if register values are invalid.
AMNF shall be set to one if a data structure or data structure revision number error occurred.

Status register

BSY shall be cleared to zero when the command is complete.
DRDY shall be set to one indicating that the device is capable of receiving any command.
DF shall be set to one indicating that a drive fault has occurred.
DRQ shall be cleared to zero indicating that there is no data to be transferred.
ERR shall be set to one if any Error register bit is set to one.

8.32.5.6 Prerequisites

DRDY set to one. SMART enabled.

8.32.5.7 Description

This command returns the Device SMART data structure to the host.

The 512 bytes that make up the Device SMART data structure are defined in Table 18. All multi-byte fields shown in this structure follow the byte ordering described in 3.2.7.

Table 18 – Device SMART data structure

Byte	F/V	Descriptions
0-361	X	Vendor specific
362	V	Off-line data collection status
363	X	Vendor specific
364-365	V	Total time in seconds to complete off-line data collection activity
366	X	Vendor specific
367	F	Off-line data collection capability
368-369	F	SMART capability
370-385	R	Reserved
386-510	X	Vendor specific
511	V	Data structure checksum

Key:
F=the content of the byte is fixed and does not change.
V=the content of the byte is variable and may change depending on the state of the device or the commands executed by the device.
X=the content of the byte is vendor specific and may be fixed or variable.
R=the content of the byte is reserved and shall be zero.

The value of the off-line data collection status byte defines the current status of the off-line activities of the device. The values and their respective definitions are listed in Table 19.

Table 19 – Off-line data collection status byte values

Value	Definition
00h or 80h	Off-line data collection activity was never started.
01h	Reserved
02h or 82h	Off-line data collection activity was completed without error.
03h	Reserved
04h or 84h	Off-line data collection activity was suspended by an interrupting command from host.
05h or 85h	Off-line data collection activity was aborted by an interrupting command from host.
06h or 86h	Off-line data collection activity was aborted by the device with a fatal error.
07h-3Fh	Reserved
40h-7Fh	Vendor specific
81h	Reserved
83h	Reserved
87h-BFh	Reserved
C0h-FFh	Vendor specific

The total time in seconds to complete off-line data collection activity word specifies how many seconds the device requires to complete its sequence of off-line data collection activity. Valid values for this word are from 0001h to FFFFh.

Off-line data collection capability

The following describes the definition for the off-line data collection capability bits. If the value of all of these bits is equal to zero, then no off-line data collection is implemented by this device.

– Bit 0 (EXECUTE OFF-LINE IMMEDIATE implemented bit) - If the value of this bit equals one, then the SMART EXECUTE OFF-LINE IMMEDIATE command is implemented by this device. If the value of this bit equals zero, then the SMART EXECUTE OFF-LINE IMMEDIATE command is not implemented by this device.

– Bit 1 (vendor specific).

– Bit 2 (abort/restart off-line by host bit) - If the value of this bit equals one, then the device shall abort all off-line data collection activity initiated by an SMART EXECUTE OFF-LINE IMMEDIATE command upon receipt of a new command. Off-line data collection activity must be restarted by a new SMART EXECUTE OFF-LINE IMMEDIATE command from the host. If the value of this bit equals zero, the device shall suspend off-line data collection activity after an interrupting command and resume off-line data collection activity after some vendor-specified event.

– Bits 3-7 (reserved)

SMART capability

The following describes the definition for the SMART capabilities bits. If the value of all of these bits is equal to zero, then automatic saving of SMART data is not implemented by this device.

– Bit 0 (power mode SMART data saving capability bit) - If the value of this bit equals one, the device shall save its SMART data prior to going into a power saving mode (Idle, Standby or Sleep) or immediately upon return to Active or Idle mode from a Standby mode. If the value of this bit equals zero, the device shall not save its SMART data prior to going into a power saving mode (Idle, Standby or Sleep) or immediately upon return to Active or Idle mode from a Standby mode.

– Bit 1 (SMART data autosave after event capability bit) - The value of this bit shall be equal to one for devices complying with this standard.

– Bits 2-15 (reserved)

The data structure checksum is the two's compliment of the result of a simple eight-bit addition of the first 511 bytes in the data structure.

8.32.6 SMART RETURN STATUS

8.32.6.1 Command code

B0h with a Feature register value of DAh.

8.32.6.2 Feature set

SMART feature set.
- Mandatory if the SMART feature set is implemented
- Use prohibited if the PACKET Command feature set is implemented

8.32.6.2 Protocol

Non-data command, see 9.8.

8.32.6.3 Inputs

The Features register shall be set to DAh. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	DAh							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	na	1	DEV	na	na	na	na
Command	B0h							

8.32.6.4 Normal outputs

If the device has not detected a threshold exceeded condition, the device sets the Cylinder Low register to 4Fh and the Cylinder High register to C2h. If the device has detected a threshold exceeded condition, the device sets the Cylinder Low register to F4h and the Cylinder High register to 2Ch.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh or F4h							
Cylinder High	C2h or 2Ch							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Cylinder Low - 4Fh if threshold not exceeded, F4h if threshold exceeded
Cylinder High - C2h if threshold not exceeded, 2Ch if threshold exceeded
Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.32.6.5 Error outputs

If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low or Cylinder High registers are invalid, an Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if this command not supported, if SMART is disabled, or if the input register values are invalid.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.32.6.6 Prerequisites

DRDY set equal to one. SMART enabled.

8.32.6.7 Description

This command is used to communicate the reliability status of the device to the host at the host's request. If a threshold exceeded condition is not detected by the device, the device shall set the Cylinder Low register to 4Fh and the Cylinder High register to C2h. If a threshold exceeded condition is detected by the device, the device shall set the Cylinder Low register to F4h and the Cylinder High register to 2Ch.

8.32.7 SMART SAVE ATTRIBUTE VALUES

8.32.7.1 Command code

B0h with a Feature register value of D3h.

8.32.7.2 Feature set

SMART feature set.

- Optional and not recommended if the SMART feature set is implemented
- Use prohibited if the PACKET Command feature set is implemented

8.32.7.2 Protocol

Non-data command, see 9.8.

8.32.7.3 Inputs

The Features register shall be set to D3h. The Cylinder Low register shall be set to 4Fh. The Cylinder High register shall be set to C2h.

Register	7	6	5	4	3	2	1	0
Features	D3h							
Sector Count	na							
Sector Number	na							
Cylinder Low	4Fh							
Cylinder High	C2h							
Device/Head	1	na	1	DEV	na	na	na	na
Command	B0h							

8.32.7.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.32.7.5 Error outputs

If the device does not support this command, if SMART is disabled or if the values in the Features, Cylinder Low or Cylinder High registers are invalid, an Aborted command error is posted.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -
ABRT shall be set to one if this command not supported, if SMART is disabled, or if the input register values are invalid.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.32.7.6 Prerequisites

DRDY set equal to one. SMART enabled.

8.32.7.7 Description

This command causes the device to immediately save any updated attribute values to the device's non-volatile memory regardless of the state of the attribute autosave timer.

8.33 STANDBY

8.33.1 Command code

E2h

8.33.2 Feature set

Power Management feature set.
- Power Management feature is mandatory if power management is not provided by a PACKET feature set command set.
- Mandatory if the Power Management feature set is implemented.

8.33.2 Protocol

Non-data command, see 9.8.

8.33.3 Inputs

The value in the Sector Count register when the STANDBY command is issued shall determine the time period programmed into the Standby timer. Table 12 defines these values.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Time period value							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E2h							

8.33.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.33.5 Error outputs

Aborted command if the device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the Power Management feature set is not supported.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.33.6 Prerequisites

DRDY set equal to one.

8.33.7 Description

This command causes the device to enter the Standby mode.

If the Sector Count register is non-zero then the Standby timer shall be enabled. The value in the Sector Count register shall be used to determine the time programmed into the Standby timer.

If the Sector Count register is zero then the Standby timer is disabled.

8.34 STANDBY IMMEDIATE

8.34.1 Command code

E0h

8.34.2 Feature set

Power Management feature set.

- Power Management feature is mandatory if power management is not provided by a PACKET feature set command set.
- Mandatory if the Power Management feature set is implemented.

8.34.2 Protocol

Non-data command, see 9.8.

8.34.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E0h							

8.34.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.34.5 Error outputs

Aborted command - The device does not support the Power Management feature set.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ABRT shall be set to one if the Power Management feature set is not supported.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.34.6 Prerequisites

DRDY set equal to one.

8.34.7 Description

This command causes the device to immediately enter the Standby mode.

8.35 WRITE BUFFER

8.35.1 Command code

E8h

8.35.2 Feature set

General feature set

- Optional for devices not implementing the PACKET Command feature set.
- Use prohibited for devices implementing the PACKET Command feature set.

8.35.2 Protocol

PIO data out, see 9.7.

8.35.3 Inputs

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Command	E8h							

8.35.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.35.5 Error outputs

Aborted command if the command is not supported.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	na	na	ABRT	na	na
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -
ABRT shall be set to one if this command not supported.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.35.6 Prerequisites

DRDY set equal to one.

8.35.7 Description

This command enables the host to write the contents of one sector in the device's buffer.

The READ BUFFER and WRITE BUFFER commands shall be synchronized within the device such that sequential WRITE BUFFER and READ BUFFER commands access the same 512 bytes within the buffer.

8.36 WRITE DMA

8.36.1 Command code

CAh or CBh

8.36.2 Feature set

General feature set

Mandatory for devices not implementing the PACKET Command feature set.
Use prohibited for devices implementing the PACKET Command feature set.

8.36.2 Protocol

DMA or Ultra DMA, see 9.9 or 9.13.

8.36.3 Inputs

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	CAh or CBh							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) starting head number or LBA address bits (27:24)

8.36.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.36.5 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Register	7	6	5	4	3	2	1	0
Error	ICRC	na	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data burst. The content of this bit is not applicable for Multiword DMA transfers.

IDNF shall be set to one if sector's ID field could not be found

ABRT shall be set to one if this command not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data burst.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be writen with address of first unrecoverable error.

Status register -

BSY shall be cleared to zero when the command is complete

DRDY shall be set to one

DF shall be set to one if a drive fault has occurred

DRQ shall be cleared to zero

ERR shall be set to one if an Error register bit is set to one

8.36.6 Prerequisites

DRDY set equal to one. The host shall initialize the DMA channel.

8.36.7 Description

The WRITE DMA command allows the host to write data using the DMA data transfer protocol.

8.37 WRITE DMA QUEUED

8.37.1 Command code

CCh

8.37.2 Feature set

Overlap and Queued feature set
Mandatory for devices not implementing the PACKET Command feature set.
Use prohibited for devices implementing the PACKET Command feature set.

8.37.3 Protocol

DMA QUEUED or Ultra DMA.

8.37.4 Inputs

Register	7	6	5	4	3	2	1	0
Features	Sector Count							

Sector Count	Tag					na	na	na
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	D	Head number or LBA			
Command	C7h							

Features - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector count - if the device supports command queuing, bits (7:3) contain the tag for the command being delivered.
Sector number - starting sector number or LBA address bits (7:0).
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8).
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16).
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address; bits (3:0) starting head number or LBA address bits (27:24).

8.37.5 Normal outputs

8.37.5.1 Release

If the device releases before transferring data for this command, the register content upon release shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	Tag					REL	I/O	C/D
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY		SERV	DRQ	na	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the command being released. If the device does not support command queuing, this field shall be zeros.
Bit 2 - REL bit shall be set indicating that the device has released an overlap command.
Bit 1 - I/O shall be cleared to zero.
Bit 0 - C/D shall be cleared to zero.

Status register -

Bit 7 - BSY shall be cleared to zero.
Bit 6 - DRDY shall be set to one.
Bit 4 - SERV shall be cleared to zero when the device releases. This bit shall be set to one when the device is ready to transfer data.
Bit 3 - DRQ bit shall be cleared to zero.
Bit 0 - ERR bit shall be cleared to zero.

8.37.5.2 Command complete

When the transfer of all requested data has occurred without error, the register content shall be as shown below.

Register	7	6	5	4	3	2	1	0
Error	00h							
Sector Count	Tag					REL	I/O	C/D

Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	D	na			
Status	BSY	DRDY	na	SERV	DRQ	na	na	ERR

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.
Bit 2 - REL shall be cleared to zero.
Bit 1 - I/O shall be set to one.
Bit 0 - C/D shall be set to one

Status register -

Bit 7 - BSY shall be cleared to zero.
Bit 6 - DRDY shall be set to one..
Bit 4 - SERV shall be cleared to zero.
Bit 3 - DRQ bit shall be cleared to zero.
Bit 0 - ERR bit shall be cleared to zero.

8.37.6 Error outputs

The Sector Count register contains the tag for this command if the device supports command queuing. Aborted command if the command is not supported or if the device has not had overlapped interrupt enabled. Aborted command if the device supports command queuing and the tag is invalid. An unrecoverable error encountered during the execution of this command results in the termination of the command and the Command Block registers contain the sector where the first unrecoverable error occurred. If a queue existed, the unrecoverable error shall cause the queue to abort. The device may remain BSY for some time when responding to these errors.

Register	7	6	5	4	3	2	1	0
Error	ICRC	na	na	IDNF	na	ABRT	na	na
Sector Count	Tag					REL	I/O	C/D
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	D	Head number or LBA			
Status	BSY	DRDY	DF	SERV	DRQ	na	na	ERR

Error register -

ICRC shall be set to one if an interface CRC error has occurred during an Ultra DMA data transfer. The content of this bit is not applicable for Multiword DMA data transfers.
IDNF shall be set to one if sector's ID field could not be found.
ABRT shall be set to one if this command not supported or if an error, including an ICRC error, has occurred during an Ultra DMA data transfer.

Sector Count register -

Bits 7-3 - Tag - If the device supports command queuing, this field shall contain the tag of the completed command. If the device does not support command queuing, this field shall be zeros.
Bit 2 - REL shall be cleared to zero.
Bit 1 - I/O shall be set to one.
Bit 0 - C/D shall be set to one

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

Status register -

BSY shall be cleared to zero.
DRDY shall be set to one.
DF shall be set to one if a drive fault has occurred.

DRQ shall be cleared to zero.
ERR shall be set to one if an Error register bit is set to one.

8.37.7 Prerequisites

DRDY set to one. The host shall initialize the DMA channel.

8.37.8 Description

This command executes in a similar manner to a WRITE DMA command. The device may release the bus or it may execute the data transfer without release if the data is ready to transfer.

If a release is executed, the host shall reselect the device using the SERVICE command.

See for the protocol utilized for overlapped commands.

8.38 WRITE MULTIPLE

8.38.1 Command code

C5h

8.38.2 Feature set

General feature set
Mandatory for devices not implementing the PACKET Command feature set.
Use prohibited for devices implementing the PACKET Command feature set.

8.38.2 Protocol

PIO data out, see 9.7.

8.38.3 Inputs

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	C5h							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) starting head number or LBA address bits (27:24)

8.38.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							

Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.38.5 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -
IDNF shall be set to one if sector's ID field could not be found
ABRT shall be set to one if this command not supported.
Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.38.6 Prerequisites

DRDY set equal to one. If bit 8 of Word 59 in the IDENTIFY DEVICE response is equal to zero, a successful SET MULTIPLE MODE command shall proceed a WRITE MULTIPLE command.

8.38.7 Description

This command is similar to the WRITE SECTOR(S) command. Interrupts are not generated on every sector, but on the transfer of a block that contains the number of sectors defined by SET MULTIPLE MODE or the default if no intervening SET MULTIPLE command has been issued..

Command execution is identical to the WRITE SECTOR(S) operation except that the number of sectors defined by the SET MULTIPLE MODE command are transferred without intervening interrupts. The DRQ bit qualification of the transfer is required only at the start of the data block, not on each sector.

The block count of sectors to be transferred without intervening interrupts is the default or programmed by the SET MULTIPLE MODE command, which shall be executed prior to the WRITE MULTIPLE command.

When the WRITE MULTIPLE command is issued, the Sector Count register contains the number of sectors (not the number of blocks or the block count) requested.

If the number of requested sectors is not evenly divisible by the block count, as many full blocks as possible are transferred, followed by a final, partial block transfer. The partial block transfer is for n sectors, where:

n = Remainder (sector count/ block count).

If the WRITE MULTIPLE command is received when WRITE MULTIPLE commands are disabled, the Write Multiple operation shall be rejected with an Aborted command error.

Device errors encountered during WRITE MULTIPLE commands are posted after the attempted device write of the block or partial block transferred. The Write command ends with the sector in error, even if it was in the middle of a block. Subsequent blocks are not transferred in the event of an error.

The contents of the Command Block Registers following the transfer of a data block which had a sector in error are undefined. The host should retry the transfer as individual requests to obtain valid error information. Interrupts are generated when the DRQ bit is set to one at the beginning of each block or partial block.

8.39 WRITE SECTOR(S)

8.39.1 Command code

30h or 31h

8.39.2 Feature set

General feature set
Mandatory for devices not implementing the PACKET Command feature set.
Use prohibited for devices implementing the PACKET Command feature set.

8.39.2 Protocol

PIO data out, see 9.7.

8.39.3 Inputs

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	30h or 31h							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address

bits (3:0) starting head number or LBA address bits (27:24)

8.39.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.39.5 Error outputs

An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Register	7	6	5	4	3	2	1	0
Error	na	na	na	IDNF	na	ABRT	na	na
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -
IDNF shall be set to one if sector's ID field could not be found
ABRT shall be set to one if this command not supported.
Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.
Status register -
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.39.6 Prerequisites

DRDY set equal to one.

8.39.7 Description

This command writes from 1 to 256 sectors as specified in the Sector Count register. A sector count of 0 requests 256 sectors.

8.40 WRITE VERIFY

8.40.1 Command code

3Ch

8.40.2 Feature set

General feature set
Optional for devices not implementing the PACKET Command feature set.
Use prohibited for devices implementing the PACKET Command feature set.

8.40.2 Protocol

PIO data out, see 9.7.

8.40.3 Inputs

The Cylinder Low, Cylinder High, Device/Head and Sector Number specify the starting sector address to be written. The Sector Count register specifies the number of sectors to be transferred.

Register	7	6	5	4	3	2	1	0
Features	na							
Sector Count	Sector count							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	LBA	1	DEV	Head number or LBA			
Command	3Ch							

Sector Count - number of sectors to be transferred. A value of 00h indicates that 256 sectors are to be transferred.
Sector Number - starting sector number or LBA address bits (7:0)
Cylinder Low - starting cylinder number bits (7:0) or LBA address bits (15:8)
Cylinder High - starting cylinder number bits (15:8) or LBA address bits (23:16)
Device/Head - bit 6 set to one if LBA address, cleared to zero if CHS address
bits (3:0) starting head number or LBA address bits (27:24)

8.40.4 Normal outputs

Register	7	6	5	4	3	2	1	0
Error	na							
Sector Count	na							
Sector Number	na							
Cylinder Low	na							
Cylinder High	na							
Device/Head	1	na	1	DEV	na	na	na	na
Status	BSY	DRDY	na	na	na	na	na	ERR

Status register
BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
ERR shall be cleared to zero

8.40.5 Error outputs

Aborted command if the command is not supported. An unrecoverable error encountered during the execution of this command results in the termination of the command. The Command Block registers contain the address of the sector where the first unrecoverable error occurred. The amount of data transferred is indeterminant.

Register	7	6	5	4	3	2	1	0
Error	na	UNC	na	IDNF	na	ABRT	na	AMNF
Sector Count	na							
Sector Number	Sector number or LBA							
Cylinder Low	Cylinder low or LBA							
Cylinder High	Cylinder high or LBA							
Device/Head	1	na	1	DEV	Head number or LBA			
Status	BSY	DRDY	DF	na	DRQ	na	na	ERR

Error register -

UNC shall be set to one if an uncorrectable data error is found
IDNF shall be set to one if sector's ID field could not be found
ABRT shall be set to one if this command not supported.
AMNF shall be set to one if the data address mark could not be found after finding correct ID field.

Sector Number, Cylinder Low, Cylinder High, Device/Head - shall be written with the address of first unrecoverable error.

Status register -

BSY shall be cleared to zero when the command is complete
DRDY shall be set to one
DF shall be set to one if a drive fault has occurred
DRQ shall be cleared to zero
ERR shall be set to one if an Error register bit is set to one

8.40.6 Prerequisites

DRDY set equal to one.

8.40.7 Description

This command is similar to the WRITE SECTOR(S) command, except that each sector is verified before the command is completed.

9 Protocol

Commands are grouped into different classes according to the protocols followed for command execution. The command classes with their associated protocols are defined below.

For all commands, the host first checks if the BSY bit is equal to one, and should proceed no further unless and until the BSY bit is equal to zero. For most commands, the host shall also wait for the DRDY bit to be equal to one before proceeding.

Data transfers may be accomplished in more ways than are described below, but these sequences should work with all known implementations of devices.

A device shall maintain either the BSY bit equal to one or the DRQ bit equal to one at all times until the command is completed. The INTRQ signal is used by the device to signal most, but not all, times when the BSY bit is changed from one to zero during command execution.

A command shall only be interrupted with a hardware or software reset. The result of writing to the Command register while the BSY bit is equal to one or the DRQ bit is equal to one is unpredictable and may result in data corruption.

9.1 Signature and persistence

A device shall place a signature in the Command Block registers for power on reset, hardware reset, soft reset , or the DEVICE RESET command. If the device does not implement the PACKET command feature set, the signature shall be:

Error	00h
Sector Count	01h
Sector Number	01h
Cylinder Low	00h
Cylinder High	00h
Device/Head	00h

If the device implements the PACKET command feature set, the signature shall be:

Error	01h
Sector Count	01h
Sector Number	01h
Cylinder Low	14h
Cylinder High	EBh
Device/Head	00h

If the PACKET command feature set is implemented by a device, then the signature values placed by the device in the Command Block registers following power on reset, hardware reset, soft reset or the DEVICE RESET command shall not be changed by the device until the device receives a PACKET command or an IDENTIFY DEVICE PACKET command. Writes by the host to the Command Block registers that contain the signature values shall overwrite the signature values and invalidate the signature.

9.2 Power on and hardware resets

This clause describes the algorithm and timing relationships for Device 0 and Device 1 during the processing of power on and hardware resets.

If the host asserts RESET- while a device is in or going to a power management mode, then the device shall execute its hardware reset sequence.

If the host reasserts RESET- before devices have completed executing their power on or hardware reset sequences, then the devices shall restart executing their hardware reset sequence at step (2).

The host should not set the SRST bit to one in the Device Control register while the BSY bit is set to one in either devices' Status register as a result of executing a power on or hardware reset sequence. If the host sets the SRST bit in the Device Control register to one before the devices have completed execution of their power on or hardware reset sequences, then the devices shall ignore the soft reset.

A host should issue an IDENTIFY DEVICE and/or IDENTIFY DEVICE PACKET command after a issuing a software reset in order to correctly determine the current status of features implemented by the device(s).

9.2.1 Power on and hardware resets - device 0

The following steps should occur sequentially as listed. Several of the steps may occur concurrently or outside of the listed sequence when explicitly allowed so long as all timing relationships are satisfied, e.g.: Device 0 may continue to sample DASP- after Device 0 has completed its hardware initialization and self-diagnostic testing.

Steps (2) through (15) shall be completed within 31s from negation of RESET- by the host.

1) The host shall assert RESET- for a minimum of 25 µs after power to the device has stabilized within the system's specified tolerance. The device shall not recognize a signal assertion shorter than 20 ns as a valid reset signal. Devices may respond to any signal assertion greater than 20 ns and shall recognize a signal equal to or greater than 25 us;
2) The device shall release PDIAG-, INTRQ, IORDY, DMARQ and DD(15:0) no later than 400 ns after RESET- is negated;
3) The device shall set the BSY bit to one no later than 400 ns after RESET- is negated;
4) The device shall determine that it is Device 0;
5) If DASP- is asserted by the device, then the device shall release DASP- no later than 1 ms afterRESET- is negated;
6) Steps (2), (3), (4) and (5) shall be completed before continuing;
7) Device 0 shall sample DASP- for assertion by Device 1. Device 0 may sample DASP- at any frequency. This sampling shall not begin until at least 1 ms after RESET- is negated. Device 0 may stop sampling DASP- upon detection of its assertion. The last sample of DASP- by Device 0 shall occur no sooner than 450 ms after RESET- is negated if assertion has not been detected before this time. Device 0 shall not sample DASP- later than 5 s after RESET- is negated;
8) Step (7) shall be completed before executing the following: Device 0 shall store whether or not Device 1 was detected in step (7). This information is needed to process any future Software reset or EXECUTE DEVICE DIAGNOSTIC command. This information shall be saved by Device 0 until the next power on or hardware reset;
9) Device 0 should begin performing its hardware initialization and self-diagnostic testing;
10) Device 0 may revert to its default condition (the device's settings may now be in different conditions than they were before RESET- was asserted by the host) All Ultra DMA modes shall be disabled;
11) Step (7) shall be completed before executing the following: if Device 0 did not detect that DASP- was asserted by Device 1 during step (7) (i.e.: Device 1 is not present), then Device 0 shall clear bit 7 to zero in the Error register and go to step (13);
12) Device 0 shall sample PDIAG- for assertion by Device 1. Device 0 may sample PDIAG- at any frequency. This sampling shall not begin until at least 1 ms after RESET- is negated. Device 0 may stop sampling PDIAG- upon detection of its assertion. The last sample of PDIAG- by Device 0 shall occur no sooner than 450 ms after RESET- is negated if assertion has not been detected before this time. Device 0 shall not sample PDIAG- later than 31 s after RESET- is negated;
    a) If Device 0 detects that PDIAG- is asserted within 31 s after RESET- is negated, then Device 0 shall clear bit 7 to zero in the Error register;
    b) If Device 0 does not detect that PDIAG- is asserted within 31 s after RESET- is negated, then Device 0 shall set bit 7 to one in the Error register;
13) If performed, the hardware initialization and self-diagnostic testing initiated in step (9) shall be completed before executing the following: Device 0 shall write its self-diagnostic testing results to bits 6-0 in the Error register. See Table 8;

14) Device 0 shall set its signature values in the Command Block registers (see 9.1);
15) Device 0 shall clear to zero bits 5, 4, 3, 2, and 0 in the Status register;
16) Clearing BSY:
    a) If the PACKET command feature set is not implemented by Device 0, then steps (8), (10), (11), (12) (as required), (13) and (14) shall be completed before executing the following: Device 0 shall clear the BSY bit to zero when ready to accept commands that do not require the DRDY bit to be equal to one;
    b) If the PACKET command feature set is implemented by Device 0, then Device 0 shall return its operating modes to their specified initial conditions: MODE SELECT conditions shall be restored to their last saved values if saved values have been established; MODE SELECT conditions for which no values have been saved shall be returned to their default values; then Device 0 shall clear the BSY bit to zero;
17) Setting DRDY:
    a) If the PACKET command feature set is not implemented by Device 0, then the DRDY bit shall be set to one within 30 s after the BSY bit has been cleared to zero. Steps (16) (a) and (17) (a) may occur at the same time;
    b) If the PACKET command feature set is implemented by Device 0, then Device 0 shall not set DRDY to one;

9.2.2 Power on and hardware resets - device 1

The following steps should occur sequentially as listed. Several of the steps may occur concurrently or outside of the listed sequence when explicitly allowed so long as all timing relationships are satisfied.

Steps (2) through (13) shall be completed by Device 1 within 30 s from negation of RESET- by the host.

1) The host shall assert RESET- for a minimum of 25 µs after power to the device has stabilized within the system's specified tolerance. The device shall not recognize a signal assertion shorter than 20 ns as a valid reset signal. Devices may respond to any signal assertion greater than 20 ns and shall recognize a signal equal to or greater than 25 us;
2) The device shall release INTRQ, IORDY, DMARQ and DD(15:0) no later than 400 ns after RESET- is negated;
3) The device shall set the BSY bit to one no later than 400 ns after RESET- is negated;
4) The device shall determine that it is Device 1;
5) Device 1 shall negate PDIAG- no later than 1 ms after RESET- is negated;
6) Steps (2), (3), (4) and (5) shall be completed before continuing;
7) Device 1 shall assert DASP- no later than 400 ms after RESET- is negated:
8) Device 1 should begin performing its hardware initialization and self-diagnostic testing;
9) Device 1 may revert to its default condition (the device's settings may now be in different conditions than they were before the RESET- was asserted by the host). All Ultra DMA modes shall be disabled;
10) If performed, the hardware initialization and self-diagnostic testing initiated in step (8) shall be completed before executing the following: Device 1 shall write its self-diagnostic testing results to the Error register. See Table 8;
11) Device 1 shall set its signature values in the Command Block registers (see 9.1);
12) Device 1 shall clear to zero bits 5, 4, 3, 2, and 0 in the Status register;
13) Clearing BSY:
    a) If the PACKET command feature set is not implemented by Device 1, then steps (7), (9), (10) and (11) shall be completed before executing the following: Device 1 shall clear the BSY bit to zero when ready to accept commands that do not require the DRDY bit to be equal to one;
    b) If the PACKET command feature set is implemented by Device 1, then Device 1 shall return its operating modes to their specified initial conditions: MODE SELECT conditions shall be restored to their last saved values if saved values have been established; MODE SELECT conditions for which no values have been saved shall be returned to their default values; then Device 1 shall clear the BSY bit to zero;
14) Step (12) shall be completed before executing the following: If Device 1 passed its self-diagnostic testing, then Device 1 shall assert PDIAG-;
15) Setting DRDY:

a) If the PACKET command feature set is not implemented by Device 1, then the DRDY bit shall be set to one within 30 s after the BSY bit has been cleared to zero. Steps (13) (a), (14), and (15) (a) may occur at the same time;
b) If the PACKET command feature set is implemented by Device 1, then Device 1 shall not set DRDY to one;

16) Device 1 shall continue to assert DASP- and PDIAG- until after the first command is received from the host or until at least 31 s after RESET- is negated or until detecting that the host has set the SRST bit to one in the Device Control register, whichever comes first;

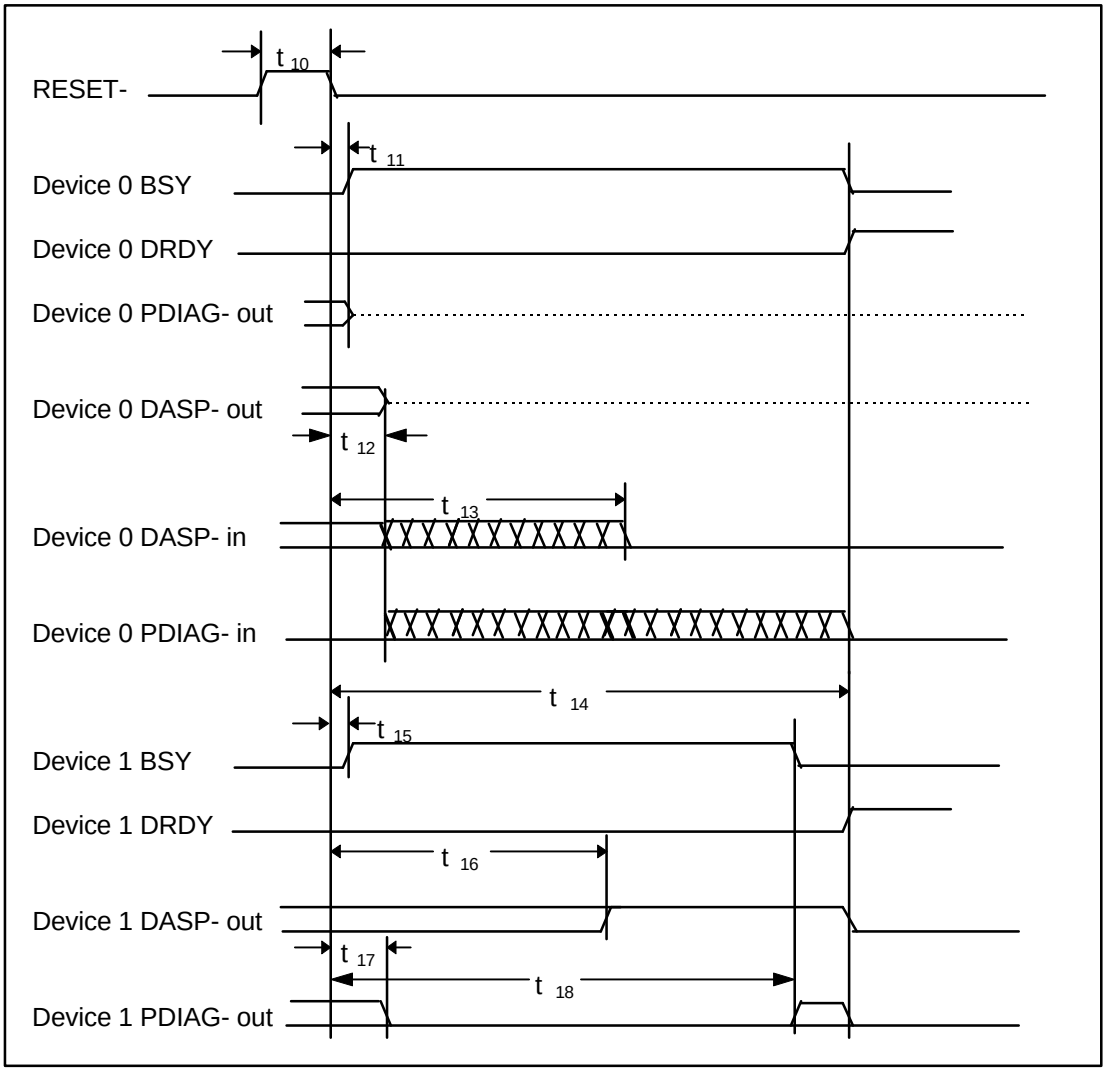


Figure 6 – BSY and DRDY timing for power on and hardware resets

Table 20 – BSY and DRDY timing for power on and hardware resets

RESET timing parameters		Min	Max	Note
t_{10}	RESET pulsewidth	25 µs		1
t_{11}	Device 0 RESET negation to BSY bit set to one, release PDIAG-		400 ns	
t_{12}	Device 0 release DASP-		1 ms	
t_{13}	Device 0 sample of DASP-	1 ms	450 ms	2
t_{14}	Device 0 sample of PDIAG-	1 ms	31 s	3
t_{15}	Device 1 RESET negation to BSY bit set to one			
t_{16}	Device 1 assert DASP-		400 ms	
t_{17}	Device 1 negate PDIAG- if asserted		1 ms	
t_{18}	Device 1 assert PDIAG-		30 s	4

Notes:
1 The device shall not recognize a RESET assertion pulse width shorter than 20 ns as a valid signal assertion.
2 Device 0 shall sample beginning 1 ms after RESET is negated. Sampling shall continue until DASP- assertion by Device 1 is sensed or 450 ms has elapsed indicating no Device 1 present.
3 Device 0 shall sample beginning 1 ms after RESET is negated. Sampling shall continue until:

a) no DASP- assertion is sensed in 450 ms,
b) DASP- assertion is sensed in 450 ms and PDIAG- assertion is sensed,
c) or DASP- assertion is sensed in 450 ms and no PDIAG- assertion is sensed in 31s.

When sampling is stopped, Device 0 shall clear the BSY bit to zero. DRDY shall be set to one when Device 0 is ready to accept any command. No maximum time is specified but a host should allow up to 30 s from the time RESET is negated.
4 Upon completion of internal diagnostics, Device 1 shall clear BSY to zero, and if diagnostics passed, assert PDIAG-. Internal diagnostics shall complete within 30 s of the negation of RESET.

9.3 Software reset

This clause describes the algorithm and timing relationships for Device 0 and Device 1 during the processing of software resets.

If the host sets the SRST bit in the Device Control register to one while a device is in or going to a power management mode, then the device shall execute its software reset sequence.

If the host asserts RESET- before devices have completed executing their software reset sequences, then the devices shall start executing their hardware reset sequence at step (2).

The host should not set the SRST bit to one in the Device Control register while the BSY bit is set to one in either devices' Status register as a result of executing a software reset sequence. If the host sets the SRST bit in the Device Control register to one before the devices have completed execution of their software reset sequences, then the devices shall restart executing their software reset sequences at step (2).

A host should issue an IDENTIFY DEVICE and/or IDENTIFY DEVICE PACKET command after a issuing a software reset in order to correctly determine the current status of features implemented by the device(s).

9.3.1 Software reset - device 0

The following steps should occur sequentially as listed. Several of the steps may occur concurrently or outside of the listed sequence when explicitly allowed so long as all timing relationships are satisfied, e.g.:

Device 0 may continue to sample PDIAG- after Device 0 has completed writing the specified values to the Sector Count, Sector Number, Cylinder Low, Cylinder High and Device/Head registers.

Steps (7) through (11) shall be completed within 31 s from Device 0 detecting that the SRST bit is cleared to zero.

1) The host shall set the SRST bit to one in the Device Control register. The host shall not clear the SRST bit to zero until at least 5 µs after setting the bit to one. The host shall not set the SRST bit to one until the bit has been cleared to zero for at least 5 µs;
2) The device shall release PDIAG-, INTRQ, IORDY, DMARQ and DD(15:0) no later than 400 ns after detecting that the SRST bit is equal to one;
3) Device 0 shall set the BSY bit to one no later than 400 ns after detecting that the SRST bit is equal to one;
4) Device 0 should begin performing its hardware initialization and self-diagnostic testing;
5) Reverting to default:
    1) If the PACKET command feature set is not implemented by Device 0, then Device 0 may revert to its default condition (the device's settings may now be in different conditions than they were before the SRST bit was set to one by the host);
    2) If the PACKET command feature set is implemented by Device 0, then Device 0 shall not revert to its default condition;
6) Device 0 shall wait for the host to clear the SRST bit to zero before continuing;
7) If Device 0 did not detect that DASP- was asserted by Device 1 during the most recent power cycle or hardware reset, then Device 0 shall clear bit 7 in the Error register to zero and go to step (9);
8) If Device 0 detected that DASP- was asserted by Device 1 during the most recent power cycle or hardware reset, then Device 0 shall sample PDIAG- for assertion by Device 1. Device 0 may sample PDIAG- at any frequency. This sampling shall not begin until at least 1 ms after SRST is cleared to zero. Device 0 may stop sampling PDIAG- upon detection of assertion. Device 0 shall not sample PDIAG- after the first command is received or later than 31 s after SRST is cleared to zero;
    a) If Device 0 detects that PDIAG- is asserted within 31 s after SRST is cleared to zero, then Device 0 shall clear bit 7 to zero in the Error register;
    b) If Device 0 does not detect that PDIAG- is asserted within 31 s after SRST is cleared to zero, then Device 0 shall set bit 7 to one in the Error register;
9) If performed, the hardware initialization and self-diagnostic testing initiated in step (4) shall be completed before executing the following: Device 0 shall write its self-diagnostic testing results to bits 6-0 in the Error register. See Table 8;
10) Device 0 shall set its signature values in the Command Block registers (see 9.1);
11) Device 0 shall clear to zero bits 5, 4, 3, 2, and 0 in the Status register;
12) Clearing BSY:
    a) If the PACKET command feature set is not implemented by Device 0, then Steps (7), (8) (as required), (9) and (10) shall be completed before executing the following: Device 0 shall clear the BSY bit to zero when ready to accept commands that do not require the DRDY bit to be equal to one.
    b) If the PACKET command feature set is implemented by Device 0, then Device 0 shall return its operating modes to their specified initial conditions: MODE SELECT conditions shall be restored to their last saved values if saved values have been established; MODE SELECT conditions for which no values have been saved shall be returned to their default values; then Device 0 shall clear the BSY bit to zero;
13) Setting DRDY:
    a) If the PACKET command feature set is not implemented by Device 0, then the DRDY bit shall be set to one within 30 s after the BSY bit has been cleared to zero. Steps (12) (a) and (13) (a) may occur at the same time;
    b) If the PACKET command feature set is implemented by Device 0, then Device 0 shall not set DRDY to one;

9.3.2 Software reset - device 1

The following steps should occur sequentially as listed. Several of the steps may occur concurrently or outside of the listed sequence when explicitly allowed so long as all timing relationships are satisfied.

Steps (8) through (11) shall be completed within 30 s from Device 1 detecting that the SRST bit is cleared to zero.

1) The host shall set the SRST bit to one in the Device Control register. The host shall not clear the SRST bit to zero until at least 5 µs after setting the bit to one. The host shall not set the SRST bit to one until the bit has been cleared to zero for at least 5 µs;
2) The device shall release INTRQ, IORDY, DMARQ and DD(15:0) no later than 400 ns after detecting that the SRST bit is equal to one;
3) Device 1 shall set the BSY bit to one no later than 400 ns after detecting that the SRST bit is equal to one;
4) Device 1 shall negate PDIAG- no later than 1 ms after detecting that the SRST bit is equal to one;
5) Device 1 should begin performing its hardware initialization and self-diagnostic testing;
6) Reverting to default:
   a) If the PACKET command feature set is not implemented by Device 1, then Device 1 may revert to its default condition (the device's settings may now be in different conditions than they were before the SRST bit was set to one by the host);
   b) If the PACKET command feature set is implemented by Device 1, then Device 1 shall not revert to its default condition;
7) Device 1 shall wait for the host to clear the SRST bit to zero before continuing;
8) If performed, the hardware initialization and self-diagnostic testing initiated in step (5) shall be completed before executing the following: Device 1 shall write its self-diagnostic testing results to the Error register. See Table 8;
9) Device 1 shall set its signature values in the Command Block registers (see 9.1);
10) Device 0 shall clear to zero bits 5, 4, 3, 2, and 0 in the Status register;
11) Clearing BSY:
   a) If the PACKET command feature set is not implemented by Device 1, then steps (8) and (9) shall be completed before executing the following: Device 1 shall clear the BSY bit to zero when ready to accept commands that do not require the DRDY bit to be equal to one;
   b) If the PACKET command feature set is implemented by Device 1, then Device 1 shall return its operating modes to their specified initial conditions: MODE SELECT conditions shall be restored to their last saved values if saved values have been established; MODE SELECT conditions for which no values have been saved shall be returned to their default values; then Device 1 shall clear the BSY bit to zero;
12) Step (10) shall be completed before executing the following: If Device 1 passed its self-diagnostic testing, then Device 1 shall assert PDIAG-;
13) Setting DRDY:
   1) If the PACKET command feature set is not implemented by Device 1, then the DRDY bit shall be set to one within 30 s after the BSY bit has been cleared to zero. Steps (11) (a), (12), and (13) (a) may occur at the same time;
   2) If the PACKET command feature set is implemented by Device 1, then Device 1 shall not set DRDY to one;
14) Device 1 shall continue to assert PDIAG- until after the first command is received from the host or until at least 31 s after detecting that SRST is cleared to zero or until detecting that the host has set the SRST bit to one in the Device Control register, whichever comes first.

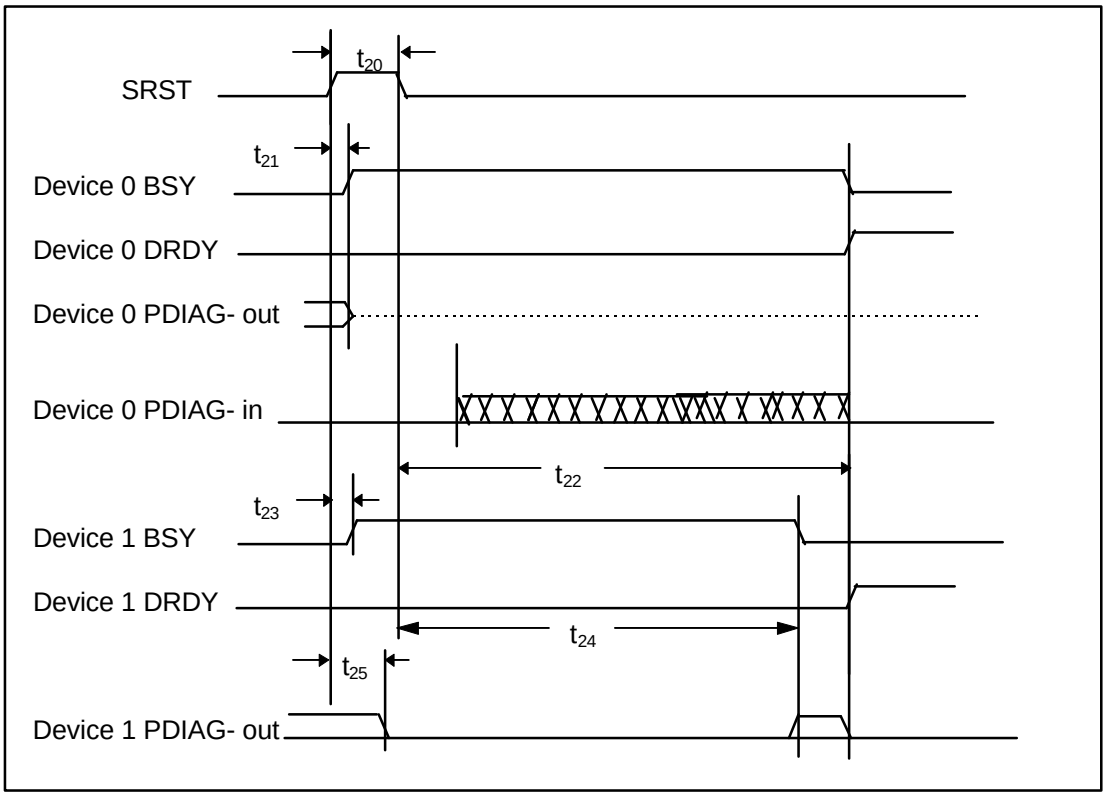


Figure 7 – BSY and DRDY timing for software reset

Table 21 – BSY and DRDY timing for software reset

SRST timing parameters		Min	Max	Note
t_{20}	SRST bit set to one	5 µs		
t_{21}	Device 0 SRST set to one to BSY bit set to one, release PDIAG-		400 ns	
t_{22}	Device 0 SRST cleared to zero to sample of PDIAG-	1 ms	31 s	1
t_{23}	Device 1 SRST set to one to BSY set to one		400 ns	
t_{24}	Device 1 SRST cleared to zero to BSY bit cleared to zero, PDIAG- asserted		30 s	2
t_{25}	Device 1 negate PDIAG- if asserted		1 ms	

Notes:
1 Device 0 shall sample beginning 1 ms after SRST is cleared to zero. Sampling shall continue until PDIAG- assertion by Device 1 is sensed or 31 s has elapsed indicating Device 1 failed diagnostic.
2 Upon completion of internal diagnostics, Device 1 shall clear BSY to zero, and if diagnostics passed, assert PDIAG-. Internal diagnostics shall complete within 30 s of the SRST being cleared to zero.

9.4 DEVICE RESET protocol

The following steps shall occur sequentially as listed.

Steps (2) through (9) shall be completed within 6 s from the device detecting that the command has been written.

1) The host shall write the DEVICE RESET command in the Command register;
2) The device shall release INTRQ, IORDY, DMARQ and DD(15:0) no later than 400 ns after detecting that the command has been written;

3) The device shall set the BSY bit to one no later than 400 ns after detecting that the command has been written;
4) The device should stop execution of any uncompleted command;
5) Reverting to default:
   a) If the PACKET command feature set is not implemented by the device, then the device shall not revert to its default condition;
   b) If the PACKET command feature set is implemented by the device, then the device should not revert to its default condition. If the device reverts to its default condition, the device shall report a Unit Attention condition to a subsequent PACKET command;
6) The device shall clear bit 7 in the Error register to zero;
7) Device 1 shall set its signature values in the Command Block registers (see 9.1);
8) Device 0 shall clear to zero bits 5, 4, 3, 2, and 0 in the Status register;
9) If the PACKET command feature set is implemented by the device, MODE SELECT conditions shall not be altered:
10) The device shall clear the BSY bit to zero when ready to accept commands that do not require the DRDY bit to be equal to one
;
11) Setting DRDY:
   1) If the PACKET command feature set is not implemented by the device and DRDY was set when the DEVICE RESET command was received, DRDY shall remain set. Otherwise the DRDY bit shall be set to one within 30 s after the BSY bit has been cleared to zero;
   2) If the PACKET command feature set is implemented by the device, then the device shall not set DRDY to one.

9.5 EXECUTE DEVICE DIAGNOSTIC protocol

The following steps should occur sequentially as listed. Several of the steps may occur concurrently or outside of the listed sequence so long as all timing relationships are satisfied, e.g.: Device 0 may continue to sample PDIAG- after Device 0 has completed writing the specified values to the Sector Count, Sector Number, Cylinder Low, Cylinder High and Device/Head registers.

If the host asserts RESET- before devices have completed executing their EXECUTE DEVICE DIAGNOSTIC sequences, then the devices shall start executing their hardware reset sequence at step (2).

If the host sets the SRST bit in the Device Control register to one before the devices have completed execution of their EXECUTE DEVICE DIAGNOSTIC sequences, then the devices shall start executing their software reset sequences at step (2).

9.5.1 EXECUTE DEVICE DIAGNOSTIC - Device 0

Device 0 performs the following operations for this command.

Steps (1) through (9) shall be completed within 6 s after the EXECUTE DEVICE DIAGNOSTIC command is received:

1) The device shall release PDIAG-, INTRQ, IORDY, DMARQ and DD(15:0) no later than 400 ns after the EXECUTE DEVICE DIAGNOSTIC command is received;
2) Device 0 shall set the BSY bit to one no later than 400 ns after the EXECUTE DEVICE DIAGNOSTIC command is received;
3) Device 0 should begin performing its self-diagnostic testing;
4) Steps (1), (2) and (3) shall be completed before continuing;
5) If Device 0 did not detect that DASP- was asserted by Device 1 during the most recent power cycle or hardware reset, then Device 0 shall clear bit 7 to zero in the Error register and go to step (7);
6) If Device 0 detected that DASP- was asserted by Device 1 during the most recent power cycle or hardware reset, then Device 0 shall sample PDIAG- for assertion by Device 1. Device 0 may sample PDIAG- at any frequency. This sampling shall not begin until at least 1 ms after the EXECUTE DEVICE DIAGNOSTIC command is received. Device 0 may stop sampling PDIAG-

upon detection of assertion. Device 0 shall not sample PDIAG- later than 6 s after the EXECUTE DEVICE DIAGNOSTIC command is received after the next command is received;
   a) If Device 0 detects that PDIAG- is asserted within 6 s after the EXECUTE DEVICE DIAGNOSTIC command is received, then Device 0 shall clear bit 7 to zero in the Error register;
   b) If Device 0 does not detect that PDIAG- is asserted within 6 s after the EXECUTE DEVICE DIAGNOSTIC command is received, then Device 0 shall set bit 7 to one in the Error register;
7) If performed, the self-diagnostic testing initiated in step (3) shall be completed before executing the following: Device 0 shall write its self-diagnostic testing results to bits 6-0 of the Error Register. See Table 8;
8) Device 0 shall set its signature values in the Command Block registers (see 9.1).
9) Clearing BSY:
   a) If the PACKET Command feature set is not implemented by Device 0, then Steps (5), (6) (as required), (7) and (8) shall be completed before executing the following: Device 0 shall clear the BSY bit to zero when ready to accept commands that do not require the DRDY bit to be equal to one.
   b) If the PACKET Command feature set is implemented by Device 0, then Device 0 shall return its operating modes to their specified initial conditions: MODE SELECT conditions shall be restored to their last saved values if saved values have been established; MODE SELECT conditions for which no values have been saved shall be returned to their default values; then Device 0 shall clear the BSY bit to zero;
10) Setting DRDY:
   a) If the PACKET Command feature set is not implemented by Device 0, then the DRDY bit shall be set to one within 30 s after the BSY bit has been cleared to zero. Steps (9) (a) and (10) (a) may occur at the same time;
   b) If the PACKET Command feature set is implemented by Device 0, then Device 0 shall not set DRDY to one;

9.5.2 EXECUTE DEVICE DIAGNOSTIC - Device 1

Device 1 performs the following operations for this command.

The following steps should occur sequentially as listed. Several of the steps may occur concurrently or outside of the listed sequence so long as all timing relationships are satisfied.

Steps (1) through (9) shall be completed within 5 s after the EXECUTE DEVICE DIAGNOSTIC command is received:

1) The device shall release INTRQ, IORDY, DMARQ and DD(15:0) no later than 400 ns after the EXECUTE DEVICE DIAGNOSTIC command is received;
2) Device 1 shall set the BSY bit to one no later than 400 ns after the EXECUTE DEVICE DIAGNOSTIC command is received;
3) Device 1 shall negate PDIAG- no later than 1 ms after the EXECUTE DEVICE DIAGNOSTIC command is received;
4) Device 1 should initiate performance of its self-diagnostic testing;
5) Steps (1), (2), (3) and (4) shall be completed before continuing.
6) If performed, the self-diagnostic testing initiated in step (4) shall be completed before executing the following: Device 1 shall write its self-diagnostic testing results to the Error register. See Table 8;
7) Device 1 shall set its signature values in the Command Block registers (see 9.1).
8) Clearing BSY:
   a) If the PACKET Command feature set is not implemented by Device 1, then steps (6) and (7) shall be completed, , before executing the following: Device 1 shall clear the BSY bit to zero when ready to accept commands that do not require the DRDY bit to be equal to one;
   b) If the PACKET Command feature set is implemented by Device 1, then Device 1 shall return its operating modes to their specified initial conditions: MODE SELECT conditions shall be restored to their last saved values if saved values have been established; MODE SELECT conditions for which no values have been saved shall be returned to their default values; then Device 1 shall clear the BSY bit to zero;

9) Step (8) shall be completed before executing the following: If Device 1 passed its self-diagnostic testing during step (4), then Device 1 shall assert PDIAG-;
10) Setting DRDY:
    a) If the PACKET Command feature set is not implemented by Device 1, then the DRDY bit shall be set to one within 30 s after the BSY bit has been cleared to zero. Steps (8) (a), (9), and (10) (a) may occur at the same time;
    b) If the PACKET Command feature set is implemented by Device 1, then Device 1 shall not set DRDY to one;
11) Device 1 shall continue to assert PDIAG- until after the first command is received from the host or until 31 s after the EXECUTE DEVICE DIAGNOSTIC command is received or until detecting that the host has set the SRST bit to one in the Device Control register, whichever comes first.

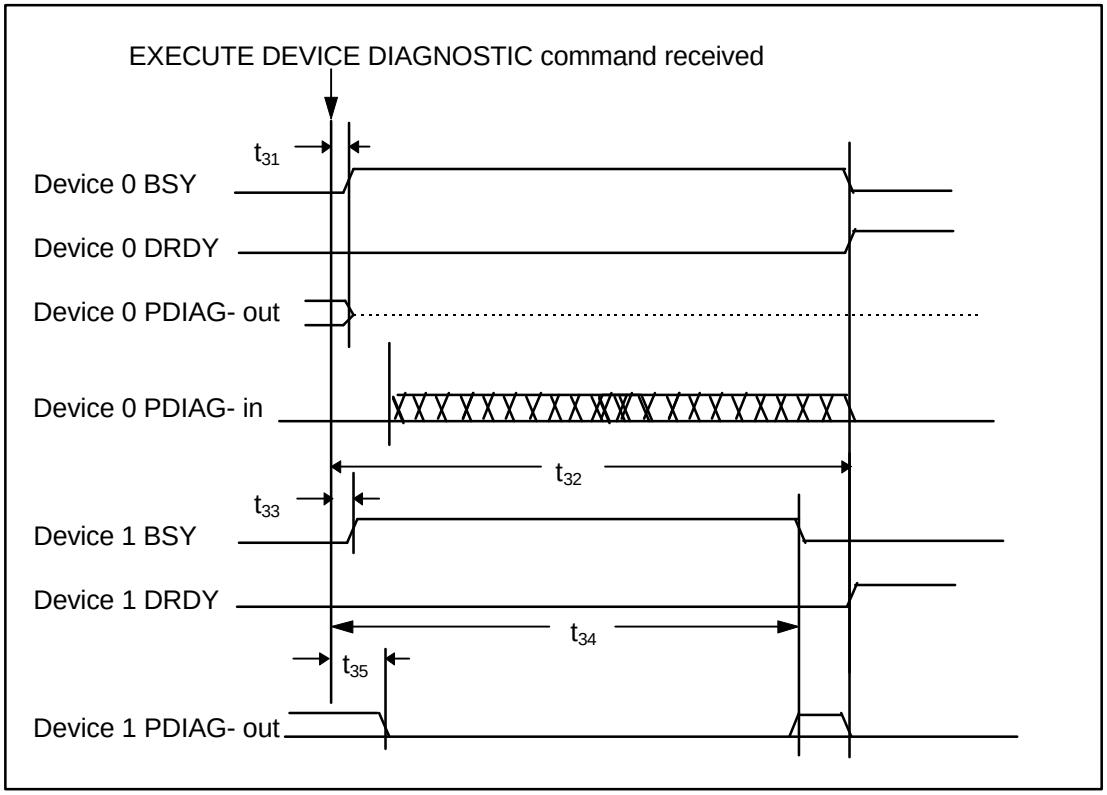


Figure 8 – BSY and DRDY timing for diagnostic command

Table 22 – BSy and DRDY timing for diagnostic command

EXECUTE DEVICE DIAGNOSTIC timing parameters		Min	Max	Note
t_{31}	Device 0 command received to BSY bit set to one, release PDIAG-		400 ns	
t_{32}	Device 0 command received to sample of PDIAG-	1 ms	6 s	1
t_{33}	Device 1 command received to BSY set to one		400 ns	
t_{34}	Device 1 command received to BSY bit cleared to zero, PDIAG- asserted		5 s	2
t_{35}	Device 1 negate PDIAG- if asserted		1 ms	

Notes:
1 Device 0 shall sample beginning 1 ms after receipt of the command. Sampling shall continue until PDIAG- assertion by Device 1 is sensed or 6 s has elapsed indicating Device 1 failed diagnostic.
2 Upon completion of internal diagnostics, Device 1 shall clear BSY to zero, and if diagnostics passed, assert PDIAG-. Internal diagnostics shall complete within 5 s of the receipt of the command.

9.6 PIO data in commands

This class includes:

- IDENTIFY DEVICE
- IDENTIFY PACKET DEVICE
- READ BUFFER
- READ SECTOR(S)
- READ MULTIPLE
- SMART READ DATA

Execution of this class of command includes the transfer of one or more blocks of data from the device to the host. Figure 9 describes the processing of a PIO data in command. This description does not include all possible error conditions.

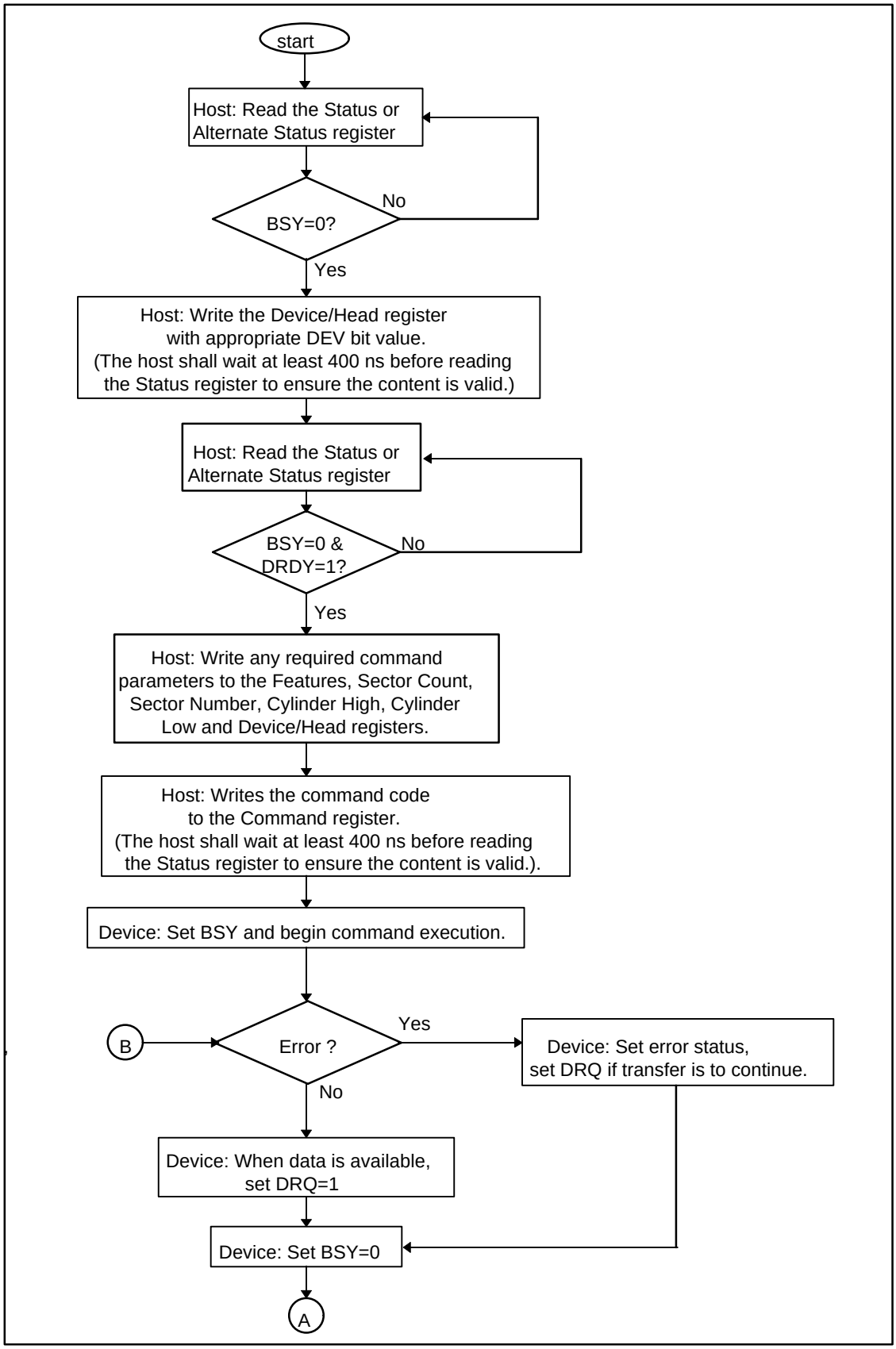


Figure 9 – **PIO data transfer in** *(continued)*

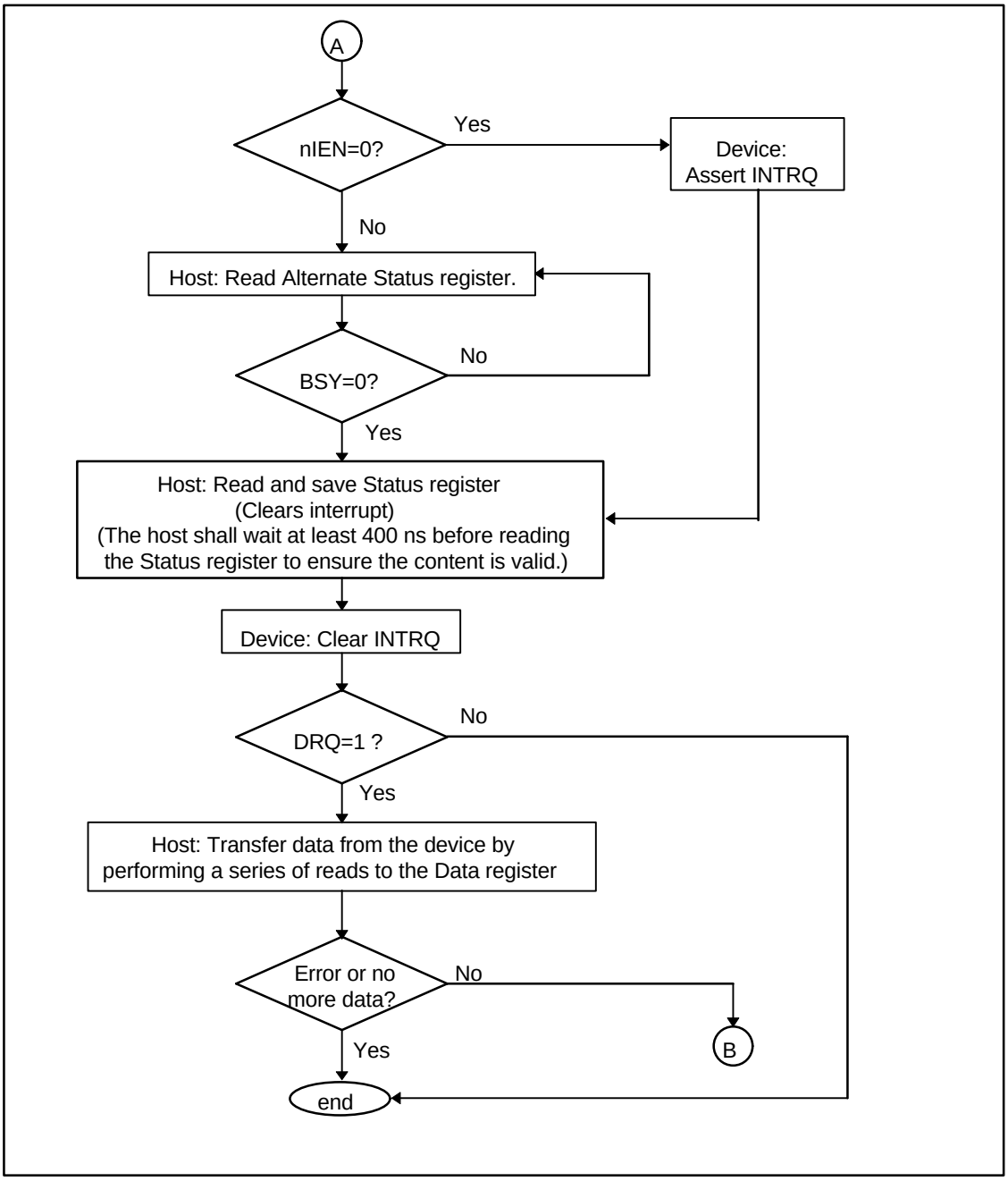


Figure 9 – **PIO data transfer in** *(concluded)*

9.7 PIO data out commands

This class includes:

- DOWNLOAD MICROCODE
- SECURITY DISABLE PASSWORD
- SECURITY ERASE UNIT
- SECURITY SET PASSWORD
- SECURITY UNLOCK
- WRITE BUFFER
- WRITE MULTIPLE
- WRITE SECTOR(S)
- WRITE VERIFY

Execution of this class of command includes the transfer of one or more blocks of data from the host to the device. Figure 10 describes the processing of a PIO data out command. This description does not include all possible error conditions.

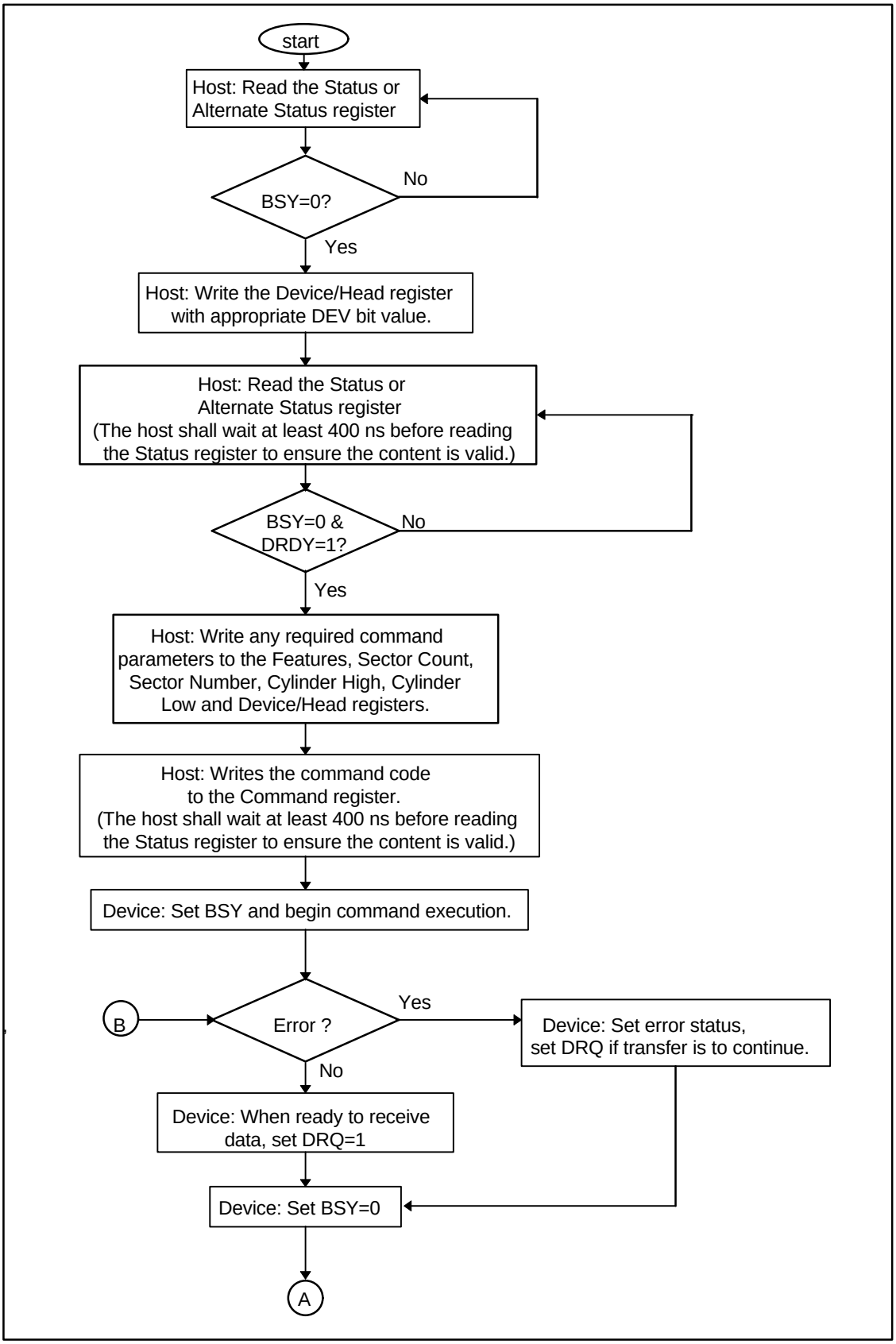


Figure 10 – **PIO data transfer out** *(continued)*

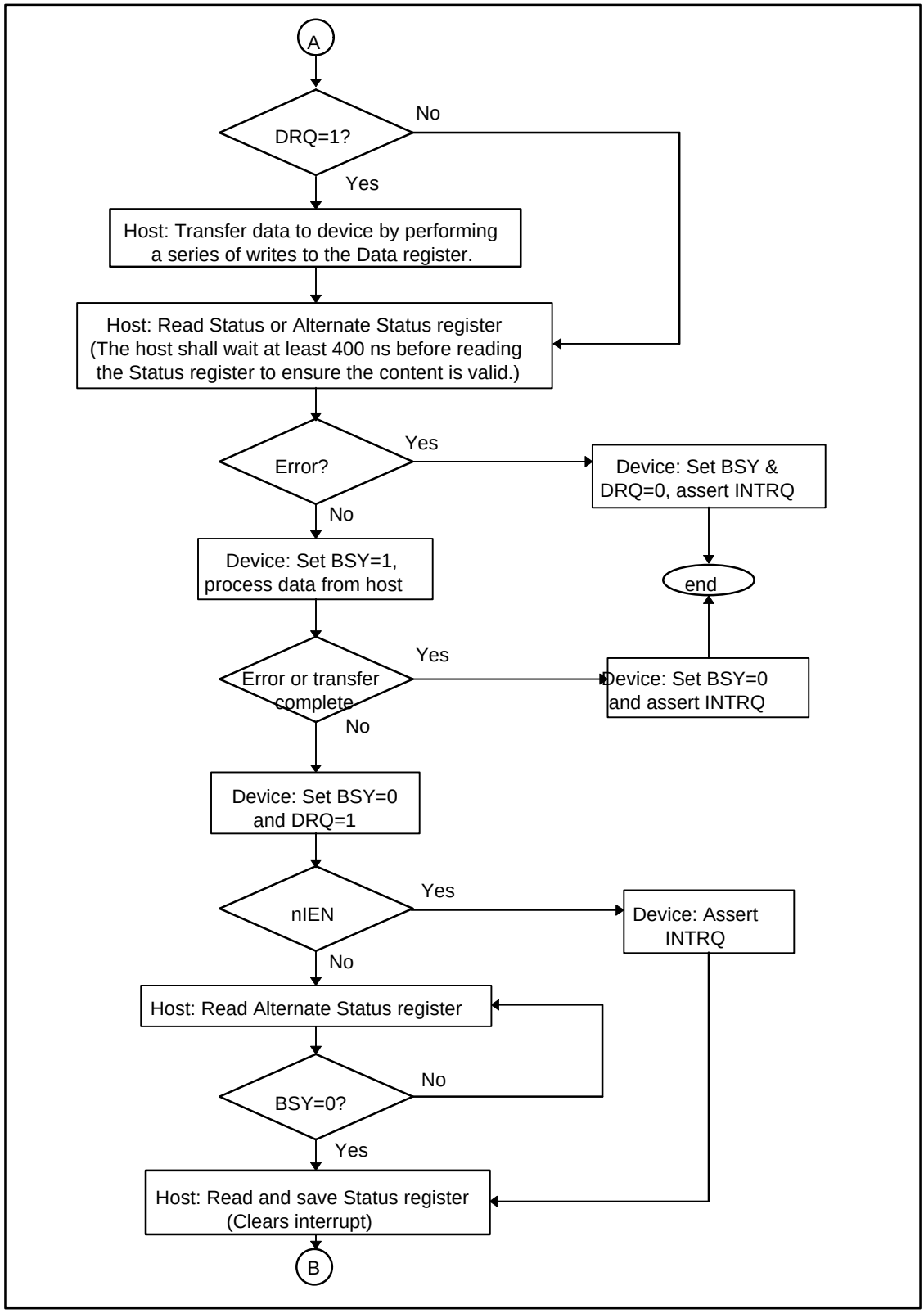


Figure 10 – **PIO data transfer out** *(concluded)*

9.8 Non-data commands

This class includes:

- CHECK POWER MODE
- DOOR LOCK
- DOOR UNLOCK
- FLUSH CACHE
- IDLE
- IDLE IMMEDIATE
- INITIALIZE DEVICE PARAMETERS
- MEDIA EJECT
- NOP
- READ NATIVE MAX ADDRESS
- READ VERIFY SECTOR(S)
- SECURITY ERASE PREPARE
- SECURITY FREEZE LOCK
- SEEK
- SET FEATURES
- SET MAX ADDRESS
- SET MULTIPLE MODE
- SLEEP
- SMART DISABLE OPERATION
- SMART ENABLE/DISABLE AUTOSAVE
- SMART ENABLE OPERATION
- SMART EXECUTE OFFLINE
- SMART RETURN STATUS
- SMART SAVE ATTRIBUTE VALUES
- STANDBY
- STANDBY IMMEDIATE

Execution of these commands involves no data transfer. Figure 11 describes the processing of a no data transfer command. This description does not include all possible error conditions.

See the NOP command description in 8.11 and the SLEEP command description in 8.31 for additional protocol requirements.

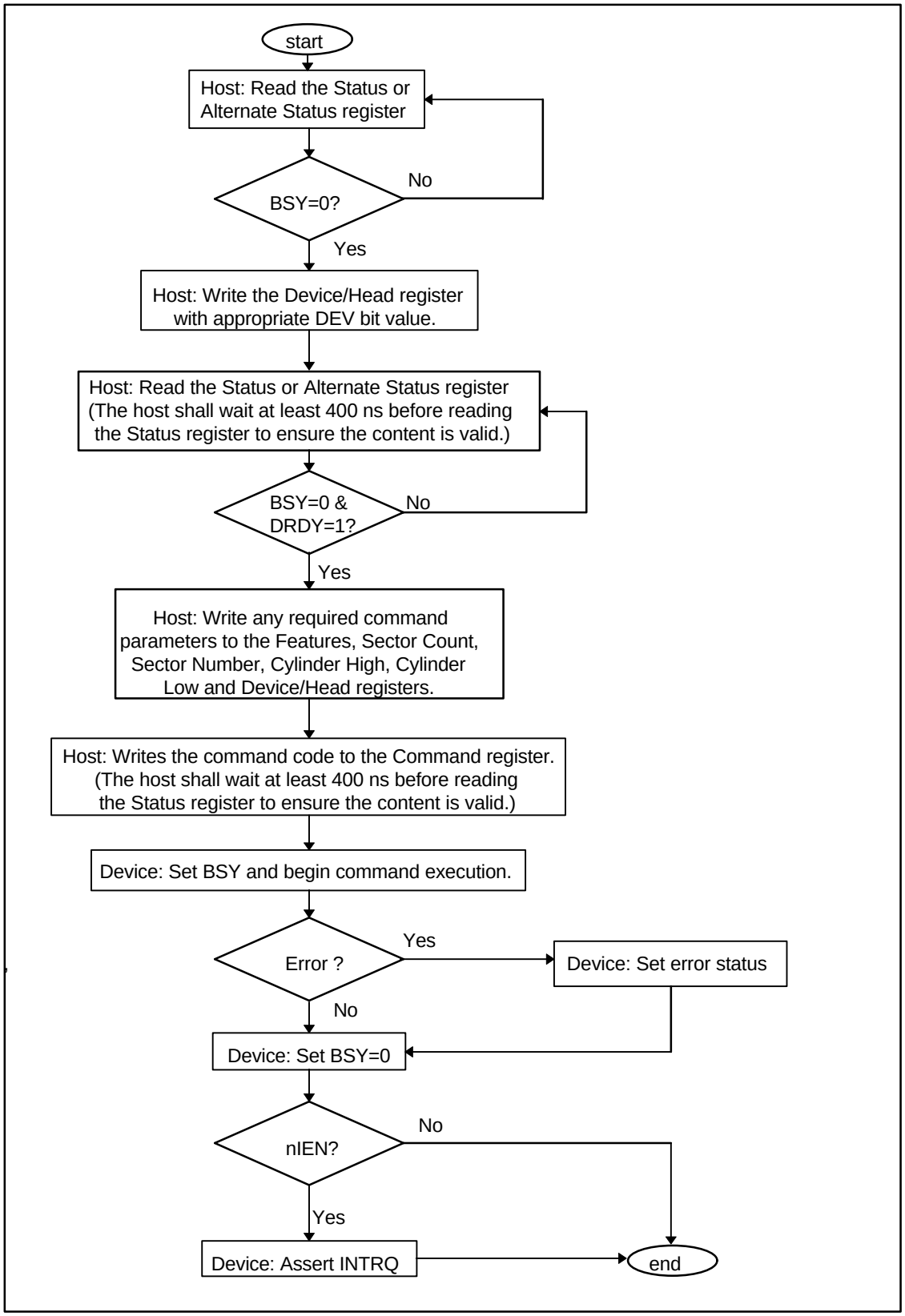


Figure 11 – Non-data transfer

9.9 DMA data transfer commands

This class comprises:

- READ DMA
- WRITE DMA

Data transfers using DMA commands differ in two ways from PIO transfers:

1) data transfers are performed using the DMA channel;

2) A Single interrupt is issued at the completion of the command.

Initiation of the DMA transfer commands is identical to the READ SECTOR(S) or WRITE SECTOR(S) commands except that the host initializes the DMA channel prior to issuing the command.

The interrupt handler for DMA transfers is different in that no intermediate sector interrupts are issued on multi-sector commands.

Figure 12 describes the execution of a DMA command..

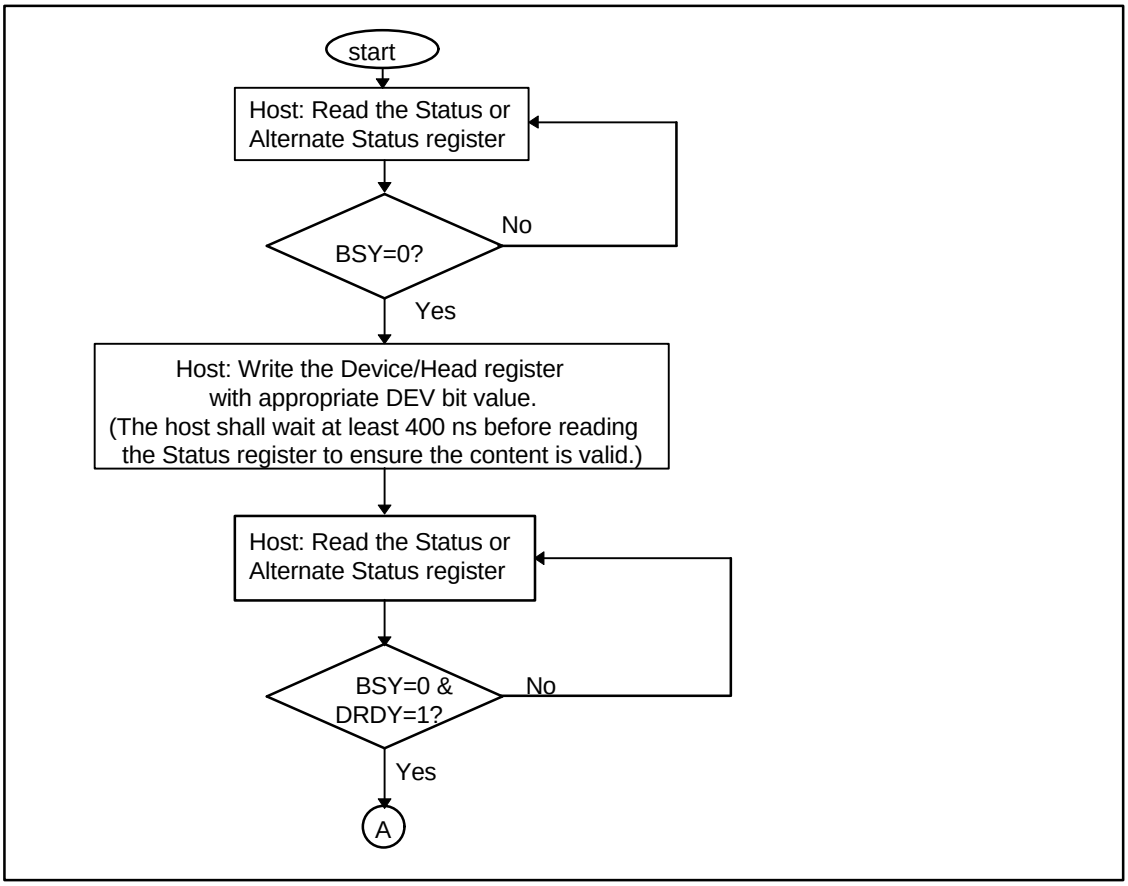


Figure 12 – **DMA data transfer** *(continued)*

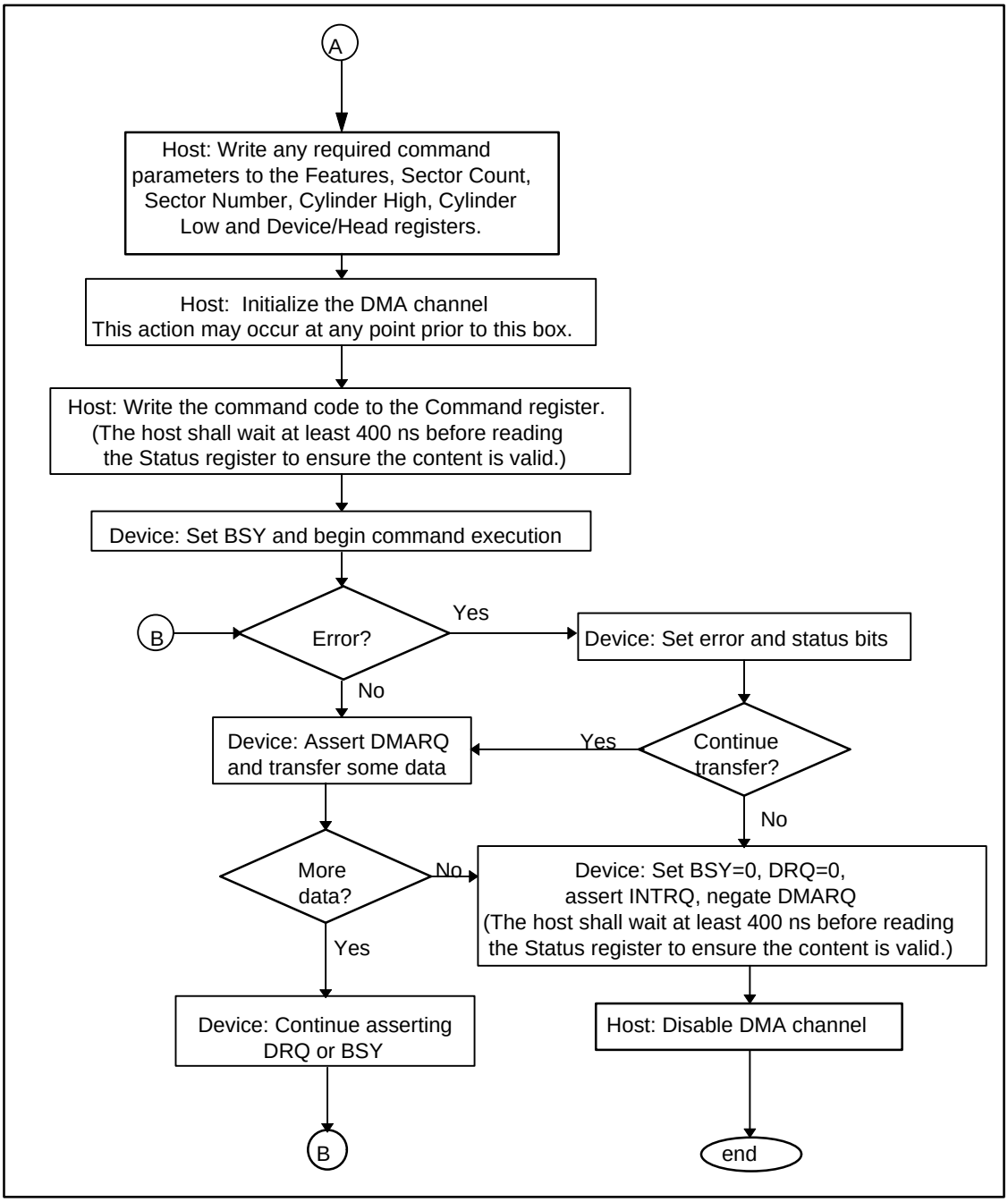


Figure 12 – **DMA data transfer** *(concluded)*

9.10 PACKET commands

This class comprises:

- PACKET
- SERVICE

The use of the PACKET command includes six different protocols. The first four protocols describe the use of the PACKET command without overlap and do not involve the use of the SERVICE command. The last two protocols describe overlapped operation with the use of the SERVICE command.

Figure 13 shows the protocol for a non-overlapped PACKET command. Figure 14 shows the protocol for a non-overlapped PACKET command for DMA data transfer. Figure 15 shows the protocol for an overlapped PACKET command.

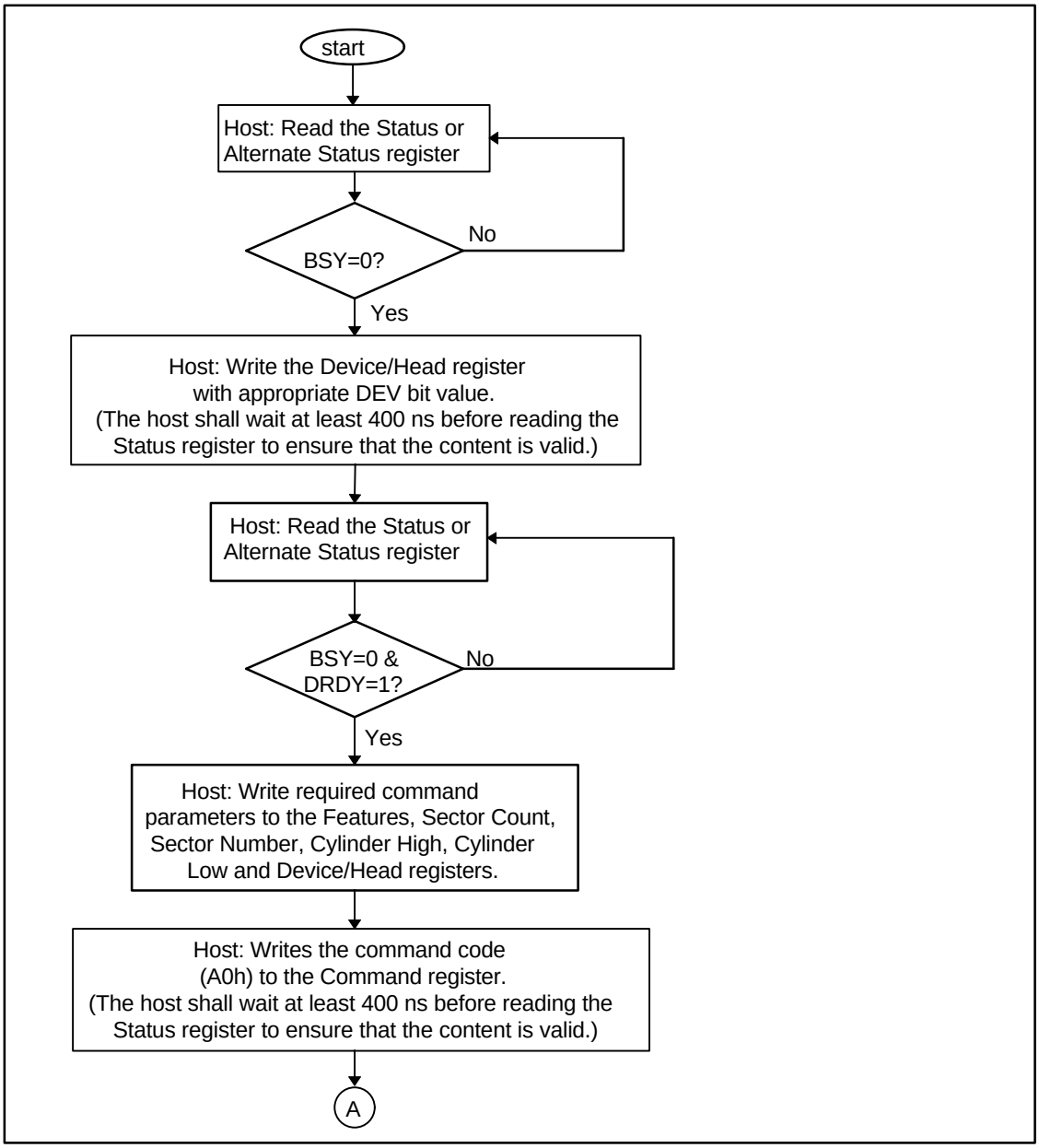
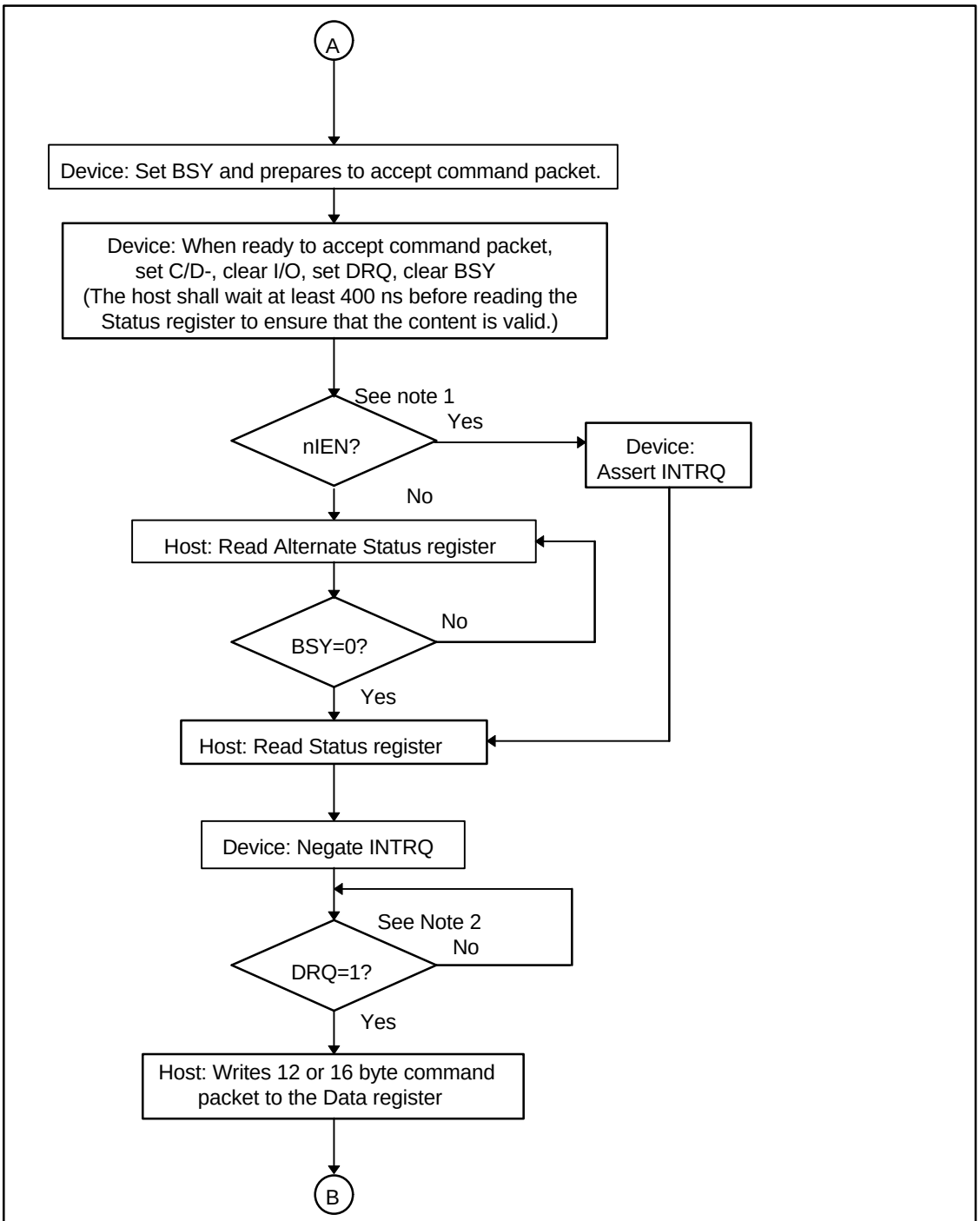


Figure 13 – Non-overlapped PACKET command *(continued)*



NOTE –
1 Some devices assert INTRQ at this point. See IDENTIFY PACKET DEVICE, word 0, bits 56 to Determine if interrupt will occur.
2 There may be a delay from the assertion of INTRQ to DRQ being sey to one.

Figure 13 – Non-overlapped PACKET command *(continued)*

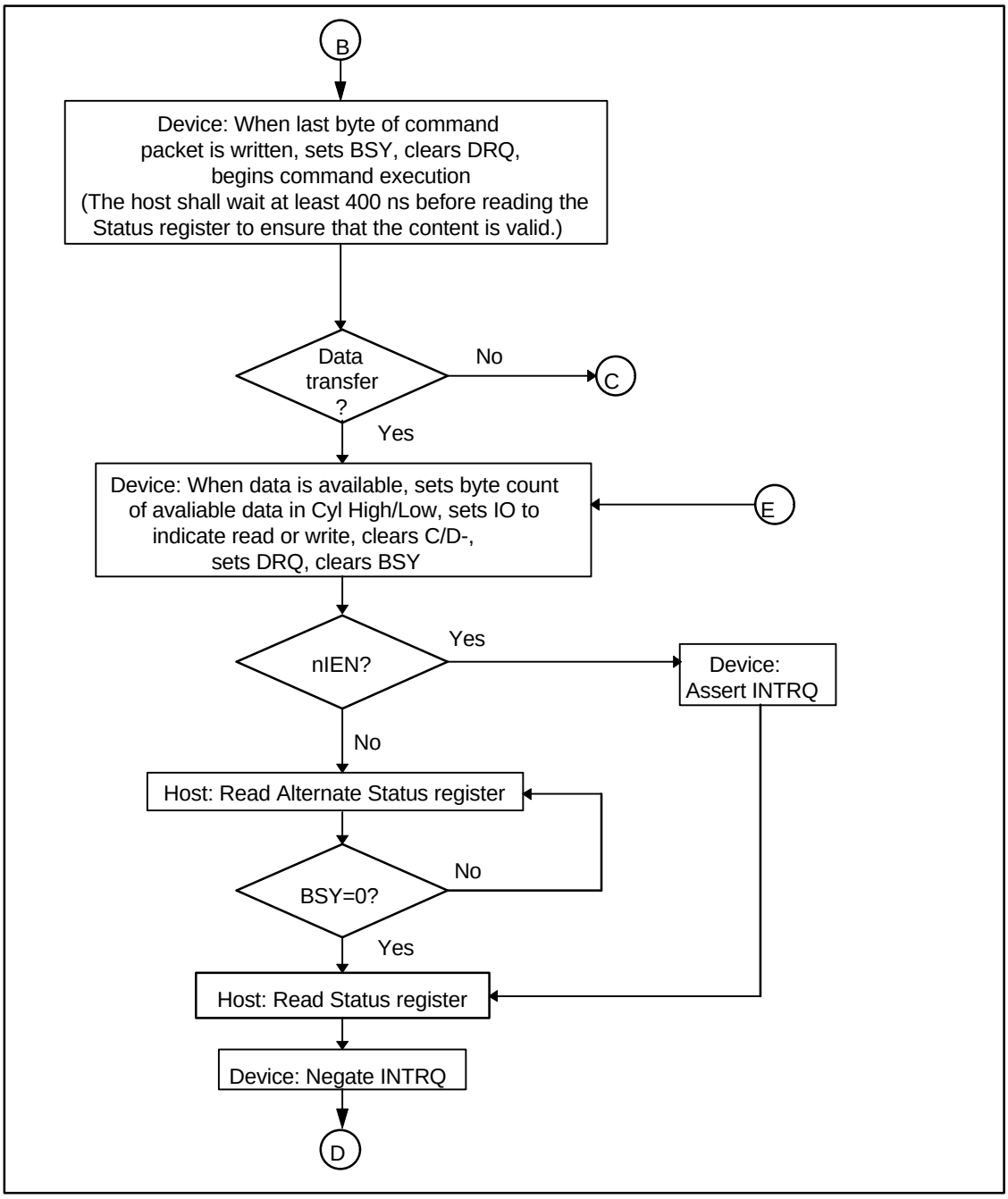


Figure 13 – **Non-overlapped PACKET command** *(continued)*

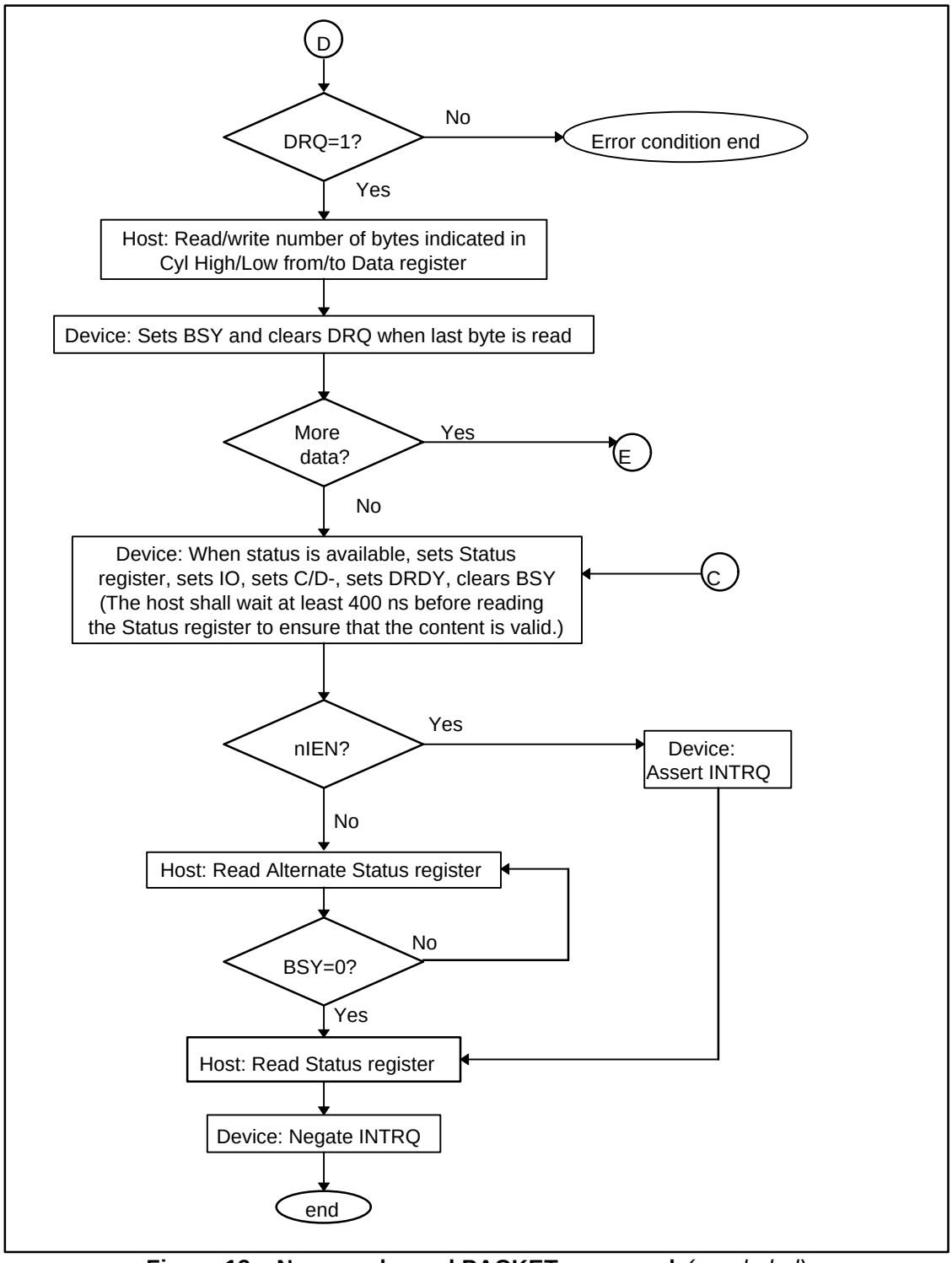


Figure 13 – **Non-overlapped PACKET command** *(concluded)*

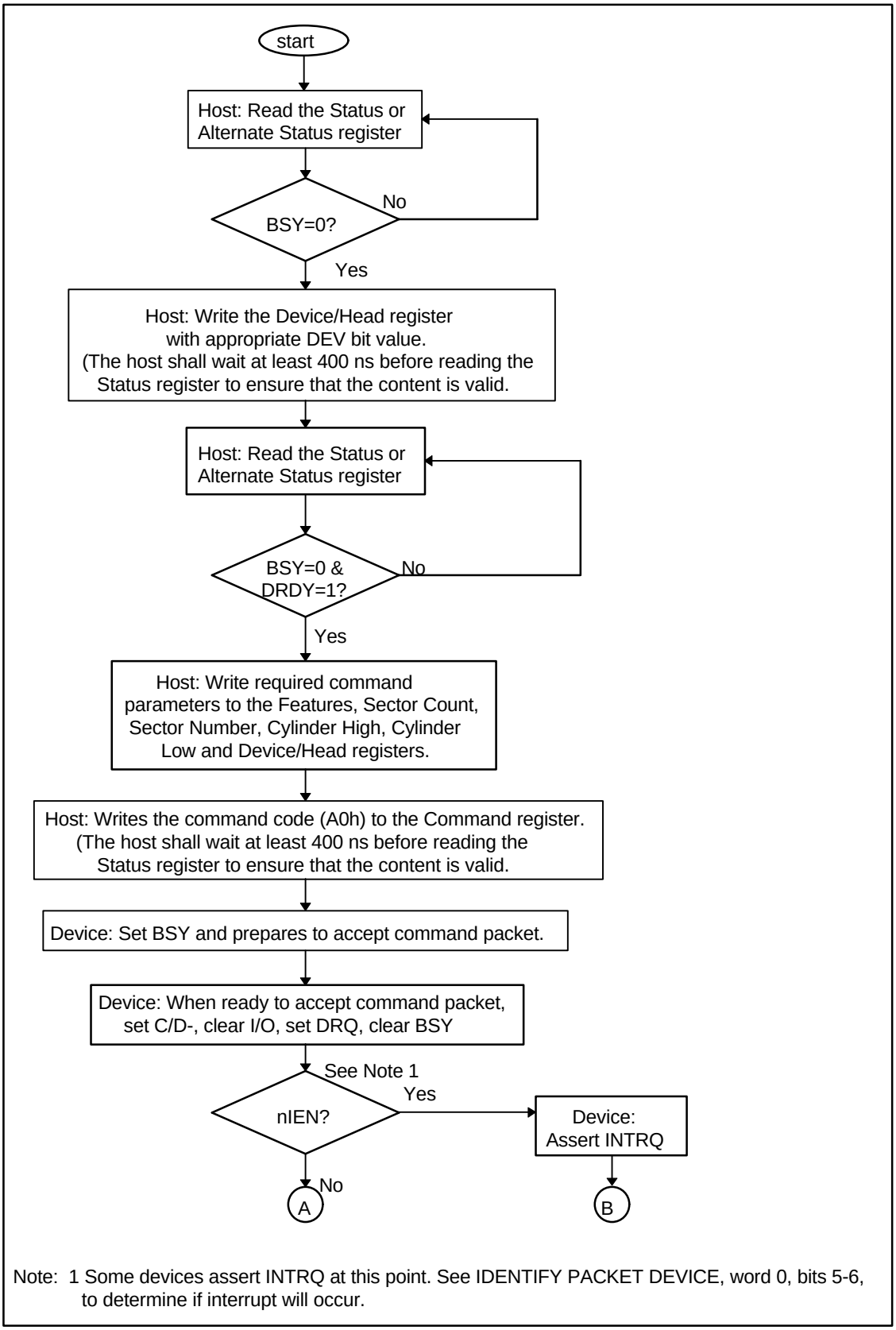


Figure 14 – Non-overlapped PACKET DMA command *(continued)*

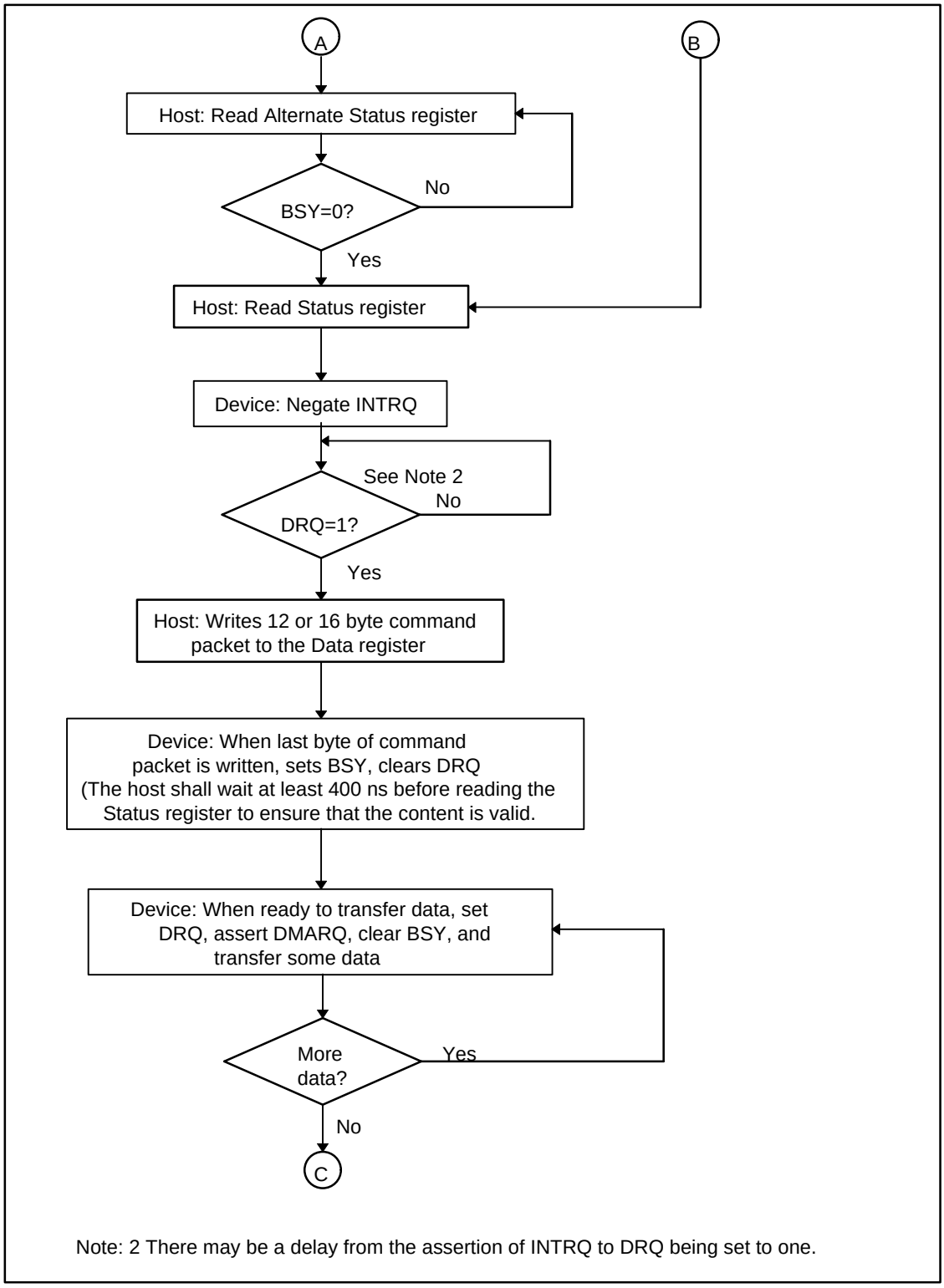


Figure 14 – **Non-overlapped PACKET DMAcommand** *(continued)*

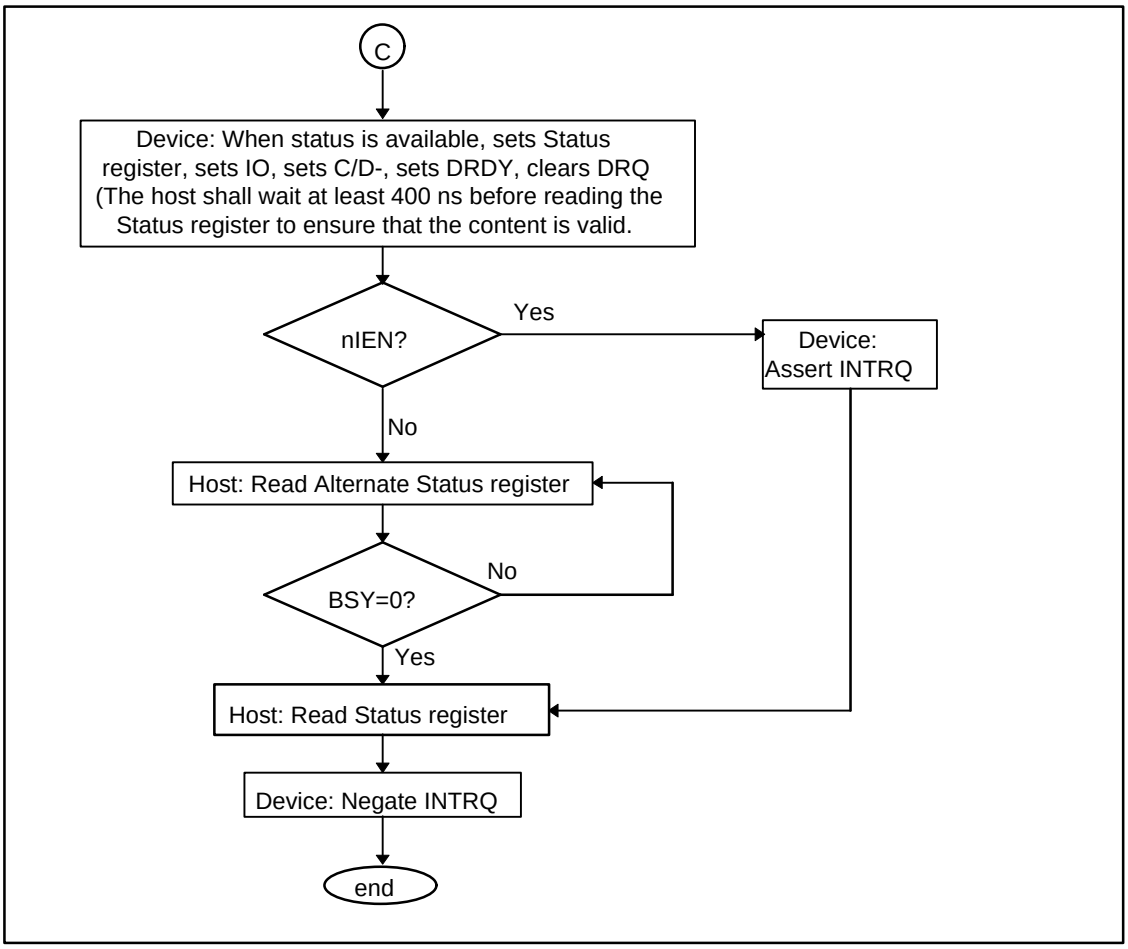
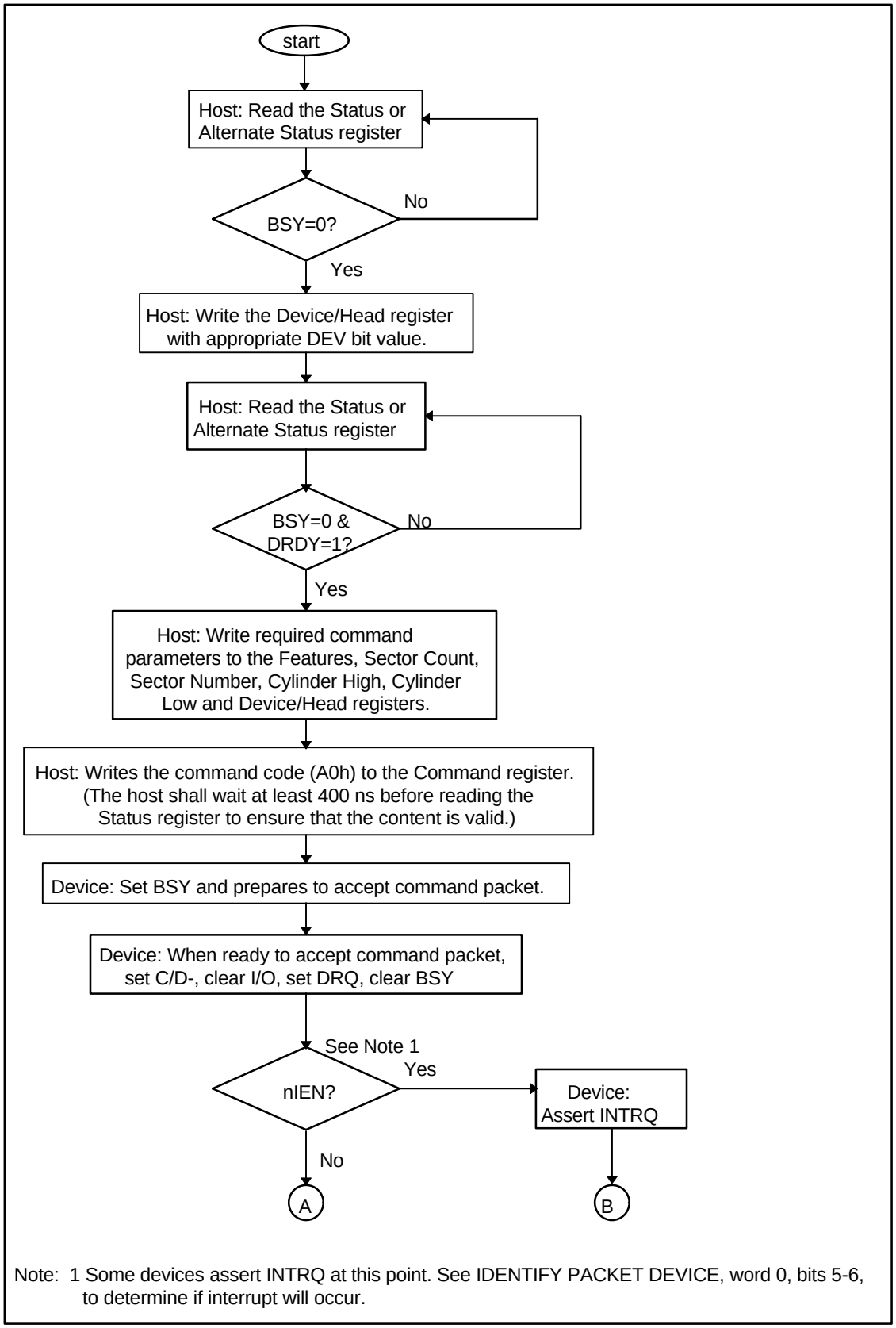


Figure 14 – **Non-overlapped PACKET DMAcommand** *(concluded)*



Note: 1 Some devices assert INTRQ at this point. See IDENTIFY PACKET DEVICE, word 0, bits 5-6, to determine if interrupt will occur.

Figure 15 – Overlapped/queued PACKET PIO command *(continued)*

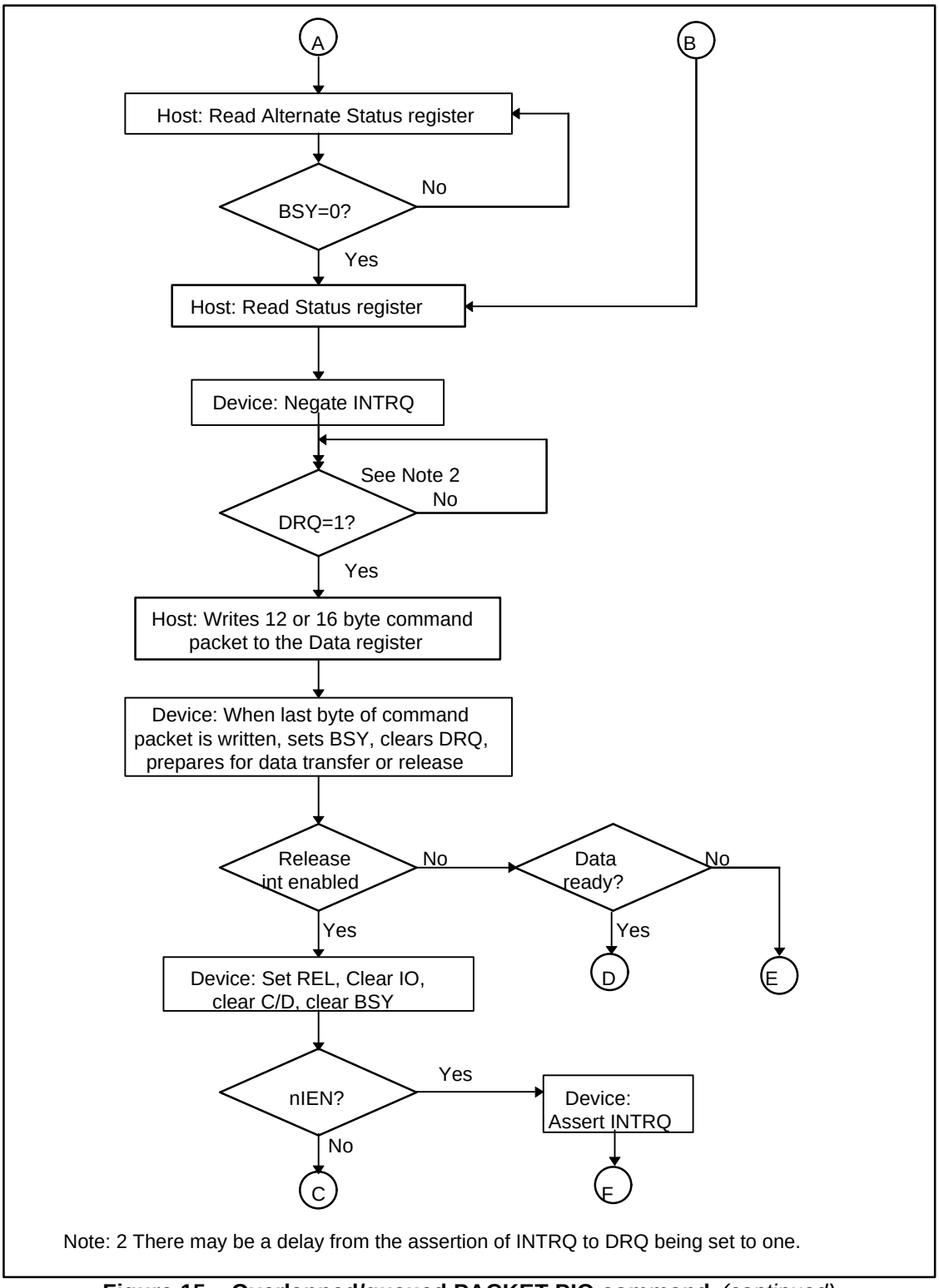


Figure 15 – **Overlapped/queued PACKET PIO command** *(continued)*

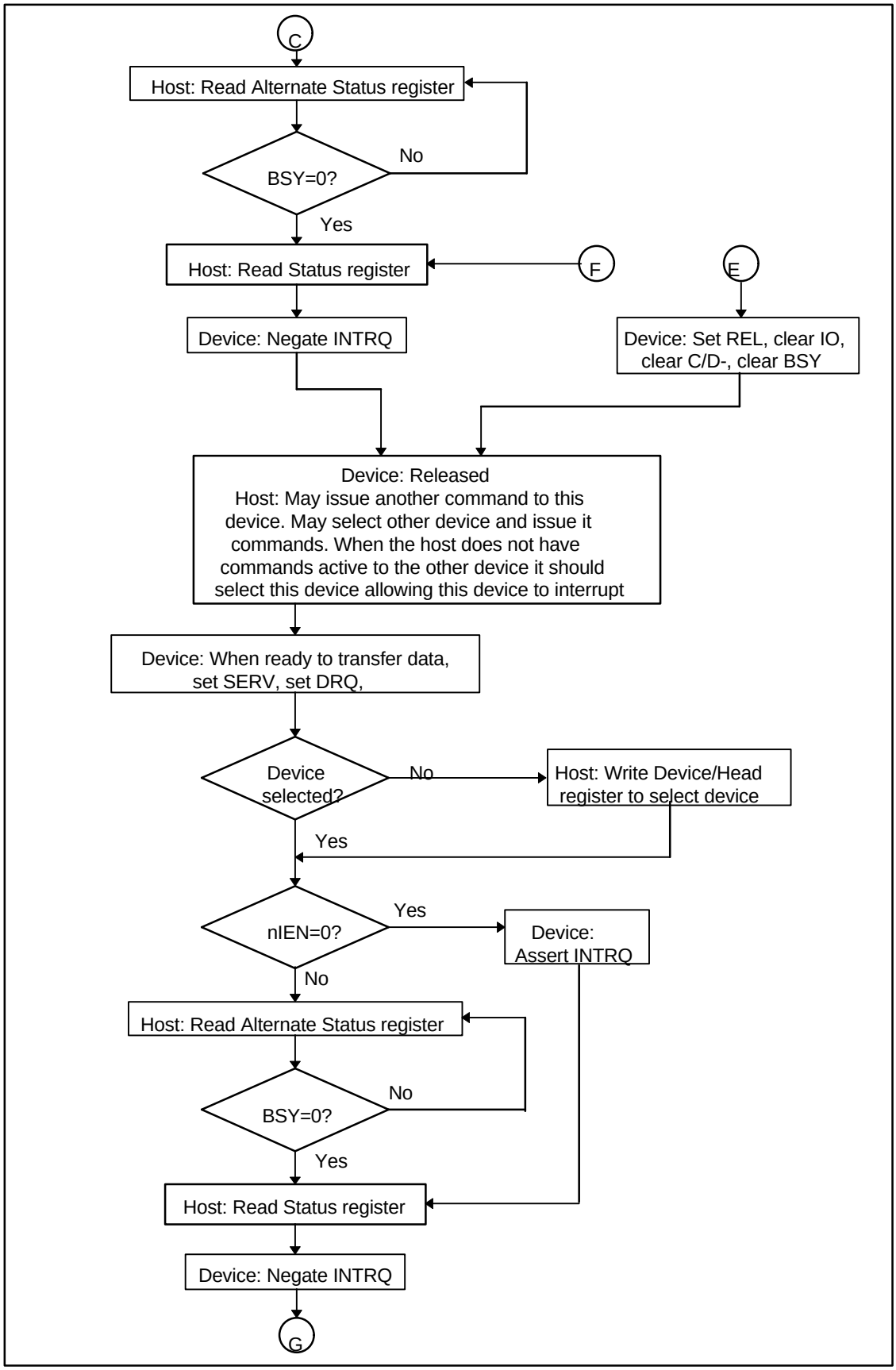


Figure 15 – **Overlapped/queued PACKET PIO command** *(continued)*

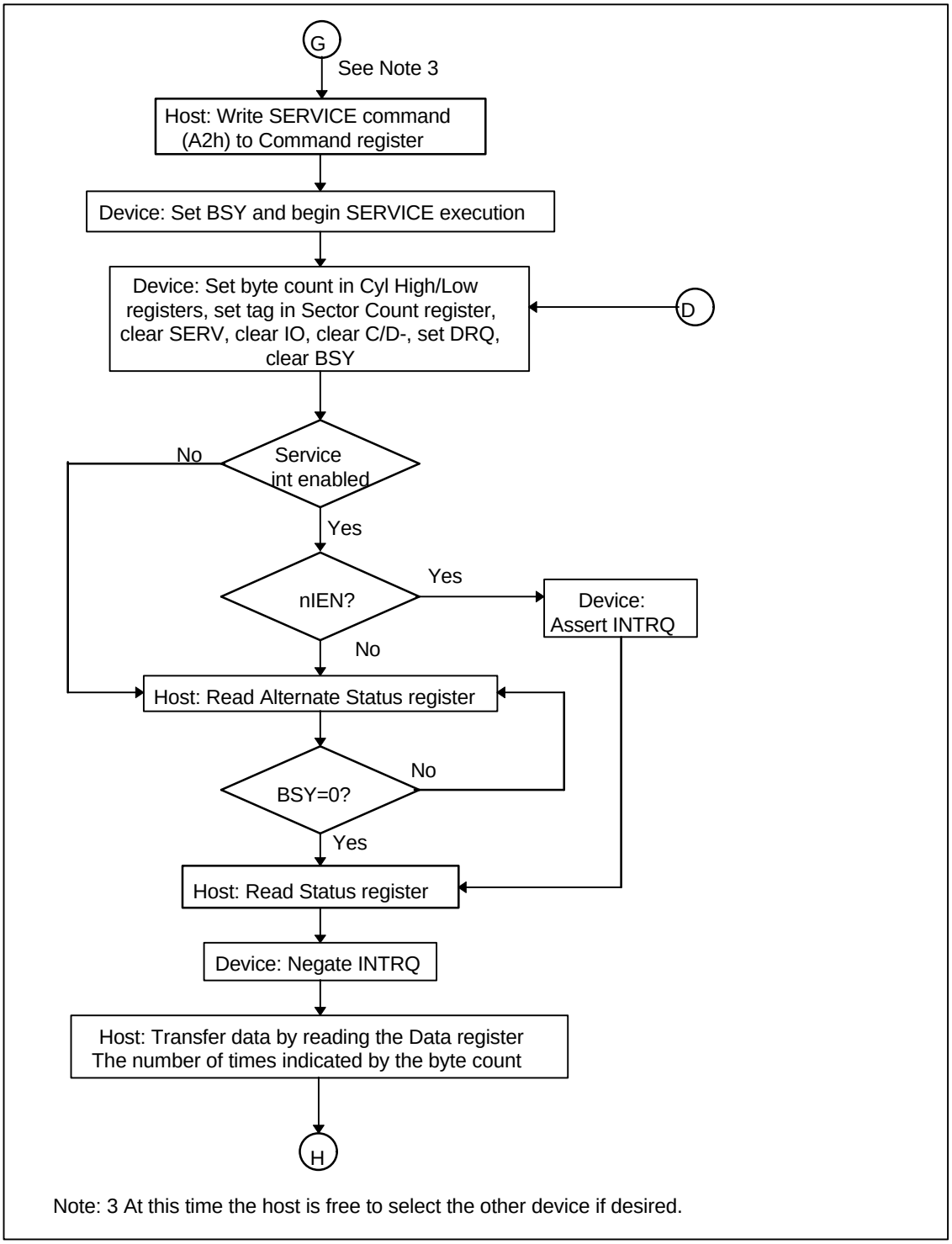


Figure 15 – **Overlapped/queued PACKET PIO command** *(continued)*

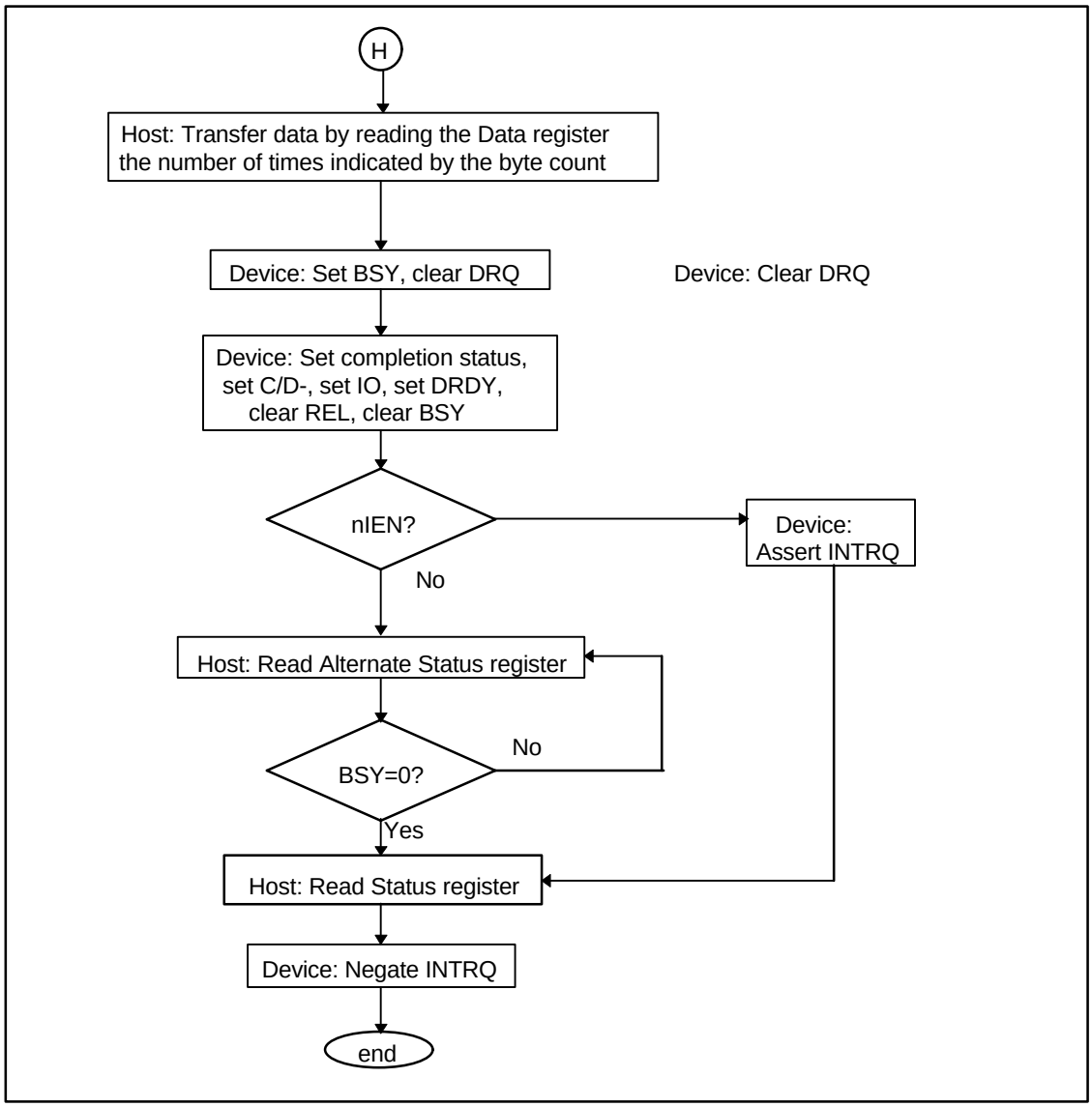


Figure 15 – **Overlapped PACKET PIO command** *(concluded)*

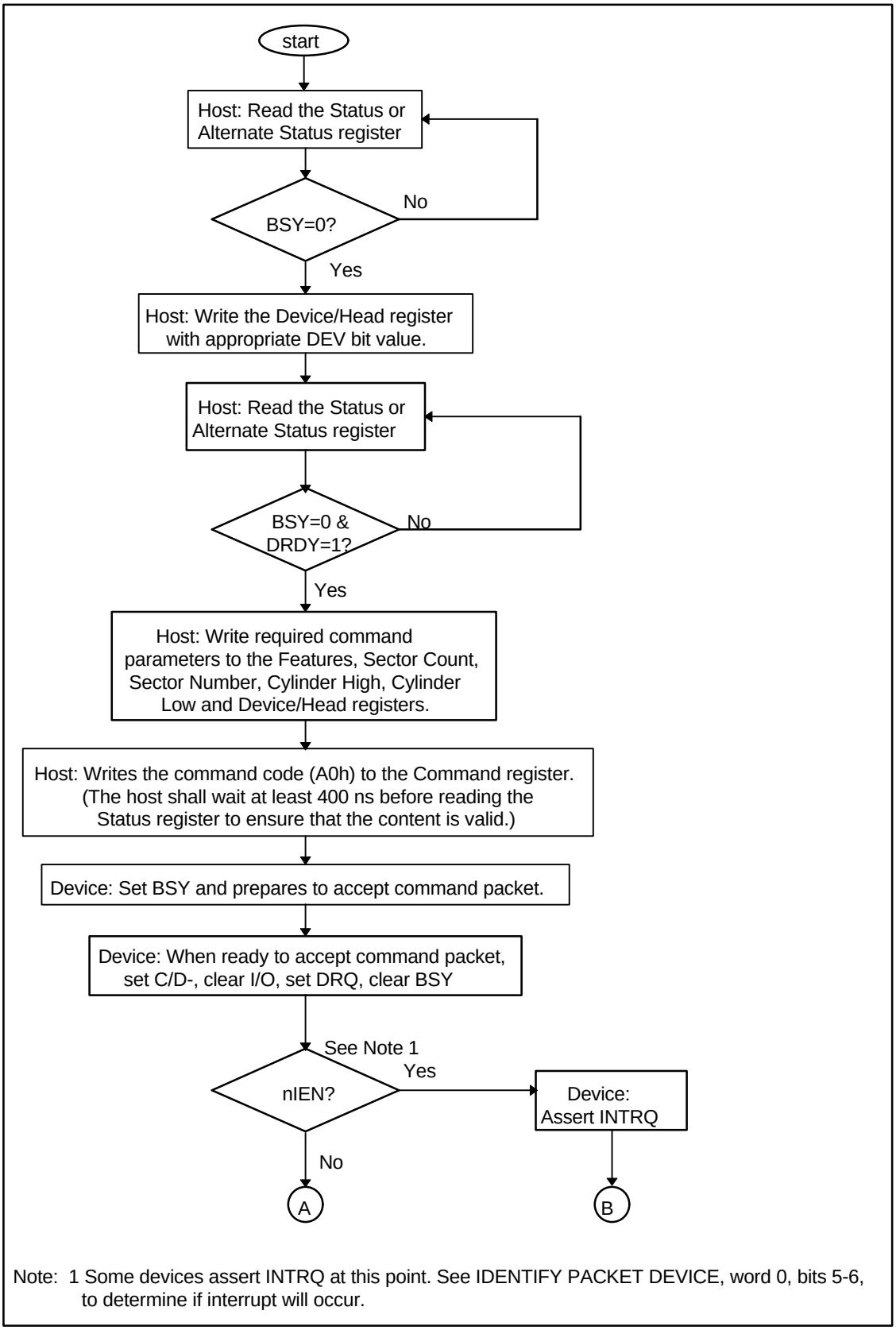


Figure 16 – Overlapped/queued PACKET DMA command *(continued)*

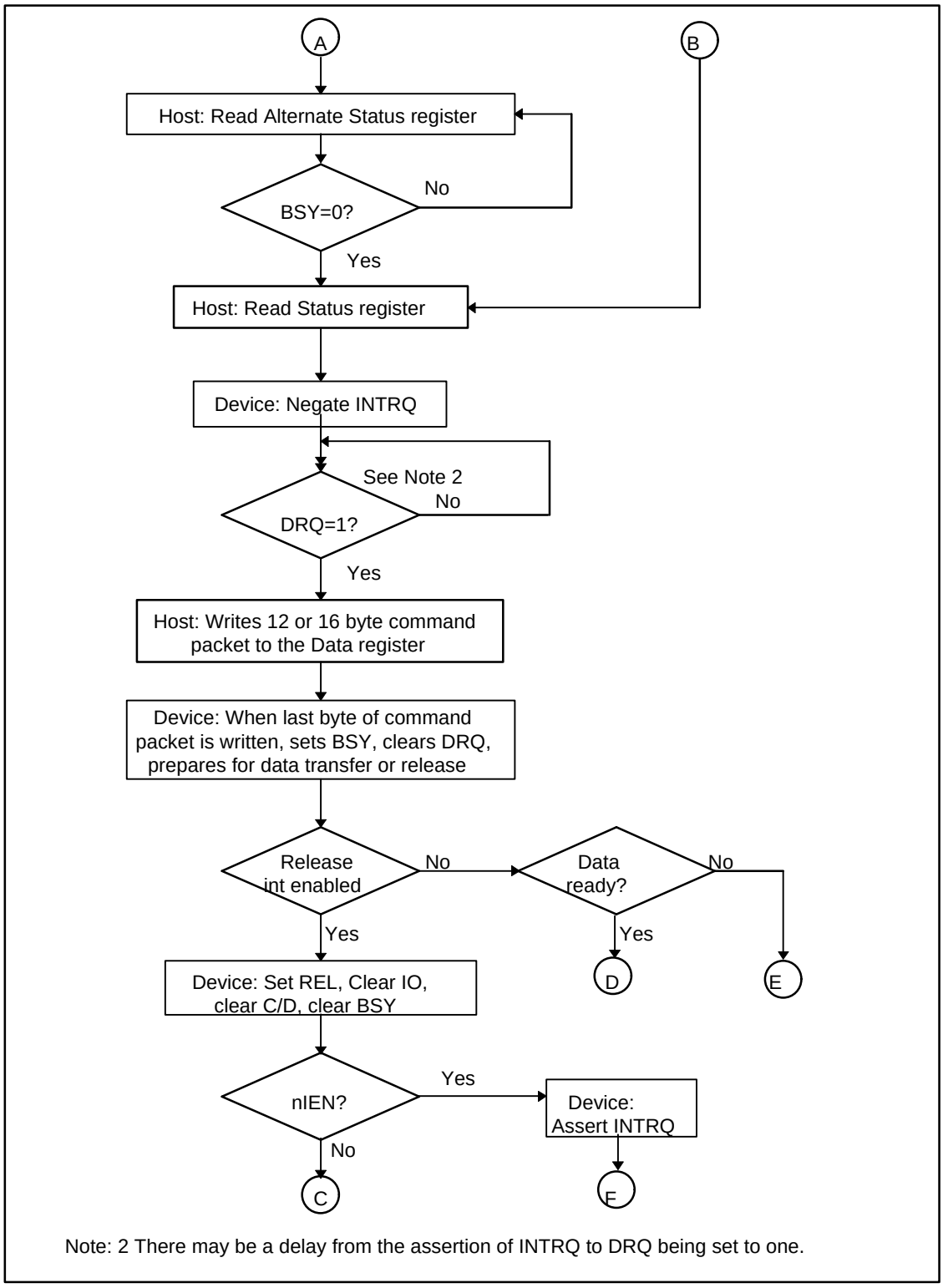


Figure 16 – **Overlapped/queued PACKET DMA command** *(continued)*

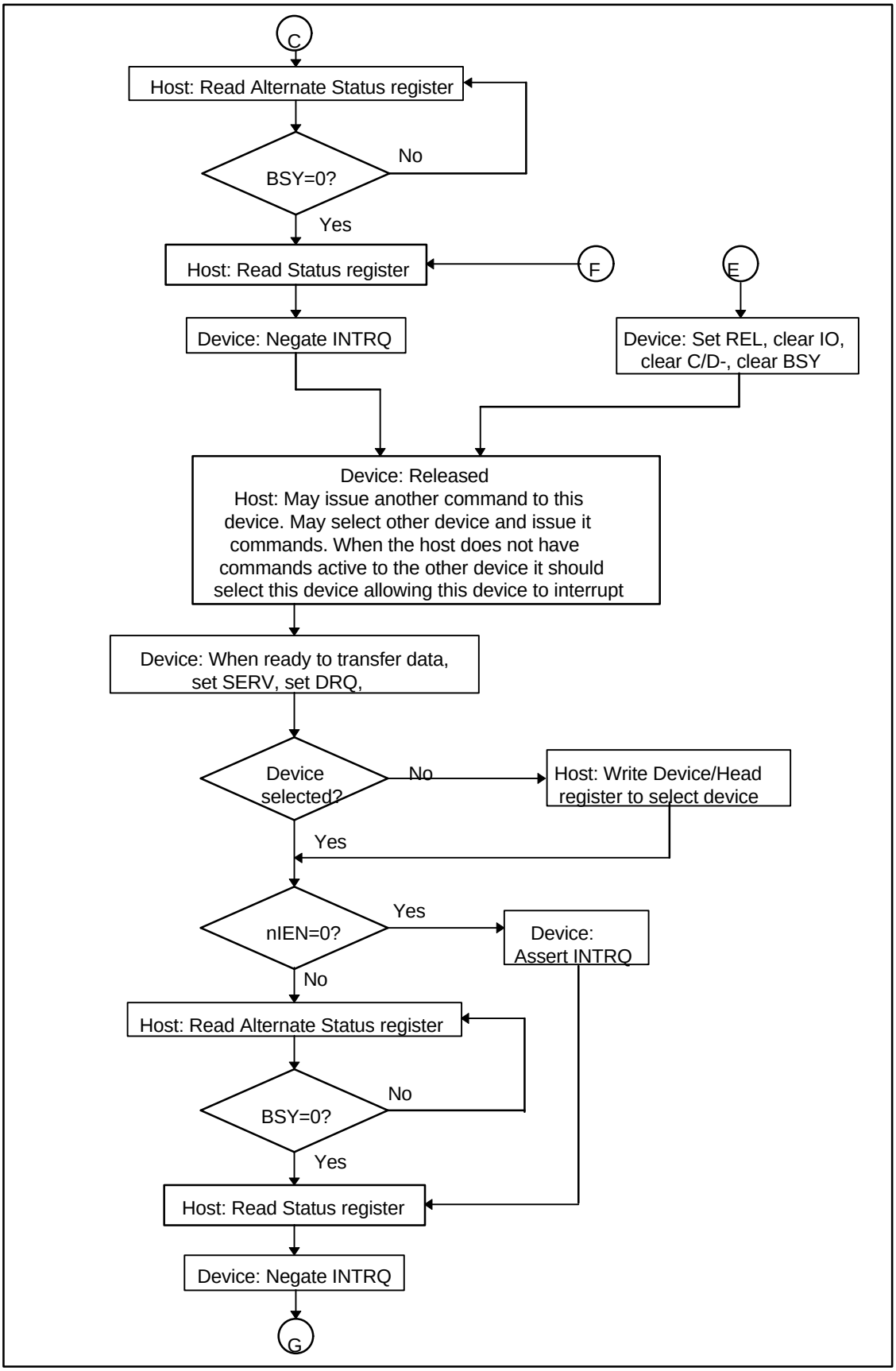


Figure 16 – **Overlapped/queued PACKET DMA command** *(continued)*

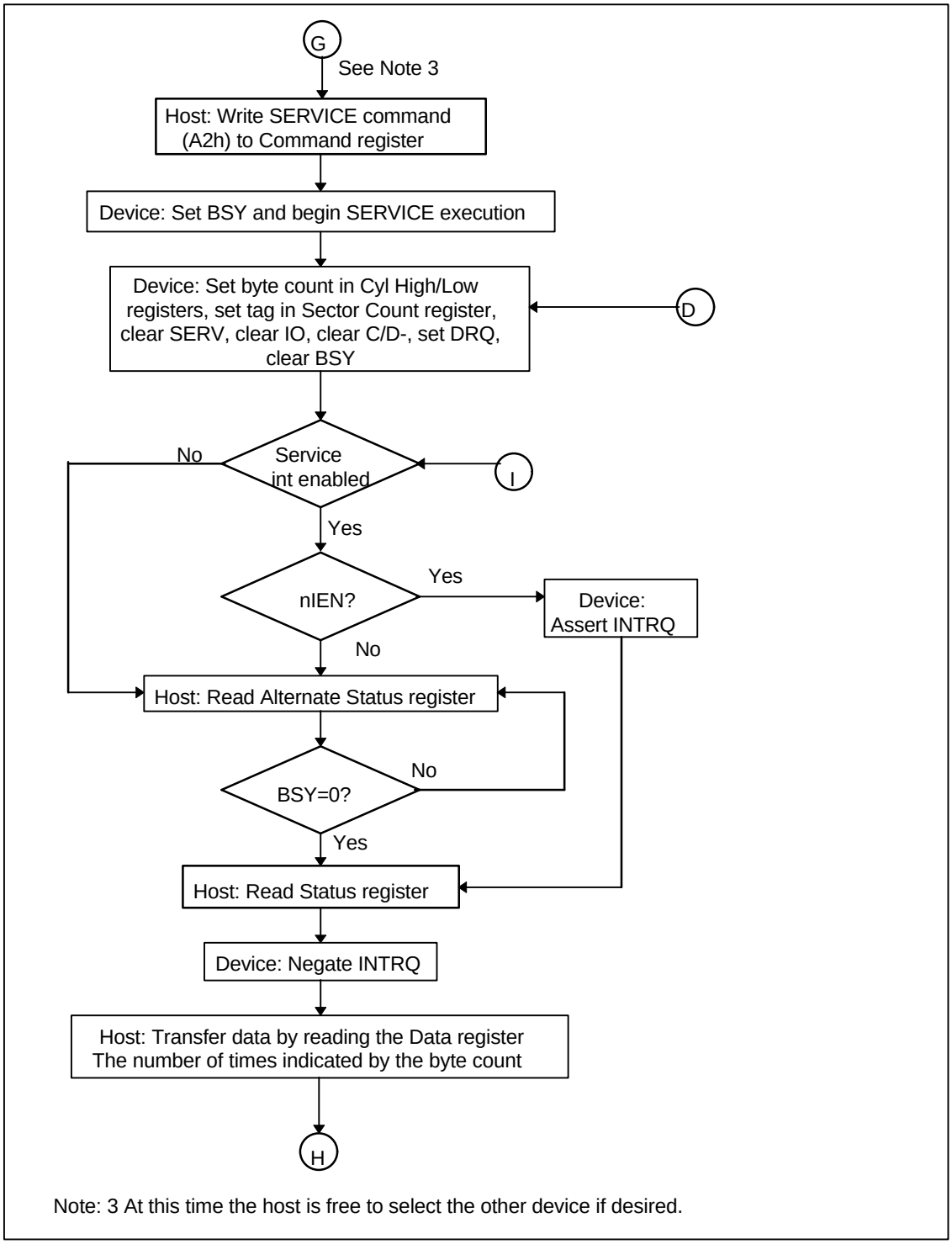


Figure 16 – **Overlapped/queued PACKET DMA command** *(continued)*

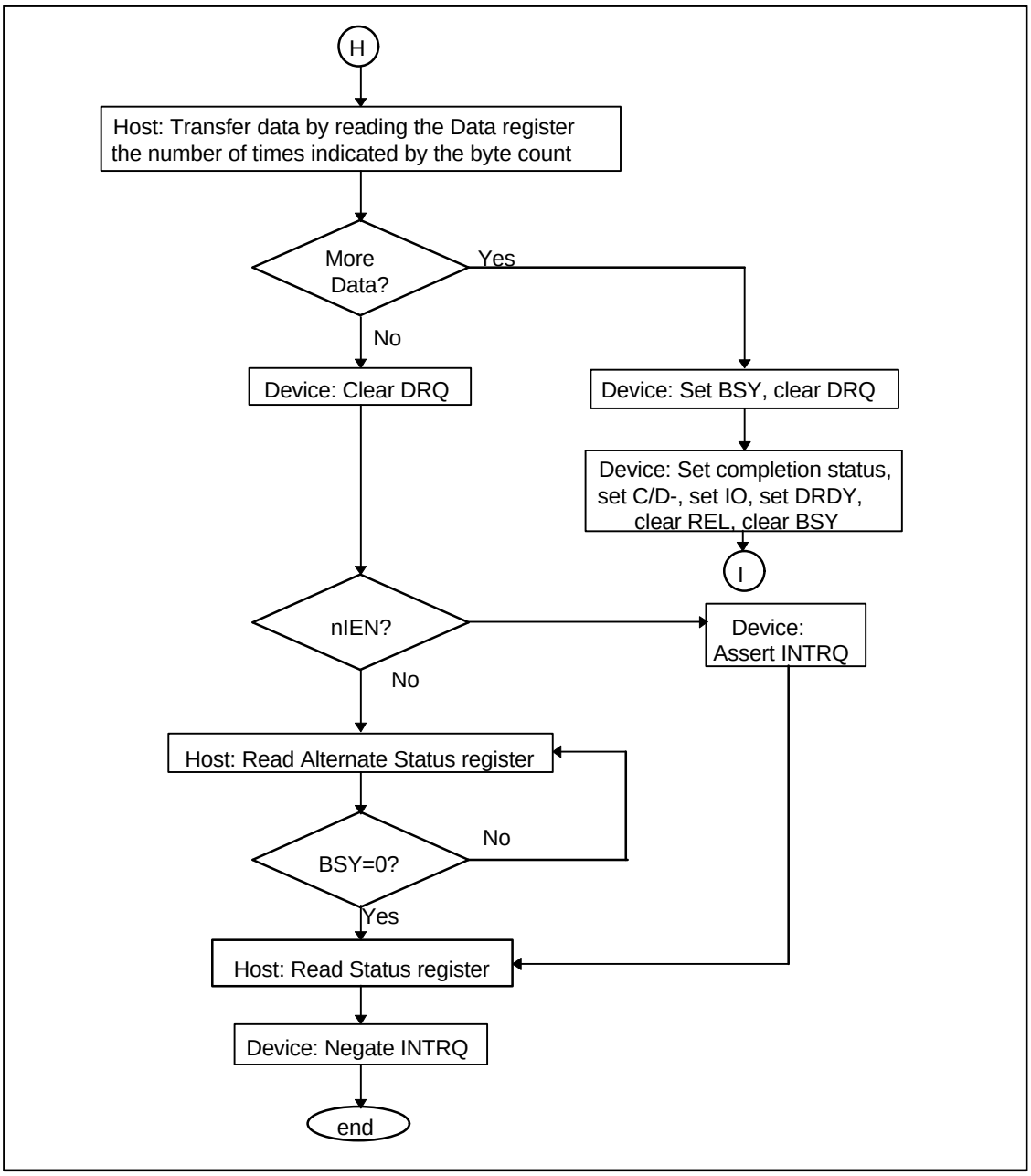


Figure 16 – **Overlapped PACKET DMA command** *(concluded)*

9.11 READ/WRITE DMA QUEUED command protocol

This class includes:

- READ DMA QUEUED
- SERVICE
- WRITE DMA QUEUED

Figure 17 describes the execution of a READ DMA QUEUED or WRITE DMA QUEUED command.

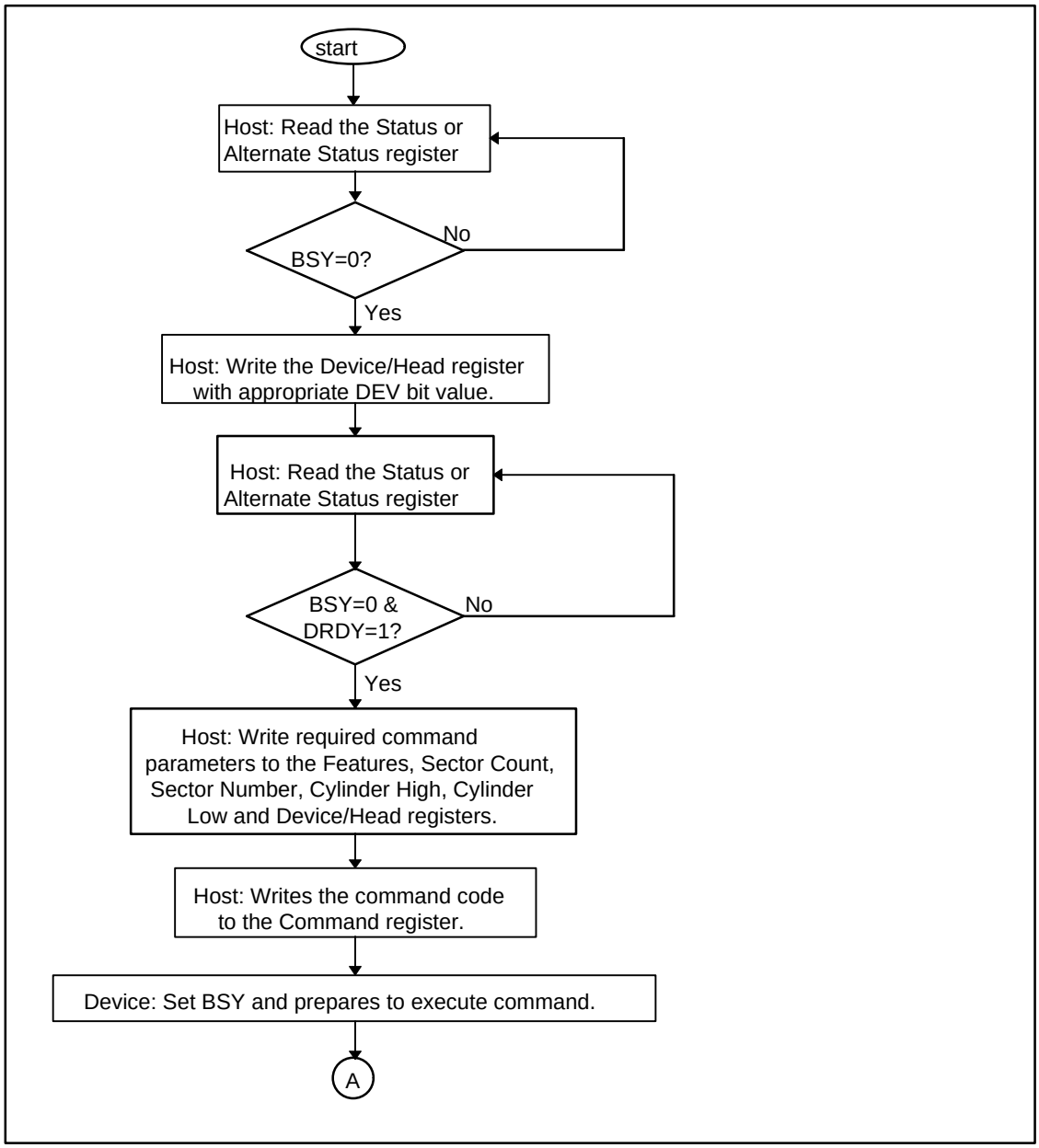


Figure 17 – READ/WRITE DMA QUEUED command *(continued)*

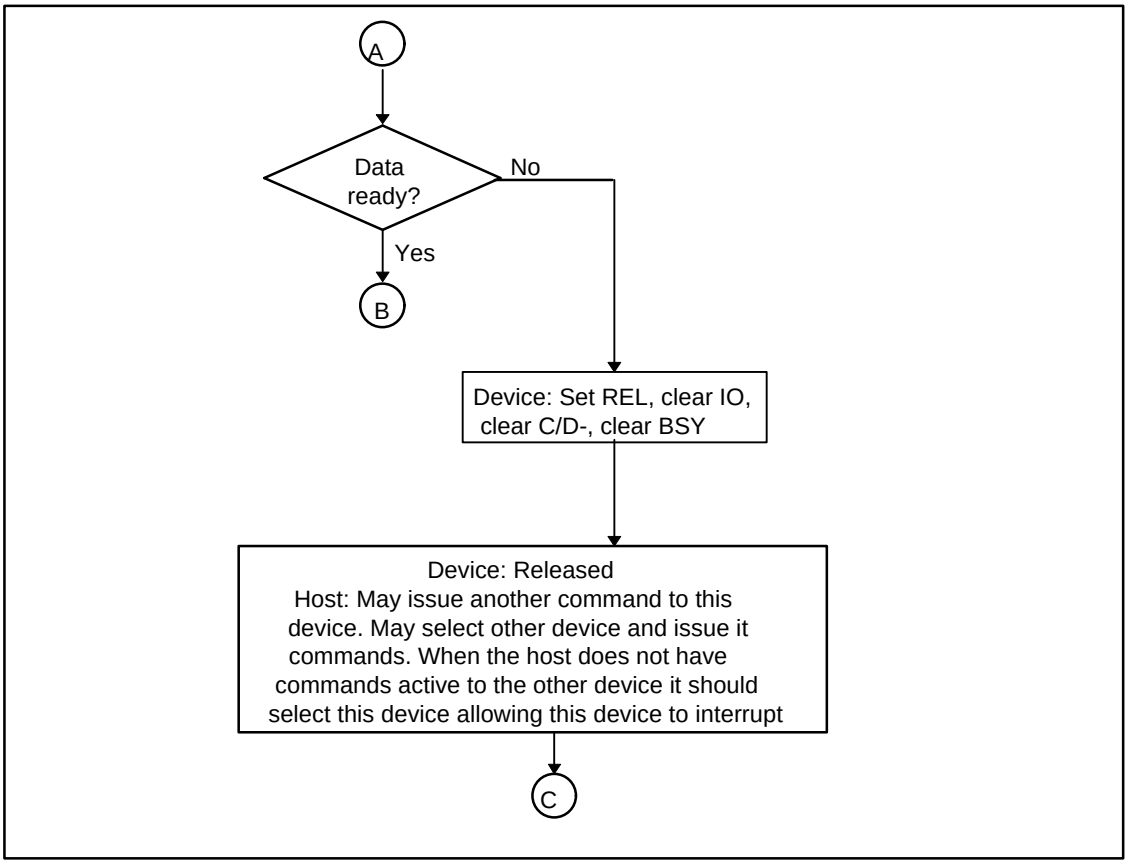
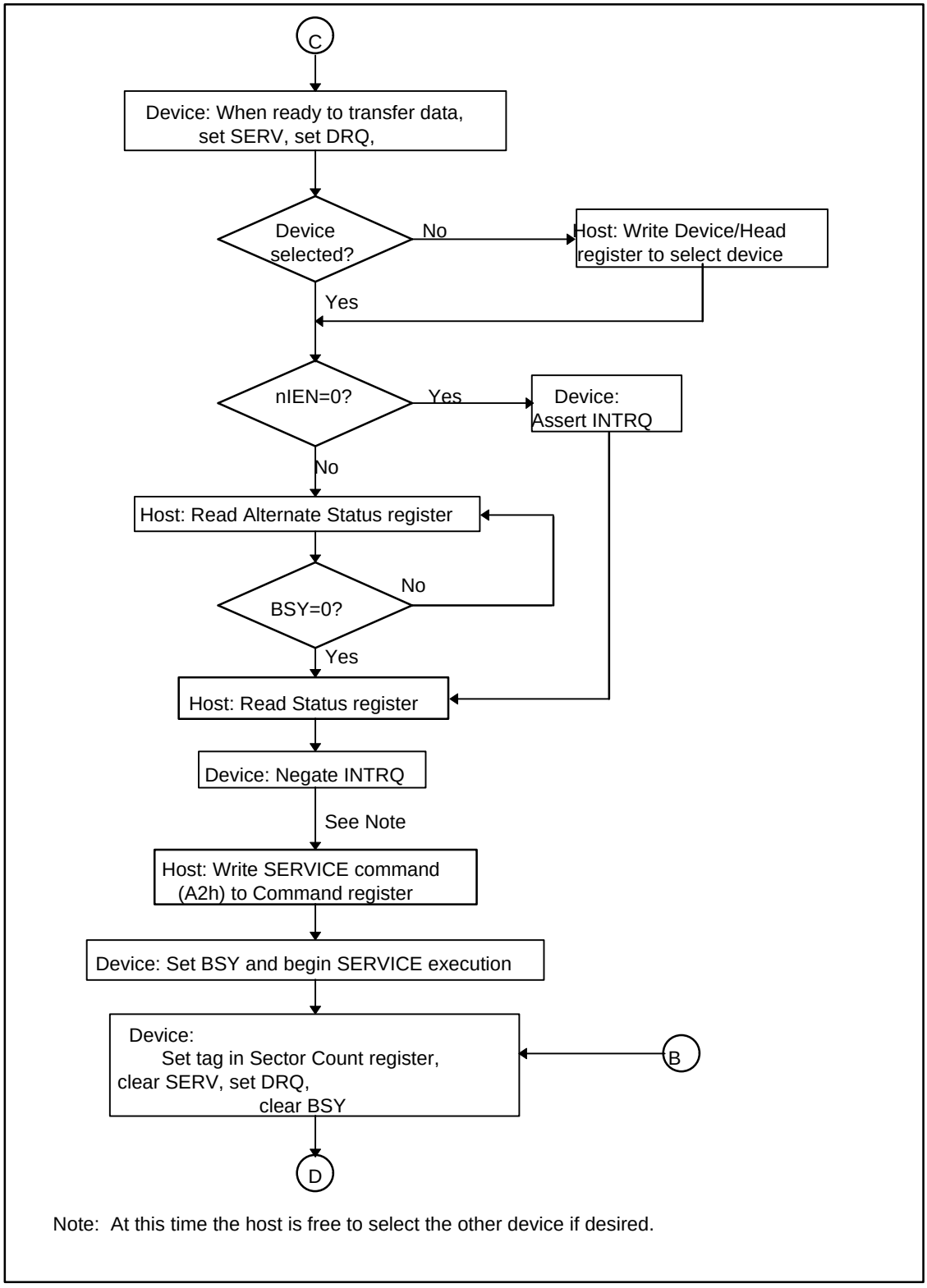


Figure 17 – READ/WRITE DMA QUEUED command*(continued)*



Note: At this time the host is free to select the other device if desired.

Figure 17 – READ/WRITE DMA QUEUED command *(continued)*

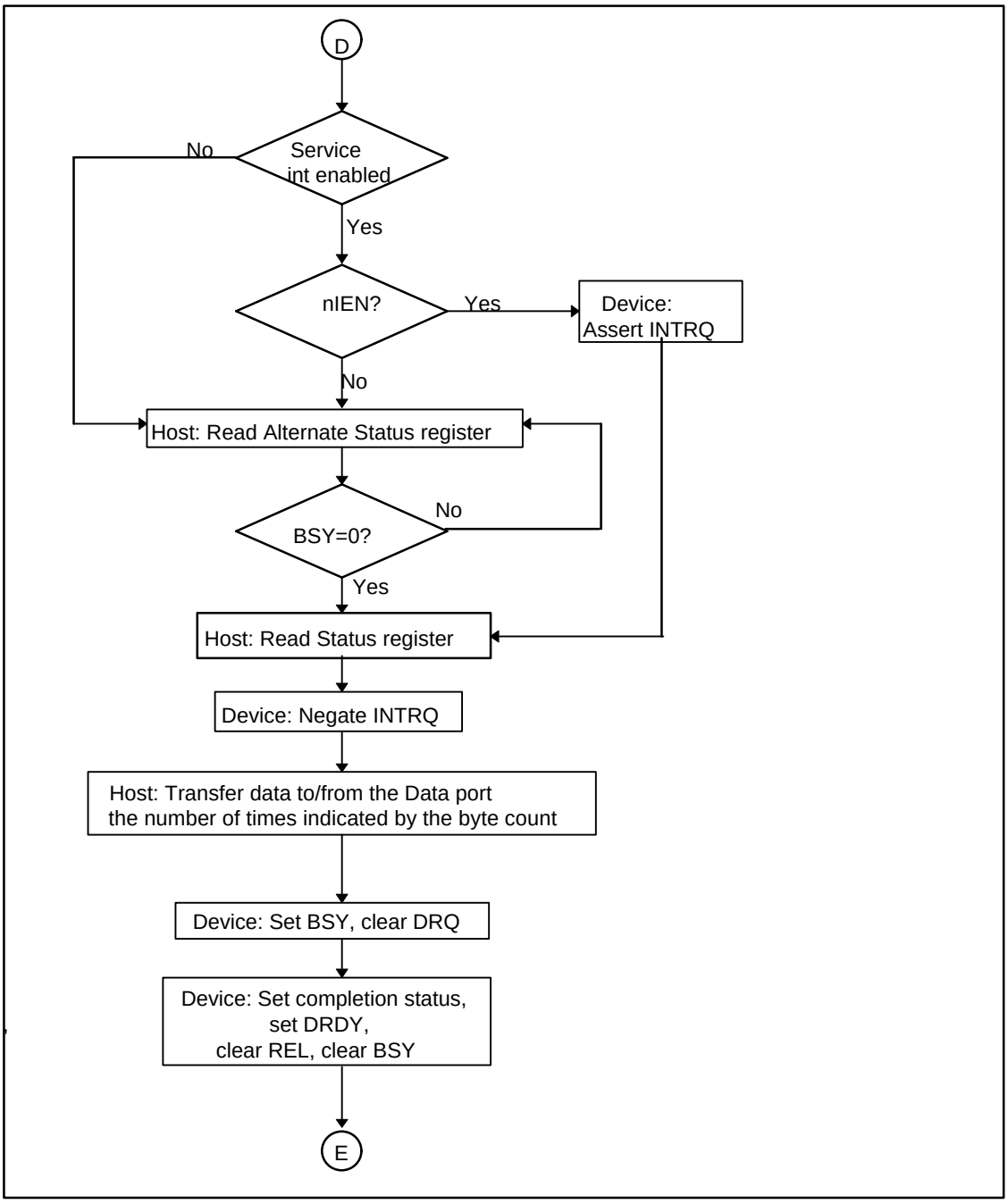


Figure 17 – READ/WRITE DMA QUEUED command*(continued)*

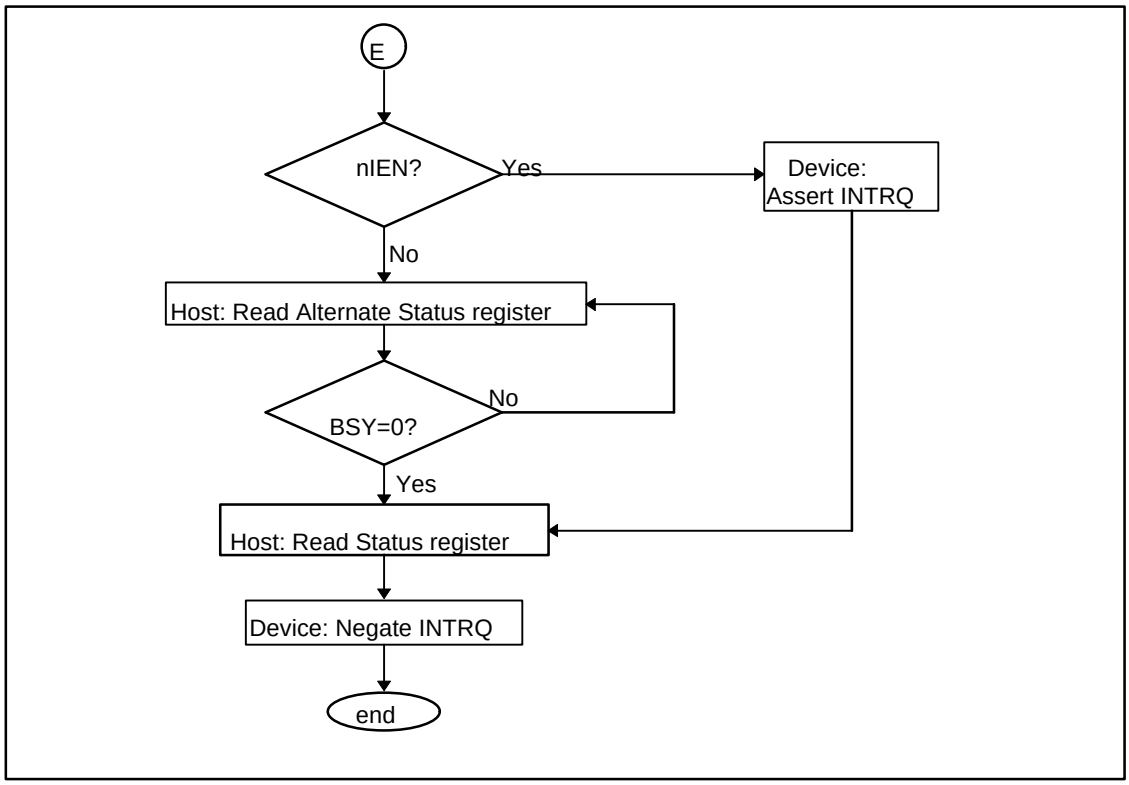


Figure 17 – **READ/WRITE DMA QUEUED command***(concluded)*

9.12 Ultra DMA data in commands

9.12.1 Initiating an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.1 and 10.2.4.11 for specific timing requirements):

1) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.
2) The device shall assert DMARQ to initiate an Ultra DMA burst. After assertion of DMARQ the device shall not negate DMARQ until after the first negation of DSTROBE.
3) Steps (3), (4) and (5) may occur in any order or at the same time. The host shall assert STOP.
4) The host shall negate HDMARDY-.
5) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.
6) Steps (3), (4) and (5) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.
7) The host shall release DD(15:0) within t_{AZ} after asserting DMACK-.
8) The device may assert DSTROBE t_{ZIORDY} after the host has asserted DMACK-. Once the device has driven DSTROBE the device shall not release DSTROBE until after the host has negated DMACK- at the end of an Ultra DMA burst.
9) The host shall negate STOP and assert HDMARDY- within t_{ENV} after asserting DMACK-. After negating STOP and asserting HDMARDY-, the host shall not change the state of either signal until after receiving the first transition of DSTROBE from the device (i.e., after the first data word has been received).
10) The device shall drive DD(15:0) no sooner than t_{ZAD} after the host has asserted DMACK-, negated STOP, and asserted HDMARDY-.
11) The device shall drive the first word of the data transfer onto DD(15:0). This step may occur when the device first drives DD(15:0) in step (10).
12) To transfer the first word of data the device shall negate DSTROBE within t_{FS} after the host has negated STOP and asserted HDMARDY-. The device shall negate DSTROBE no sooner than t_{DVS} after driving the first word of data onto DD(15:0).

9.12.2 The data in transfer

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.2 and 10.2.4.11):

1) The device shall drive a data word onto DD(15:0).
2) The device shall generate a DSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD(15:0). The device shall generate a DSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA Mode.
3) The device shall not change the state of DD(15:0) until at least t_{DVH} after generating a DSTROBE edge to latch the data.
4) The device shall repeat steps (1), (2) and (3) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

9.12.3 Pausing an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.3 and 10.2.4.11 for specific timing requirements).

9.12.3.1 Device pausing an Ultra DMA data in burst

1) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
2) The device shall pause an Ultra DMA burst by not generating DSTROBE edges. The host shall not immediately assert STOP when the device stops generating STROBE edges. If the device does not negate DMARQ and the host wishes to terminate the Ultra DMA burst, the host shall negate HDMARDY- and wait t_{RP} before asserting STOP.

3) The device shall resume an Ultra DMA burst by generating DSTROBE edges.

9.12.3.2 Host pausing an Ultra DMA data in burst

1) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
2) The host shall pause an Ultra DMA burst by negating HDMARDY-.
3) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.
4) If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
5) The host shall resume an Ultra DMA burst by asserting HDMARDY-.

9.12.4 Terminating an Ultra DMA data in burst

9.12.4.1 Device terminating an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.4 and 10.2.4.11 for specific timing requirements):

1) The device shall initiate termination of an Ultra DMA burst by not generating DSTROBE edges.
2) The device shall negate DMARQ no sooner than t_{SS} after generating the last DSTROBE edge. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
3) The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.
4) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
5) The host shall negate HDMARDY- within t_{LI} after the device has negated DMARQ. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated. Steps (4) and (5) may occur at the same time.
6) The host shall drive DD(15:0) no sooner than t_{ZAH} after the device has negated DMARQ
7) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
8) The host shall place the result of its CRC calculation on DD(15:0). See 9.14 for calculation of CRC. Step (8) may occur as soon as step (6).
9) The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of its CRC calculation on DD(15:0).
10) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
11) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs, the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See 9.14 for calculation of CRC.
12) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.
13) The host shall not negate STOP nor assert HDMARDY- until at least t_{ACK} after negating DMACK-.
14) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

9.12.4.2 Host terminating an Ultra DMA data in burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.5 and 10.2.4.11 for specific timing requirements):

1) The host shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
2) The host shall initiate Ultra DMA burst termination by negating HDMARDY-. The host shall continue to negate HDMARDY- until the Ultra DMA burst is terminated.

3) The device shall stop generating DSTROBE edges within t_{RFS} of the host negating HDMARDY-.
4) If the host negates HDMARDY- within t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero or one additional data words. If the host negates HDMARDY- greater than t_{SR} after the device has generated a DSTROBE edge, then the host shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the device.
5) The host shall assert STOP no sooner than t_{RP} after negating HDMARDY-. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
6) The device shall negate DMARQ within t_{LI} after the host has asserted STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
7) If DSTROBE is negated, the device shall assert DSTROBE within t_{LI} after the host has asserted STOP. No data shall be transferred during this assertion. The host shall ignore this transition on DSTROBE. DSTROBE shall remain asserted until the Ultra DMA burst is terminated.
8) The device shall release DD(15:0) no later than t_{AZ} after negating DMARQ.
9) The host shall drive DD(15:0) no sooner than t_{ZAH} after the device has negated DMARQ.
10) The host shall place the result of its CRC calculation on DD(15:0). See 9.14 for calculation of CRC.
11) The host shall negate DMACK- no sooner than t_{MLI} after the device has asserted DSTROBE and negated DMARQ and the host has asserted STOP and negated HDMARDY-, and no sooner than t_{DVS} after the host places the result of its CRC calculation on DD(15:0).
12) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
13) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs, the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See 9.14 for calculation of CRC.
14) The device shall release DSTROBE within t_{IORDYZ} after the host negates DMACK-.
15) The host shall neither negate STOP nor assert HDMARDY- until at least t_{ACK} after the host has negated DMACK-.
16) The host shall not assert DIOR-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

9.13 Ultra DMA data out commands

9.13.1 Initiating an Ultra DMA data out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.6 and 10.2.4.11 for specific timing requirements):

1) The host shall keep DMACK- in the negated state before an Ultra DMA burst is initiated.
2) The device shall assert DMARQ to initiate an Ultra DMA burst.
3) Steps (3), (4), and (5) may occur in any order or at the same time. The host shall assert STOP.
4) The host shall assert HSTROBE.
5) The host shall negate CS0-, CS1-, DA2, DA1, and DA0. The host shall keep CS0-, CS1-, DA2, DA1, and DA0 negated until after negating DMACK- at the end of the burst.
6) Steps (3), (4), and (5) shall have occurred at least t_{ACK} before the host asserts DMACK-. The host shall keep DMACK- asserted until the end of an Ultra DMA burst.
7) The device may negate DDMARDY- t_{ZIORDY} after the host has asserted DMACK-. Once the device has negated DDMARDY-, the device shall not release DDMARDY- until after the host has negated DMACK- at the end of an Ultra DMA burst.
8) The host shall negate STOP within t_{ENV} after asserting DMACK-. The host shall not assert STOP until after the first negation of HSTROBE.
9) The device shall assert DDMARDY- within t_{LI} after the host has negated STOP. After asserting DMARQ and DDMARDY- the device shall not negate either signal until after the first negation of HSTROBE by the host.
10) The host shall drive the first word of the data transfer onto DD(15:0). This step may occur any time during Ultra DMA burst initiation.
11) To transfer the first word of data: the host shall negate HSTROBE no sooner than t_{UI} after the device has asserted DDMARDY-. The host shall negate HSTROBE no sooner than t_{DVS} after the driving the first word of data onto DD(15:0).

9.13.2 The data out transfer

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.7 and 10.2.4.11 for specific timing requirements):

1) The host shall drive a data word onto DD(15:0).
2) The host shall generate an HSTROBE edge to latch the new word no sooner than t_{DVS} after changing the state of DD(15:0). The host shall generate an HSTROBE edge no more frequently than t_{CYC} for the selected Ultra DMA Mode.
3) The host shall not change the state of DD(15:0) until at least t_{DVH} after generating an HSTROBE edge to latch the data.
4) The host shall repeat steps (1), (2) and (3) until the data transfer is complete or an Ultra DMA burst is paused, whichever occurs first.

9.13.3 Pausing an Ultra DMA data out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.8 and 10.2.4.11 for specific timing requirements).

9.13.3.1 Host pausing an Ultra DMA data out burst

1) The host shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
2) The host shall pause an Ultra DMA burst by not generating an HSTROBE edge. The device shall not immediately negate DMARQ when the host stops generating STROBE edges. If the host does not assert STOP and the device wishes to terminate the Ultra DMA burst, the device shall negate DDMARDY- and wait t_{RP} before negating DMARQ.
3) The host shall resume an Ultra DMA burst by generating HSTROBE edges.

9.13.3.2 Device pausing an Ultra DMA data out burst

1) The device shall not pause an Ultra DMA burst until at least one data word of an Ultra DMA burst has been transferred.
2) The device shall pause an Ultra DMA burst by negating DDMARDY-.
3) The host shall stop generating HSTROBE edges within t_{RFS} of the device negating DDMARDY-.
4) If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
5) The device shall resume an Ultra DMA burst by asserting DDMARDY-.

9.13.4 Terminating an Ultra DMA data out burst

9.13.4.1 Host terminating an Ultra DMA data out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.9 and 10.2.4.11 for specific timing requirements):

1) The host shall initiate termination of an Ultra DMA burst by not generating HSTROBE edges.
2) The host shall assert STOP no sooner than t_{SS} after it last generated an HSTROBE edge. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
3) The device shall negate DMARQ within t_{LI} after the host asserts STOP. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
4) The device shall negate DDMARDY- within t_{LI} after the host has negated STOP. The device shall not assert DDMARDY- again until after the Ultra DMA burst termination is complete.

5) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition on HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
6) The host shall place the result of its CRC calculation on DD(15:0). See 9.14 for calculation of CRC.
7) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t_{DVS} after placing the result of its CRC calculation on DD(15:0).
8) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
9) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See 9.14 for calculation of CRC.
10) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.
11) The host shall neither negate STOP nor negate HSTROBE until at least t_{ACK} after negating DMACK-.
12) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

9.13.4.2 Device terminating an Ultra DMA data out burst

The following steps shall occur in the order they are listed unless otherwise specifically allowed (see 10.2.4.10 and 10.2.4.11 for specific timing requirements):

1) The device shall not initiate Ultra DMA burst termination until at least one data word of an Ultra DMA burst has been transferred.
2) The device shall initiate Ultra DMA burst termination by negating DDMARDY-.
3) The host shall stop generating an HSTROBE edges within t_{RFS} of the device negating DDMARDY-.
4) If the device negates DDMARDY- within t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero or one additional data words. If the device negates DDMARDY- greater than t_{SR} after the host has generated an HSTROBE edge, then the device shall be prepared to receive zero, one or two additional data words. The additional data words are a result of cable round trip delay and t_{RFS} timing for the host.
5) The device shall negate DMARQ no sooner than t_{RP} after negating DDMARDY-. The device shall not assert DMARQ again until after the Ultra DMA burst is terminated.
6) The host shall assert STOP within t_{LI} after the device has negated DMARQ. The host shall not negate STOP again until after the Ultra DMA burst is terminated.
7) If HSTROBE is negated, the host shall assert HSTROBE within t_{LI} after the device has negated DMARQ. No data shall be transferred during this assertion. The device shall ignore this transition of HSTROBE. HSTROBE shall remain asserted until the Ultra DMA burst is terminated.
8) The host shall place the result of its CRC calculation on DD(15:0). See 9.14 for calculation of CRC.
9) The host shall negate DMACK- no sooner than t_{MLI} after the host has asserted HSTROBE and STOP and the device has negated DMARQ and DDMARDY-, and no sooner than t_{DVS} after placing the result of its CRC calculation on DD(15:0).
10) The device shall latch the host's CRC data from DD(15:0) on the negating edge of DMACK-.
11) The device shall compare the CRC data received from the host with the results of its own CRC calculation. If a miscompare error occurs the device shall retain the fact that a miscompare error has occurred for reporting at the end of the command. See 9.14 for calculation of CRC.
12) The device shall release DDMARDY- within t_{IORDYZ} after the host has negated DMACK-.
13) The host shall neither negate STOP nor HSTROBE until at least t_{ACK} after negating DMACK-.
14) The host shall not assert DIOW-, CS0-, CS1-, DA2, DA1, or DA0 until at least t_{ACK} after negating DMACK.

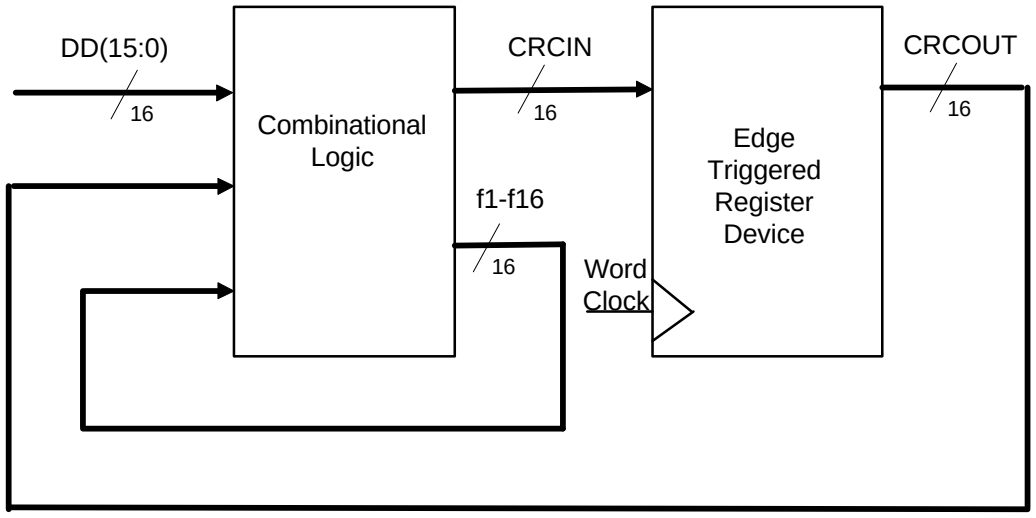
9.14 Ultra DMA CRC rules

The following is a list of rules for calculating CRC, determining if a CRC error has occurred during an Ultra DMA burst, and reporting any error that occurs at the end of a command.

a) Both the host and the device shall have a 16-bit CRC calculation function.
b) Both the host and the device shall calculate a CRC value for each Ultra DMA burst.

c) The CRC function in the host and the device shall be initialized with a seed of 4ABAh at the beginning of an Ultra DMA burst before any data is transferred.
d) For each STROBE transition used for data transfer, both the host and the device shall calculate a new CRC value by applying the CRC polynomial to the current value of their individual CRC functions and the word being transferred. CRC is not calculated for the return of STROBE to the asserted state after the Ultra DMA burst termination request has been acknowledged.
e) At the end of any Ultra DMA burst the host shall send the results of its CRC calculation function to the device on DD(15:0) with the negation of DMACK-.
f) The device shall then compare the CRC data from the host with the calculated value in its own CRC calculation function. If the two values do not match, the device shall save the error and report it at the end of the command. A subsequent Ultra DMA burst for the same command that does not have a CRC error shall not clear an error saved from a previous Ultra DMA burst in the same command.
g) For READ DMA, WRITE DMA, READ DMA O/Q or WRITE DMA O/Q commands: When a CRC error is detected, it shall be reported by setting both ICRC and ABRT (bit 7 and bit 2 in the Error register) to one. ICRC is defined as the “Interface CRC Error” bit. All ATA host driver software shall detect and respond to this error type. The response by a host to this error should be to re-issue the command. It is recommended that new host device drivers respond to this error by notifying the user of the CRC error and re-issuing the command.
h) For a REQUEST SENSE packet command: When a CRC error is detected during transmission of sense data the device shall complete the command and set CHK to one. The device shall report a Sense key of 0Bh (ABORTED COMMAND). The device shall preserve the original sense data that was being returned when the CRC error occurred. The device shall not place any additional sense data specific to the CRC error in its queue. The host device driver may retry the REQUEST SENSE command or may consider this a fatal error and retry the command that caused the Check Condition.
g) For any packet command except a REQUEST SENSE command: If a CRC error is detected, the device shall complete the command with CHK set to one. The device shall report a Sense key of 04h (HARDWARE ERROR). The sense data supplied via a subsequent REQUEST SENSE command shall report an ASC/ASCQ value of 08h/03h (LOGICAL UNIT COMMUNICATION CRC ERROR). It is expected that host drivers will retry the command during which the HARDWARE ERROR occurred.
i) A host may send extra data words on the last Ultra DMA burst of a data out command. If a device determines that all data has been transferred for a command, the device shall terminate the burst. A device may have already received more data words than were required for the command. These extra words are used by both the host and the device to calculate the CRC, but, on an Ultra DMA data out burst, the extra words shall be discarded by the device.
j) The CRC generator polynomial is: G(X) = X16 + X12 + X5 + 1. The equations for 16-bit parallel generation of the resulting polynomial (based on a word boundary) are described in Table c1.

Note: Since no bit clock is available, the recommended approach for calculating CRC is to use a word clock derived from the bus strobe. The combinatorial logic shall then be equivalent to shifting sixteen bits serially through the generator polynomial where DD0 is shifted in first and DD15 is shifted in last.



Example - Parallel CRC generator

Table c1 - Equations for parallel generation of a CRC polynomial

CRCIN0 = f16	CRCIN8 = f8 XOR f13
CRCIN1 = f15	CRCIN9 = f7 XOR f12
CRCIN2 = f14	CRCIN10 = f6 XOR f11
CRCIN3 = f13	CRCIN11 = f5 XOR f10
CRCIN4 = f12	CRCIN12 = f4 XOR f9 XOR f16
CRCIN5 = f11 XOR f16	CRCIN13 = f3 XOR f8 XOR f15
CRCIN6 = f10 XOR f15	CRCIN14 = f2 XOR f7 XOR f14
CRCIN7 = f9 XOR f14	CRCIN15 = f1 XOR f6 XOR f13

f1 = DD0 XOR CRCOUT15	f9 = DD8 XOR CRCOUT7 XOR f5
f2 = DD1 XOR CRCOUT14	f10 = DD9 XOR CRCOUT6 XOR f6
f3 = DD2 XOR CRCOUT13	f11 = DD10 XOR CRCOUT5 XOR f7
f4 = DD3 XOR CRCOUT12	f12 = DD11 XOR CRCOUT4 XOR f1 XOR f8
f5 = DD4 XOR CRCOUT11 XOR f1	f13 = DD12 XOR CRCOUT3 XOR f2 XOR f9
f6 = DD5 XOR CRCOUT10 XOR f2	f14 = DD13 XOR CRCOUT2 XOR f3 XOR f10
f7 = DD6 XOR CRCOUT9 XOR f3	f15 = DD14 XOR CRCOUT1 XOR f4 XOR f11
f8 = DD7 XOR CRCOUT8 XOR f4	f16 = DD15 XOR CRCOUT0 XOR f5 XOR f12

Notes:
1) f = feedback
2) DD = Data to or from the bus
3) CRCOUT = 16-bit edge triggered result (current CRC)
4) CRCOUT(15:0) are sent on matching order bits of DD(15:0)
5) CRCIN = Output of combinatorial logic (next CRC)

9.15 Single device configurations

9.15.1 Device 0 only configurations

In a single device configuration where Device 0 is the only device and the host selects Device 1, Device 0 shall respond as follows:

a) A write to the Device Control register shall complete as if Device 0 was the selected device;

b) A write to a Command Block register, other than the Command register, shall complete as if Device 0 was selected;

c) A write to the Command register shall be ignored, except for EXECUTE DEVICE DIAGNOSTIC;

d) A read of the Control Block or Command Block registers, other than the Status or Alternate Status registers, shall complete as if Device 0 was selected;

e) A read of the Status or Alternate status register shall return the value 00h;

9.15.2 Device 1 only configurations

Host support of Device 1 only configurations is host specific.

In a single device configuration where Device 1 is the only device and the host selects Device 0, Device 1 shall respond to accesses of the Command Block and Control Block registers in the same way it would if Device 0 was present. This is because Device 1 cannot determine if Device 0 is, or is not, present.

Host implementation of read and write operations to the Command and Control Block registers of non-existent Device 0 are host specific.

NOTE – The remainder of this section is a host implementation note.

The host implementor should be aware of the following when supporting Device 1 only configurations:

a) Following a hardware reset or software reset, Device 1 will not be selected. The following steps may be used to reselect Device 1:

   1) Write to the Device/Head register with DRV bit set to one;
   2) Using one or more of the Command Block registers that may be both written and read, such as the Sector Count or Sector Number, write a data pattern other than 00h or FFh to the register(s);
   3) Read the register(s) written in step (2). If the data read is the same as the data written, proceed to step (5);
   4) Repeat steps (1) to (3) until the data matches in step (3) or until 31 s has past. After 31 s it may probably be assumed that Device 1 is not functioning properly;
   5) Read the Status register and Error registers. Check the Status and Error register contents for any error conditions that Device 1 may have posted.

b) Following the execution of an EXECUTE DEVICE DIAGNOSTIC command, Device 1 will not be selected. Also, no interrupt will be generated to signal the completion of the

command. After writing the EXECUTE DEVICE DIAGNOSTIC command to the Command register, execute steps (1) to (5) as described in (a) above;

c) At all other times, do not write zero into the DRV bit of the Device/Head register. All other commands execute normally.

10 Timing

10.1 Deskewing

The host shall provide cable deskewing for all signals originating from the device. The device shall provide cable deskewing for all signals originating at the host.

All timing values and diagrams are shown and measured at the connector of either device connected to the interface. No values are given for measurement at the host interface.

See 3.2.6 for timing diagram conventions.

10.2 Transfer timing

The minimum cycle time supported by the device in PIO Mode 3, 4 and Multiword DMA Mode 1, 2 respectively shall always be greater than or equal to the minimum cycle time defined by the associated Mode e.g., a drive supporting PIO Mode 4 timing shall not report a value less than 120 ns, the minimum cycle time defined for PIO Mode 4 timings.

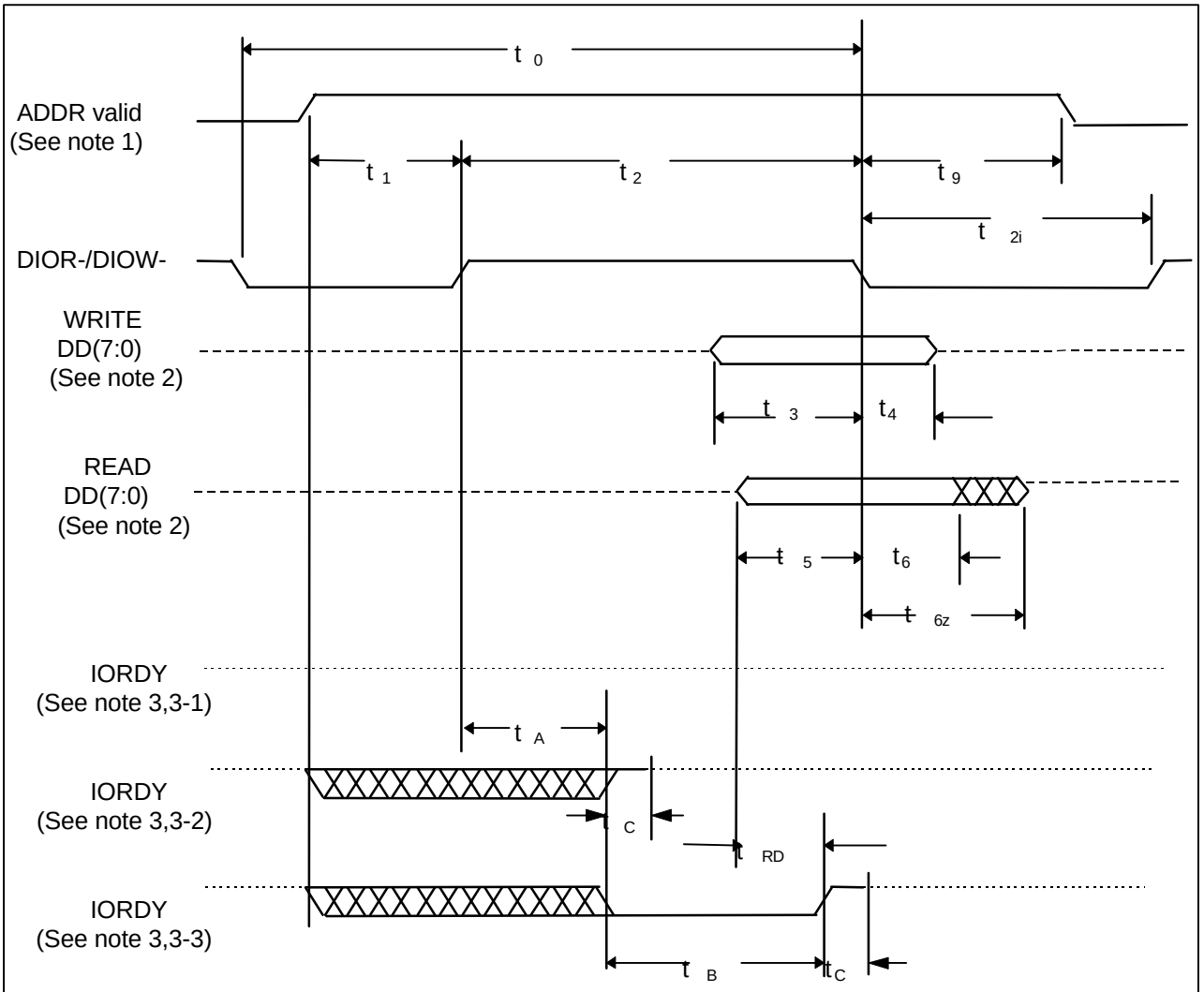
10.2.1 Register transfers

Figure 18 defines the relationships between the interface signals for register transfers. Peripherals reporting support for PIO Mode 3 or 4 shall power up in a PIO Mode 0, 1, or 2.

For PIO Modes 3 and above, the minimum value of t_0 is specified by word 68 in the Identify Drive parameter list. Table 23 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.

NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO Mode 3 and enable IORDY as the default.



Notes:
1 Device address consists of signals CS0-, CS1- and DA(2:0)
2 Data consists of DD(7:0).
3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
3-2 Device negates IORDY before t A, but causes IORDY to be asserted before t A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
3-3 Device negates IORDY before t A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(7:0) for t_{RD} before asserting IORDY.

Figure 18 – Register transfer to/from device

Table 23 – Register transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time	(min)	600	383	240	180	120	1
t_1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t_2	DIOR-/DIOW- pulse width 8-bit	(min)	290	290	290	80	70	1
t_{2i}	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t_3	DIOW- data setup	(min)	60	45	30	30	20	
t_4	DIOW- data hold	(min)	30	20	15	10	10	
t_5	DIOR- data setup	(min)	50	35	20	20	20	
t_6	DIOR- data hold	(min)	5	5	5	5	5	
t_{6Z}	DIOR- data tristate	(max)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after tA)	(min)	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	3
t_B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	

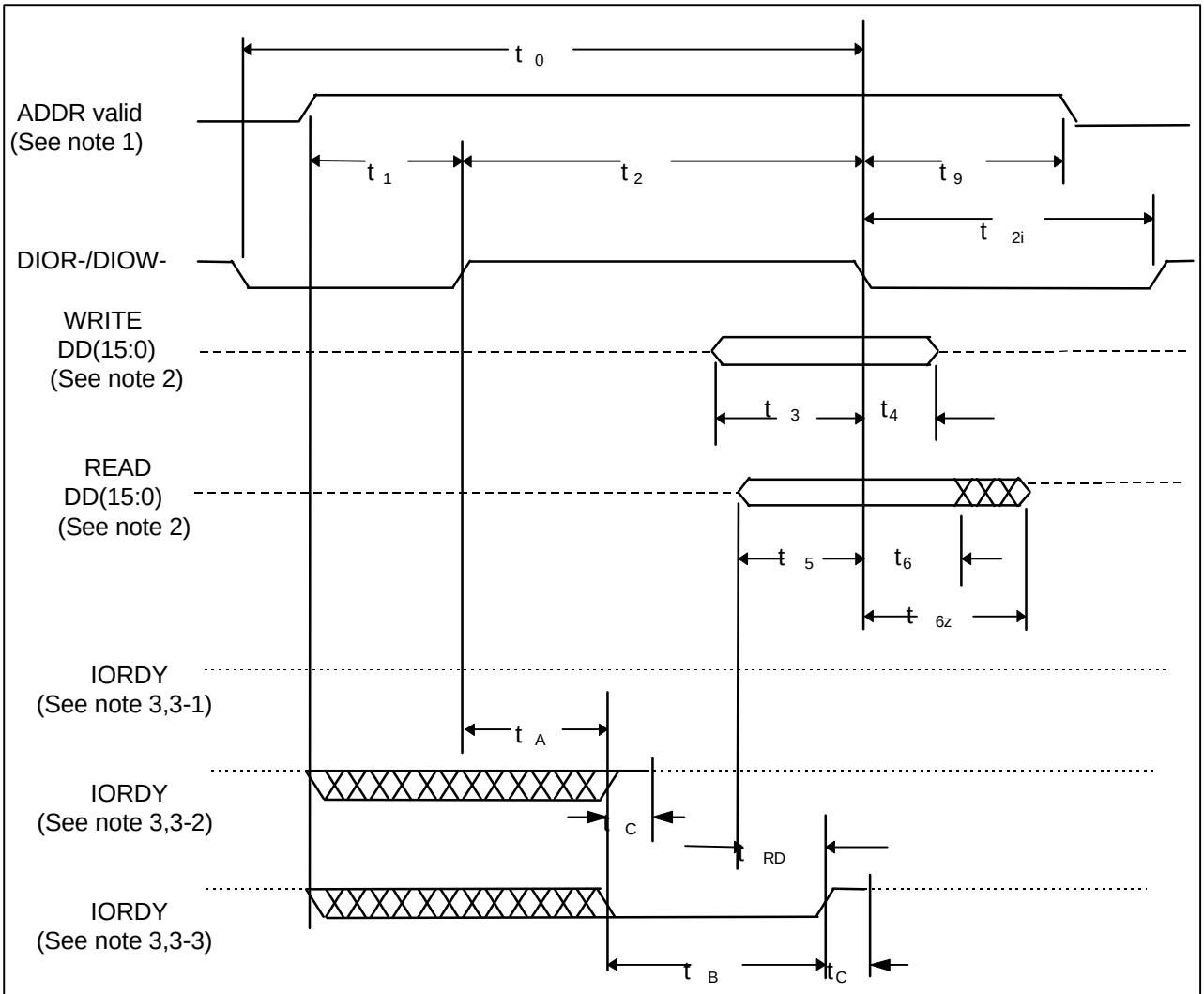
NOTES –

1 t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements is greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.

10.2.2 PIO data transfers



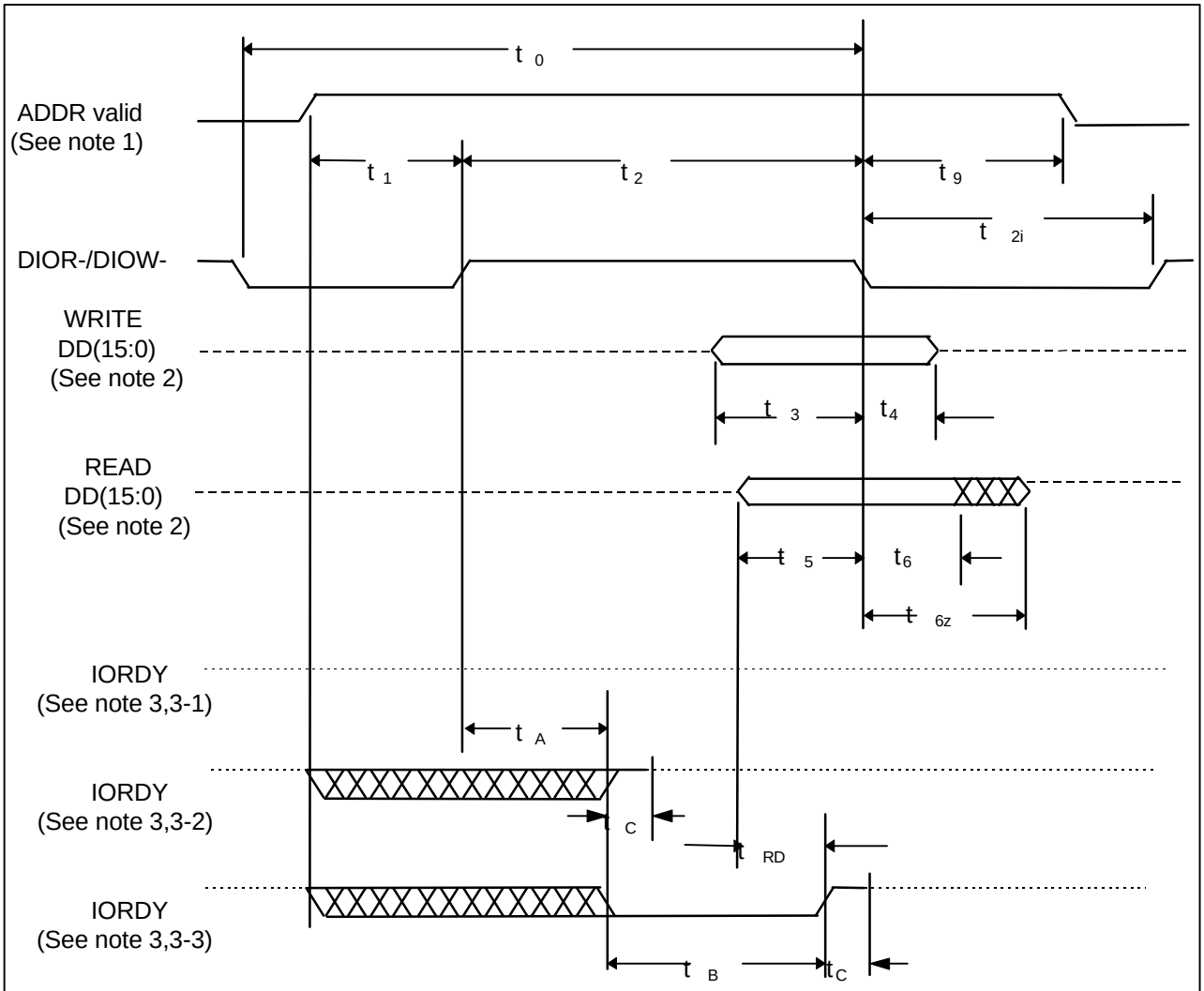
Notes:
1 Device address consists of signals CS0-, CS1- and DA(2:0)
2 Data consists of DD(15:0).
3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(15:0) for t_{RD} before asserting IORDY.

Figure 19 defines the relationships between the interface signals for PIO data transfers. Peripherals reporting support for PIO Mode 3 or 4 shall power up in a PIO Mode 0, 1 or 2.

For PIO Modes 3 and above, the minimum value of t_0 is specified by word 68 in the Identify Drive parameter list. Table 24 defines the minimum value that shall be placed in word 68.

IORDY shall be supported when PIO Mode 3 or 4 are the current mode of operation.

NOTE – Some devices implementing the PACKET Command feature set prior to this standard power up in PIO Mode 3 and enable IORDY as the default.



Notes:
1 Device address consists of signals CS0-, CS1- and DA(2:0)
2 Data consists of DD(15:0).
3 The negation of IORDY by the device is used to extend the PIO cycle. The determination of whether the cycle is to be extended is made by the host after t_A from the assertion of DIOR- or DIOW-. The assertion and negation of IORDY are described in the following three cases:
3-1 Device never negates IORDY, devices keeps IORDY released: no wait is generated.
3-2 Device negates IORDY before t_A, but causes IORDY to be asserted before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: no wait generated.
3-3 Device negates IORDY before t_A. IORDY is released prior to negation and may be asserted for no more than 5 ns before release: wait generated. The cycle completes after IORDY is reasserted. For cycles where a wait is generated and DIOR- is asserted, the device shall place read data on DD(15:0) for t_{RD} before asserting IORDY.

Figure 19 – PIO data transfer to/from device

Table 24 – PIO data transfer to/from device

PIO timing parameters			Mode 0 ns	Mode 1 ns	Mode 2 ns	Mode 3 ns	Mode 4 ns	Note
t_0	Cycle time	(min)	600	383	240	180	120	1
t_1	Address valid to DIOR-/DIOW- setup	(min)	70	50	30	30	25	
t_2	DIOR-/DIOW- 16-bit	(min)	165	125	100	80	70	1
t_{2i}	DIOR-/DIOW- recovery time	(min)	-	-	-	70	25	1
t_3	DIOW- data setup	(min)	60	45	30	30	20	
t_4	DIOW- data hold	(min)	30	20	15	10	10	
t_5	DIOR- data setup	(min)	50	35	20	20	20	
t_6	DIOR- data hold	(min)	5	5	5	5	5	
t_{6Z}	DIOR- data tristate	(max)	30	30	30	30	30	2
t_9	DIOR-/DIOW- to address valid hold	(min)	20	15	10	10	10	
t_{RD}	Read Data Valid to IORDY active (if IORDY initially low after tA)	(min)	0	0	0	0	0	
t_A	IORDY Setup time		35	35	35	35	35	3
t_B	IORDY Pulse Width	(max)	1250	1250	1250	1250	1250	

NOTES –

1 t_0 is the minimum total cycle time, t_2 is the minimum command active time, and t_{2i} is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_2, and t_{2i} shall be met. The minimum total cycle time requirements is greater than the sum of t_2 and t_{2i}. This means a host implementation may lengthen either or both t_2 or t_{2i} to ensure that t_0 is equal to or greater than the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

2 This parameter specifies the time from the negation edge of DIOR- to the time that the data bus is no longer driven by the device (tri-state).

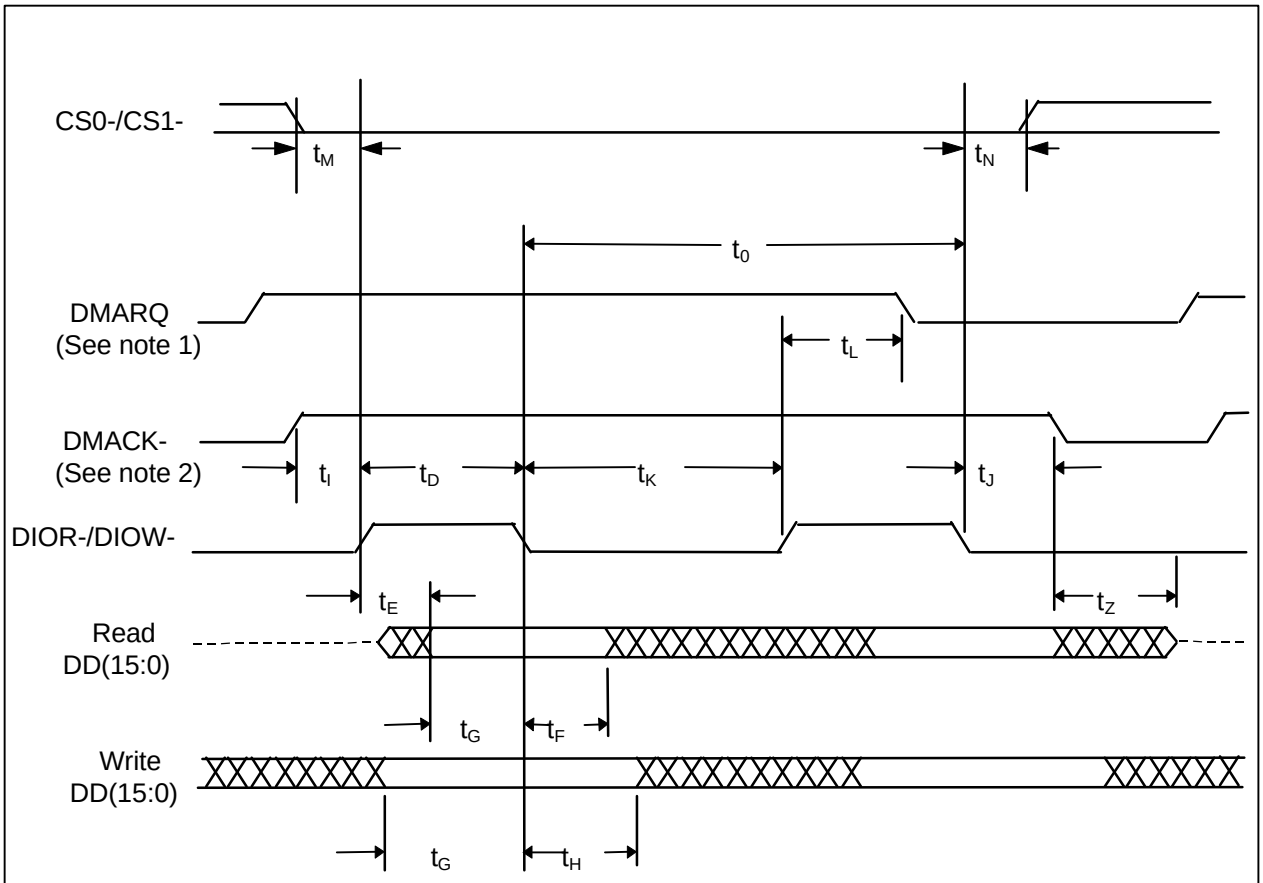
3 The delay from the activation of DIOR- or DIOW- until the state of IORDY is first sampled. If IORDY is inactive then the host shall wait until IORDY is active before the PIO cycle is completed. If the device is not driving IORDY negated at the t_A after the activation of DIOR- or DIOW-, then t_5 shall be met and tRD is not applicable. If the device is driving IORDY negated at the time t_A after the activation of DIOR- or DIOW-, then t_{RD} shall be met and t_5 is not applicable.

10.2.3 Multiword DMA data transfer

Figure 20 defines the timings associated with Multiword DMA transfers.

For Multiword DMA Modes 1 and above, the minimum value of t_0 is specified by word 65 in the Identify Drive parameter list. Table 25 defines the minimum value that shall be placed in word 65.

Devices reporting support for Multiword DMA Mode 2 shall also support Multiword DMA Transfer Mode 0 and 1 and shall power up with Mode 0 as the default Multiword DMA mode.



NOTE:
1 For Multi-Word DMA transfers, the Device may negate DMARQ within the t_L specified time once DMACK- is asserted and reassert it again at a later time to resume the DMA operation. Alternatively, if the device is able to continue the transfer of data, the device may leave DMARQ asserted and wait for the host to reassert DMACK-.
2 This signal may be negated by the Host to suspend the DMA transfer in process.

Figure 20 – Multiword DMA data transfer

Table 25 – Multiword DMA data transfer

	Multiword DMA timing parameters		Mode 0 ns	Mode 1 ns	Mode 2 ns	Note
t_0	Cycle time	(min)	480	150	120	see note
t_C	DMACK to DMARQ delay					
t_D	DIOR-/DIOW-	(min)	215	80	70	see note
t_E	DIOR- data access	(max)	150	60		
t_F	DIOR- data hold	(min)	5	5	5	
t_G	DIOR-/DIOW- data setup	(min)	100	30	20	
t_H	DIOW- data hold	(min)	20	15	10	
t_I	DMACK to DIOR-/DIOW- setup	(min)	0	0	0	
t_J	DIOR-/DIOW- to DMACK hold	(min)	20	5	5	
t_{KR}	DIOR- negated pulse width	(min)	50	50	25	see note
t_{KW}	DIOW- negated pulse width	(min)	215	50	25	see note
t_{LR}	DIOR- to DMARQ delay	(max)	120	40	35	
t_{LW}	DIOW- to DMARQ delay	(max)	40	40	35	
t_Z	DMACK- to tristate	(max)	20	25	25	

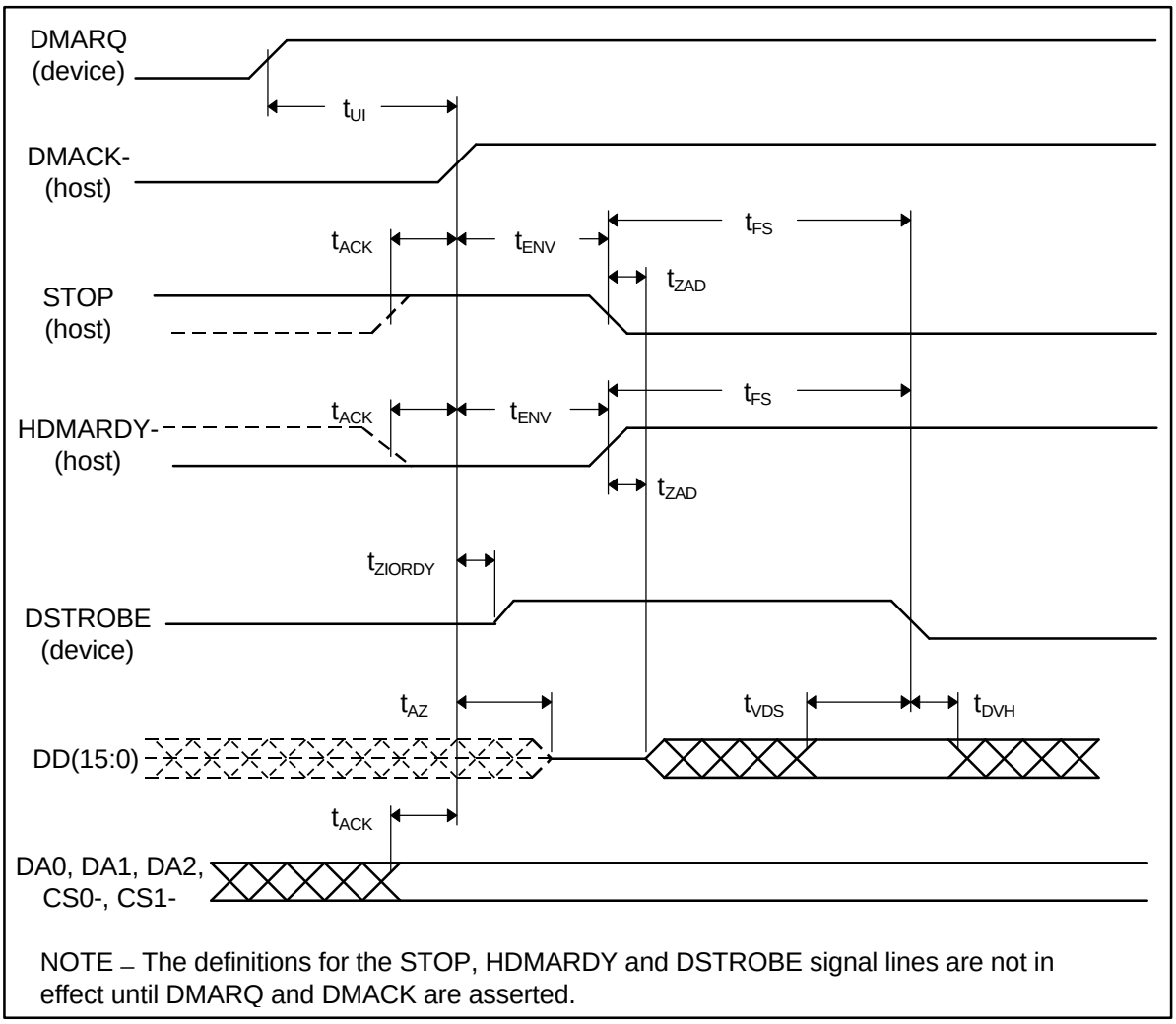
NOTE – t_0 is the minimum total cycle time, t_D is the minimum command active time, and t_K (t_{KR} or t_{KW}, as appropriate) is the minimum command recovery time or command inactive time. The actual cycle time equals the sum of the actual command active time and the actual command inactive time. The three timing requirements of t_0, t_D, t_K shall be met. The minimum total cycle time requirement, t_0, is greater than the sum of t_D and t_K. This means a host implementation may lengthen either or both t_D or t_K to ensure that t_0 is equal to the value reported in the devices identify drive data. A device implementation shall support any legal host implementation.

10.2.4 Ultra DMA data transfer

Figure 21 through Figure 30 define the timings associated with all phases of Ultra DMA bursts.

Table 26 contains the values for the timings for each of the Ultra DMA Modes.

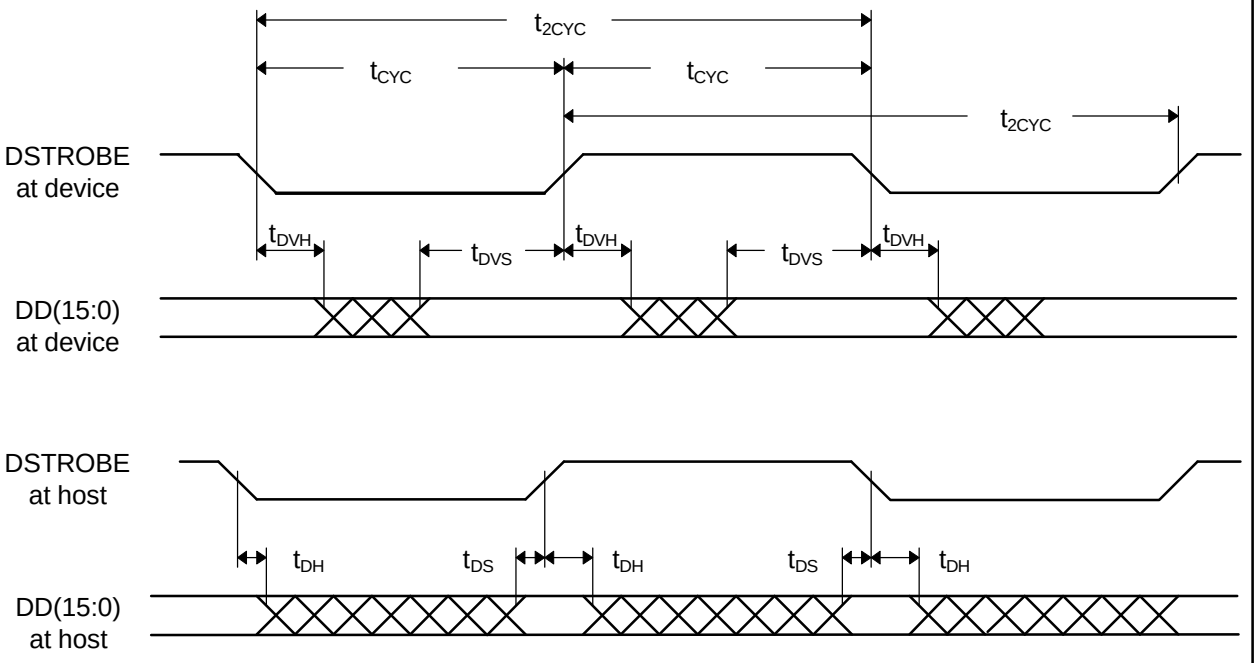
10.2.4.1 Initiating an Ultra DMA data in burst



NOTE – The definitions for the STOP, HDMARDY and DSTROBE signal lines are not in effect until DMARQ and DMACK are asserted.

Figure 21 – Initiating an Ultra DMA data in burst

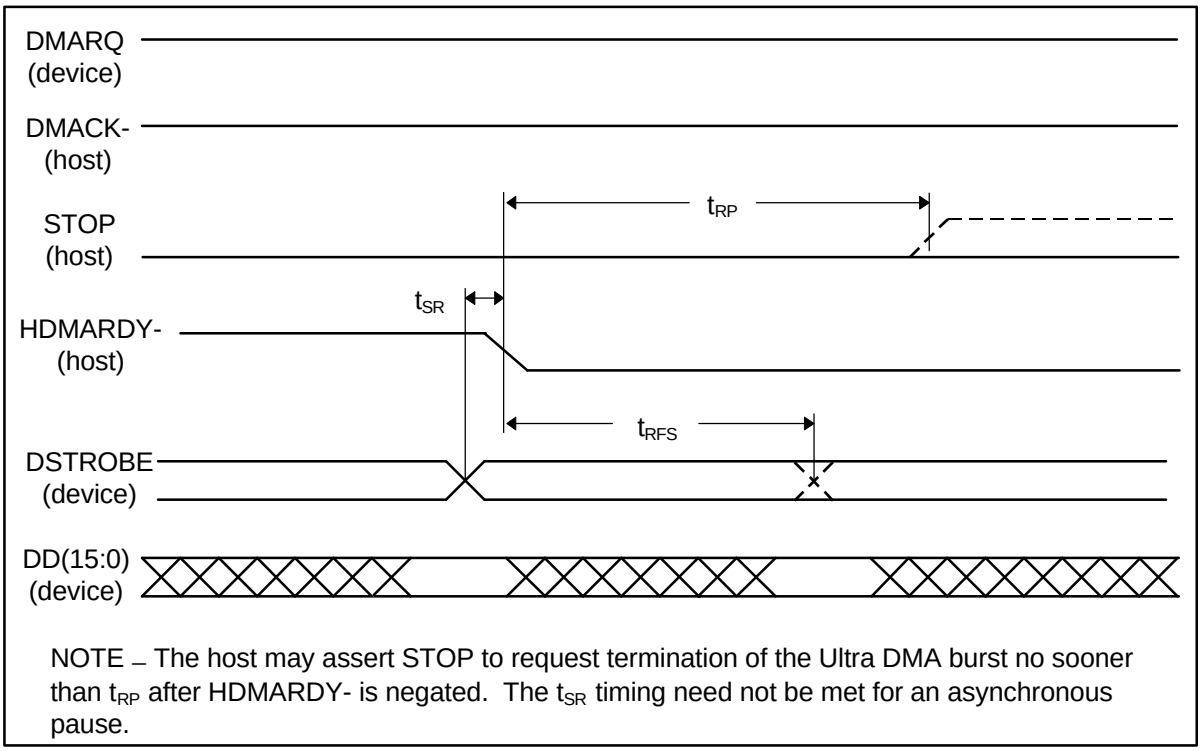
10.2.4.2 Sustained Ultra DMA data in burst



NOTE – DD(15:0) and DSTROBE signals are shown at both the host and the device to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the host until some time after they are driven by the device.

Figure 22 – Sustained Ultra DMA data in burst

10.2.4.3 Host pausing an Ultra DMA data in burst



NOTE – The host may assert STOP to request termination of the Ultra DMA burst no sooner than t_{RP} after HDMARDY- is negated. The t_{SR} timing need not be met for an asynchronous pause.

Figure 23 – Host pausing an Ultra DMA data in burst

10.2.4.4 Device terminating an Ultra DMA data in burst

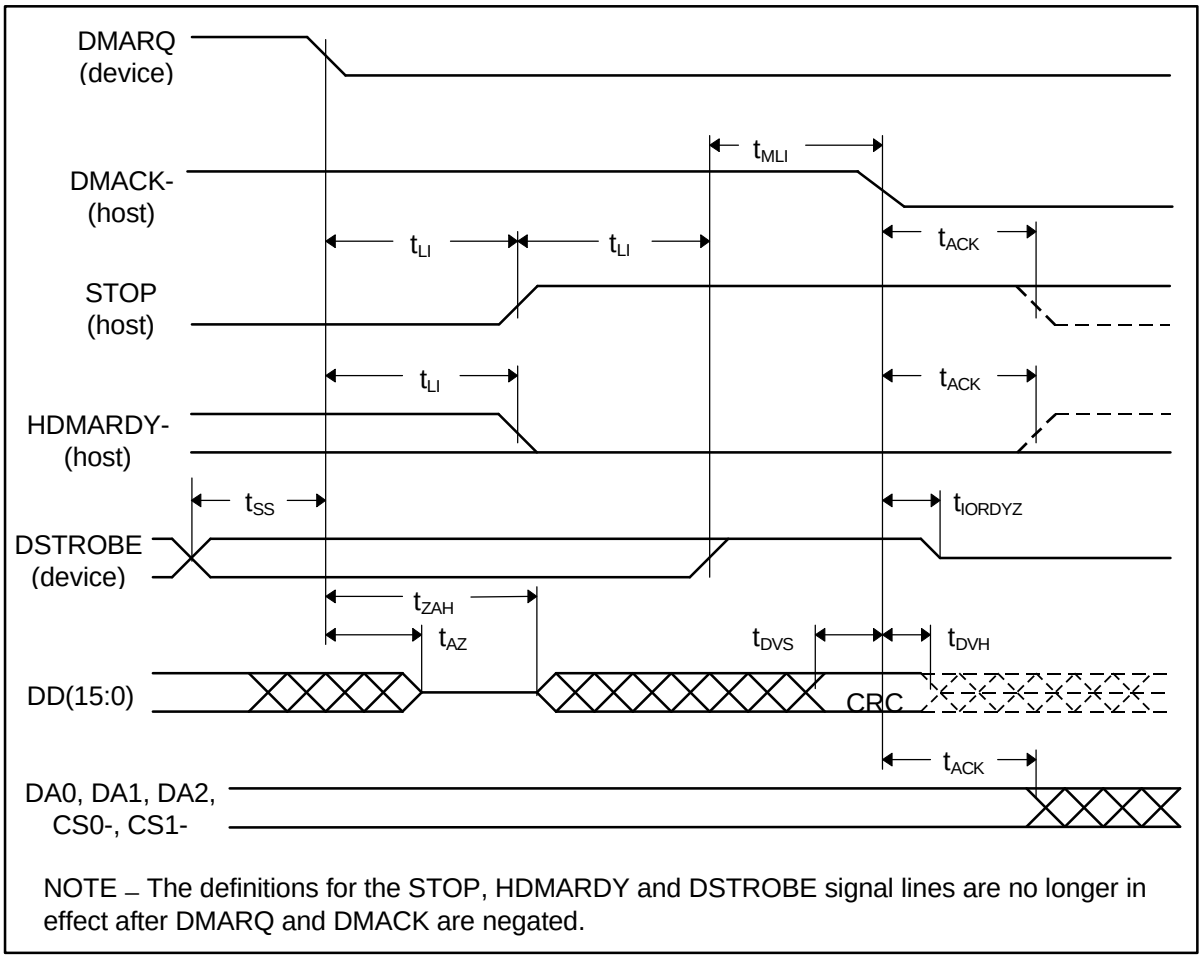
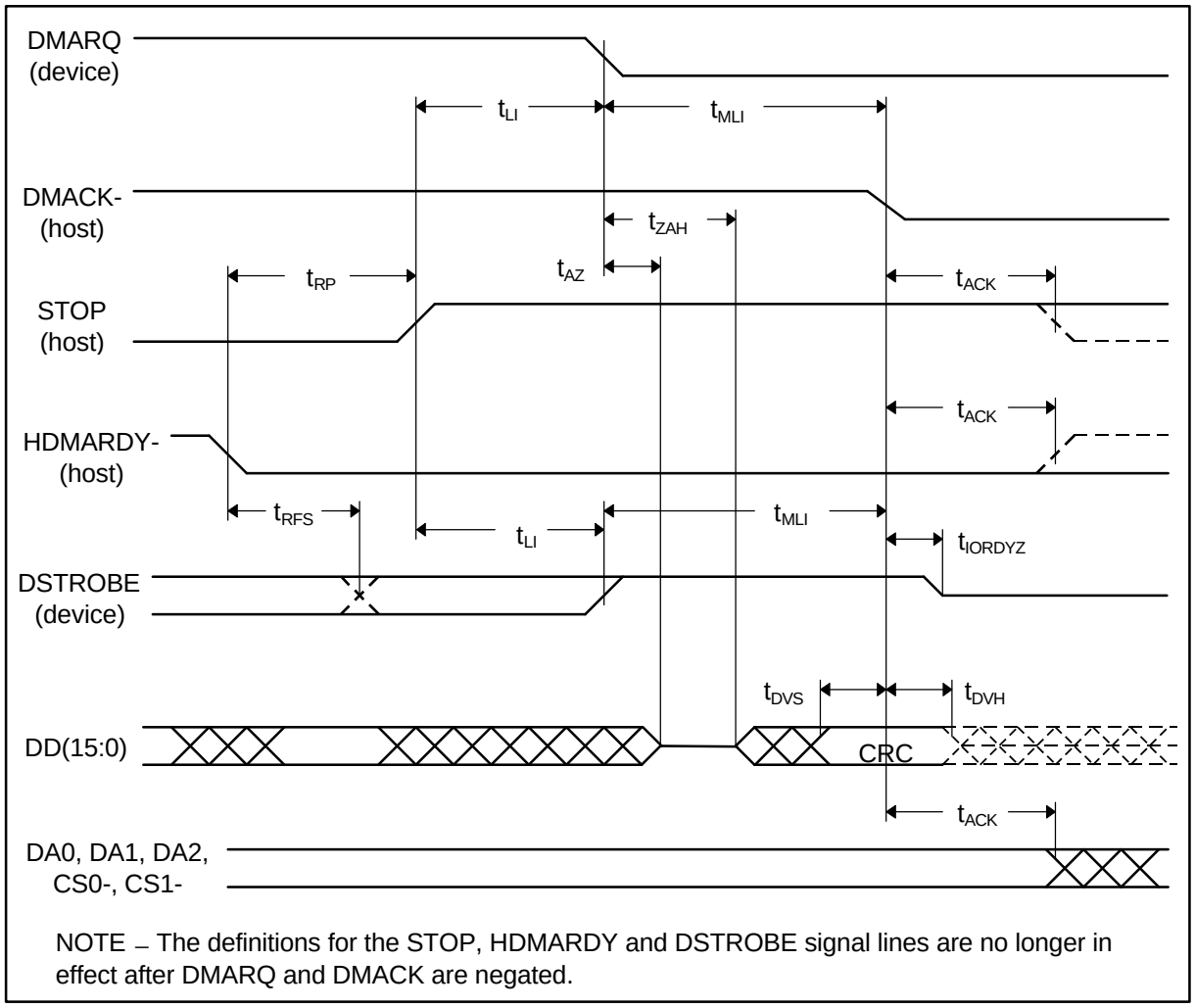


Figure 24 – Device terminating an Ultra DMA data in burst

10.2.4.5 Host terminating an Ultra DMA data in burst



NOTE – The definitions for the STOP, HDMARDY and DSTROBE signal lines are no longer in effect after DMARQ and DMACK are negated.

Figure 25 – Host terminating an Ultra DMA data in burst

10.2.4.6 Initiating an Ultra DMA data out burst

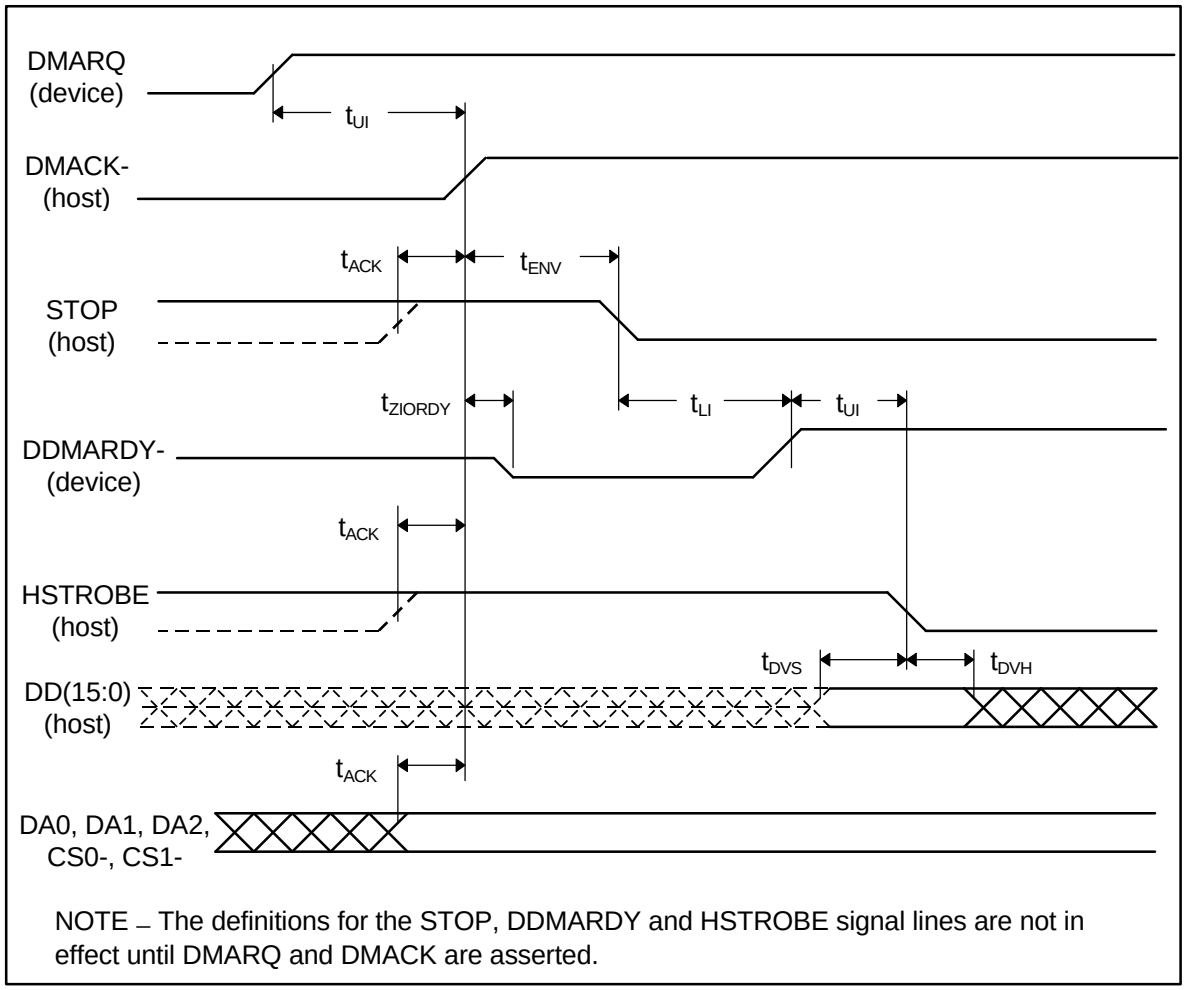
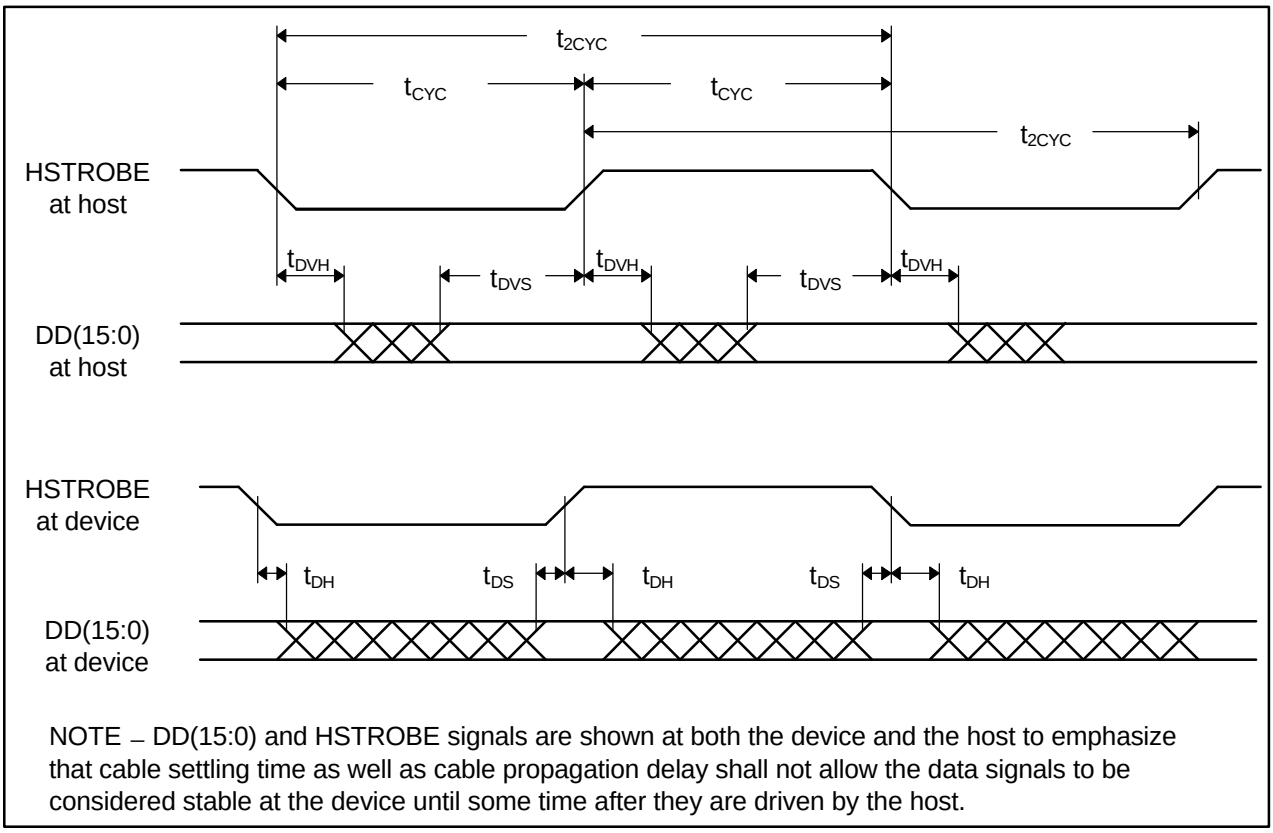


Figure 26 – Initiating an Ultra DMA data out burst

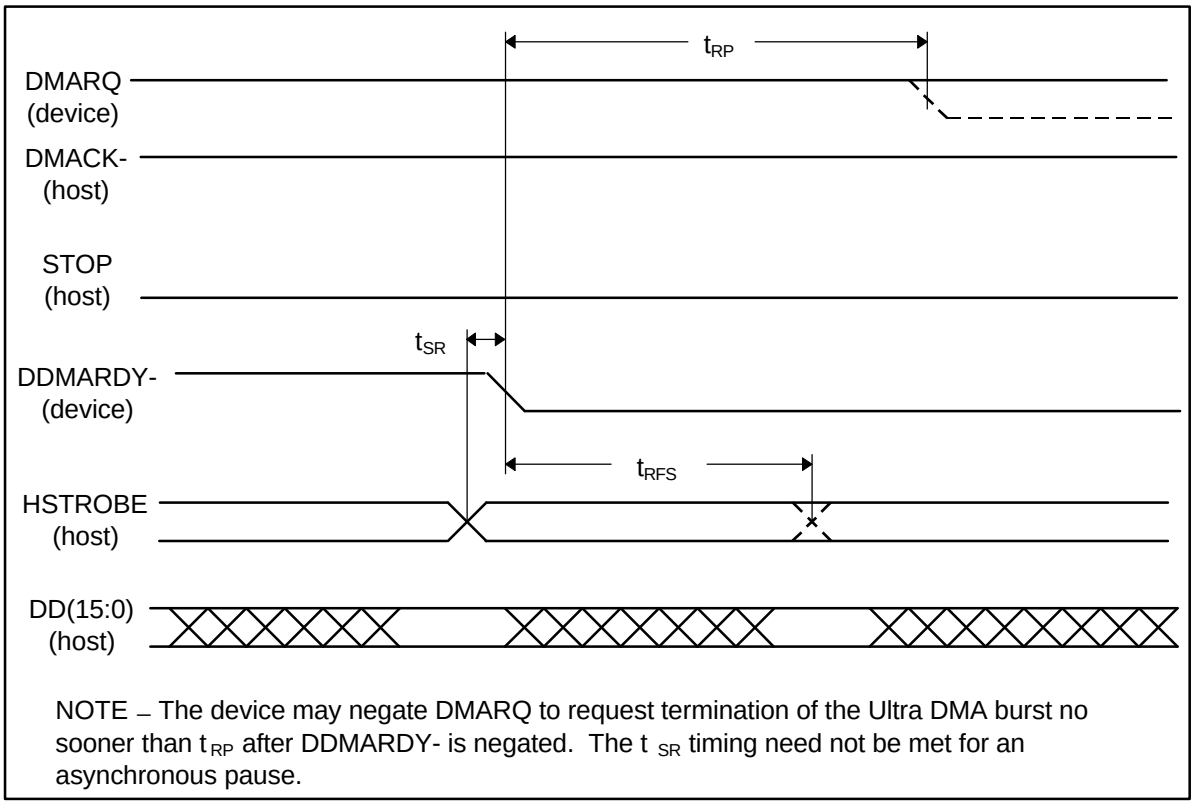
10.2.4.7 Sustained Ultra DMA data out burst



NOTE – DD(15:0) and HSTROBE signals are shown at both the device and the host to emphasize that cable settling time as well as cable propagation delay shall not allow the data signals to be considered stable at the device until some time after they are driven by the host.

Figure 27 – Sustained Ultra DMA data out burst

10.2.4.8 Device pausing an Ultra DMA data out burst



NOTE – The device may negate DMARQ to request termination of the Ultra DMA burst no sooner than t_{RP} after DDMARDY- is negated. The t_{SR} timing need not be met for an asynchronous pause.

Figure 28 – Device pausing an Ultra DMA data out burst

10.2.4.9 Host terminating an Ultra DMA data out burst

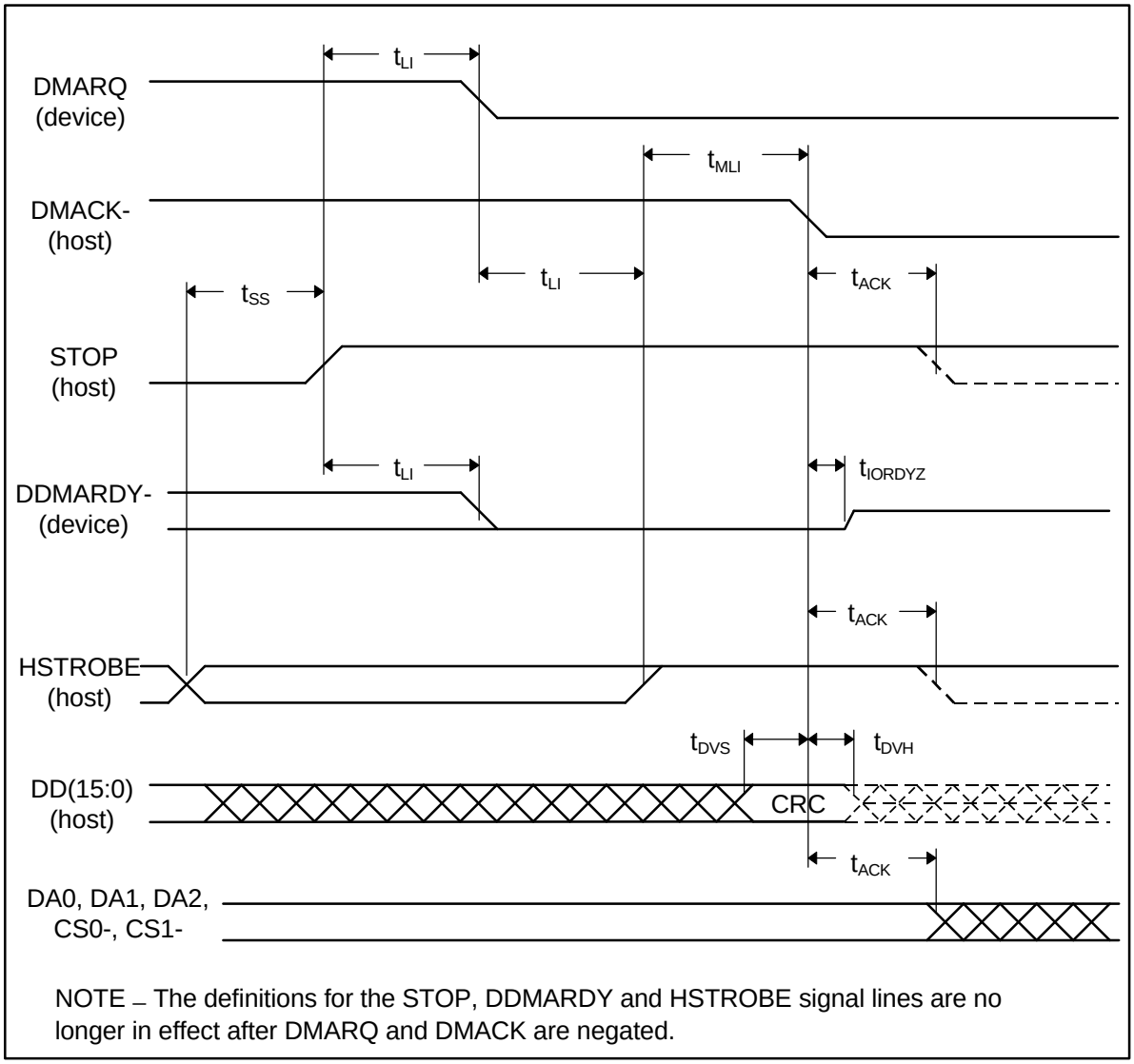


Figure 29 – Host terminating an Ultra DMA data out burst

10.2.4.10 Device terminating an Ultra DMA data out burst

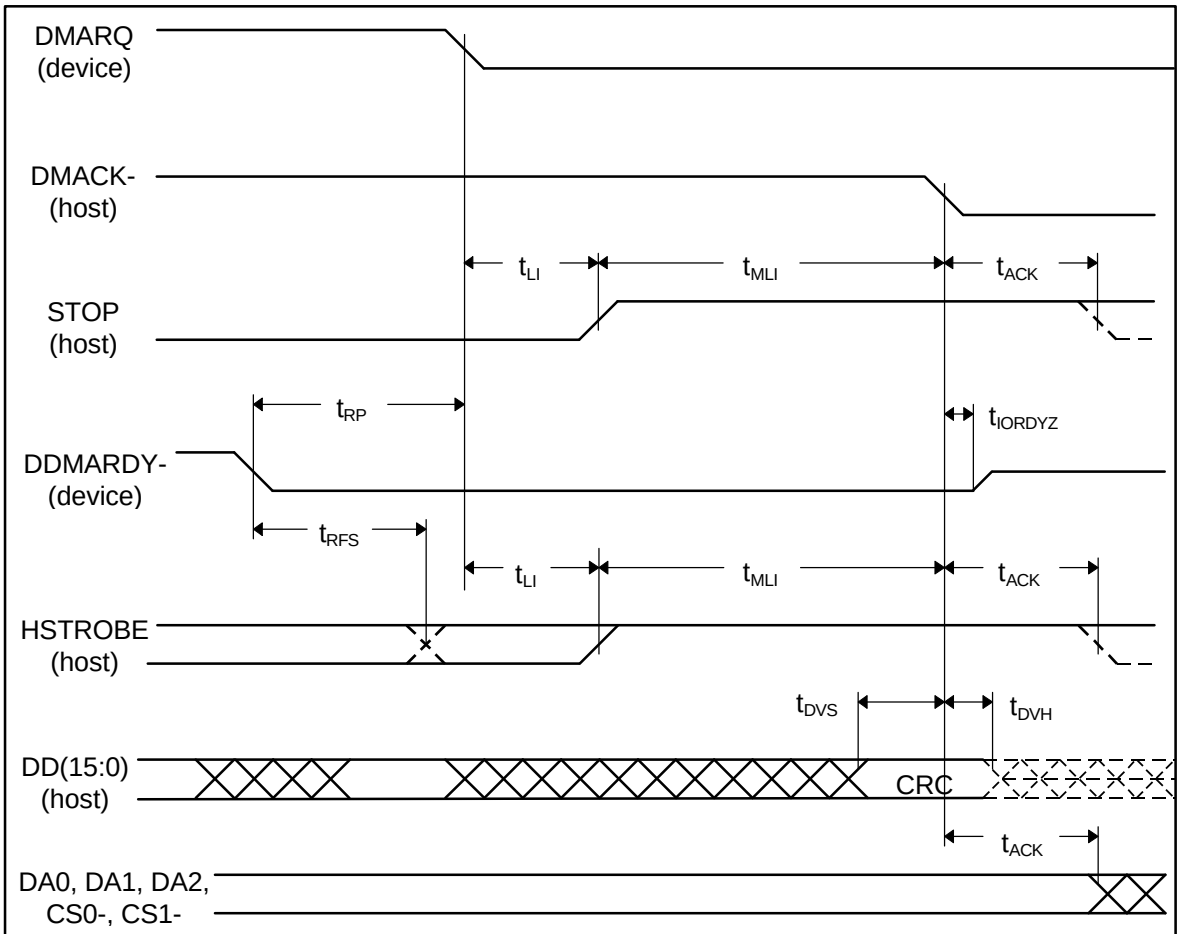


Figure 30 – Device terminating an Ultra DMA data out burst

10.2.4.11 Ultra DMA data burst timing requirements

Table 26 – Ultra DMA data burst timing requirements

NAME	MODE 0 (in ns)		MODE 1 (in ns)		MODE 2 (in ns)		COMMENT
	MIN	MAX	MIN	MAX	MIN	MAX	
t_{CYC}	114		75		55		Cycle time (from STROBE edge to STROBE edge)
$t2_{CYC}$	235		156		117		Two cycle time (from rising edge to next rising edge or from falling edge to next falling edge of STROBE)
t_{DS}	15		10		7		Data setup time (at recipient)
t_{DH}	5		5		5		Data hold time (at recipient)
t_{DVS}	70		48		34		Data valid setup time at sender (time from data bus being valid until STROBE edge)
t_{DVH}	6		6		6		Data valid hold time at sender (time from STROBE edge until data may go invalid)
t_{FS}	0	230	0	200	0	170	First STROBE (time for device to send first STROBE)
t_{LI}	0	150	0	150	0	150	Limited interlock time (time allowed between an action by one agent, either host or device, and the following action by the other agent)
t_{MLI}	20		20		20		Interlock time with minimum
t_{UI}	0		0		0		Unlimited interlock time
t_{AZ}		10		10		10	Maximum time allowed for outputs to release
t_{ZAH}	20		20		20		Minimum delay time required for output drivers turning on (from released state)
t_{ZAD}	0		0		0		
t_{ENV}	20	70	20	70	20	70	Envelope time (all control signal transitions are within the DMACK envelope by this much time)
t_{SR}		50		30		20	STROBE to DMARDY (response time to ensure the synchronous pause case when the recipient is pausing)
t_{RFS}		75		60		50	Ready-to-final-STROBE time (no more STROBE edges may be sent this long after receiving DMARDY- negation)
t_{RP}	160		125		100		Ready-to-pause time (time until a recipient may assume that the sender has paused after negation of DMARDY-)
t_{IORDYZ}		20		20		20	Pull-up time before allowing IORDY to be released
t_{ZIORDY}	0		0		0		Minimum time device shall wait before driving IORDY
t_{ACK}	20		20		20		Setup and hold times before assertion and negation of DMACK-
t_{SS}	50		50		50		Time from STROBE edge to STOP assertion when the sender is stopping

Notes:
1) The timing parameters t_{UI} and t_{LI} indicate device-to-host or host-to-device interlocks, that is, one agent (either host or device) is waiting for the other agent to respond with a signal on the bus before proceeding. t_{UI} is an unlimited interlock, or one which has no maximum time value. t_{LI} is a limited time-out, or one which has a defined maximum.
2) All timing parameters are measured at the connector of the device to which the parameter applies. For example, the sender shall stop generating STROBE edges t_{RFS} after the negation of DMARDY-. Both STROBE and DMARDY- timing measurements are taken at the connector of the sender.
3) All timing measurement switching points (low to high and high to low) are to be taken at 1.5V.

Annex A
(normative)
Connectors

A.1 40-pin connector

The I/O connector is a 40-pin connector as shown in figure A.1, with pin assignments as shown in table A.1. The connector shall be keyed to prevent the possibility of installing it upside down. A key is provided by the removal of pin 20. The corresponding pin on the cable connector shall be plugged.

The pin locations are governed by the cable plug, not the receptacle. The way in which the receptacle is mounted on the printed circuit board affects the pin positions, and pin 1 shall remain in the same relative position. This means the pin numbers of the receptacle may not reflect the conductor number of the plug. The header receptacle is not polarized, and all the signals are relative to pin 20, which is keyed.

By using the plug positions as primary, a straight cable connects devices. As shown in figure A.1, conductor 1 on pin 1 of the plug shall be in the same relative position no matter what the receptacle numbering looks like. If receptacle numbering was followed, the cable would have to twist 180 degrees between a device with top-mounted receptacles, and a device with bottom-mounted receptacles.

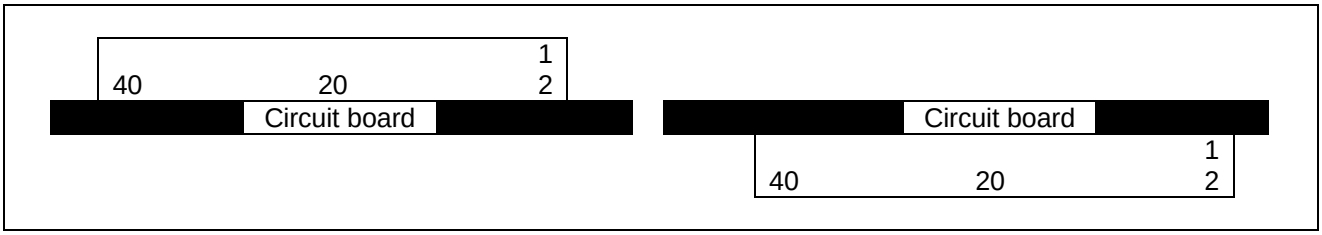


Figure A.1 – 40-pin connector mounting

Table A.1 – 40-pin connector interface signals

Signal name	Connector contact	Conductor		Connector contact	Signal name
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-:STOP	23	23	24	24	Ground
DIOR-:HDMARDY-:HSTROBE	25	25	26	26	Ground
IORDY:DDMARDY-:DSTROBE	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground

Recommended part numbers for the mating connector and cable are shown below, but equivalent parts may be used.

Connector (40 pin) : 3M 3417-7000 or equivalent
Strain relief : 3M 3448-2040 or equivalent

Flat cable (stranded 28 AWG) : 3M 3365-40 or equivalent
Flat cable (stranded 28 AWG) : 3M 3517-40 (shielded) or equivalent

A.1.1 4-pin power connector

When the device uses the 40-pin connector, the device receives DC power through a 4-pin connector. The pin assignments are shown in table A.2. Recommended part numbers for the mating connector to 18 AWG cable are shown below, but compatible parts may be used.

Connector (4 pin) : AMP 1-480424-0 or compatible
Contacts (loose piece) : AMP 60619-4 or compatible
Contacts (strip) : AMP 61117-4 or compatible

Table A.2 – DC interface using 4-pin power connector

Power line designation	Pin Number
+12 Volts	1
+12 Volt return	2
+5 Volt return	3
+5 Volts	4

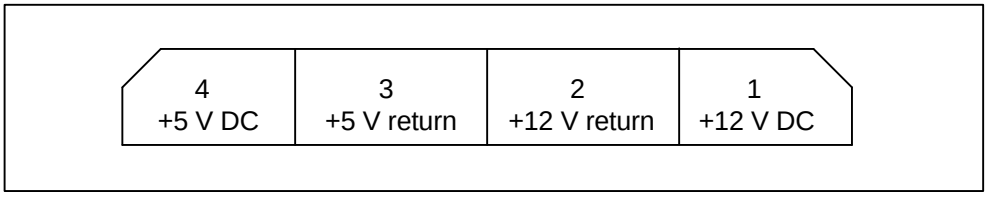


Figure A.2 – Drive side connector pin numbering

A.2 44-pin small form factor connector

This annex describes a connector alternative often used for 2 1/2 inch or smaller devices. This alternative was developed by the Small Form Factor (SFF) Committee, an industry ad hoc group.

In an effort to broaden the applications for small form factor devices, a group of companies representing system integrators, device suppliers, and component suppliers decided to address the issues involved.

A primary purpose of the SFF Committee was to define the external dimensions of small form factor devices so that products from different vendors could be used in the same mounting configurations.

The restricted area and the mating of devices directly to a motherboard required that the number of connectors be reduced, which caused the assignment of additional pins for power. Power is provided to the devices on the same connector as used for the signals, and addresses are set by the receptacle into which the devices are plugged.

The 50-pin connector that has been widely adopted across industry for SFF devices is a low density 2 mm connector which has no shroud on the plug which is mounted on the device. A number of suppliers provide intermatable components. The following information has been provided to assist users in specifying components used in an implementation.

Signals Connector Plug :	DuPont 86451 or equivalent
Signals Connector Receptacle :	DuPont 86455 or equivalent

A.2.1 44-pin signal assignments

The signals assigned for 44-pin applications are described in table A.3. Although there are 50 pins in the plug, a 44-pin mating receptacle may be used (the removal of pins E and F provides room for the wall of the receptacle).

Some devices may utilize pins A, B, C, and D for option selection via physical jumpers. Such implementations may require use of the 44-pin receptacle.

Pins A through D of the connector plug located on the device shall not to be connected to the host, as they are reserved for manufacturer's use. Pins E, F, and 20 are keys, and are removed (see figure A.3).

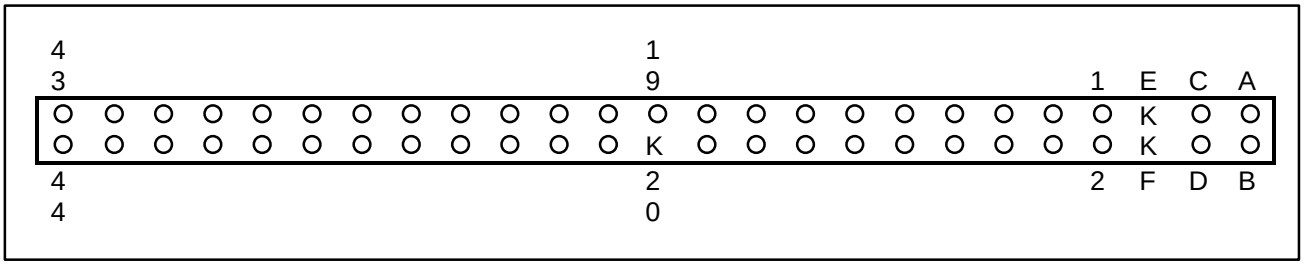


Figure A.3 – 44-pin connector

A.2.2 Use of pins A-D for device selection

If a device uses pins A, B, C, and D for device selection, it is recommended that when no jumper is present the device is designated as Device 0. It is recommended that when a jumper is present between pins B and D, the device is to respond to the CSEL signal to determine its device number.

Table A.3 – Signal assignments for 44-pin connector

Signal name	Connector contact	Conductor		Connector contact	Signal name
Vendor specific	A			B	Vendor specific
Vendor specific	C			D	Vendor specific
(keypin)	E			F	(keypin)
RESET-	1	1	2	2	Ground
DD7	3	3	4	4	DD8
DD6	5	5	6	6	DD9
DD5	7	7	8	8	DD10
DD4	9	9	10	10	DD11
DD3	11	11	12	12	DD12
DD2	13	13	14	14	DD13
DD1	15	15	16	16	DD14
DD0	17	17	18	18	DD15
Ground	19	19	20	20	(keypin)
DMARQ	21	21	22	22	Ground
DIOW-:STOP	23	23	24	24	Ground
DIOR-:HDMARDY-:HSTROBE	25	25	26	26	Ground
IORDY:DDMARDY-:DSTROBE	27	27	28	28	CSEL
DMACK-	29	29	30	30	Ground
INTRQ	31	31	32	32	reserved
DA1	33	33	34	34	PDIAG-
DA0	35	35	36	36	DA2
CS0-	37	37	38	38	CS1-
DASP-	39	39	40	40	Ground
+5 V (logic) (see note)	41	41	42	42	+5 V (Motor) (see note)
Ground(return) (see note)	43	43	44	44	TYPE- (0=ATA) (see note)
NOTE – Pins which are additional to those of the 40-pin cable.					

A.3 68-pin small form factor connector

This clause defines the pinouts used for the 68-pin alternative connector for the AT Attachment Interface. This connector is the same as the one defined by PCMCIA. This clause defines a pinout alternative that allows a device to function as an AT Attachment Interface compliant device, while also allowing the device to be compliant with PC Card ATA mode defined by PCMCIA. The signal protocol allows the device to identify the host interface as being 68-pin as defined in this standard or PC Card ATA.

To simplify the implementation of dual-interface devices, the 68-pin AT Attachment Interface maintains commonality with as many PC Card ATA signals as possible, while supporting full command and signal compliance with the this standard.

The 68-pin pinout shall not cause damage or loss of data if a PCMCIA card is accidentally plugged into a host slot supporting this interface. The inversion of the reset signal between this standard and PCMCIA interfaces prevents loss of data if the device is unable to reconfigure itself to the appropriate host interface.

A.3.1 Signals

This specification relies upon the electrical and mechanical characteristics of PCMCIA and unless otherwise noted, all signals and registers with the same names as PCMCIA signals and registers have the same meaning as defined in PCMCIA.

The PC Card-ATA specification is used as a reference to identify the signal protocol used to identify the host interface protocol.

A.3.2 Signal descriptions

Any signals not defined below shall be as described in this standard, PCMCIA, or the PC Card ATA documents.

Table A.4 shows the signals and relationships such as direction, as well as providing the signal name of the PCMCIA equivalent.

Table A.4Signal assignments for 68-pin connector

Pin	Signal	Hst	Dir	Dev	PCMCIA	Pin	Signal	Hst	Dir	Dev	PCMCIA
1	Ground	x	→	x	Ground	35	Ground	x	→	x	Ground
2	DD3	x	↔	x	D3	36	CD1-	x	←	x	CD1-
3	DD4	x	↔	x	D4	37	DD11	x	↔	x	D11
4	DD5	x	↔	x	D5	38	DD12	x	↔	x	D12
5	DD6	x	↔	x	D6	39	DD13	x	↔	x	D13
6	DD7	x	↔	x	D7	40	DD14	x	↔	x	D14
7	CS0-	x	→	x	CE1-	41	DD15	x	↔	x	D15
8			→	i	A10	42	CS1-	x	→	x(1)	CE2-
9	SELATA-	x	→	x	OE-	43			←	i	VS1-
10						44	DIOR-	x	→	x	IORD-
11	CS1-	x	→	x(1)	A9	45	DIOW-	x	→	x	IOWR-
12			→	i	A8	46					
13						47					
14						48					
15			→	i	WE-	49					
16	INTRQ	x	←	x	READY/ IREQ-	50					
17	Vcc	x	→	x	Vcc	51	Vcc	x	→	x	Vcc
18						52					
19						53					
20						54					
21						55	M/S-	x	→	x(2)	
22			→	i	A7	56	CSEL	x	→	x(2)	
23			→	i	A6	57			←	i	VS2-
24			→	i	A5	58	RESET-	x	→	x	RESET
25			→	i	A4	59	IORDY	o	←	x(3)	WAIT-
26			→	i	A3	60	DMARQ	o	←	x(3)	INPACK-
27	DA2	x	→	x	A2	61	DMACK-	o	→	o	REG-
28	DA1	x	→	x	A1	62	DASP-	x	↔	x	BVD2/ SPKR-
29	DA0	x	→	x	A0	63	PDIAG-	x	↔	x	BVD1/ STSCHG
30	DD0	x	↔	x	D0	64	DD8	x	↔	x	D8
31	DD1	x	↔	x	D1	65	DD9	x	↔	x	D9
32	DD2	x	↔	x	D2	66	DD10	x	↔	x	D10
33		x	←	x	WP/ IOIS16	67	CD2-	x	←	x	CD2-
34	Ground	x	→	x	Ground	68	Ground	x	→	x	Ground

Key:
Dir = the direction of the signal between host and device.
x in the Hst column = this signal shall be supported by the Host.
x in the Dev column = this signal shall be supported by the device.
i in the Dev column = this signal shall be ignored by the device while in 68-pin mode as defined in this standard.
o = this signal is Optional.
Nothing in Dev column = no connection should be made to that pin.

NOTES –
1 The device shall support only one CS1- signal pin.
2 The device shall support either M/S- or CSEL but not both.

3 The device shall hold this signal negated if it does not support the function.

A.3.2.1 CD1- (Card Detect 1)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

A.3.2.2 CD2- (Card Detect 2)

This signal shall be grounded by the device. CD1- and CD2- are used by the host to detect the presence of the device.

A.3.2.3 CS1- (Device chip select 1)

Hosts shall provide CS1- on both the pins identified in table A.4.

Devices shall recognize only one of the two pins as CS1-.

A.3.2.4 DMACK- (DMA acknowledge)

This signal is optional for hosts and devices.

If this signal is supported by the host or the device, the function of DMARQ shall also be supported.

A.3.2.5 DMARQ (DMA request)

This signal is optional for hosts.

If this signal is supported by the host or the device, the function of DMACK- shall also be supported.

A.3.2.6 IORDY (I/O channel ready)

This signal is optional for hosts.

A.3.2.7 M/S- (Master/slave)

This signal is the inverted form of CSEL. Hosts shall support both M/S- and CSEL though devices need only support one or the other.

Hosts shall assert CSEL and M/S- prior to applying VCC to the connector.

A.3.2.8 SELATA- (Select 68-pin ATA)

This pin is used by the host to select which mode to use, PC Card-ATA mode or the 68-pin mode defined in this standard. To select 68-pin ATA mode, the host shall assert SELATA- prior to applying power to the connector, and shall hold SELATA- asserted.

The device shall not re-sample SELATA- as a result of either a Hard or Soft Reset. The device shall ignore all interface signals for 19 ms after the host supplies Vcc within the device's voltage tolerance. If SELATA- is negated following this time, the device shall either configure itself for PC Card-ATA mode or not respond to further inputs from the host.

A.3.3 Removability considerations

This specification supports the removability of devices which use the protocol. As removability is a new consideration for devices, several issues need to be considered with regard to the insertion or removal of devices.

A.3.3.1 Device recommendations

The following are recommendations to device implementors:

- CS0-, CS1-, RESET- and SELATA- signals be negated on the device to prevent false selection during hot insertion.

- Ignore all interface signals except SELATA- until 19 ms after the host supplies VCC within the device's voltage tolerance. This time is necessary to de-bounce the device's power on reset sequence. Once in the 68-pin mode as defined in this standard, if SELATA- is ever negated following the 19 ms de-bounce delay time, the device disables itself until VCC is removed.

- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register are used to prevent unexpected removal of the device or media.

A.3.3.2 Host recommendations

The following are recommendations to host implementors:

- Connector pin sequencing to protect the device by making contact to ground before any other signal in the system.

- SELATA- to be asserted at all times.

- All devices reset and reconfigured to the same base address each time a device at that address is inserted or removed.

- The removal or insertion of a device at the same address to be detected so as to prevent the corruption of a command.

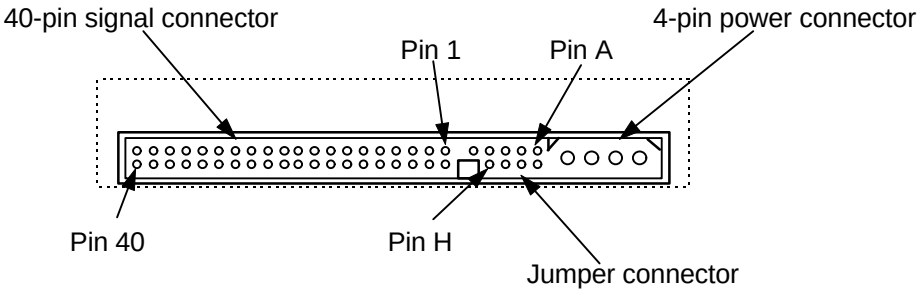
- The DOOR LOCK and DOOR UNLOCK commands and the MC and MCR bits in the Error register used to prevent unexpected removal of the device or media.

A.4 Unitized connectors

The Small Form Factor committee has defined two unitzed connectors for use on ATA/ATAPI devices of 3.5” and larger form factor. Each of these connectors consists of a signal portion that complies with the 40-pin signal definition of A.1 and a 4-pin power portion that complies with the definition in A.1.1. In addition, each has a jumper connector portion.

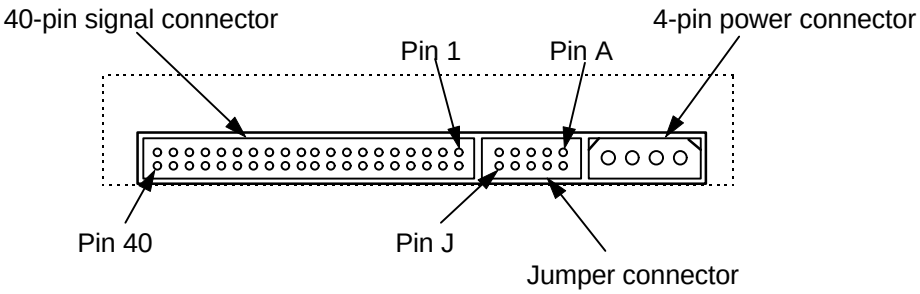
Figure A.4 shows the unitized connector defined by SFF8xxx and defines the usage of the jumper connector pins.

Figure A.5 shows the unitized connector defined by SFF8yyy and defines the usage of the jumper connector pins.



Jumpers: E-F - CSEL
No jumper - Slave
G-H - Master
G-H and E-F - Master w/Slave present
Use of pins A through D is vendor specific
Pin I is reserved

Figure A.4 – SFF 8xxx connector



Jumpers: A-B - CSEL
C-D - Slave
E-F - Master
Use of pins G through J is vendor specific

Figure A.5 – SFF 8yyy connector

Annex B
(informative)
Identify device data for devices below 8 GB

B.1 Definitions and background information

The following abbreviations are used in this annex:

- 528 MB is used to describe a device that has 1,032,192 sectors or 528,482,304 bytes.
- 8 GB is used to describe a device that has 16,515,072 sectors or 8,455,716,864 bytes.

The original IBM PC BIOS (Basic Input/Output System) imposed several restrictions on the support of devices, and these have been incorporated into many higher level software products. One such restriction limits the capacity of a device. Most BIOS software cannot support a device with more than 1,024 cylinders, 16 heads and 63 sectors per track. The maximum addressable capacity of a device under this scheme is 528 MB.

There is growing support of auto-configuration for devices on PC systems. The auto-configuration capability usually resides in the BIOS and uses the IDENTIFY DEVICE command data to configure a device.

This annex defines rules for the IDENTIFY DEVICE data of all capacity devices and allows BIOS support of devices up to 8 GB using Cylinder/Head/Sector (CHS) addressing.

This specification defines information that newer BIOSs and system software may use to determine the true size of a device and access the full capacity of the device.

B.2 Cylinder, head, and sector addressing

BIOSs and other software that operate a device in CHS (Cylinder, Head and Sector) addressing mode use IDENTIFY DEVICE data words 1, 3, 6, and words 53-58 to ascertain the appropriate translation mode to use and determine the capacity of a device.

Maximum compatibility is achieved if the following rules are obeyed. These rules limit the values placed into words 1, 3, 6, and 53-58. The rules specified here for CHS addressing apply to devices up to 8 GB.

B.2.1 Word 1

For devices less than or equal to 528 MB, IDENTIFY DEVICE data word 1 (Default Cylinders) does not specify a value greater than 1,024.

If a device is greater than 528 MB but less than or equal to 8 GB, the maximum value that is placed into this word is determined by the value in Word 3 as shown in table B.1.

The value in this word does not change.

NOTE – This algorithm reserves a gap at cylinder address 16,384 to support the legacy of a maintenance cylinder.

Table B.1 – Word 1 value

Value in Word 3	Maximum value in Word 1
1 1h	65,535 FFFFh
2 2h	65,535 FFFFh
3 3h	65,535 FFFFh
4 4h	65,535 FFFFh
5 5h	32,767 7FFFh
6 6h	32,767 7FFFh
7 7h	32,767 7FFFh
8 8h	32,767 7FFFh
9 9h	16,383 3FFFh
10 Ah	16,383 3FFFh
11 Bh	16,383 3FFFh
12 Ch	16,383 3FFFh
13 Dh	16,383 3FFFh
14 Eh	16,383 3FFFh
15 Fh	16,383 3FFFh
16 10h	16,383 3FFFh

B.2.2 Word 3

IDENTIFY DEVICE data word 3 (Default Heads) does not specify a value greater than 16.

The value in this word does not change.

B.2.3 Word 6

For devices of 8 GB or less, IDENTIFY DEVICE data word 6 (Default Sectors) does not specify a value greater than 63.

The value in this word does not change.

B.2.4 Use of words 53 through 58

Devices that are over 528 MB implement words 53-58. Devices not over 528 MB may also implement these words. These words define the addressing for all sectors accessible in CHS mode.

B.2.5 Word 53

IDENTIFY DEVICE data word 53 bit 0 is set to one at all times that the device is in a valid translation mode. Some devices may have translation modes that cannot be supported. An attempt to put a device into one of these unsupported modes causes word 53 bit 0 to be cleared to zero with words 54-58 cleared to zero until a valid translation mode is established.

B.2.6 Word 54

IDENTIFY DEVICE data word 54 (Current Cylinders) specifies the number of full logical cylinders that may be accessed in the current translation mode. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word is the same as word 1. If an INITIALIZE DEVICE PARAMETERS command has been executed, this word is the integer result of dividing the total number of user sectors (this value may be in words 60-61) by the number of sectors per logical cylinder ([word55] x [word56]), but is not a value greater than 65,535.

B.2.7 Word 55

IDENTIFY DEVICE data word 55 (Current Heads) is the number of heads specified by the last INITIALIZE DEVICE PARAMETERS command. This word contains a value of between 1 and 16. If an INITIALIZE

DEVICE PARAMETERS command has not been executed, the contents of this word are the same as word 3.

B.2.8 Word 56

IDENTIFY DEVICE data word 56 (Current Sectors) is the number of sectors specified by the last INITIALIZE DEVICE PARAMETERS command. This word may contain a value of between 1 and 255. If an INITIALIZE DEVICE PARAMETERS command has not been executed, the contents of this word are the same as word 6.

B.2.9 Words 57-58

IDENTIFY DEVICE data words 57-58 contain a 32-bit value that is equal to [word54] x [word55] x [word56]. Words 57-58 are less than or equal to the value in words 60-61 at all times.

B.3 Orphan sectors

The sectors, if any, between the last sector addressable in CHS mode and the last sector addressable in LBA mode are known as "orphan" sectors. A device may or may not allow access to these sectors in CHS addressing mode.

The values in words 1, 3, and 6 are selected such that the number of orphan sectors is minimized. Normally, the number of orphan sectors should not exceed ([word55] x [word56] - 1). However, the host system may create conditions where there are a larger number of orphans sectors by issuing the INITIALIZE DEVICE PARAMETERS command with values other than the values in words 3 and 6.

Annex C
(informative)
Signal integrity

C.1 Introduction

The bus (a.k.a. IDE bus) is a disk drive interface originally designed for the ISA Bus of the IBM PC/AT™. With the advent of faster disk drives the definition of the bus has been expanded to include new operating modes. Each of the PIO modes, numbered zero through four, is faster than the one before it (higher numbers translate to faster transfer rates). Modes 0, 1, and 2 correspond to the interface as originally defined. PIO Mode 3 defines a maximum transfer rate of 11.1 MB/s and PIO Mode 4 defines a maximum rate of 16.7 MB/s. Additional DMA modes have also been defined, with Multiword DMA Mode 0 corresponding to the original interface, and DMA Modes 1 and 2 being faster transfer rates. Multiword DMA Mode 2 is the same speed as the new PIO Mode 4.

With this increased speed the weaknesses of the original cabling scheme has become apparent on desktop systems. System manufacturers, chipset designers, and disk drive manufacturers must all take measures to insure that signal integrity is maintained on the bus. The areas of concern are:

a) ringing due to improper termination;
b) crosstalk between signals;
c) bus timing.

The intended audience for this annex is digital and analog engineers who design circuits interfacing to the bus. Familiarity with the specification and a basic understanding of circuit theory is assumed.

C.1.1 The problems

Early implementations of the bus used LS-TTL parts to drive an 18-inch cable. The slow edges of LS-TTL and the short cable length worked well at the time. PIO Modes 3 and 4 demand higher performance. In an effort to cut cycle times, edge rates have inadvertently been increased, causing ringing on the cable and increased crosstalk between adjacent signals.

When a host adapter was little more than a few buffers and some gates there was no issue with host adapter timing. With the advent of local bus architectures and faster transfer rates, timing issues have become more important. Propagation delay with worst-case loads must now be taken into account when designing host adapters.

One of the frequently asked questions is why are problems with ringing on the bus seen now when they were not seen before. The answer is in the edge speed of the logic. How the edge speed changed may be found by looking at the history of the IBM PC.

When the IBM PC/AT™ was introduced in 1983, the 8 MHz 80286 processor quickly became the dominant platform. The AT bus (now called the ISA bus) became standardized around an 8 MHz processor speed. When the first disk drive was introduced a few years later, it was designed as a simple extension of the bus – hence the name “AT Attachment” interface (see figure C.1). The idea was to remove the disk drive controller electronics from the PC and place them on the drive instead. What remained on the PC was a pair of bidirectional data buffers and an address decoder. This simple interface was most often implemented with a pair of 74LS245 buffers and a programmable logic device such as a PAL. These TTL devices had rise and fall times in the 5 to 6 ns range. Although this was fast enough to cause some ringing on the bus, it was not so severe as to prevent millions of successful system implementations.

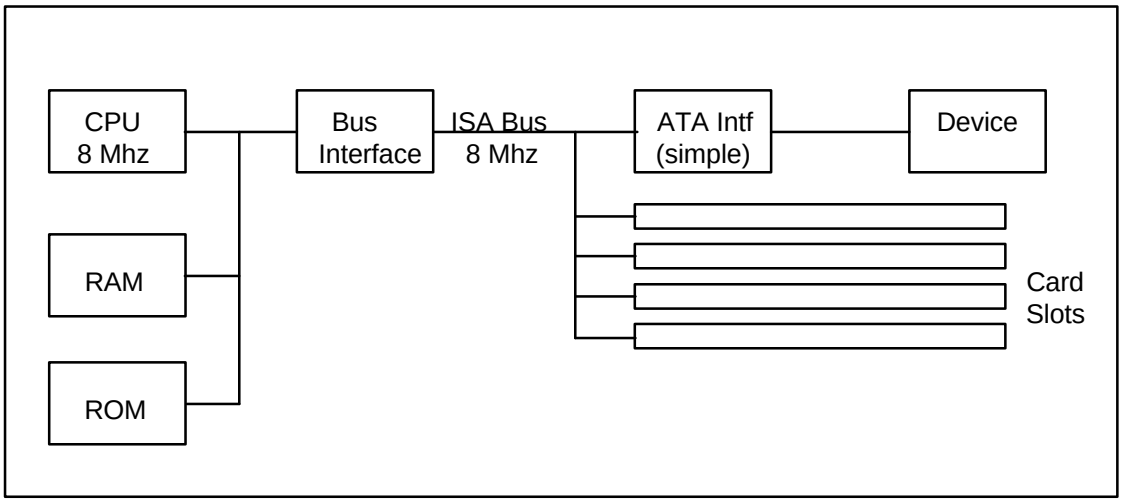


Figure C.1 – Original IBM PC/AT architecture

The architecture of modern PCs has changed somewhat from the original PC/AT™. As the processor speed increased it became necessary to separate the processor bus from the ISA bus (see figure C.2). To maintain compatibility the ISA bus continues to run at an 8 MHz rate. Processors, and their associated busses, have increased from 8 MHz to 12, 16, 25, and now 33 Mhz.

NOTE – Processors that run faster than 33 MHz, such as the 486DX2-66, still tend to keep the external processor bus at 33 MHz.

Disk drives have also increased in speed. The increase in rotational speed and linear bit density has increased the rate at which data comes off the heads, and the presence of cache on the drive makes data available at the access rates of RAM. This has created a data bottleneck at the ISA bus. The drive is faster, the processor is faster, but the data can't be moved from one to the other any faster.

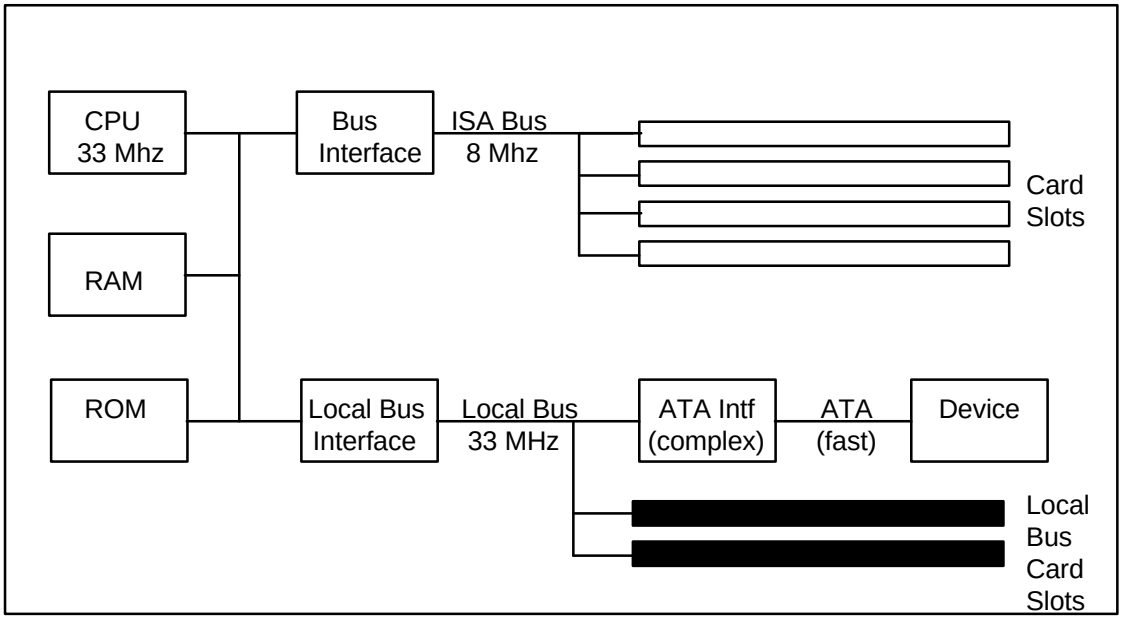


Figure C.2 – Modern PC architecture

This bottleneck inspired the invention of new, faster interfaces to the processor. Local busses are designed to run at the speed of the processor bus. Two local bus standards have emerged, the VESA Local Bus (VLB) and the Peripheral Component Interconnect bus (PCI). These local busses have the potential for faster data transfer from the disk drive to the processor.

To allow disk drives to transfer data faster, the standard had to be updated to allow faster transfer rates. These enhanced modes are still not as fast as a processor bus. To synchronize the data flow between 32-bit 33 MHz processor busses and slower 16-bit disk drives, a VLSI chip is required. Most of these bridge chips were implemented with fast CMOS processes to achieve the required bus speeds. As a result the edge rates on the bus were often 1 to 2 ns, and sometimes less. These fast edges have aggravated the ringing on the bus to the point that system/drive combinations fail to work.

In summary, the reason for signal integrity problems appearing now, when they were absent before, is the advent of faster transfer rates on the bus coupled with a change of IC process at the interface. The problems are not insurmountable, and in time it is likely that the bus will be known as a robust, fast, and inexpensive interface.

C.1.2 The goals

The recommendations in this document make the following assumptions. The word “device” is used generically to describe disk drives and other peripheral devices on the bus.

- Backward compatibility must be maintained. Old devices must work with new host adapters, and old host adapters must work with new devices.
- The ATA-2 standard must be followed as closely as possible. Without this, solutions implemented by different manufacturers will tend to diverge, creating incompatible systems.
- Solutions must be simple and inexpensive. The market for products is very cost sensitive.

C.2 Termination

When analyzing the bus, the standard 18-inch ribbon cable used to connect devices could be considered to be either a transmission line or a lumped LC circuit. Analog circuit designers generally use the rule of thumb that if the edge rate is less than four times the cable propagation delay, then it is a transmission line. Otherwise it is considered to be a lumped LC.

> NOTE – Different ratios are used by different designers. A survey of textbooks shows that values of three times, four times, six times, and even sqrt(2*pi) have been suggested.

The cable used almost exclusively is a PVC-coated 40-conductor ribbon cable with 0.05 inch spacing. This cable is modeled as a transmission line with a typical characteristic impedance of 110 ohms and propagation velocity of 60% c. This gives a propagation delay of 2.5 ns. The edge rates from both hosts and devices are usually faster than 10 ns (4 x 2.5 ns), so a transmission line model applies.

> NOTE – Measurements taken on a sample cable gave an impedance of 107 ohms and a delay of 2.6 ns (59% c propagation velocity).

C.2.1 The problem

Many users have experienced problems with early implementations of PIO Mode 3 devices and hosts. Most failures in the systems observed are attributed to signal integrity problems on the control lines that go from the host to the device. The problem appears most frequently as ringing on the DIOR- (read command) and DIOW- (write command) lines.

During a read cycle when DIOR- is asserted, it is possible for the ringing to create a short duration deassertion pulse (see figure C.3). This pulse occurs early in the read cycle. Inside the interface portion of the datapath controller chip is a FIFO buffer that contains the data to be read. The extra pulse on the DIOR- line advances the FIFO pointer by one. This results in losing one word of data. The host system read operation therefore receives one word too few, and the remaining bytes are shifted. A typical data sequence might look like . . .W7, W8, W9, W11, W12 . . . Notice that word 10 is missing from the returned data. This also means that the host tries to read one more word from the device than the device has remaining. Depending on the implementation of the BIOS, this locks-up the system or simply returns a byte of garbage at the end of the sector.

Pulse slivers due to ringing on the DIOW- line cause a similar problem during writes. The pulse sliver advances the FIFO pointer by one unexpectedly, writing an extra word of garbage into the FIFO. Subsequent data bytes are shifted by one word. A typical stored data sequence on the device might look like . . . W7, W8, W9, XX, W10, W11 . . . In this example an extra word was inserted during the write cycle for word 10. From the device's point of view, the host is trying to write 514 bytes rather than the expected 512 bytes. The device throws away the final word and should flag an error. A properly written BIOS detects this error and indicates a problem to the user.

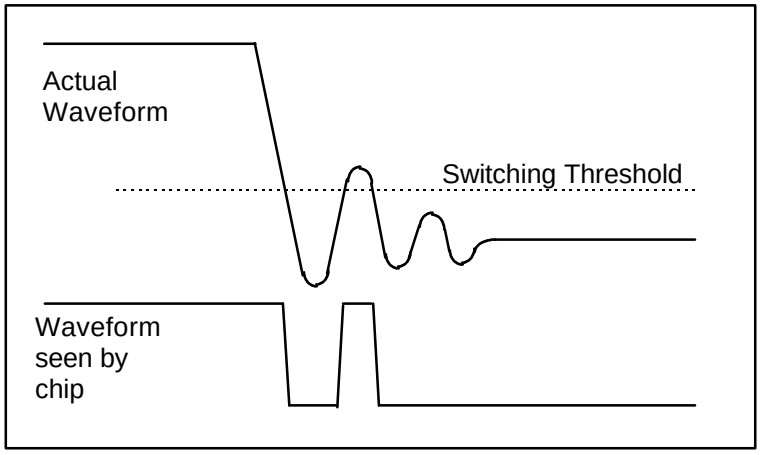


Figure C.3 – Typical ringing on bus and its effect

These are only two examples of a systemic problem. Ringing on any control signal, and possibly on data lines, may cause system failures or data loss. To address this problem it is necessary to examine the circuit structure of the bus.

Figure C.4 shows the seven basic driver/receiver structures that appear in bus interfaces. The host circuitry appears on the left side of the diagram and the device circuitry appears on the right. The first circuit in figure C.4 shows the structure of the seven control lines that go from the host to the device. A SPICE model of the circuit is designed if some assumptions are made about the circuitry at the host and device. Virtually all devices today use a CMOS VLSI chip as part of the bus interface. This high-impedance input is modeled with clamp diodes to supply and ground and a typical input capacitance of 8 pF, see figure C.4. Since the ringing problem is worse with CMOS VLSI bridge chips at the source the host is modeled as a voltage source with 1 ns edges, a 12 ohm output impedance, and clamp diodes to supply and ground. The ribbon cable is modeled as a 110 ohm transmission line. The resulting SPICE model appears in figure C.5.

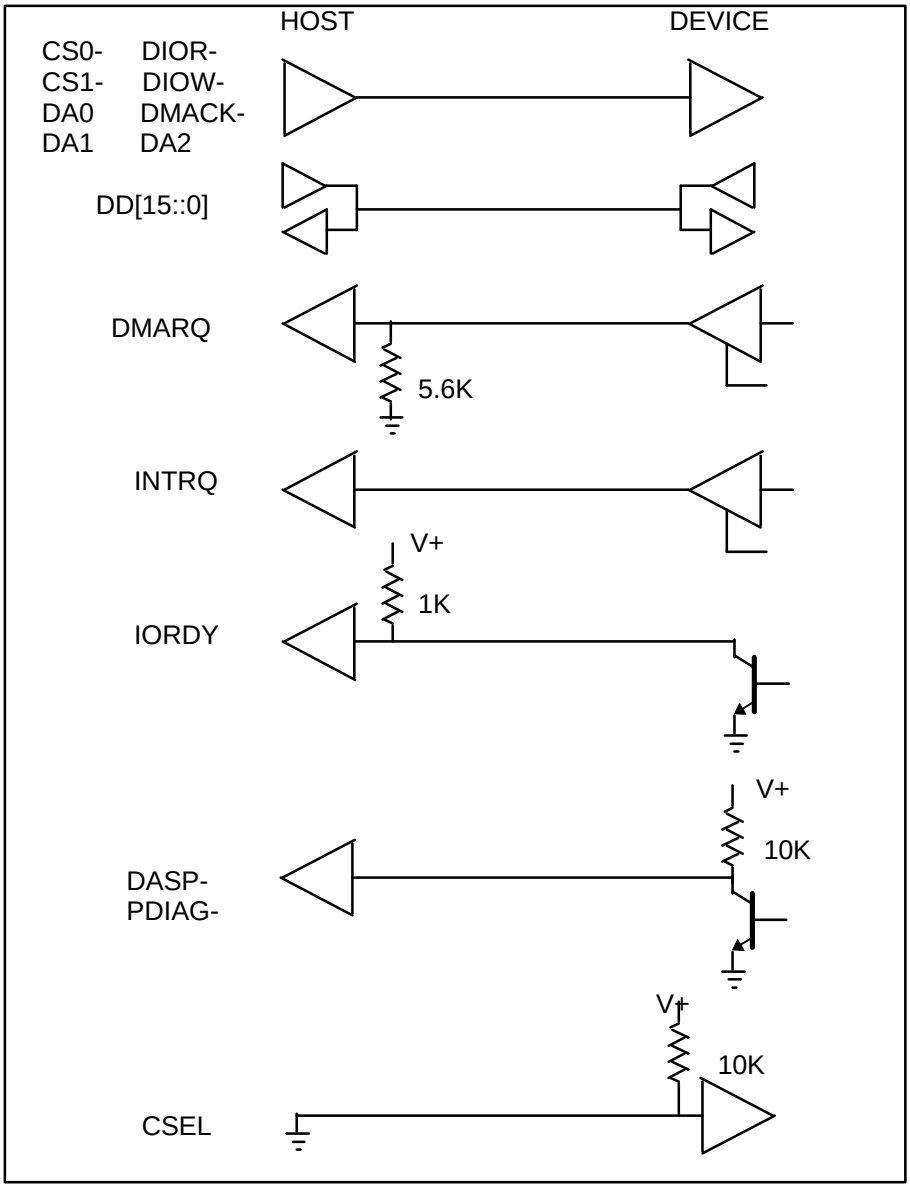


Figure C.4 – The seven basic driver/receiver structures

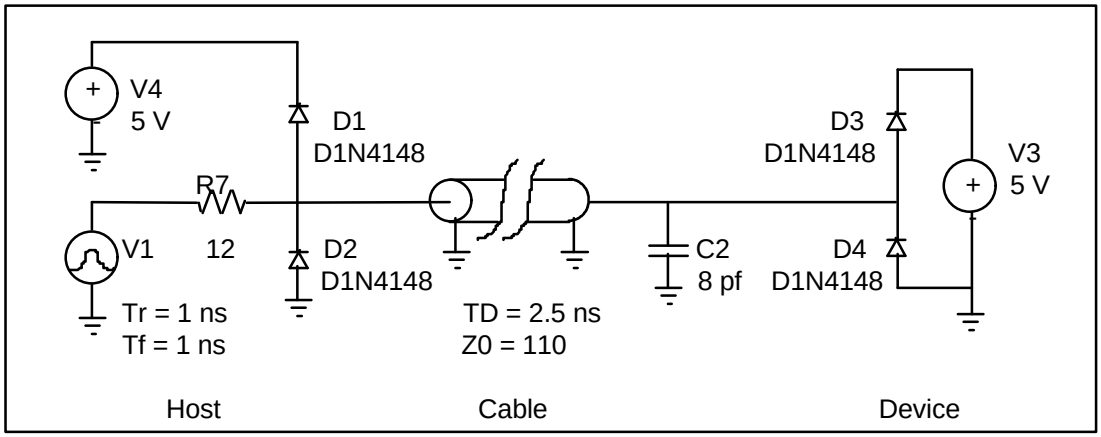


Figure C.5 – Schematic of SPICE simulation model

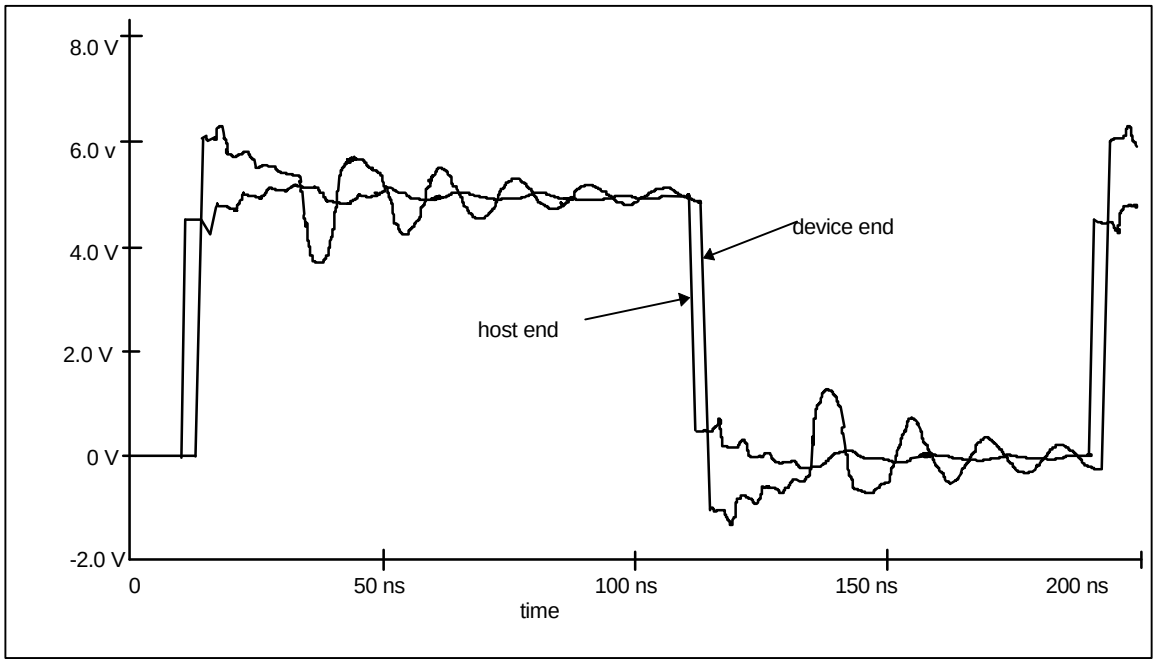


Figure C.6 – Simulation waveforms at host and device ends of cable

The simulation results in figure C.6 show the waveforms at both the host and device ends of the cable. The signal at the device end has ringing of sufficient amplitude to cause false triggering of the device. This is confirmed by transmission line theory which indicates that ringing will occur whenever the source impedance is lower than the characteristic impedance of the cable, and the termination is of higher impedance than the cable. The greater the mismatch, the greater the amplitude of the ringing. The oscilloscope trace shown in figure C.7 confirms the results of the simulations.

The latest trend in interface chips has aggravated the ringing problem. In an effort to decrease propagation delay, some bridge chip manufacturers have increased the output drive current of the host in order to slew the output signal faster with the capacitive load of the cable. This has caused the edge rates and the output impedance to decrease, both of which increase the ringing at the device end of the cable. The oscilloscope trace in figure C.7 uses a generic driver and receiver – the problem of ringing is a fundamental characteristic of the interface. This has not always been the case.

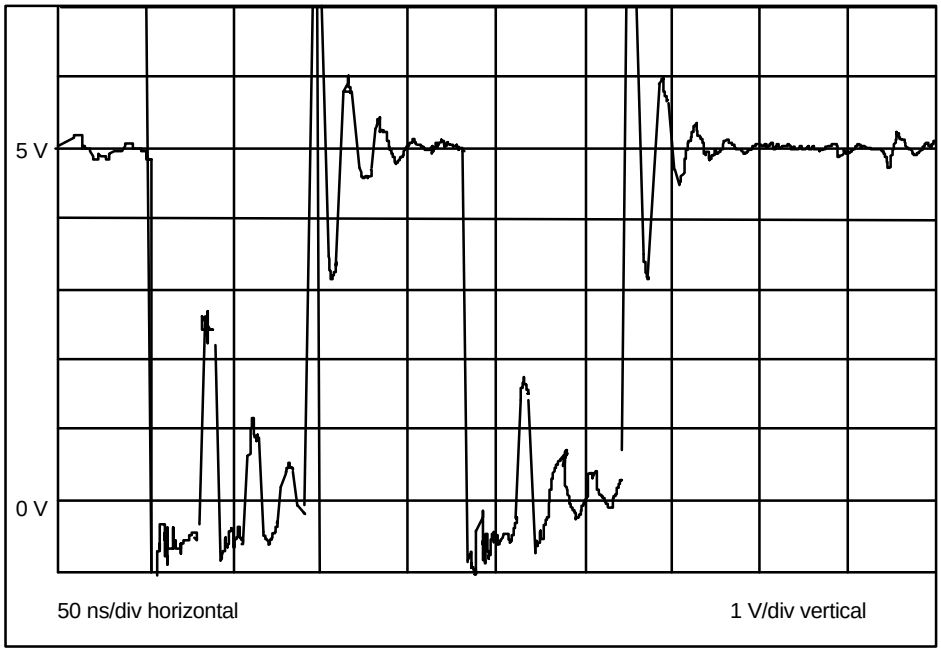


Figure C.7 – Oscilloscope trace at device end of DIOR- signal on a typical system

C.2.2 What are the options?

The proper solution is to terminate the transmission line. Either a series termination at the source or a parallel termination at the device is acceptable. Unfortunately, each of these solutions has problems of its own. A 110 ohm termination at the device end causes excessive DC loading. Having a termination on both devices in a two-device configuration results in too low of a load impedance, causing reflections on the cable again.

Matching the source impedance of the host to the cable has similar problems. The impedance required is different when the host is in the middle of the cable as opposed to being at the end. Even with the host at one end of the cable, ringing may occur with a two device configuration. This is because the input impedance of the devices is not infinite: they appear as a reactive load due to their input stray capacitance.

The SCSI interface standard avoids ringing by requiring terminations at each end of the physical cable and having each device drive the cable with a current sink. However, real SCSI configurations often have too many, too few, or improperly located terminations. Changing the standard to a user-installed termination scheme loses all backward compatibility and is therefore not considered to be a viable option.

One of the solutions used in the past to “fix” failing configurations has been to place a capacitor at the input of the device. Since the ringing is the result of a resonant system, adding purely reactive elements (capacitors and inductors) which simply change the frequency of oscillation is not recommended. These elements may fix a given configuration of a device and cable, but they really just move the interfering resonance peaks to a different frequency, solving the problem only for that particular configuration. Proper solutions include resistive elements to dissipate the energy stored in the transmission line.

No single solution meets the dual criteria of solving the ringing problem and being backward compatible with current systems. The suggested approach uses partial solutions in three different areas: partial termination at the host, partial termination at the device, and edge rate control at both the host and the device.

C.2.3 Design goals

Before a solution can be designed the design goals must be explicitly stated. This leads to the question of “How much ringing is acceptable?” To answer this question the design and specification of the bus is considered.

The bus was originally designed to use standard TTL signals. TTL was designed with built-in noise margin. All drivers are required to have a “low” (zero) signal level of 0.5 V or less, and a “high” (one) signal level of 2.4 V or more. All receivers are specified to accept any signal below 0.8 V as a logical zero and any signal above 2.0 V as a logical one. This results in a low-side noise margin of 0.3 V (0.8 - 0.5) and a high-side margin of 0.4 V (2.4 - 2.0). Signals between 0.5 V and 2.0 V are in no man’s land, interpreted by the receiver as either a zero or a one. TTL compatible inputs typically use a switching threshold of 1.3 to 1.4 V.

Bus designers have long known that the noise margins of TTL are insufficient for signals passed on cables. To improve the noise margin inherent in TTL systems, hysteresis has been added to the receiver input. Hysteresis changes the input switching threshold depending on the present state of the logic output of the receiver. For example, if the receiver is currently in a zero state, it might require an input voltage of 1.7 V before changing to a one. Once in a one state, the receiver might require the input voltage to drop below 0.9 V before changing back to a zero. Modern design practice dictates that all signals passing across a bus be received with hysteresis.

It is desirable that, even with ringing, the input signal remain less than 0.5 V after a falling edge and remain above 2.4 V after a rising edge. With CMOS drivers only the falling edge is of concern. This is due to the input switching threshold of TTL (typically 1.4 V) being closer to ground than to the supply. It turns out that designing to the 0.5 V requirement is too restrictive, so the looser requirement of 0.8 V is used here. This relaxed requirement essentially removes the noise margin inherent in TTL and depends on receiver hysteresis for proper operation. As input hysteresis has been the norm in drive design for many years now, this limitation is not considered unreasonable.

Depending on system timing and other issues, a designer may elect to use a looser threshold of 0.9 V or a tighter one of 0.7 V. For these cases circuit simulation of the bus and receiver is done to verify the design. The resulting termination circuits have different values from those derived here.

C.2.4 Source termination

A series resistor at the source (host) acts as a termination to the transmission line. When the value of the resistor matches the characteristic impedance of the cable (110 ohms) then the ringing is reduced to zero. Resistor values less than 110 ohms will partially terminate the cable and reduce the ringing.

> NOTE – This assumes that the output impedance of the driver is zero. In reality, an optimum match occurs when the output impedance and the series resistor together equal the cable impedance.

The specification requires that a source sink 4 mA while maintaining a logical low output voltage of 0.5 V or less (see 4.3). Adding a series resistor in the output of the driver causes the output logical zero voltage to increase with greater resistance. For example, if the unterminated logical zero output of the driver is 0.4 V, then a maximum series resistance of 25 ohms is allowed ((0.5-0.4)/4 mA). This DC voltage drop requirement acts in opposition to the higher resistance values required for cable termination. A 5%, 22 ohm resistor meets the 25 ohm requirement. Note that this places an addition requirement on the host interface chip: timing measurements use a logical threshold of 0.4 V rather than 0.5 V as in the past.

Is a 22 ohm resistor adequate for reducing the ringing? The simulation was repeated using the same model as shown in figure C.5 with a 22 ohm series resistor added. The results of that simulation appear in figure C.8. The ringing is significantly reduced from the previous simulation in figure C.6.

For maximum ringing it is assumed that the device(s) have CMOS input stages that do not provide significant DC loading. Yet for the series termination resistor calculation it is assumed a logical low sink current of 4 mA. Both of these conditions cannot simultaneously occur in practice, but assuming the worst-case sink current gives the best compatibility with older devices.

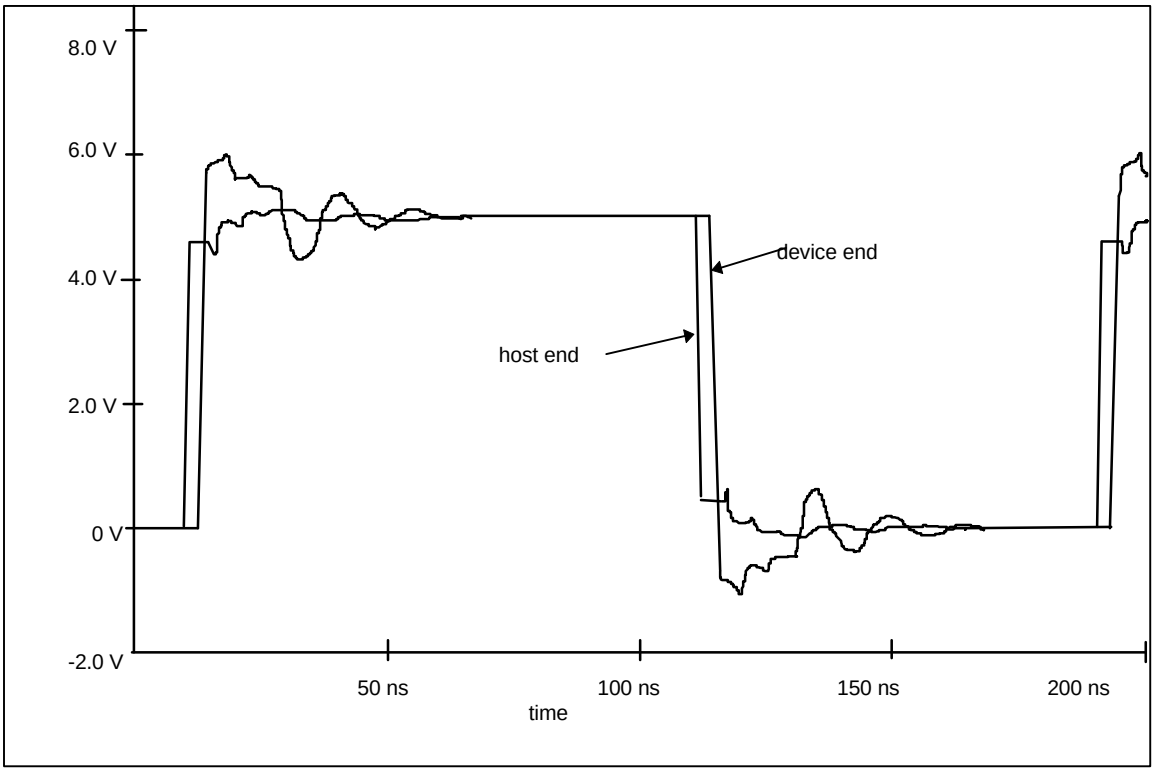


Figure C.8 – Waveforms with 22 ohm series resistor at source

C.2.5 Receiver termination

Receiver termination is more difficult than source termination. Viable solutions must work with one or two drives located anywhere along the cable. The host may be located at one end or in the middle of the cable. The host may or may not have termination. These and other considerations make drive termination a multifaceted problem.

The first constraint is the maximum DC loading allowed. The specification requires that the host be capable of providing 400 µA of current while in a logical one state. Assuming each device is allowed to take half of that amount, the minimum DC resistance allowed is 25K ohms.

> NOTE – This assumes a CMOS output with a high output voltage of 5.0 V : 5.0 V/200 µA = 25 KΩ

For a 110 ohm transmission line, 25K ohms is as good as infinity. This means that any practical termination solution must not have significant DC loading.

One way of terminating the cable is with an “AC termination.” This is a simple RC network that provides termination for high-frequency signals but does not load the line at DC (see figure C.9). This circuit acts as both a cable termination and a filter for the ringing. The termination characteristics can be observed by looking at the ringing signal at the host when the circuit is connected or removed. When the circuit is in place, less energy is reflected back to the host, so the host waveform has less ringing. The lowpass filter characteristics of the circuit help decrease the amount of ringing presented to the interface circuitry of the device.

Although this may appear to be an unusual method of terminating the cable, it is not without precedent. The IEEE P996 committee recognized the problems inherent in the design of the IBM PC/AT™ bus and recommended a series RC termination for increased “data integrity and system reliability.” They suggested that the termination circuit be added to each end of the backplane or motherboard. The recommended values are 40 to 60 ohms for the resistor and 30 to 70 pF for the capacitor.

Deriving the optimum values for a bus AC termination circuit is difficult. The easiest way of determining the values is to perform a number of trial-and-error SPICE simulations for different host and device configurations. The recommended values are 82 ohms and 10 pF. Simulations show that capacitance values between 8 pF and 20 pF work well. Since the input capacitance of many interface chips is between 8 and 10 pF, a discrete capacitor is often unnecessary. This reduces the cost of implementation on the device. A conservative approach is to place pads so additional capacitance can be added if required.

Device manufacturers need to ensure that any partial termination circuits they implement present an effective capacitance of 20 pF or less. What is an effective capacitance? From a practical point of view, any circuit is valid provided it does not increase the propagation delay of a worst-case cable. This is because systems manufacturers are counting on a certain cable delay in their design. The easiest way to answer the question of acceptability is to run a SPICE simulation and measure the delay. The simulation should be run twice: once with a simple 20 pF load, and again with the proposed termination circuit. If the resulting delay of the proposed termination circuit is less than or equal to that obtained with a 20 pF load, then it meets the criterion for acceptance. The recommended termination of 82 ohms and 10 pF passes the test.

The major drawback of the RC termination circuit is that it adds delay to the signal. Since the specification defines the timing at the input to the device (see clause 10), device manufacturers must ensure that their interface chip still works properly with the additional delay. The delay can be calculated for rising edges (2.0 V threshold) and falling edges (0.8 V threshold) with a fairly straightforward SPICE simulation. For the 82 ohm and 10 pF termination the delay is less than 1.5 ns.

NOTE – 0.7 ns for the rising edge, 1.2 ns for the falling edge, derived from simulations.

Will termination at both the host and the device “over-terminate” the transmission line? Figure C.10 shows the simulation results for device termination with no host termination, and figure C.11 shows the same simulation with a 22 ohm host termination added. It is clear that termination at both the host and the device results in the best signal integrity. To completely confirm the validity of the termination circuits more simulations must be performed with source termination and two devices with receiver termination; two devices, one with and one without termination; etc.

Another option for controlling ringing at the device is the use of a clamping circuit. Biased diodes have been shown to be excellent solutions, reducing the ringing to virtually zero. The advantage of clamp circuits is that they do not require any components in series with the signal, and therefore do not add any delay. This is particularly important for PIO Mode 4 operation. The disadvantage of clamping circuits is that they take considerably more space on the circuit board and cost much more than passive elements. Some implementations have used clamping circuits on sensitive edge-triggered lines (such as DIOR- and DIOW-) and used passive terminations on less sensitive lines (such as data). Clamping circuits work well both with and without host-end termination and are worthy of further investigation.

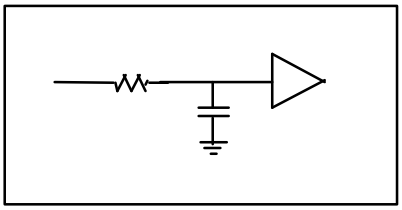


Figure C.9 – AC termination circuit at device end of cable

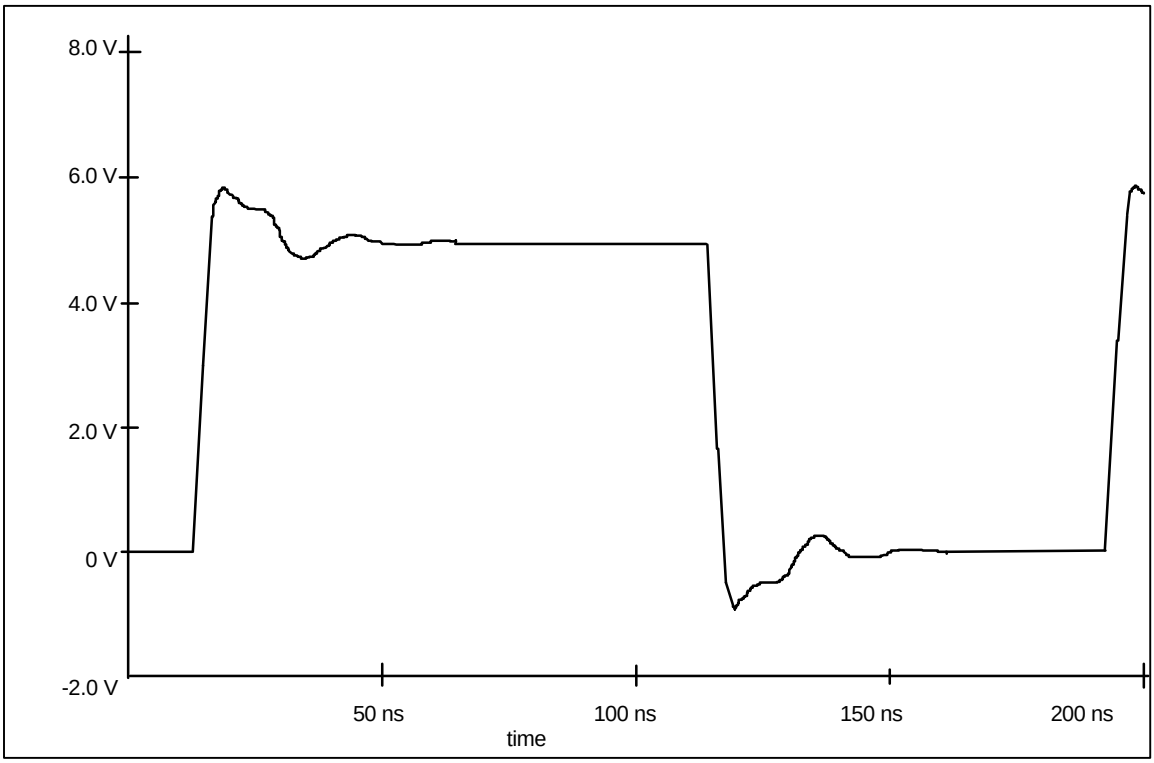


Figure C.10 – Device waveform with device termination and no host termination

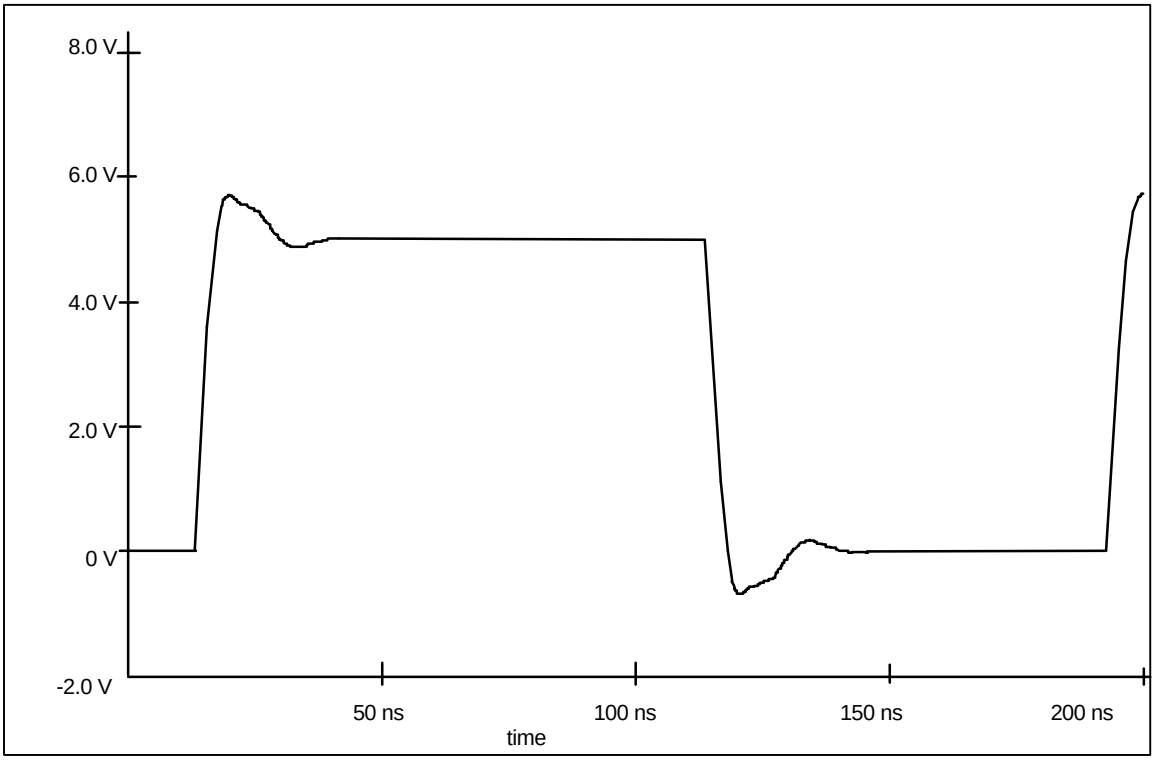


Figure C.11 – Device waveform with both device and host terminations

C.2.6 Edge rate control

The specification requires that all sources have a rise time of not less than 5 ns (see 4.3). The original intent of this requirement was to avoid transmission line problems on the bus. One of the common misconceptions is that limiting the rise time of the source to 5 ns will fix the ringing problem.

A rule-of-thumb for analog designers is that when the propagation delay of the cable exceeds one-quarter of the signal rise time, cable termination be used.

> NOTE – In reality this rule-of-thumb varies considerably. Various books use values of one-half, one-third, one-fifth, and even one over the square root of two times pi.

In the case of the bus, the worst case propagation delay of the cable is approximately 4 ns so by this rule rise times of less than 16 ns require termination. Many local bus to bridge chips available today have rise times of 1 to 2 ns, in violation of the requirement of 5 ns.

> NOTE – Assuming 18-inch cable, 60% c velocity factor; two drives, each drive having a maximum load of 25 pF.

The document says that the rise time must be a minimum of 5 ns into a 40 pF load. The easiest way to implement this from a chip designer's point of view is to decrease the drive of the I/O cell until the timing requirement is met. Unfortunately, very few systems in the real world ever approach 40 pF. Although the cable and the devices have maximum capacitance specifications, these capacitance values are never seen by the host. At DC and low frequencies the cable looks like a capacitor. But at high frequencies (or fast edge rates) the cable appears as a transmission line.

One of the results from transmission line theory is that a properly terminated transmission line appears to be a resistor with no capacitance or inductance. From the driving end of the line the transmission line looks just like a resistor whose value is the characteristic impedance of the line. The distributed capacitance of the transmission line does not appear as a capacitive load: it interacts with the inductance of the line and the termination to appear resistive. As a result, real-world systems rarely see more than 30 pF of capacitive loading at the host. The reduced capacitance causes the I/O cell to slew faster, creating rise times less than 5 ns.

The best solution is to use special I/O cells that have slew rate feedback to keep the rise time at 5 ns regardless of load. These are more difficult to design than conventional I/O cells and consume more die area. This could be a problem for interface chip designs that are already pad ring limited. Another approach is to use a conventional I/O cell that is designed to have 5 ns rise times into a 10 pF or 20 pF load. The total delay of the cell is greater for heavier loads, but the maximum delay is determined with SPICE modeling of a worst-case cable and load.

Rise time control is still an important tool for controlling ringing. Although it is not the total solution, simulations show marked improvement between sources with 1 ns rise times and sources with 5 ns rise times. Slower rise times give the added benefit of reduced crosstalk.

C.2.7 The solution: A combination

No one element – source termination, receiver termination, nor rise time control – completely addresses the problem of ringing on the bus. The recommended solution is a combination of all three. Each item must be enough to exert some control over the ringing problem in order to maintain backward compatibility. With the

faster transfer rates of PIO Mode 4 (and DMA Mode 2) it is even more important to control undesired ringing on the bus.

The above discussion only addressed a particular group of signals driven by the host and received by the device. There are other signals driven by the device and received by the host that are equally susceptible to ringing. These signals need termination, but in the opposite manner. The device inserts 22 ohm resistors in series with signals it drives and the host has an RC (or just R) receiving end termination.

The data lines are different in that they are data bidirectional. Strictly speaking, the data lines are not edge sensitive and are unaffected by ringing. This is true as long as the data signals have sufficient setup time to allow for bus settling. The settling time is as long as 60 ns in severe cases. Excessive ringing on the data lines induces spurious signals on adjacent control lines (crosstalk). Good design dictates that some type of ringing control be used on data lines, but perhaps not as much as on edge-sensitive control lines. A good compromise is to insert 22 ohm series resistors on data lines at both the host and the device. The driving end sees the same source termination as before. The receiving end sees an RC network of 22 ohms combined with the input capacitance of the interface chip. This is enough to substantially reduce the ringing and minimize settling time.

The one remaining bus structure not discussed is the open collector output driven by the device (IORDY). This signal is driven by a current source rather than a voltage source. Usually the transistor driving this signal is relatively slow and does not cause an excessive amount of ringing. The nature of IORDY makes it relatively insensitive to ringing that might occur.

Table C.1 summarizes the recommended changes to the signal lines on the bus:

Table C.1 – Recommended termination

Signal Name	Host Termination	Device Termination
DIOR-, DIOW-	22 ohm series	82 ohm series
CS0-, CS1-	22 ohm series	82 ohm series
DA0, DA1, DA2	22 ohm series	82 ohm series
DMACK-	22 ohm series	82 ohm series
RESET-	no change	no change
DD0 through DD15	22 ohm series	22 ohm series
DMARQ	82 ohm series	22 ohm series
INTRQ	82 ohm series	22 ohm series
IORDY	no change	no change
DASP-, PDIAG-	no change	no change
CSEL	no change	no change
NOTE – For the 82 ohm series termination, an additional parallel capacitor may be needed if the interface chip and circuit board layout have less than 8 pF of capacitance.		

C.2.7.1 Example of device-end termination timing

Assume that 82 ohm series resistors are inserted on all receive signals and 22 ohm series resistors on all transmit and bidirectional signals. Also assume that the input capacitance of the interface chip is 10 pF. There are three different RC configurations that occur (see figure C.12). All receive signals will see an 82 ohm and 10 pF network. The data lines will see a 22 ohm and 10 pF network when the device is receiving data. Signals driven back to the host (including data lines during a read) will see 22 ohms and 50 pF. The 50 pF assumption is the worst-case condition of both the host and another device being located nearby (negligible cable length), and both of them having the maximum allowed input capacitance.

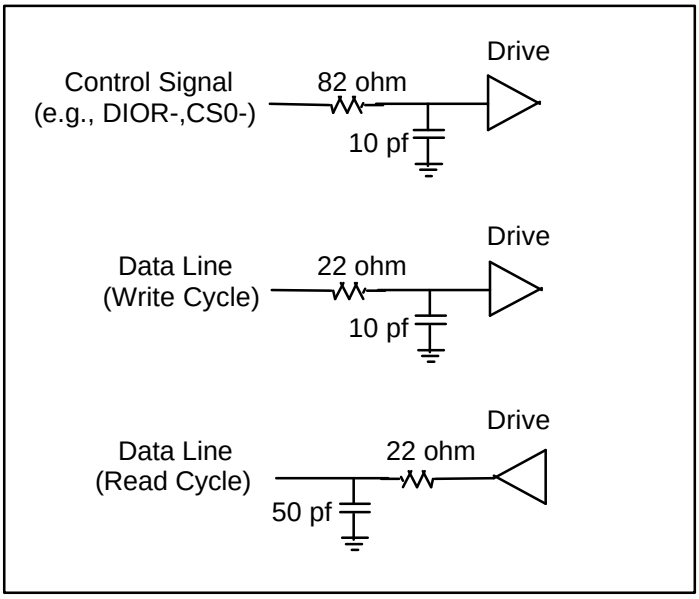


Figure C.12 – Signal models for device-end timing calculations

A simple SPICE simulation with a signal source and an RC load will show what the delays are through these three networks. Because the switching thresholds are not symmetrical with respect to the supply (0.8 V and 2.0 V) the delay for rising edges is different than that for falling edges. Since the input edge rate is unknown, both fast and slow edge inputs are simulated. The worst-case delay occurs with slow edges for rise times and fast edges for fall times. This mixture of slow rise time and fast fall time does not occur in real life, but since the edge speed is not known the worst case is planned for. The SPICE signal source is programmed for a rise time of 6.25 ns (same as 5 ns for 10% to 90%) and a fall time of 0.1 ns. The net result is six delay values. The results of the SPICE simulations are shown in table C.2.

Table C.2 – Typical device-end propagation delay times

Symbol	Description	Value
Tphlc	Propagation delay, high to low, control line	1.0 ns
Tplhc	Propagation delay, low to high, control line	0.9 ns
Tphldi	Propagation delay, high to low, data in	0.5 ns
Tplhdi	Propagation delay, low to high, data in	0.3 ns
Tphldo	Propagation delay, high to low, data out	2.5 ns
Tplhdo	Propagation delay, low to high, data out	1.1 ns

These delay values, combined with the interface chip timing specifications, will give the timing at the pins of the device. The trick is to figure out how each one of the timing parameters is affected by the delays.

For example, consider the DIOW- Data Setup time (value t3). This is the amount of time that the data must be stable before the rising edge of DIOW-. Assume that the interface chip has a value of 2.0 ns. It is known that DIOW- is a control signal and the rising edge of control signals are delayed by 0.9 ns. This means that the setup time at the chip is actually greater than expected. But the data is delayed too. It is not known what the data pattern is so it is assumed that the delay time is the maximum of Tphldi and Tplhdi. The actual setup time is 2.0 + 0.9 - MAX(0.3, 0.5) = 2.4 ns. This is less than the requirement of 30 ns (for PIO Mode 3) and therefore within spec.

This careful thought process must be repeated for all 15 of the PIO timing parameters (and for DMA also). The easiest way to do this is to make a spreadsheet and enter the six values for RC delay and the interface chip timing parameters. Spreadsheet formulas can then compute the timing at the pins of the device and highlight any that are not within specification. In this manner the difficult calculations need only be derived once and it becomes easier to verify results.

C.2.7.2 Example of host-end termination timing calculation

The host-end timing calculations are similar to the device-end calculations described above with a few more complicating factors added in. The four different signal configurations are shown in figure C.13. For this design 82 ohm series resistors are used on control lines received by the host and 22 ohm resistors on the data lines and control lines driven by the host. It is assumed that the host adapter chip input capacitance plus stray capacitance is 15 pF.

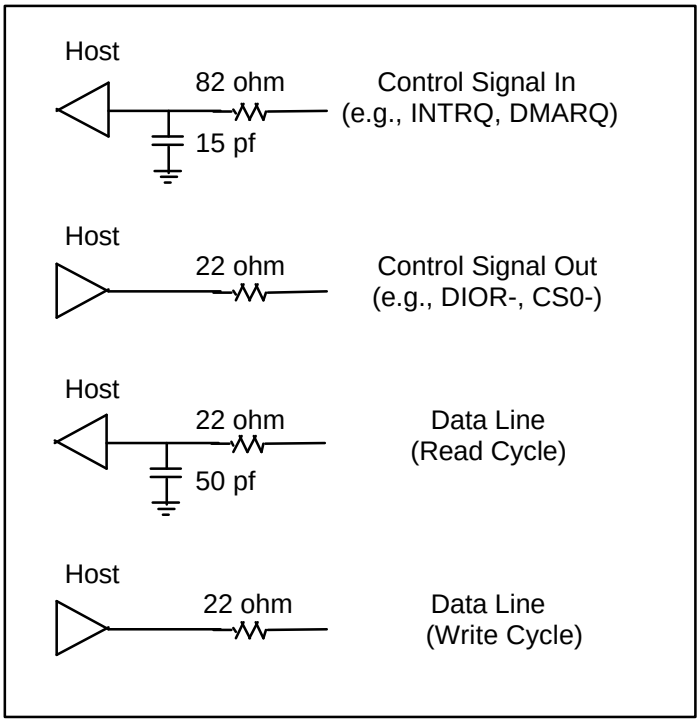


Figure C.13 – Host-end signal configurations with terminations

For these values, the control signal out and the data out models look the same. One simulation can be used to determine both values. The greatest uncertainty is the delay through the cable for received signals. The total cable delay depends on the source impedance of the device. This can be anything from zero to 82 ohms; the greater the impedance, the greater the delay. It is assumed for this example that the device vendor has read this document and has decided to use 22 ohms resistors. If it is desired later to make a worst-case assumption of 82 ohms, then approximately 2 ns are added to the numbers.

Using SPICE models similar to the one shown in figure C.14 the eight delay parameters required are derived. A second device appears in the model as a lumped capacitance of 25 pF which causes the maximum delay. The resulting values appear in table C.3. By examining the values in the table it should be clear why the cable propagation delay is often referred to as being about 5 ns.

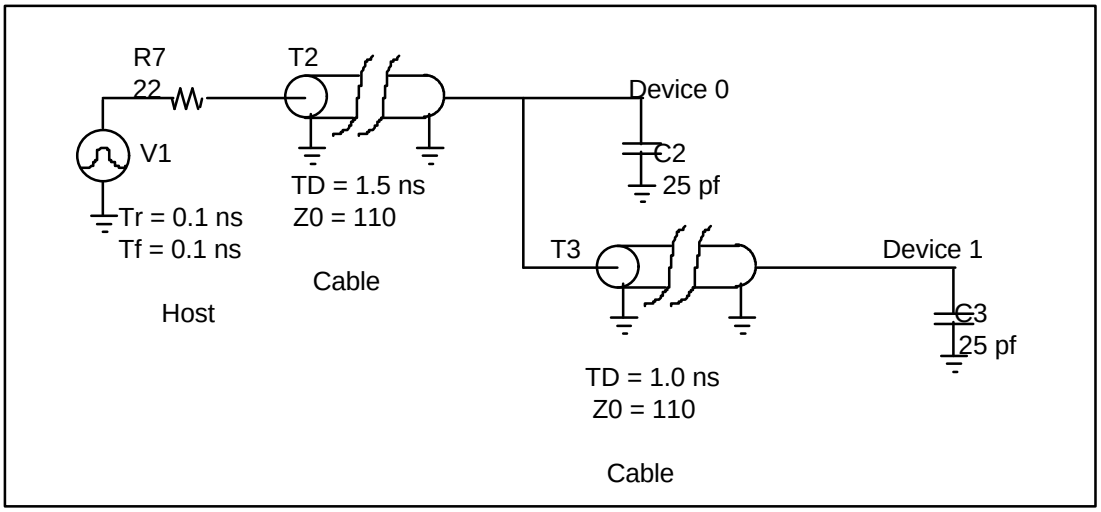


Figure C.14 – SPICE model for control signal out delay calculation

Table C.3 – Typical host-end propagation delay times

Symbol	Description	Value
Tphlci	Propagation delay, high to low, control in	6.4 ns
Tplhci	Propagation delay, low to high, control in	4.7 ns
Tphlco	Propagation delay, high to low, control out	5.9 ns
Tplhco	Propagation delay, low to high, control out	4.6 ns
Tphldi	Propagation delay, high to low, data in	5.7 ns
Tplhdi	Propagation delay, low to high, data in	4.3 ns
Tphldo	Propagation delay, high to low, data out	5.9 ns
Tplhdo	Propagation delay, low to high, data out	4.6 ns

The process of finding the timing values is the same as for the device-end example. The propagation delay times are added to and subtracted from the host adapter chip timings to obtain the timings at the input to the device, in this case calculating the timing at the drive furthest from the host adapter. The resulting timing values are compared against the values to determine what mode the device operates at.

C.2.8 Dual port cabling

One of the recent enhancements to the bus has been the use of primary and secondary ports, allowing the user to attach up to four devices. The optimal way to implement dual ports is to have two completely separate interfaces that have no circuitry in common. This guarantees isolation between the ports and insures that no interference will occur.

> NOTE – At the 1995 Windows Hardware Engineering Conference (WinHEC), Microsoft recommended the use of fully independent primary and secondary ports.

The advent of local bus bridge chips has introduced new driving forces to the dual port cabling issue. Implementing two independent ports on a single chip requires 66 I/O pins. Due to the cost of pins, some designs have combined the data lines of the two ports into one set of pins. Sharing the data lines (or any other lines) in this way without termination is asking for trouble. Simulations confirm that the ringing in such configurations is large and complex, particularly if the loads on the two cables are not balanced.

One alternative pin-saving solution would be to add a set of external buffers. This would require three new control lines but would save 16 data lines for a net improvement of 13 pins. This also would require additional packages on the circuit board.

An economical solution is to add independent series resistors for each line (see figure C.15). Energy reflected back from the first cable passes through one termination resistor before getting to the host. The

reflected signal is further attenuated as it passes through the second resistor and into the second cable. This signal is reflected from the end of the second cable (with loss), and must pass through the termination resistor again before arriving at the host. This provides sufficient attenuation of reflected signals.

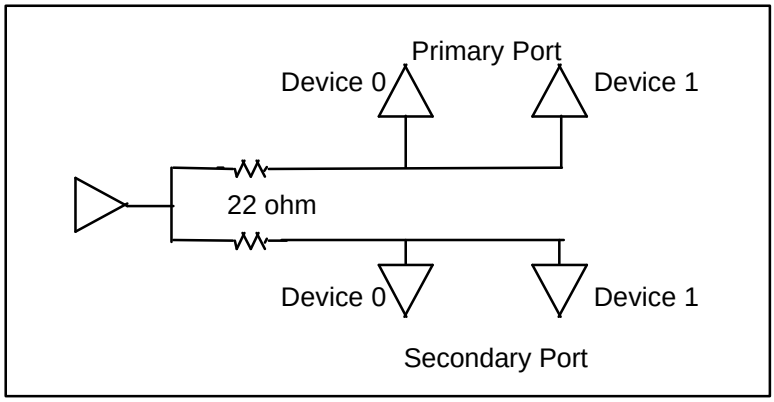


Figure C.15 – Preferred connection for shared lines in dual port systems

Not all of the signal lines in a shared dual port interface can be shared. If the chip selects (CS0-, CS1-) and the data strobes (DIOR-, DIOW-) are shared, then it is impossible to differentiate between the primary and secondary ports. A write to a device on one port causes the same action to occur on the other port, destroying the data on the other device. The data strobe lines are sensitive edge-triggered signals while the chip selects act more like level-sensitive address lines. It is recommended that designers share the less sensitive chip selects and not share the data strobes.

Table C.4 makes some assumptions about how the dual porting is being implemented. If the data lines are shared, there are not simultaneous accesses to the primary and secondary ports. This in theory allows the DMACK- and IORDY lines also to be shared. The INTRQ and DMARQ signals are driven by tristate buffers on the devices. Either the master or slave enables its tristate driver depending on the state of the DEV bit in the Device/Head Register. Therefore INTRQ and DMARQ cannot be shared because either the master or slave device will be driving these lines at all times. The primary port devices do not know about the secondary port devices, so sharing these lines would create a conflict. In theory the DMACK- line could be shared since it is driven by the host. In practice this is not recommended. It is likely that some devices respond unconditionally to the DMACK- signal, whether they ever requested a DMA cycle or not. This could lead to a conflict on a DMA cycle between a primary port device and a secondary port device during the data cycle. For these reasons the INTRQ, DMARQ, and DMACK- lines cannot be shared.

Table C.4 – Possible sharing of signals in dual port configurations

Signal name	
DIOR-, DIOW-	Not shareable
CS0-, CS1-	Shareable
DA0, DA1, DA2	Shareable
DMACK-	Not shareable
RESET-	Shareable
DD0 – DD15	Shareable
DMARQ	Not shareable
INTRQ	Not shareable
IORDY	Shareable
DASP-, PDIAG-	Not shareable
CSEL	Not shareable

The DASP- lines cannot be shared. Assume there are two devices on the primary port, and one device on the secondary port. With the DASP- lines connected, the single device on the secondary port will incorrectly “see” the slave device on the primary port. This would be a problem for all manufacturers who follow the specifications. Similar problems can occur with the PDIAG- lines; they cannot be shared.

C.3 Crosstalk

Crosstalk is switching on one signal line causing induced signals in an adjacent line. Crosstalk has not been a significant issue in the past with slower edge rates; in newer systems the problem is often masked by ringing. Once the cable is terminated and the ringing is under control, then the presence of crosstalk becomes apparent.

C.3.1 Coupling mechanisms

There are two mechanisms by which a signal couples into an adjacent line. The first is coupling capacitance, and the second is mutual inductance. As a switching signal wavefront propagates down the cable it couples energy into the adjacent line. Once this energy is in the second transmission line, it propagates in both directions: forward toward the receiver and back toward the source (see figure C.16).

First the forward coupling components are examined. The voltage induced in the second transmission line is proportional to the coupling coefficient, the inductance, and the rate of change of current in the primary side. This is a negative voltage: a positive current spike in the primary line results in a negative voltage spike in the secondary line.

The coupling capacitance between the two line causes a current pulse in the secondary line proportional to the capacitance and the rate of change of voltage on the primary side. A positive voltage step on the primary line causes a positive voltage spike on the secondary line.

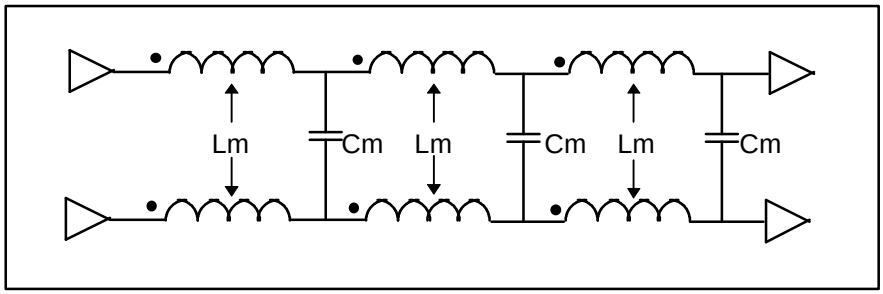


Figure C.16 – Crosstalk coupling mechanisms

These two coupling mechanisms have some interesting characteristics. The polarity of the coupling is opposite for the mutual inductance and coupling capacitance. If the magnitudes of these effects are comparable, then they will cancel, resulting in no forward crosstalk. Unfortunately, accurately computing these values is difficult, and the easiest way to determine the actual amount of crosstalk is to measure it. The other noteworthy characteristic is that the magnitude of the coupled signal is proportional to the rate of change of the signal in the primary line. This is a major reason for controlling the slew rate on bus drivers. Earlier it was said that ringing on the data lines is not necessarily a problem. Here it is seen that fast edge rates and ringing on the data lines can couple by crosstalk into adjacent control lines, causing control sequence errors through mistriggering. It is unlikely crosstalk from data lines causes observable failures in a laboratory environment. But the presence of crosstalk-induced voltage spikes on the control signals reduces the noise margin, and can increase the long-term error rate.

The amplitude of the coupled signal is proportional to the total amount of coupling capacitance and mutual inductance, and is therefore proportional to cable length. Once a line is terminated properly, ringing is no longer a function of length. This leaves crosstalk as the major factor limiting cable length.

Reducing crosstalk involves reducing the mutual inductance, reducing the coupling capacitance, or decreasing the source signal amplitude. Controlling the inductance and capacitance can be done by either keeping the length of the cable short or by increasing the distance between conductors. Placing a ground conductor between critical signals increases the separation of the signals and also adds a shielding effect from the intervening ground. In this environment the only control that can be exercised over the cable is to keep the length at 18 inches or less. The amplitude of the source signal cannot be reduced and still maintain compatibility, but there is control over some elements of the source signal. Slew rate limitation reduces the high-frequency components of the source signal and therefore reduces the coupling of these components

into adjacent lines. Terminating the lines reduces ringing which also decreases the amount of energy coupled at the ringing frequency.

C.4 Bus timing

Terminating the bus has its cost. Partial terminations at the host and the device increase propagation delays throughout the system. The standard specifies that timing is referenced to the input pins of the device (see clause 10). This means that most of the timing issues must be addressed by systems manufacturers and bridge chip designers.

C.4.1 The issues

The most significant timing issue is the propagation delay of the cable. This needs to be added to the host-side timing. The SPICE model in figure C.17 shows an unterminated host with very fast rise times driving a cable with worst case loads. Two unterminated devices are assumed with the maximum allowed capacitive loading of 25 pF.

NOTE – 25 pf was specified in ATA-2.

The simulation results are shown in figure C.18. The period of the ringing is four times the propagation delay of the cable. This simulation shows a cable propagation delay of 5.6 ns. This is twice the value obtained by assuming an 18-inch cable with a propagation velocity of 60% c. The additional delay is due to the presence of the capacitive loads on the cable. This result is important to system designers who take into account worst-case cable delay when specifying the bridge chip timing.

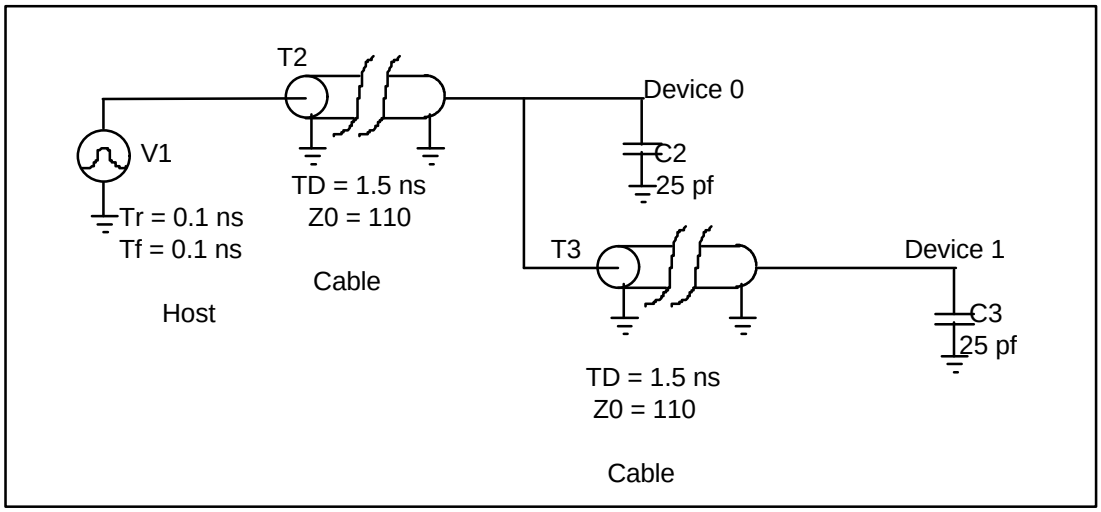


Figure C.17 – SPICE model of cable with worst case loads

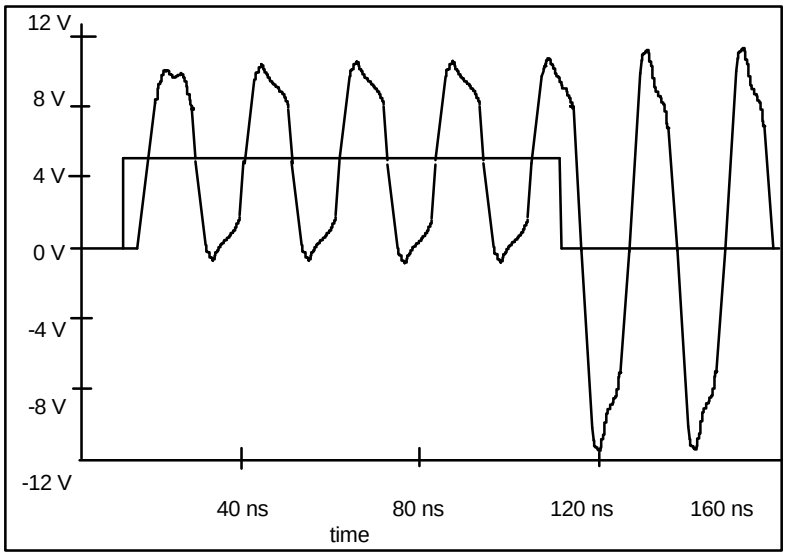


Figure C.18 – Simulation of unterminated cable with worst case loads

From the host point of view, all of the timings are corrected by adding the propagation delay of the cable to insure that the timing is correct at the input pins of the furthest device. Figure C.19 shows a typical corrected result using the read cycle data setup time as an example. The document specifies a setup time at the device of 20 ns (PIO Mode 3). The remaining setup time at the host is only 8.8 ns (20 - 2 x 5.6).

C.4.2 The influence of termination

If the host has a series partial termination resistor then the bridge chip includes additional timing margin to account for the RC delay of that resistor. Simulations show that the incremental delay added by a series termination resistor at the host is approximately 0.1 ns for a 22 ohm resistor and 1.7 ns for an 82 ohm resistor.

NOTE – Assuming Two drive load, 25 pF at each drive, 18-inch cable, 25 pF at host

The extra delay of higher resistor values is one of the reasons that 22 ohm series resistors at the host are recommended.

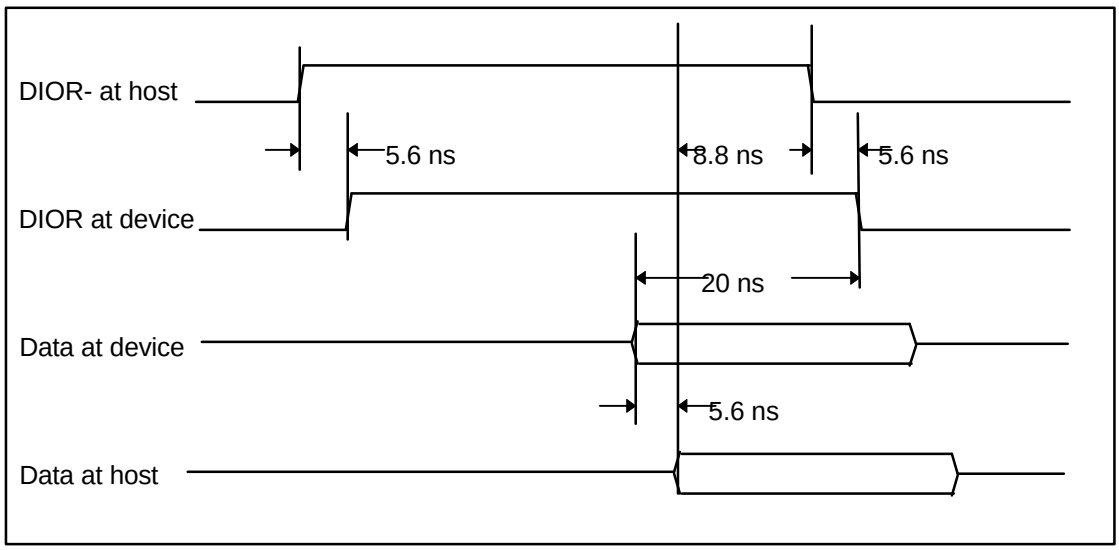


Figure C.19 – Host data setup time during a read cycle

The series resistor at the host is located as close as possible to the connector. To see the importance of this, SPICE simulations are done with the stray capacitance on the driver side of the series resistor and again with the stray capacitance on the cable side. The ringing is reduced when the stray capacitance of the host is on the driver side of the series resistor. A related issue is the distance from the host adapter chip (or chipset) to the connector. Some motherboards have the chip located up to 10 inches away from the connector. This effectively adds another 10 inches to the 18-inch ribbon cable, resulting in an equivalent cable length of 28 inches.

> NOTE – The traces on the circuit board are from 50 to 200 ohm impedance, so the electrical length of the trace cannot simply be added to the 110 ohm ribbon cable. A SPICE simulation can be used to find the actual delay.

This additional length is not necessarily a problem. If the system manufacturer takes the extra trace delay into account in the application of the host adapter chip, and the total capacitance is kept below the host limit of 25 pF, then in theory there is no difference. Real-world experience indicates that this calculation is rarely done. The distance from the chip to the connector is not addressed in the specification. Keeping the connector within 3 inches (by trace length) of the host adapter chip is recommended.

C.4.3 Calculating rise time

Chip designers often use a lumped capacitance model for simulating the delay of the output cell. For the simulations this sometimes consists of adding the maximum capacitance allowed for the host and the devices (3 x 25 pF) to an estimated capacitance value for the cable (25 pF). Simulation is then performed with 100 pF capacitance on the output. This does not give an accurate measurement of the timing. A better approximation is to use an output capacitance for the motherboard, a host end termination resistor, and a transmission line to the devices (see figure C.20).

To illustrate how these models are different, suppose that the propagation delay of the output cell simulation is 2 ns too slow. The chip designer (using a 100 pF model) increases the drive current of the output devices. With enough drive current into a purely capacitive load, the 2 ns is removed, bringing the output cell timing back into spec.

Increasing the drive of the output cell in the transmission line model, the length of the cable is not increased and nor increase the speed of signal propagation in the cable is not increased. The 2 ns required time reduction is not achieved by increasing the output drive current. Increasing the output drive current only increases the edge speed, making the ringing worse at the device end (some time is gained with the faster edge speed, but not nearly as much as is predicted with a simple capacitive load model). It is not possible to decrease the overhead by increasing the drive current.

Most ASIC designers find that simulations using the recommended model of figure C.20 show their output cells to be faster than in models with a 100 pF load.

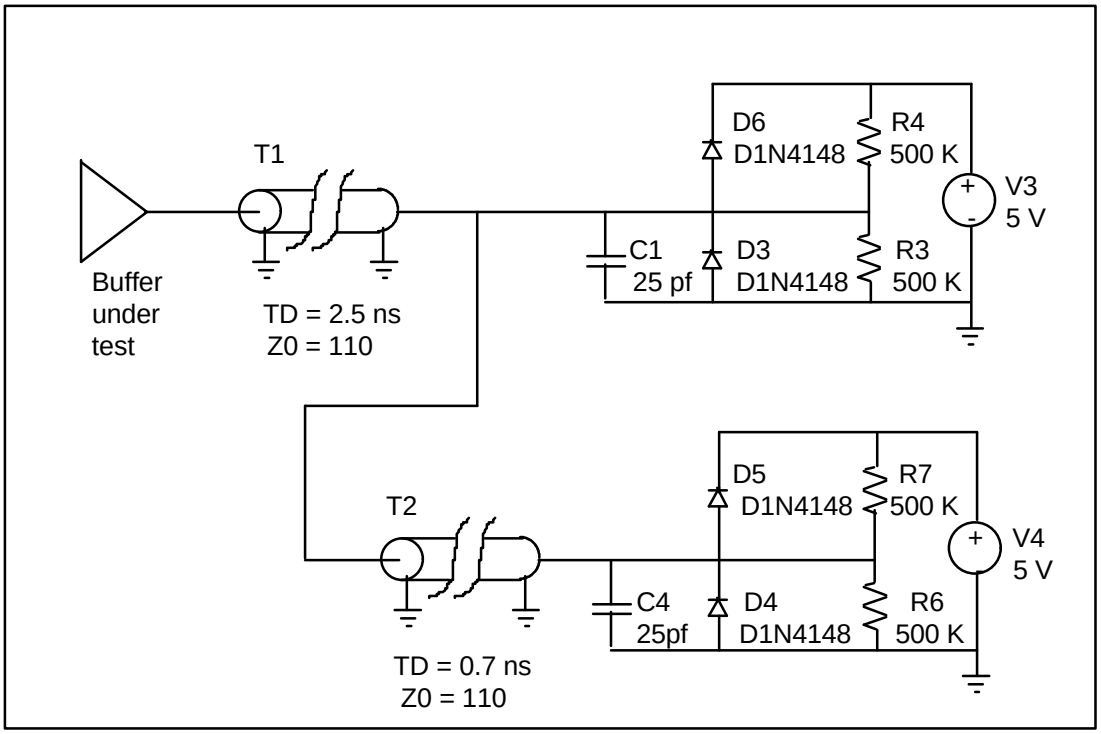


Figure C.20 – Recommended model for I/O cell propagation delay

C.4.4 Measuring propagation delay

Propagation delay times at the host (and at the device) are measured to the standard of 0.8 V for high to low transitions and 2.0 V for low to high transitions. Many IC manufacturers measure propagation delay at the typical switch point for TTL of 1.4 V. This is not appropriate for the interface since virtually every chip manufacturer (both host and device end) has included hysteresis for noise immunity. Since both the hysteresis window and hysteresis offset of a given receiver move with process, voltage, and temperature, the only guaranteed switch points are the TTL high and low values (0.8 V and 2.0 V).

C.5 Summary of guidelines

This summary is a collection of reminders for device, system, and chipset designers. They are separated into three groups by relevancy. The guidelines below are not intended to be a strict mandate, but a tool to help everyone build compatible, reliable, high-performance products.

C.5.1 Guidelines for device designers

- Terminate signals as shown in table C.1. Consider adding capacitors to ground on these lines if the input capacitance is less than 8 pF, or use active clamping circuits. Place these resistors as close to the connector as possible.
- Verify that the termination circuit used on received signals has less than 20 pF of equivalent capacitance.
- Perform a timing analysis to verify that timings are met at the input to the device. Include the time delay due to propagation and cable termination circuits.

C.5.2 Guidelines for system designers

- Do not use any value less than 1 ohm for pull up resistors on open-collector signals such as IORDY (as per the standard).

- The host adapter chip should be located as close as possible to the connector. Keep the trace length between them less than 3 inches.
- After circuit board fabrication, verify that the total input capacitance at the host is less than 25 pF.
- Terminate signals as shown in figure C.1. Place these resistors as close to the connector as possible.
- Perform a system timing analysis to verify that timings are met at the input to the device.
- For dual port implementations, terminate signals as shown in figure C.15. These resistors should be placed as close to the connector of that port as possible.
- For dual port implementations, the signal lines CS0- and CS1- should be shared.
- For dual port implementations, the signal lines DIOR- and DIOW- should not be shared.
- For dual port implementations, do not share DASP- or PDIAG- signal lines.
- For dual port implementations, perform a system timing analysis to verify that timings are met at the input of the device. In particular watch the assertion widths of DIOR- and DIOW- to insure that they meet the specification.
- Route cable away from chassis, power supplies and high speed circuits.
- Use the shortest cable practical and never greater than 18 in.

C.5.3 Guidelines for chip designers

- Design I/O cells to have rise and fall times of 5 ns or more under both minimum and maximum load conditions.
- Perform timing simulations using a transmission line load model, not a 100 pF capacitor model.
- Take worst-case cable delay into account when designing the interface. Ensure that timing can be met at the device-end of the cable. Provide typical application data with timing for system manufacturers.

Annex D
(informative)
Bibliography

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AT Attachment Interface with Extensions, ANSI X3.279-1996
AT Attachment - 3, ANSI X3.298-1996
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ATA Packet Interface (ATAPI) for Streaming Tape, QIC-157
Suite of 2.5" Form Factor Specifications, SFF-8200, SFF-8201, SFF-8212[1]
Suite of 3.5" Form Factor Specifications, SFF-8300, SFF-8301, SFF-8302
BIOS Enchanced Disk Drive Specification (EDD), X3T13/1226DT
ATA Packet Interface for CD-ROMs, SFF-8020i
PC Card Standard, February 1995, PCMCIA[2]

1) SFF documents are published by:
SFF
14426 Black Walnut Court, Saratoga, California 95070
FaxAccess: 408 741-1600

2) The PC Card Standard is published by:
Personal Computer Memory Card International Association
2635 North First Street, Suite 209, San Jose, California 95131

Annex E
(informative)
Command set summary

The following four tables are provided to facilitate the understanding of the command set. Table E.1 provides information on which command codes are currently defined. Table E.2 provides a list of all of the commands in order of command code. Table E.3 provides a summary of all commands with the protocol, required use, command code and registers used for each. Table E.4 shows the status and error bits used by each command.

Table E.1 – Command matrix

	x0	x1	x2	x3	x4	x5	x6	x7	x8	x9	xA	xB	xC	xD	xE	xF
0x	C	R	R	R	R	R	R	R	C*	R	R	R	R	R	R	R
1x	O	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*
2x	C	C	O*	O*	R	R	R	R	R	R	R	R	R	R	R	R
3x	C	C	O*	O*	R	R	R	R	R	R	R	R	C	R	R	R
4x	C	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R
5x	O*	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
6x	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
7x	C	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*	E*
8x	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V	V
9x	C	C	C	R	E*	E*	E*	E*	E*	E*	V	R	R	R	R	R
Ax	C*	C*	C*	R	R	R	R	R	R	R	R	R	R	R	R	R
Bx	C	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R
Cx	V	V	V	V	C	C	C	C*	C	C	C	C	C*	R	R	R
Dx	R	R	R	R	R	R	R	R	R	R	R	E*	E*	E*	C	C
Ex	C	C	C	C	C	C	C	C*	C	E*	R	R	C*	C	O*	C
Fx	V	C	C	C	C	C	C	V	C	C*	V	V	V	V	V	V

Key:
C = a defined command, R = Reserved, undefined in current specifications, V = Vender specific commands
O = Obsolete, E=a retired command, * indicates that the definition of this command has changed from ATA-3, X3.298-1996.

Table E.2 – Commands sorted by command value

Command name	Command code
NOP	00h
DEVICE RESET	08h
READ SECTOR(S)	20h-21h
WRITE SECTOR(S)	30h-31h
WRITE VERIFY	3Ch
READ VERIFY SECTOR(S)	40h-41h
SEEK	70h
EXECUTE DEVICE DIAGNOSTIC	90h
INITIALIZE DEVICE PARAMETERS	91h
DOWNLOAD MICROCODE	92h
PACKET	A0h
IDENTIFY PACKET DEVICE	A1h
SERVICE	A2h
SMART	B0h
READ MULTIPLE	C4h
WRITE MULTIPLE	C5h
SET MULTIPLE MODE	C6h
READ DMA QUEUED	C7h
READ DMA	C8h-C9h
WRITE DMA	CAh-CBh
WRITE DMA QUEUED	CCh
DOOR LOCK	DEh
DOOR UNLOCK	DFh
STANDBY IMMEDIATE	E0h
IDLE IMMEDIATE	E1h
STANDBY	E2h
IDLE	E3h
READ BUFFER	E4h
CHECK POWER MODE	E5h
SLEEP	E6h
FLUSH CACHE	E7h
WRITE BUFFER	E8h
IDENTIFY DEVICE	ECh
MEDIA EJECT	EDh
SET FEATURES	EFh
SECURITY SET PASSWORD	F1h
SECURITY UNLOCK	F2h
SECURITY ERASE PREPARE	F3h
SECURITY ERASE UNIT	F4h
SECURITY FREEZE	F5h
SECURITY DISABLE PASSWORD	F6h
READ NATIVE MAX ADDRESS	F8h
SET MAX ADDRESS	F9h

Table E.3 – Command codes and parameters

proto	Command	typ	PKT fea	Command code	Parameters used				
					FR	SC	SN	CY	DH
ND	CHECK POWER MODE	O	M	E5h		y			D
DR	DEVICE RESET	O	M	08h					D
ND	DOOR LOCK	O	N	DEh					D
ND	DOOR UNLOCK	O	N	DFh					D
PO	DOWNLOAD MICROCODE	O	N	92h	y	y	y	y	D
DD	EXECUTE DEVICE DIAGNOSTIC	M	M	90h					D*
ND	FLUSH CACHE	O	O	E7h		y	y	y	y
PI	IDENTIFY DEVICE	M	N	ECh					D
PI	IDENTIFY PACKET DEVICE	N	M	A1h					
ND	IDLE	O	O	E3h		y			D
ND	IDLE IMMEDIATE	O	M	E1h					D
ND	INITIALIZE DEVICE PARAMETERS	M	N	91h		y			y
ND	MEDIA EJECT	O	N	EDh					D
ND	NOP	O	M	00h					D
P	PACKET	N	M	A0h	y	y	y	y	D
PI	READ BUFFER	O	N	E4h					D
DM	READ DMA	M	N	C8h C9h		y	y	y	y
DMO	READ DMA QUEUED	O	N	C7h	y	y	y	y	y
PI	READ MULTIPLE	M	N	C4h		y	y	y	y
ND	READ NATIVE MAX ADDRESS	O	N	F8h					D
PI	READ SECTOR(S)	M	N	20h 21h		y	y	y	y
ND	READ VERIFY SECTOR(S)	M	N	40h 41h		y	y	y	y
PO	SECURITY DISABLE PASSWORD	O	O	F6h					D
ND	SECURITY ERASE PREPARE	O	O	F3h					D
PO	SECURITY ERASE UNIT	O	O	F4h					D
ND	SECURITY FREEZE	O	O	F5					D
PO	SECURITY SET PASSWORD	O	O	F1H					D
PO	SECURITY UNLOCK	O	O	F2h					D
ND	SEEK	M	N	70h			y	y	y
P	SERVICE	N	O	A2h		y	y	y	D
ND	SET FEATURES	M	M	EFh	y				D
ND	SET MAX ADDRESS	O	N	F9h		y	y	y	y
ND	SET MULTIPLE MODE	M	N	C6h		y			D
ND	SLEEP	O	M	E6h					D
ND	SMART DISABLE OPERATIONS	O	O	B0h	y			y	D
ND	SMART ENABLE/DISABLE AUTOSAV	O	O	B0h	y	y		y	D
ND	SMART ENABLE OPERATIONS	O	O	B0h	y			y	D
ND	SMART EXECUTE OFF_LINE	O	O	B0h	y			y	D
PI	SMART READ DATA	O	O	B0h	y			y	D
ND	SMART RETURN STATUS	O	O	B0h	y			y	D
ND	STANDBY	O	O	E2h		y			D
ND	STANDBY IMMEDIATE	O	M	E0h					D
PO	WRITE BUFFER	O	N	E8h					D
DM	WRITE DMA	M	N	CAh CBh		y	y	y	y

(continued)

Table E.3 – Command codes and parameters *(concluded)*

proto	Command	typ	PKT fea	Command code	Parameters used				
					FR	SC	SN	CY	DH
DMO	WRITE DMA QUEUED	O	N	CCh	y	y	y	y	y
PO	WRITE MULTIPLE	M	N	C5h	%	y	y	y	y
PO	WRITE SECTOR(S)	M	N	30h 31h	%	y	y	y	y
PO	WRITE VERIFY	O	N	3Ch	%	y	y	y	y
VS	Vendor specific	V	V	9Ah,C0h-C3h,8xh, F0h,F7h, FAh-FFh					
-	Reserved: all remaining codes	R	R						

Key:
DM = DMA command ND = Non-data command PI = PIO data in command
PO = PIO data out command VS = Vendor specific command O = Optional P=PACKET command
DR = DEVICE RESET protocol DD = EXECUTE DEVICE DIAGNOSTIC protocol
DMO = Overlapped/queued DMA
typ=Command type PKT fea=Command type when PACKET Command feature set implemented
M = Mandatory R = Reserved N=Not to be used V = Vendor specific implementation
CY = Cylinder registers SC = Sector Count register DH = Device/Head register
SN = Sector Number register FR = Features register (see command descriptions for use)
y = the register contains a valid parameter for this command. For the Device/Head register, y means both the device and head parameters are used.
D = only the device parameter is valid and not the head parameter.
d = the device parameter is valid, the usage of the head parameter vendor specific.
D* = Addressed to device 0 but both devices execute it.
% = Maintained for compatibility (see 7.2.10)

Table E.4 – Status and error usage

	Status register				Error register					
	DRDY	DF	CORR	ERR	ICRC	UNC	IDNF	ABRT	TK0NF	AMNF
CHECK POWER MODE	V	V		V				V		
DOOR LOCK	V	V		V				V		
DOOR UNLOCK	V	V		V				V		
DOWNLOAD MICROCODE	V	V		V				V		
EXECUTE DEVICE DIAGNOSTIC	V	V		V	(see 7.6)					
FLUSH CACHE	V	V		V				V		
IDENTIFY DEVICE	V									
IDENTIFY DEVICE DMA	V									
IDLE	V	V		V				V		
IDLE IMMEDIATE	V	V		V				V		
INITIALIZE DEVICE PARAMETERS	V	V								
MEDIA EJECT	V	V		V				V		
NOP	V	V		V				V		
READ BUFFER	V	V		V				V		
READ DMA	V	V	V	V	V	V	V	V		V
READ DMA QUEUED	V	V	V	V	V	V	V	V		V
READ MULTIPLE	V	V	V	V		V	V	V		V
READ NATIVE MAX ADDR	V			V				V		
READ SECTOR(S)	V	V	V	V		V	V	V		V
READ VERIFY SECTOR(S)	V	V	V	V		V	V	V		V
SECURITY DIS PASSWORD	V	V		V				V		
SECURITY ERASE PREP	V	V		V				V		
SECURITY ERASE UNIT	V	V		V				V		
SECURITY FREEZE	V	V		V				V		
SECURITY SET PASSWRD	V	V		V				V		
SECURITY UNLOCK	V	V		V				V		
SEEK	V	V		V			V	V		
SET FEATURES	V	V		V				V		
SET MAX ADDRESS	V			V				V		
SET MULTIPLE MODE	V	V		V				V		
SLEEP	V	V		V				V		
SMART DISABLE OPS	V			V				V		
SMART EN/DIS AUTOSAVE	V			V				V		
SMART ENABLE OPS	V			V				V		
SMART EXECUTE OFF_LIN	V			V			V	V		V
SMART READ DATA	V			V		V	V	V		V
SMART RETURN STATUS	V			V		V	V	V		V
STANDBY	V	V		V				V		
STANDBY IMMEDIATE	V	V		V				V		
WRITE BUFFER	V	V		V				V		
WRITE DMA	V	V		V	V		V	V		
WRITE DMA QUEUED	V	V		V	V		V	V		
WRITE MULTIPLE	V	V		V			V	V		
WRITE SECTOR(S)	V	V		V			V	V		
WRITE VERIFY	V	V	V	V		V	V	V		V
Invalid command code	V	V		V				V		
Key: V = valid on this command										

Table E.5 – I/O port functions and selection addresses except PACKET and SERVICE commands

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	x	x	x	Data bus high impedence	Not used
					Control block registers	
N	A	0	x	x	Data bus high impedence	Not used
N	A	1	0	x	Data bus high impedence	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	(See note 1)	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Sector Count	Sector Count
A	N	0	1	1	Sector Number	Sector Number
A	N	1	0	0	Cylinder Low	Cylinder Low
A	N	1	0	1	Cylinder High	Cylinder High
A	N	1	1	0	Device/Head	Device/Head
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

Key:
A = signal asserted, N = signal negated, x = don't care
NOTES –
1 This register is obsolete. It is recommended that a device not respond to a read of this address (see 4.3.1).
2 Register content may change for some commands.

Table E.6 – I/O port functions and selection addresses for PACKET and SERVICE commands

Addresses					Functions	
CS0-	CS1-	DA2	DA1	DA0	Read (DIOR-)	Write (DIOW-)
N	N	x	x	x	Data bus high impedence	Not used
					Control block registers	
N	A	0	x	x	Data bus high impedence	Not used
N	A	1	0	x	Data bus high impedence	Not used
N	A	1	1	0	Alternate Status	Device Control
N	A	1	1	1	(see note)	Not used
					Command block registers	
A	N	0	0	0	Data	Data
A	N	0	0	1	Error	Features
A	N	0	1	0	Interrupt reason	
A	N	0	1	1		
A	N	1	0	0	Byte count low	Byte count low
A	N	1	0	1	Byte count high	Byte count high
A	N	1	1	0	Device select	Device select
A	N	1	1	1	Status	Command
A	A	x	x	x	Invalid address	Invalid address

Key:
A = signal asserted, N = signal negated, x = don't care
NOTE – This register is obsolete. It is recommended that a device not respond to a read of this address (see 4.3.1).

Annex F
(informative)
Command packet format example

Table F.1 is an example of the typical command packet for most PACKET commands.

Table F.1 – Typical command packet

Byte	7	6	5	4	3	2	1	0
0	Operation code							
1	reserved			reserved				
2	(MSB)							
3	Logical block address (if required)							
4								
5								(LSB)
6	reserved							
7-8	(MSB)		Transfer length (if required) or Parameter list length (if required) or Allocation length (if required)					(LSB)
9	reserved							
10	reserved							
11	reserved							