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**Bài tập tuần 4**

**Bài 1:**

module cau1(SW, KEY, LEDR);

    input [2:0]SW; // SW0 = D0, SW1 = D1, SW2 = s

    input [0:0]KEY;

    output [0:0]LEDR; // LEDR0 = q

    wire d;

    mux\_21(SW[0], SW[1], SW[2], d);

    FF\_D(d, KEY[0], LEDR[0]);

endmodule

module mux\_21(x, y, s, m);

    input x, y, s;

    output m;

    assign m = s?y:x;

endmodule

module FF\_D(d, clk, q);

    input d, clk;

    output reg q;

    always @(posedge clk)

        q <= d;

endmodule

**Bài 2:**

module cau2(SW, KEY, LEDR);

    input [8:0]SW; // SW[3:0] = D0, SW[7:4] = D1, SW[8] = s

    input [0:0]KEY;

    output wire [3:0]LEDR; // LEDR[3:0] = q

    wire [3:0]d;

    mux\_21\_4b(SW[3:0], SW[7:4], SW[8], d);

    FF\_D\_4b(d, KEY[0], LEDR[3:0]);

endmodule

module mux\_21\_4b(x, y, s, m);

    input [3:0]x, y;

    input s;

    output [3:0]m;

    assign m = s?y:x;

endmodule

module FF\_D\_4b(d, clk, q);

    input [3:0]d;

    input clk;

    output reg [3:0]q;

    always @(posedge clk)

        q <= d;

endmodule

**Bài 3:**

module cau3(SW, KEY, LEDR);

    input [0:0]SW, KEY; // t = SW0, clk = KEY0

    output [0:0]LEDR; // q = LEDR

    FF\_T(SW[0], KEY[0], LEDR[0]);

endmodule

module FF\_T(t, clk, q);

    input t, clk;

    output q;

    wire m1, m2, d;

    and(m1, ~t, q);

    and(m2, t, ~q);

    or(d, m1, m2);

    FF\_D(d, clk, q);

endmodule

module FF\_D(d, clk, q);

    input d, clk;

    output reg q;

    always @(posedge clk)

        q <= d;

endmodule

**Bài 4:**

module cau4(SW, KEY, LEDR);

    input [1:0]SW;

    input [0:0]KEY; // j = SW0, k = SW1, clk = KEY0

    output [0:0]LEDR; // q = LEDR

    FF\_T(SW[0], SW[1], KEY[0], LEDR[0]);

endmodule

module FF\_T(j, k, clk, q);

    input j, k, clk;

    output q;

    wire m1, m2, d;

    and(m1, j, ~q);

    and(m2, ~k, q);

    or(d, m1, m2);

    FF\_D(d, clk, q);

endmodule

module FF\_D(d, clk, q);

    input d, clk;

    output reg q;

    always @(posedge clk)

        q <= d;

endmodule

**Bài 5:**

module cau5(SW, KEY, LEDR);

    input [0:0]SW; // d = SW0

    input [1:0]KEY;// clk = KEY0, r = KEY1

    output [3:0]LEDR; // q = LEDR0

    wire q1, q2, q3;

    FF\_D(SW[0], KEY[1], KEY[0], LEDR[0]);

    FF\_D(LEDR[0], KEY[1], KEY[0], LEDR[1]);

    FF\_D(LEDR[1], KEY[1], KEY[0], LEDR[2]);

    FF\_D(LEDR[2], KEY[1], KEY[0], LEDR[3]);

endmodule

module FF\_D(d, r, clk, q);

    input d, r, clk;

    output reg q;

    always @(posedge clk)

        if(r == 0)

            q <= 0;

        else

            q <= d;

endmodule