University of Mauritius

Faculty of Information ,Communication and Digital Technologies

Computer Architecture and Organisation Assignment 1

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Course : BSc (Hons) Computer Science Level 1

Module : ICT 1206Y Computer Architecture and Organisation

Table of Contents

1. Sequence recognition problem

Implement a circuit (one input X and one output Z) that recognizes the occurrence of the sequence of bits 1001 on the input X by making the output Z equal to 1 when the previous three inputs to the circuit were 100 and current input is a 1. Use D flip-flops.

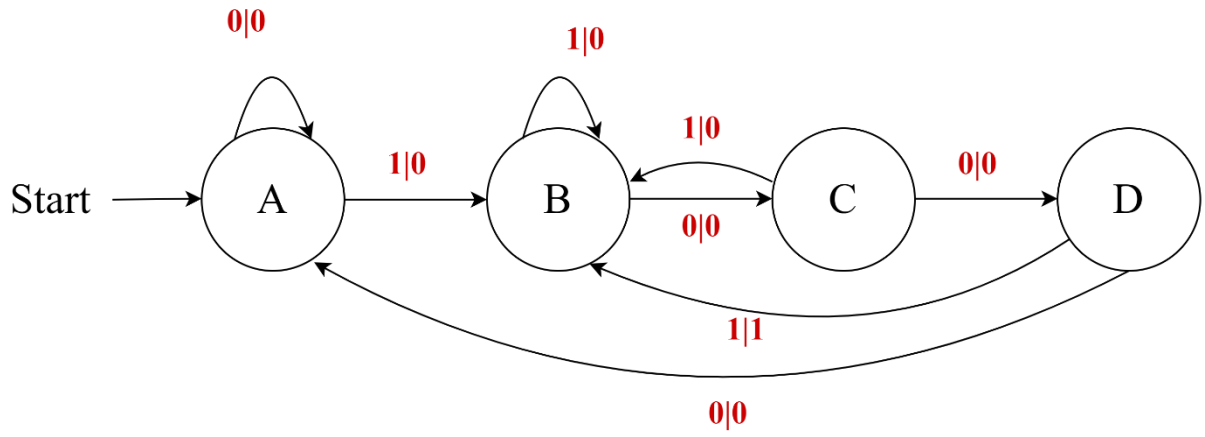
For example:

X: 0 0 1 1 0 0 1 0 0 1 1 0 1 0 0 1 1 1 . . . .

Z: 0 0 0 0 0 0 1 0 0 1 0 0 0 0 0 1 0 0 . . . .

1.1 State transition diagram

State	Meaning	Q_1 Q_0
A	No valid sequence detected	0 0
B	Sequence 1 detected	0 1
C	Sequence 10 detected	1 0
D	Sequence 100 detected	1 1



Notation : X|Z

1.2 State table

Present State	Input	Next State	Output
A	0	A	0
A	1	B	0
B	0	C	0
B	1	B	0
C	0	D	0
C	1	B	0
D	0	A	0
D	1	B	1

State	Q_1 Q_0
A =	0 0
B =	0 1
C =	1 0
D =	1 1

1.3 Assigned binary code to states

Present State		Input	Next State		Output
Q_1	Q_0	X	Q_1	Q_0	Z
0	0	0	0	0	0
0	0	1	0	1	0
0	1	0	1	0	0
0	1	1	0	1	0
1	0	0	1	1	0
1	0	1	0	1	0
1	1	0	0	0	0
1	1	1	0	1	1

1.4 Determined flip-flop input values

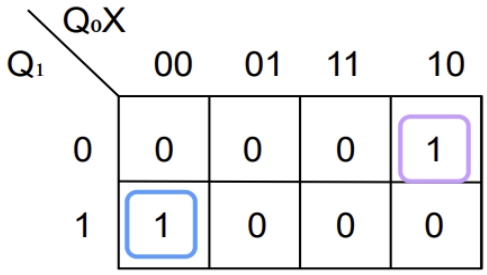
Present State		Input	Next State		Flip-Flop		Output
Q_1	Q_0	X	Q_1	Q_0	D_1	D_0	Z
0	0	0	0	0	0	0	0
0	0	1	0	1	0	1	0
0	1	0	1	0	1	0	0
0	1	1	0	1	0	1	0
1	0	0	1	1	1	1	0
1	0	1	0	1	0	1	0
1	1	0	0	0	0	0	0
1	1	1	0	1	0	1	1

D excitation table :

Q_1	Q_0	D	Operation
0	0	0	Reset
0	1	1	Set
1	0	0	Reset
1	1	1	Set

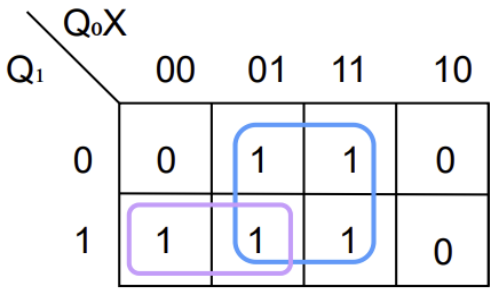
1.5 Karnaugh maps

For D_1 :



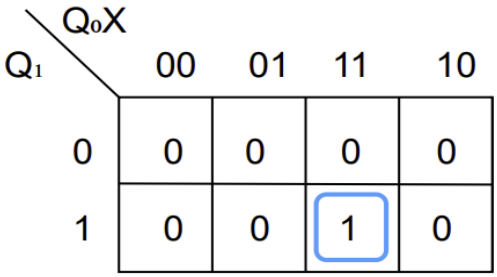
$$D_1 = \bar{Q}_1 Q_0 \bar{X} + Q_1 \bar{Q}_0 \bar{X}$$

For D_0 :



$$D_0 = X + Q_1 \bar{Q}_0$$

For Z :



$$Z = Q_1 Q_0 X$$

1.6 Logic circuits

1.6.1 Subcircuits

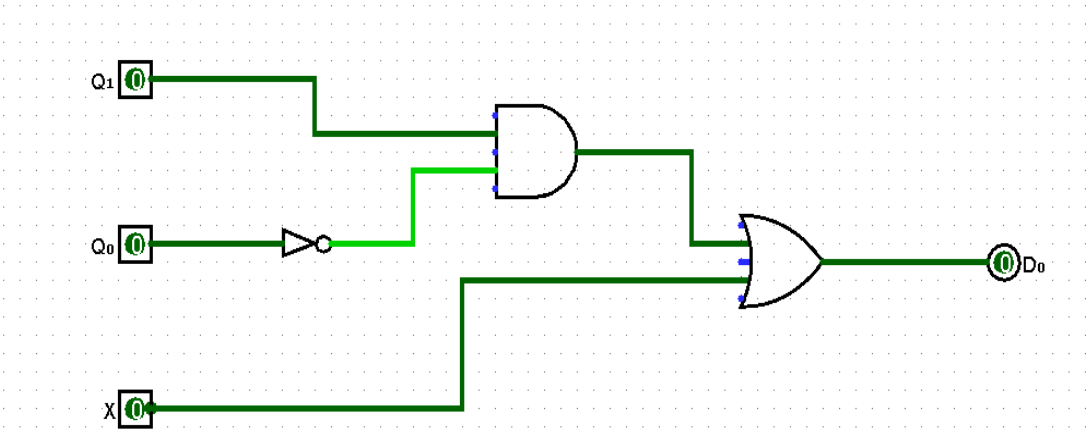


Figure 1 - D Flip - flop 0

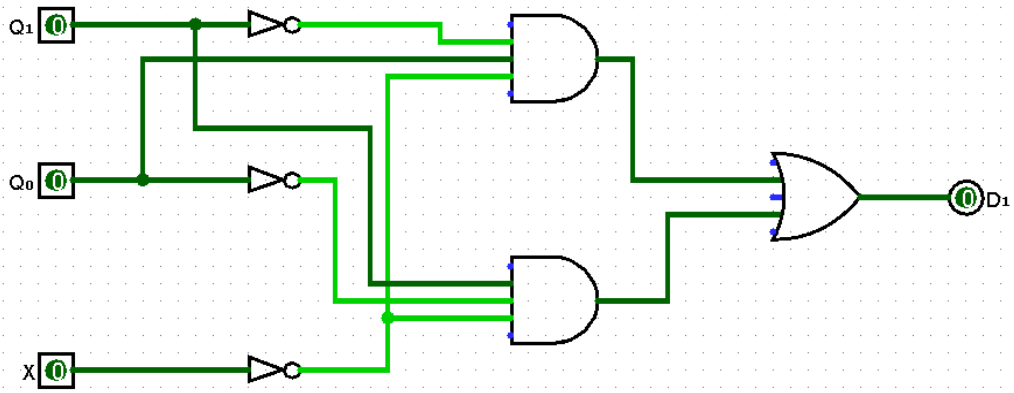


Figure 2 - D Flip - flop 1

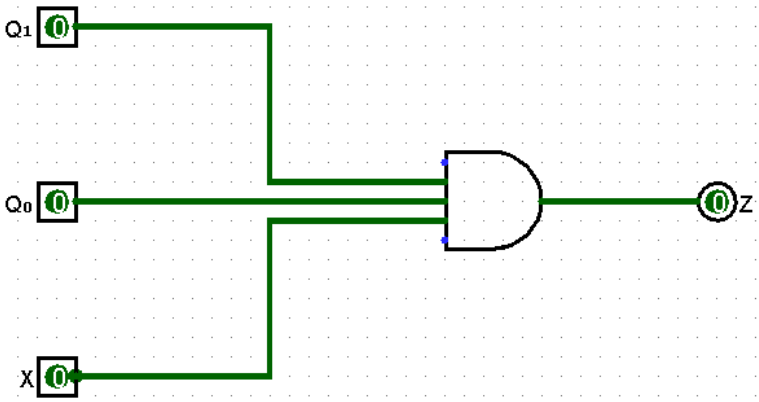
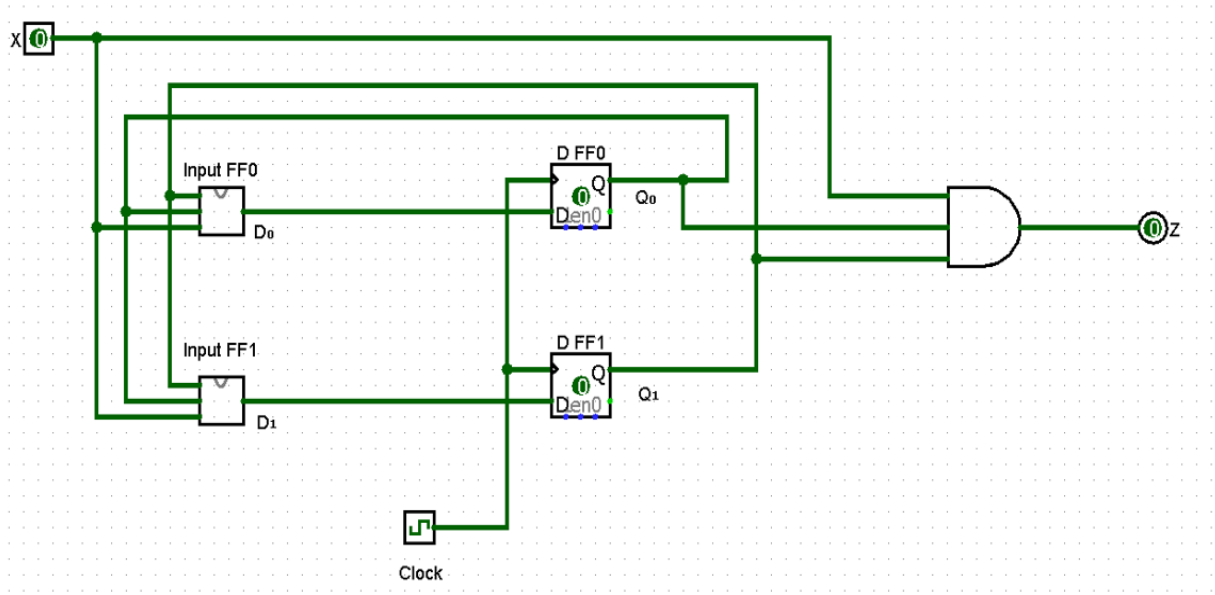


Figure 3 – Output Z

1.6.2 Main circuit

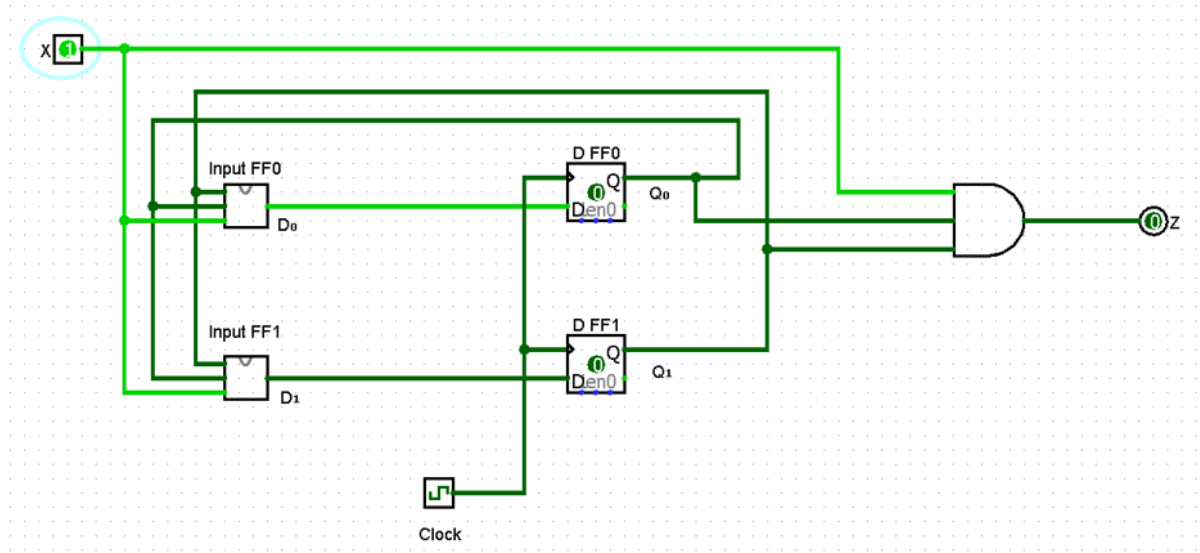
The main circuit consists of two D flip-flops.



1.7 Circuit simulation

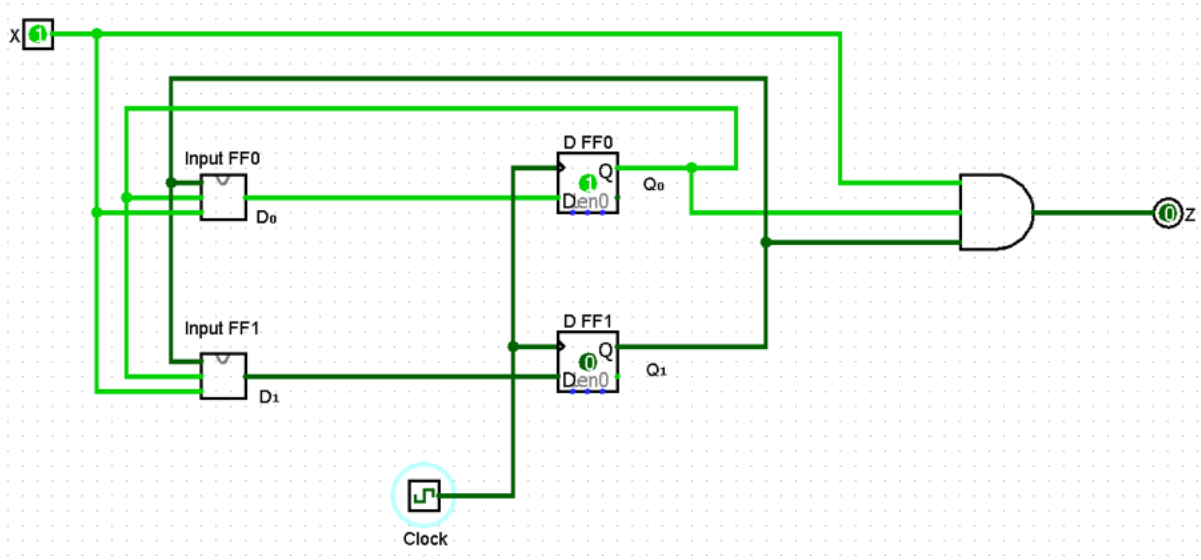
Input test : 101001

Step 1 : Set X = 1 [101001]



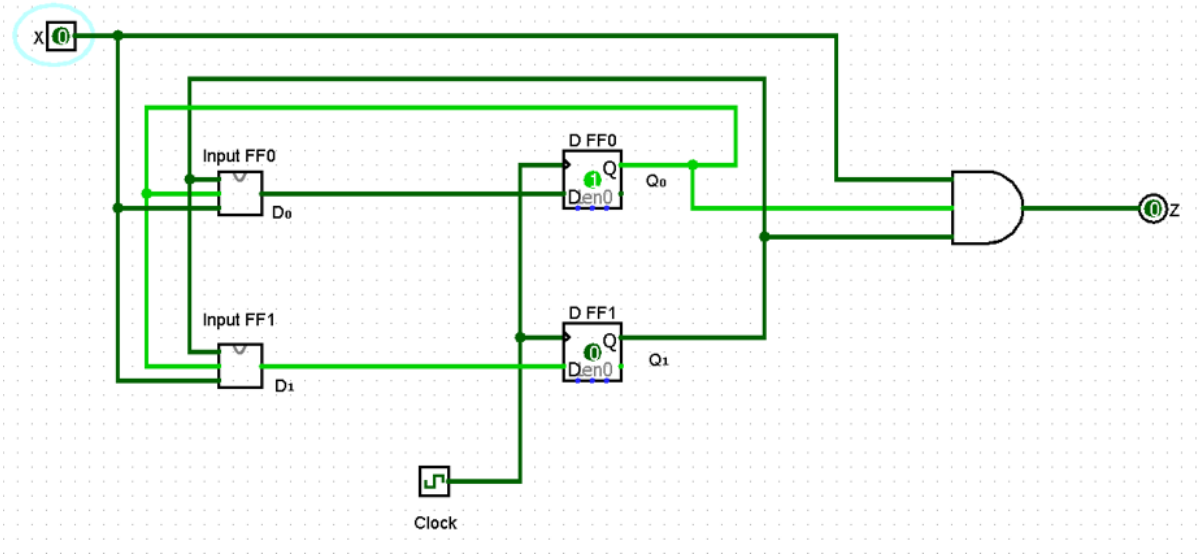
- Z = 0. Sequence 1001 is not detected. The sequence 1 has been detected.

Step 2 : Toggle clock



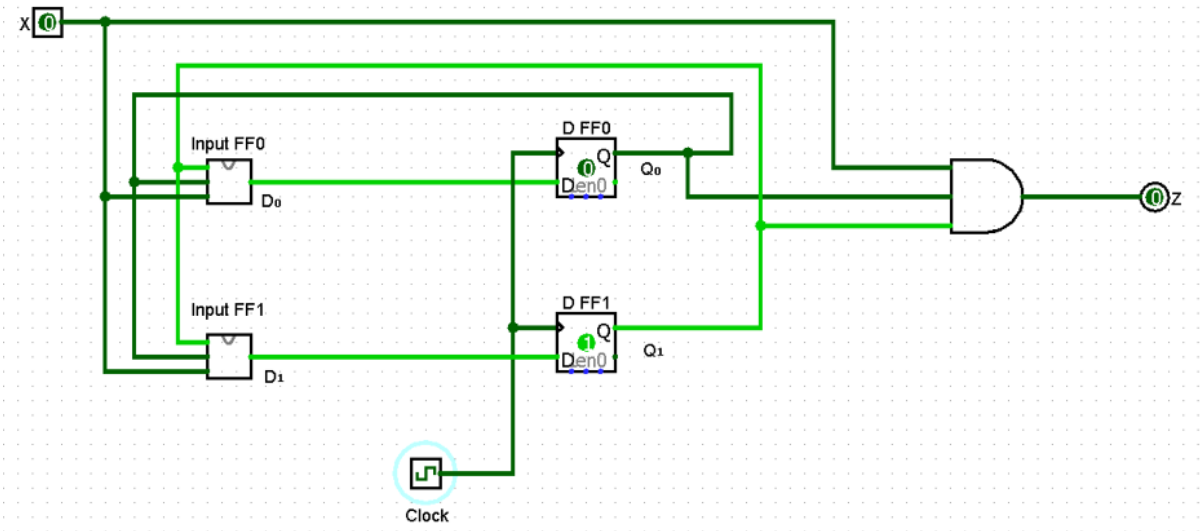
➢ Since Q_1 Q_0 = 01, circuit is in state B.

Step 3 : Set X = 0 [101001]



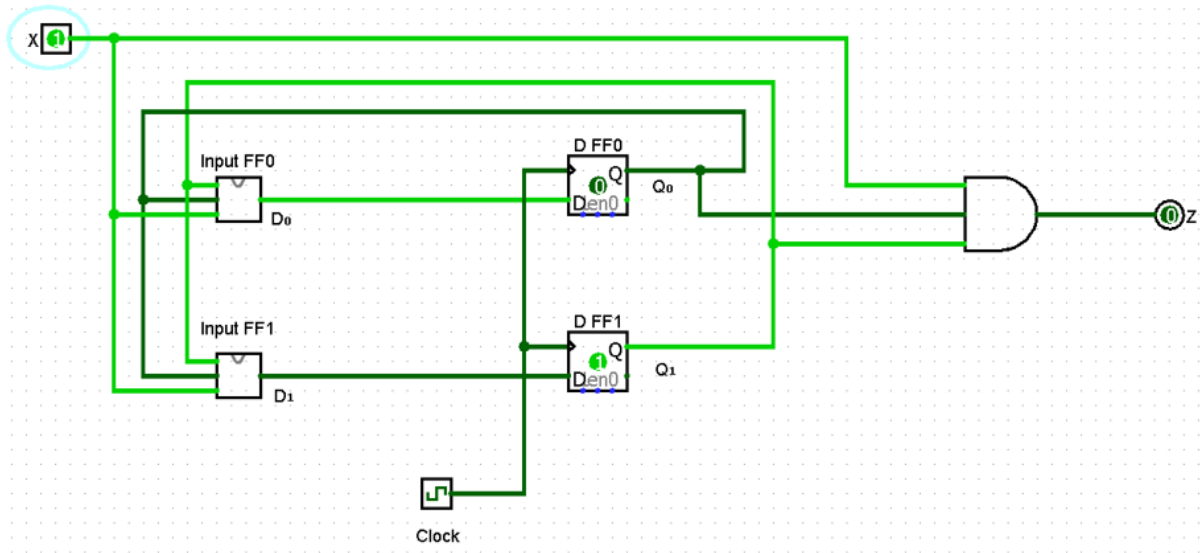
➢ Z = 0. Sequence 1001 is not detected.

Step 4 : Toggle clock



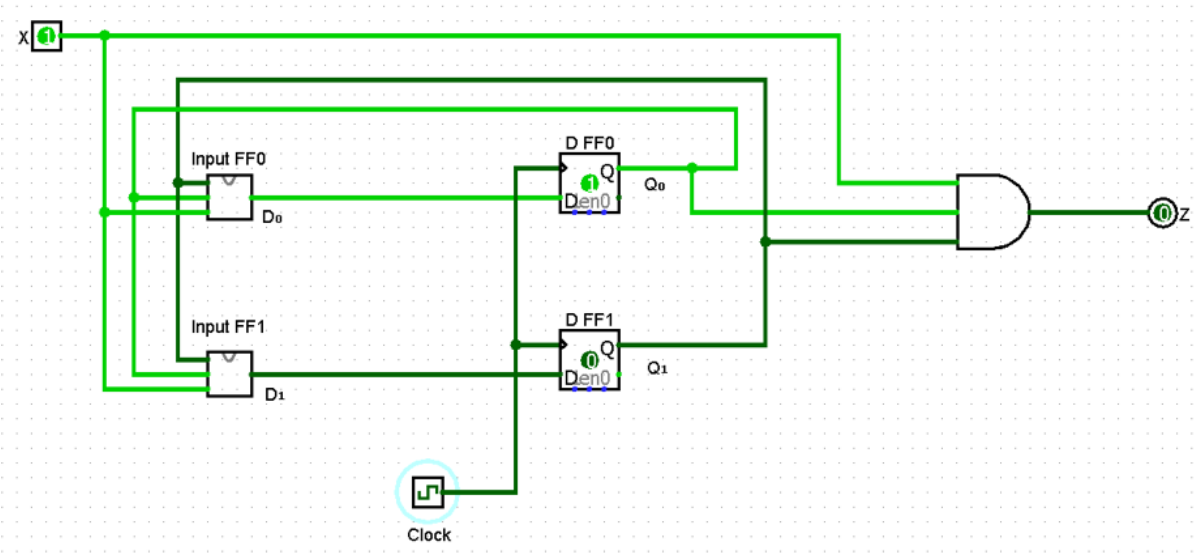
➢ Since Q_1 Q_0 = 10, circuit moves to state C.

Step 5 : Set X = 1 [1011001]



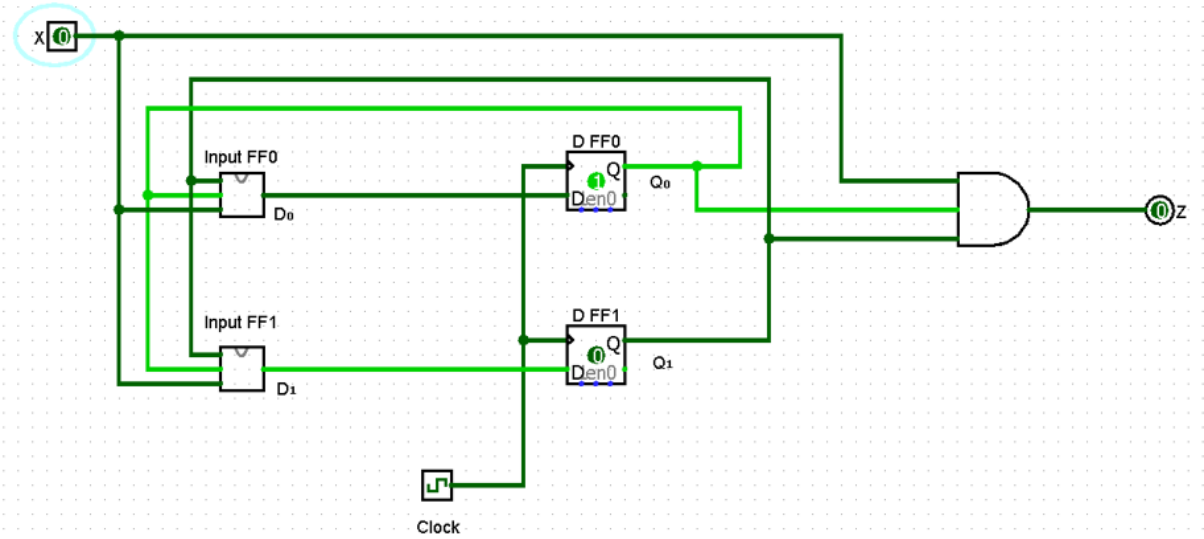
➢ Z = 0. Sequence 1001 is not detected. The sequence 1 has been detected.

Step 6 : Toggle clock



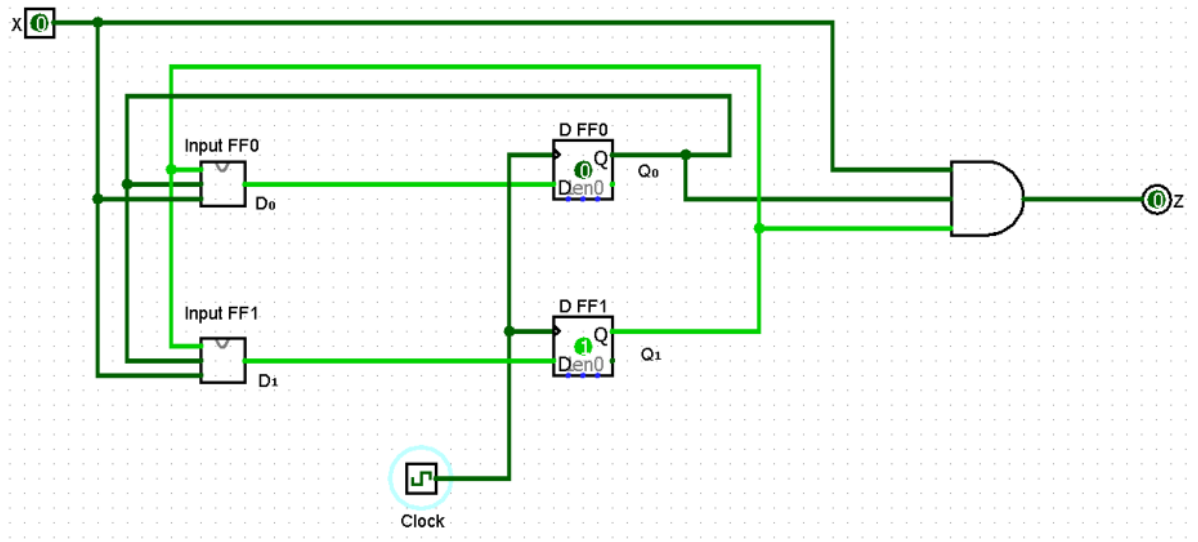
- Since $Q_1\ Q_0 = 01$, circuit moves to state B.

Step 7 : Set X = 0 [101001]



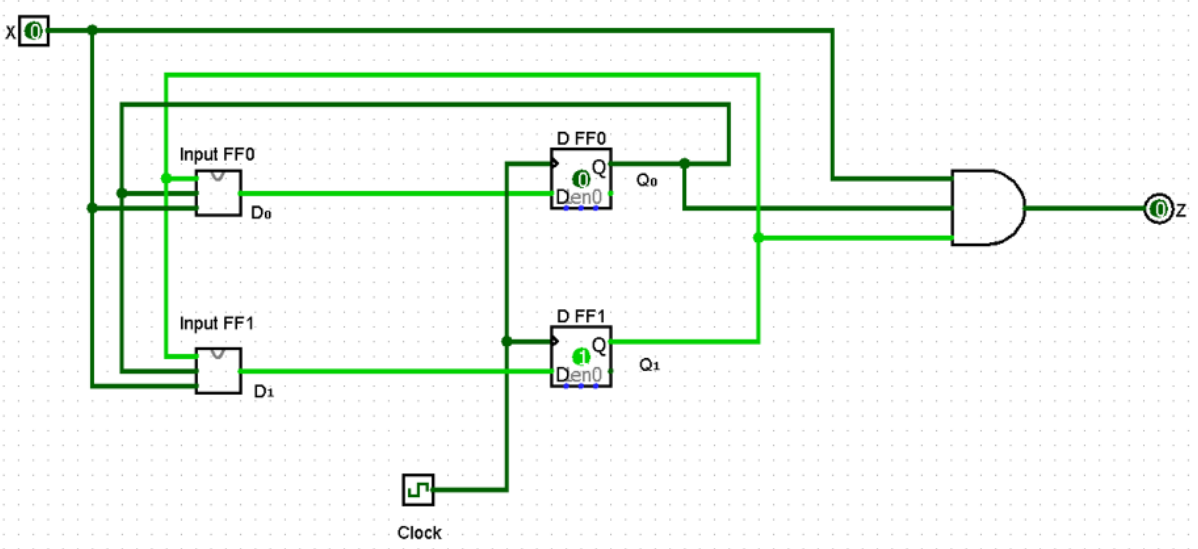
- Z = 0. Sequence 1001 is not detected. The sequence 10 has been detected.

Step 8 : Toggle clock



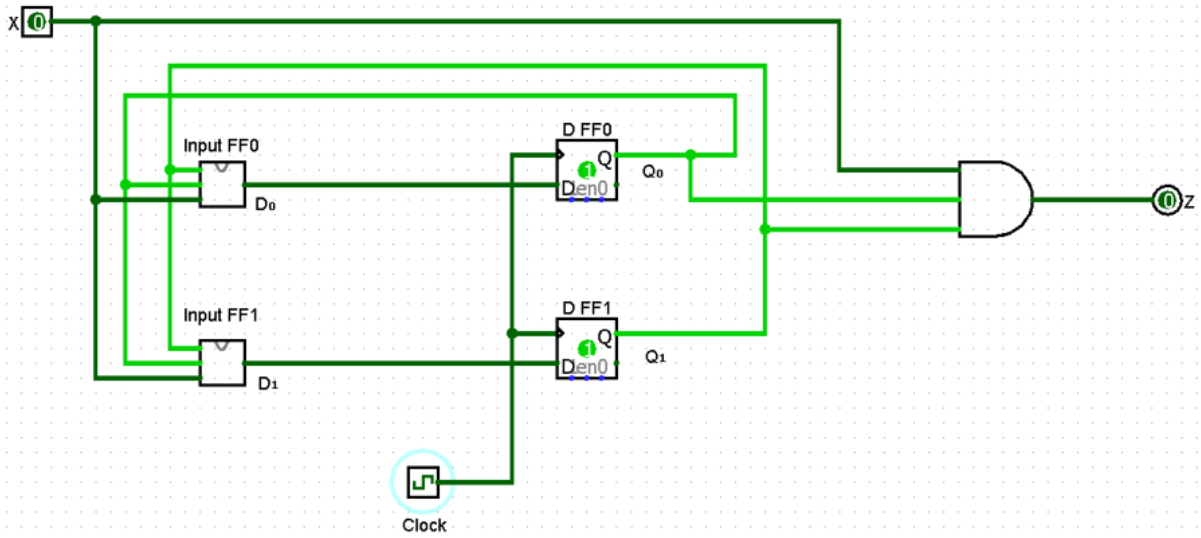
➢ Since Q_1 Q_0 = 10, circuit moves to state C.

Step 9 : Set X = 0 [101001]



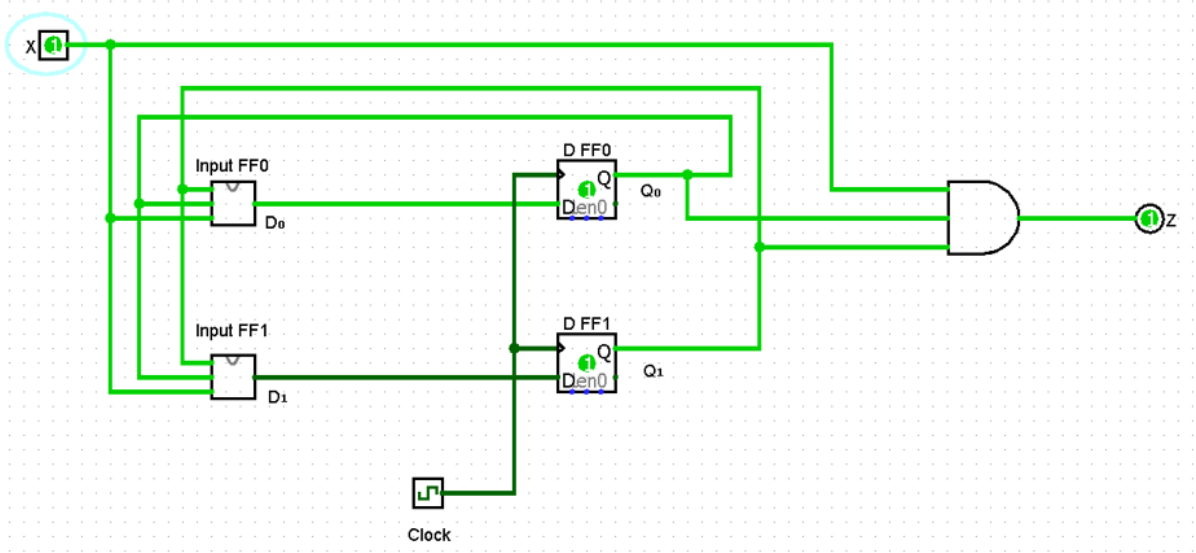
➢ Z = 0. Sequence 1001 is not detected. The sequence 100 has been detected.

Step 10 : Toggle clock



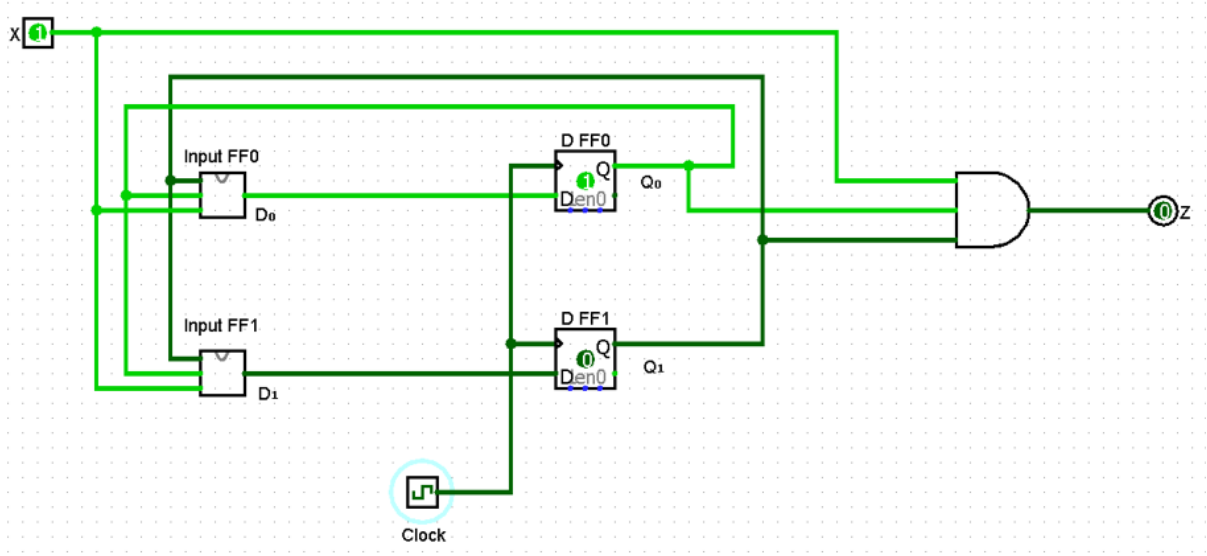
➢ Since Q_1 Q_0 = 11, circuit moves to state D.

Step 11 : Set X = 1 [101001]



➢ Z = 1. Sequence 1001 has been detected.

Step 12 : Toggle clock



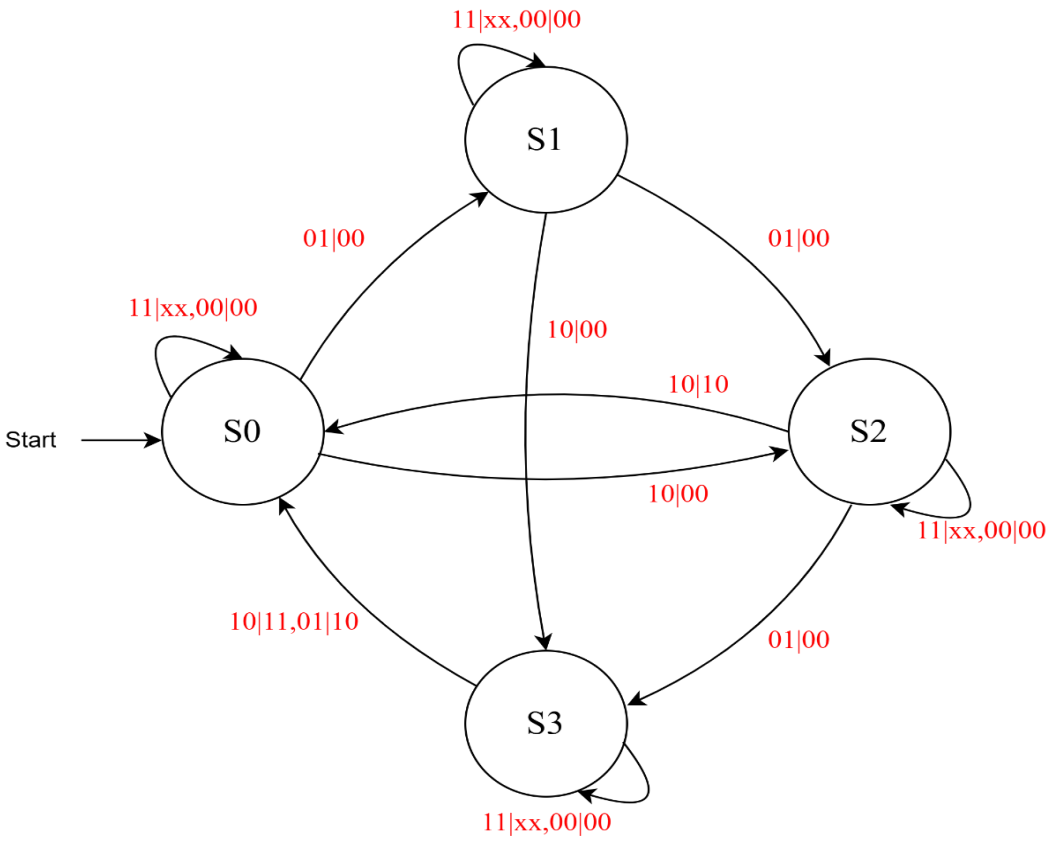
- Since $Q_1\ Q_0 = 01$, circuit moves to state B.

2. Vending machine problem

You are to build a FSM (sequential circuit) for a vendor machine which can take only Rs 10 and Rs 5 coins via a coin slot. The vendor machine has internal mechanisms to deliver a can drink AND/OR change. Assuming a can drink costs Rs 20, build the sequential circuit to control the vendor machine.

2.1 State transition diagram

State	Meaning	Q_1 Q_0
S0	No money has been inserted	0 0
S1	Rs 5 has been inserted	0 1
S2	Rs 10 has been inserted	1 0
S3	Rs 15 has been inserted	1 1



Notation : TF|DC where T = Rs 5 , F = Rs 10 , D = Drink , C = Change

2.2 State table

Present State	Input		Next State	Output	
	T	F		D	C
S0	0	0	S0	0	0
S0	0	1	S1	0	0
S0	1	0	S2	0	0
S0	1	1	S0	X	X
S1	0	0	S1	0	0
S1	0	1	S2	0	0
S1	1	0	S3	0	0
S1	1	1	S1	X	X
S2	0	0	S2	0	0
S2	0	1	S3	0	0
S2	1	0	S0	1	0
S2	1	1	S2	X	X
S3	0	0	S3	0	0
S3	0	1	S0	1	0
S3	1	0	S0	1	1
S3	1	1	S3	X	X

State	Q_1 Q_0
S0	0 0
S1	0 1
S2	1 0
S3	1 1

2.3 Assigned binary code to states

Present State	Input		Next State		Output	
	T	F	Q_1	Q_0	D	C
S0	0	0	0	0	0	0
S0	0	1	0	1	0	0
S0	1	0	1	0	0	0
S0	1	1	0	0	X	X
S1	0	0	0	1	0	0
S1	0	1	1	0	0	0
S1	1	0	1	1	0	0
S1	1	1	0	1	X	X
S2	0	0	1	0	0	0
S2	0	1	1	1	0	0
S2	1	0	0	0	1	0
S2	1	1	1	0	X	X
S3	0	0	1	1	0	0
S3	0	1	0	0	1	0
S3	1	0	0	0	1	1
S3	1	1	1	1	X	X

2.4 Determined flip-flop input values

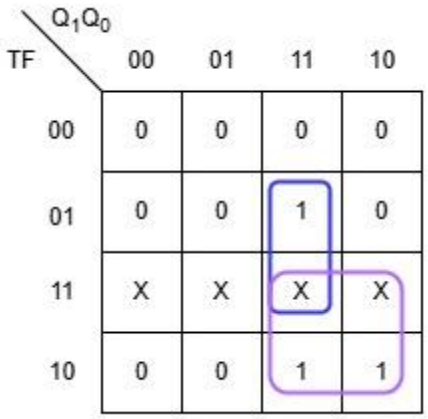
D excitation table :

Q_1	Q_0	D	Operation
0	0	0	Reset
0	1	1	Set
1	0	0	Reset
1	1	1	Set

Present State		Input		Next State		Output		Flip-Flop	
Q_1	Q_0	T	F	Q_1	Q_0	D	C	D_1	D_0
0	0	0	0	0	0	0	0	0	0
0	0	0	1	0	1	0	0	0	1
0	0	1	0	1	0	0	0	1	0
0	0	1	1	0	0	X	X	0	0
0	1	0	0	0	1	0	0	0	1
0	1	0	1	1	0	0	0	1	0
0	1	1	0	1	1	0	0	1	1
0	1	1	1	0	1	X	X	0	1
1	0	0	0	1	0	0	0	1	0
1	0	0	1	1	1	0	0	1	1
1	0	1	0	0	0	1	0	0	0
1	0	1	1	1	0	X	X	1	0
1	1	0	0	1	1	0	0	1	1
1	1	0	1	0	0	1	0	0	0
1	1	1	0	0	0	1	1	0	0
1	1	1	1	1	1	X	X	1	1

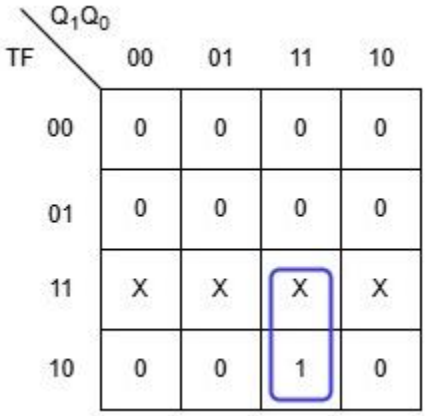
2.5 Karnaugh maps

For D :



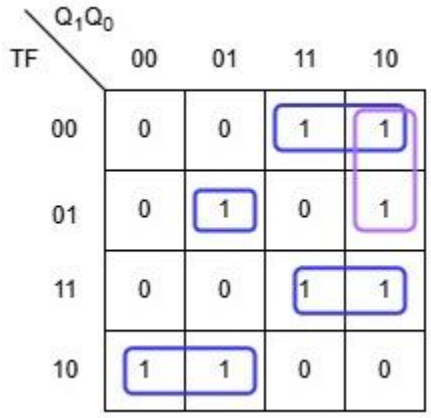
$D = TQ_1 + FQ_1Q_0$

For C :



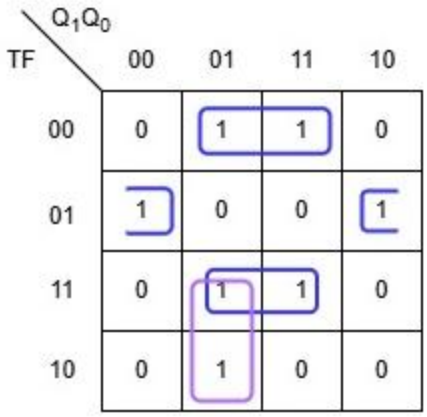
$C = TQ_1Q_0$

For D_1 :



$D_1 = \overline{T}\overline{F}Q_1 + \overline{T}Q_1\overline{Q}_0 + \overline{T}F\overline{Q}_1Q_0 + TFQ_1 + T\overline{F}\overline{Q}_1$

For D_0 :



$D_0 = \overline{T}\overline{F}Q_0 + \overline{T}F\overline{Q}_0 + TFQ_0 + T\overline{Q}_1Q_0$

2.6 Logic circuits

2.6.1 Subcircuits

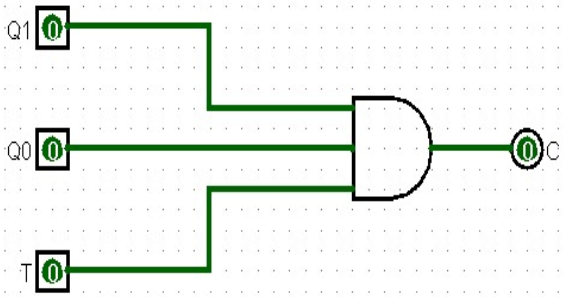


Figure 4 - Output C (Give change)

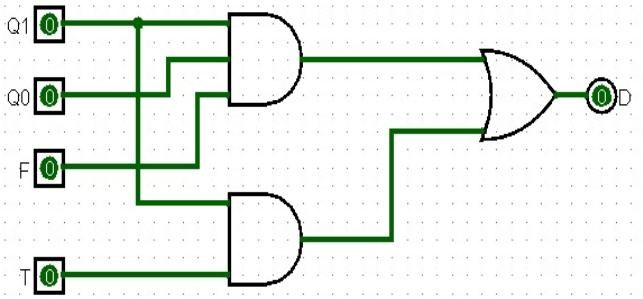


Figure 5 - Output D (Give drink)

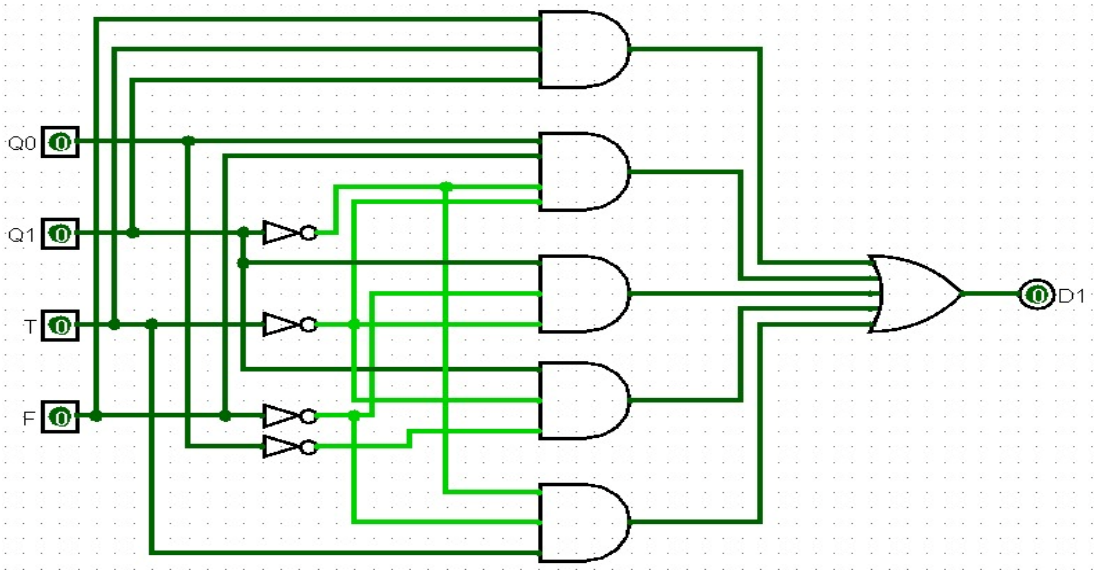


Figure 6 - D Flip-flop 1

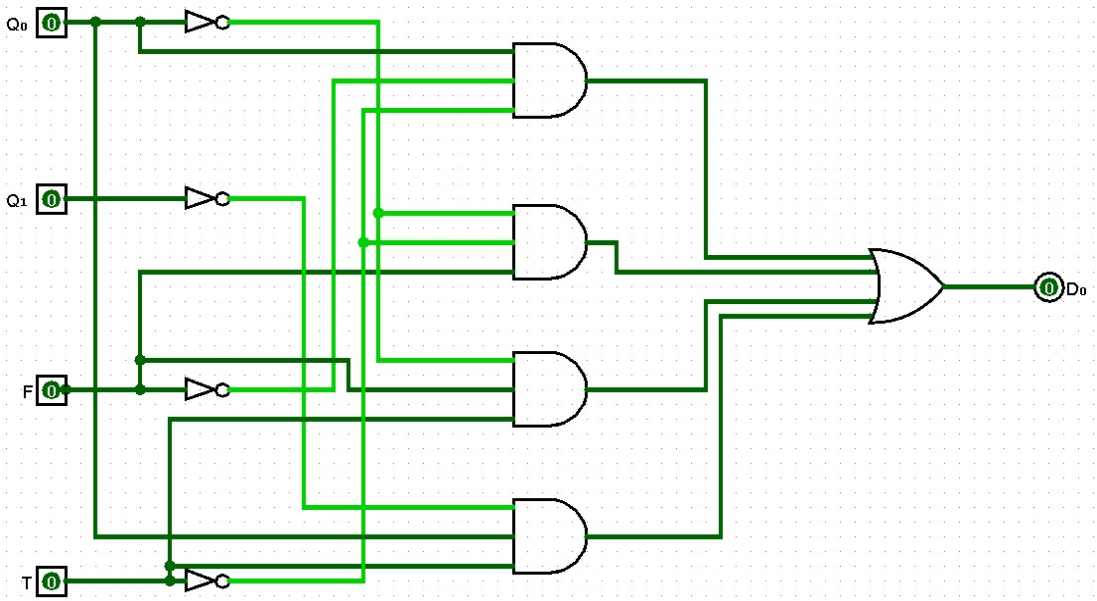
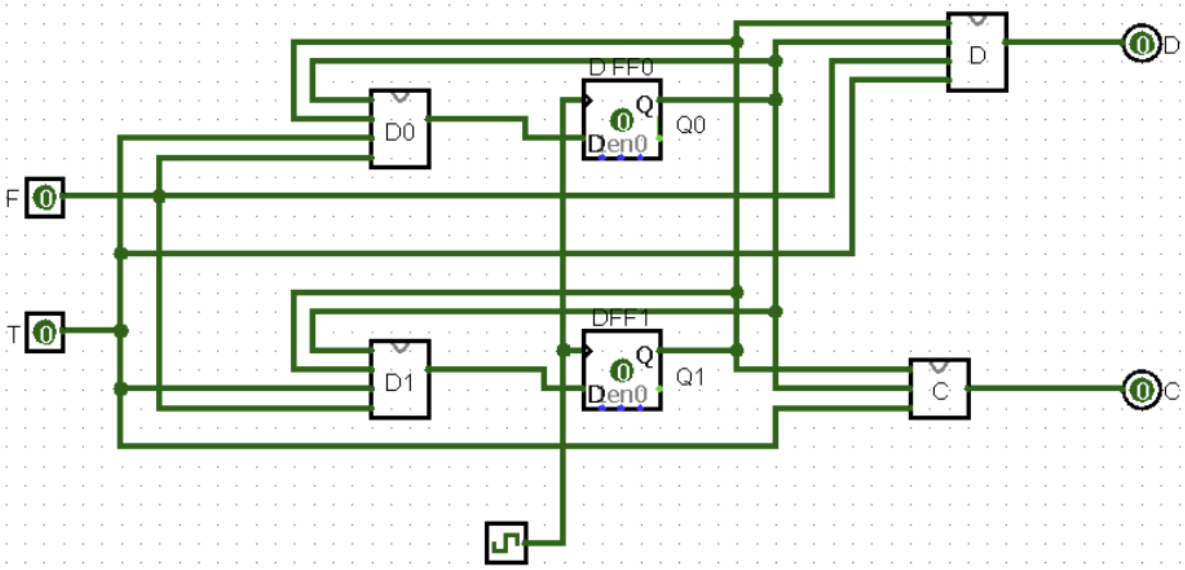


Figure 7 - D Flip-flop 0

2.6.2 Main circuit

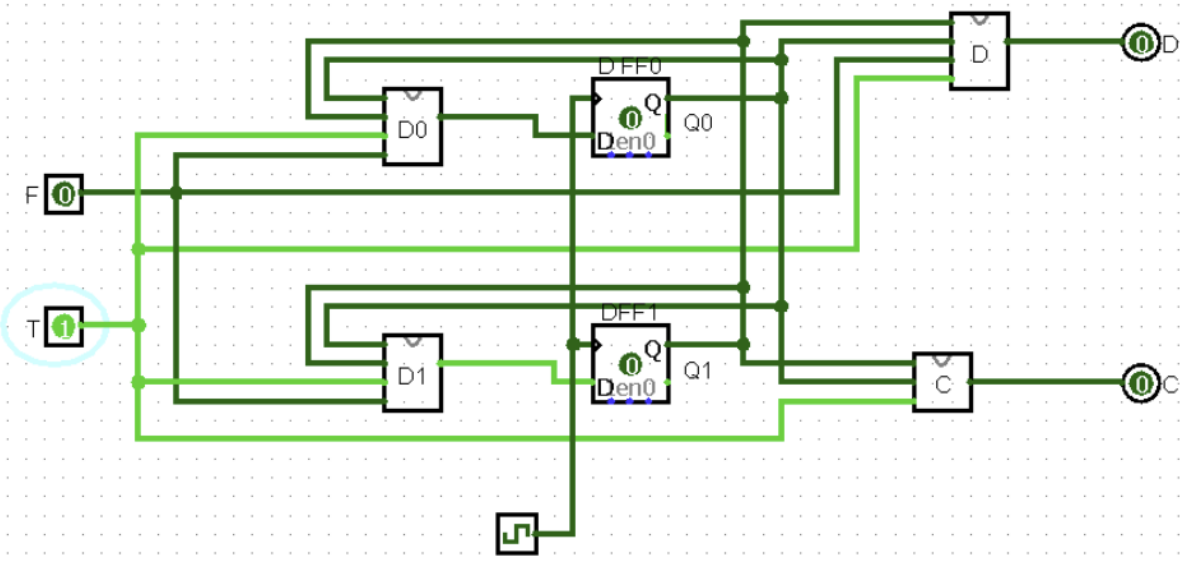
The main circuit consists of two D flip-flops.



2.7 Circuit simulation

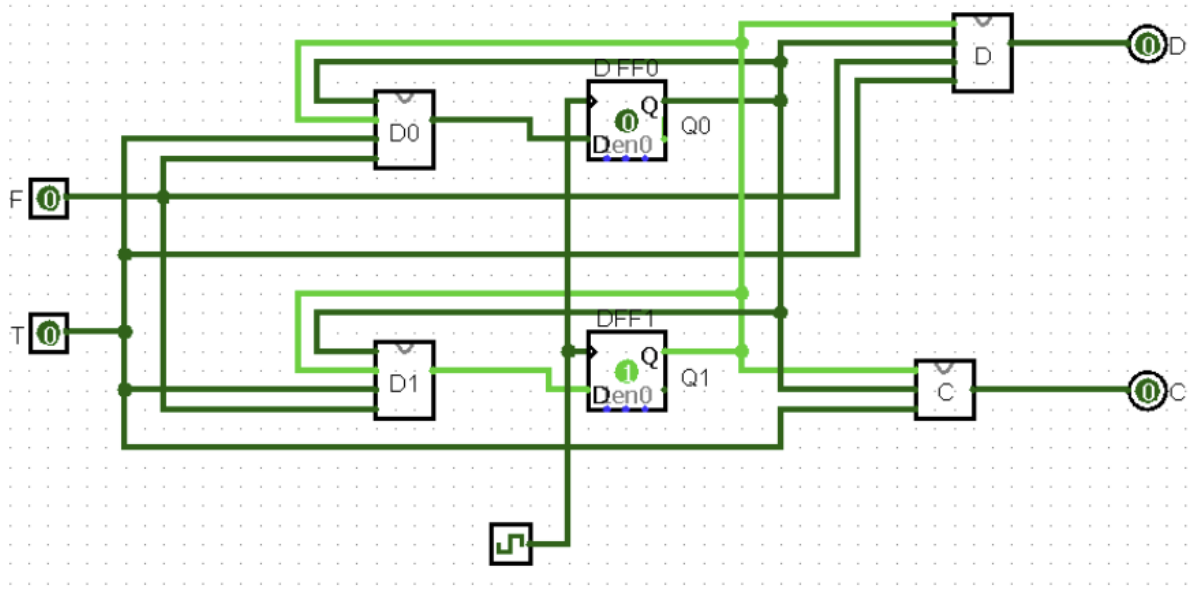
Input test 1 : 10,5,5

Step 1 : Set T = 1 [10,5,5]



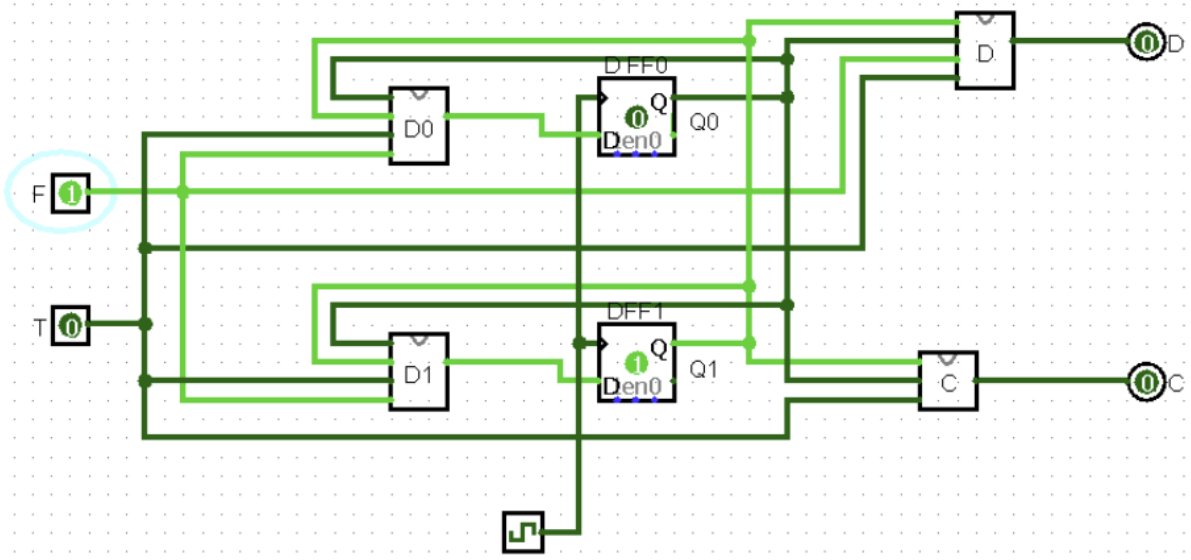
- C = 0 , D = 0. Machine takes no action.

Step 2 : Toggle clock then reset T.



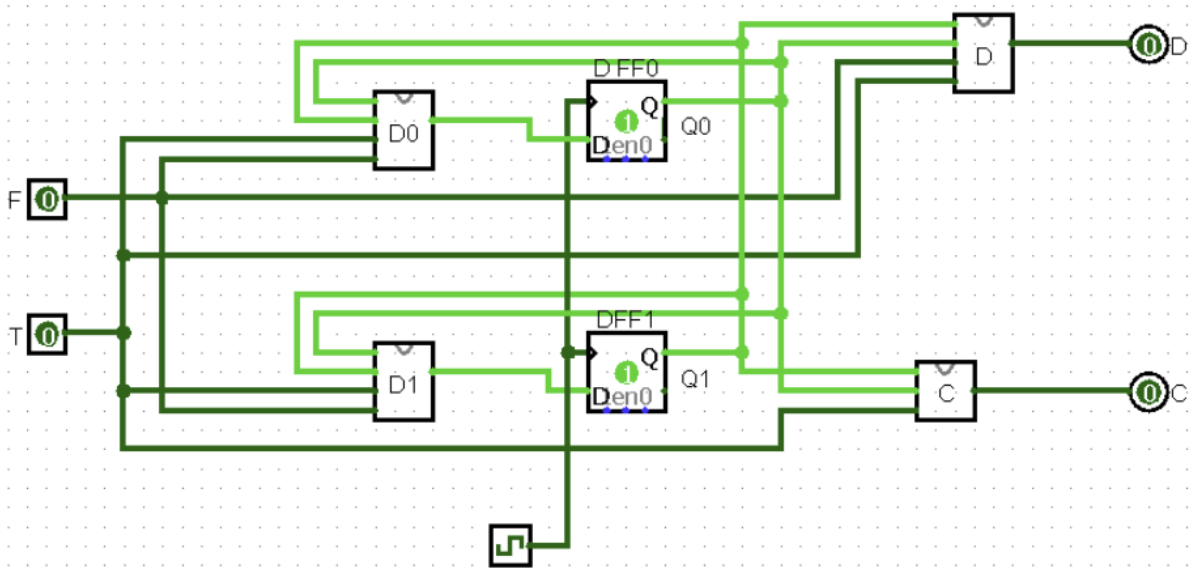
➢ Since Q_1Q_0 = 10, circuit is in state S2.

Step 3 : Set F = 1 [10,5,5]



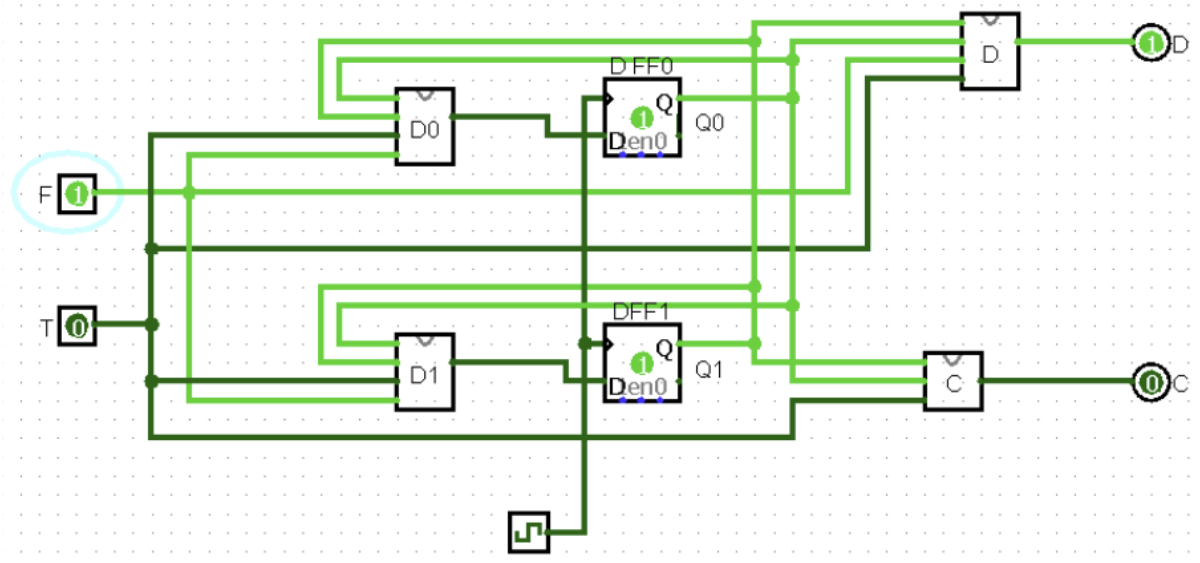
➢ C = 0 , D = 0. Machine takes no action.

Step 4 : Toggle clock then reset F.



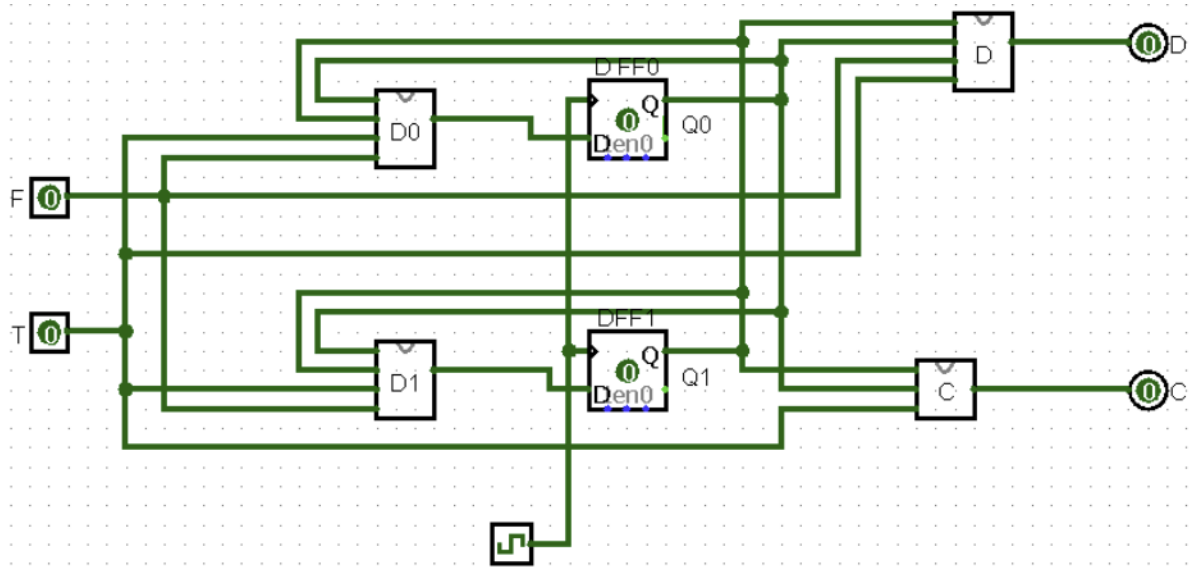
➢ Since $Q_1Q_0 = 11$, circuit moves to state S3.

Step 5 : Set F = 1 [10,5,5]



➢ C = 0 , D = 1. Machine must give drink only.

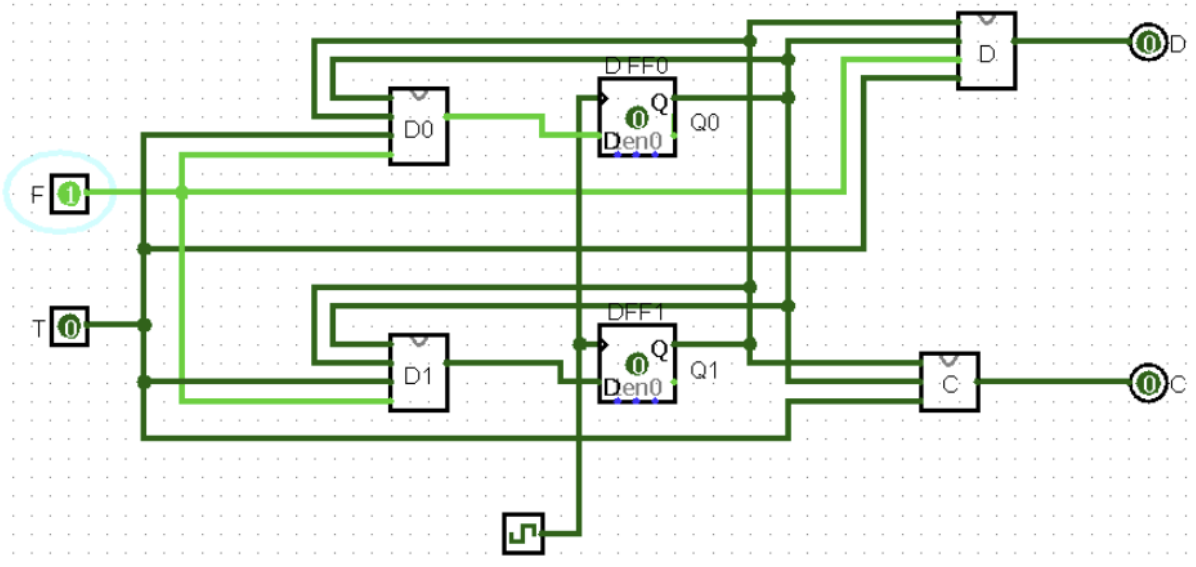
Step 6 : Toggle clock then reset F.



➢ Since $Q_1Q_0 = 00$, circuit moves to state S0.

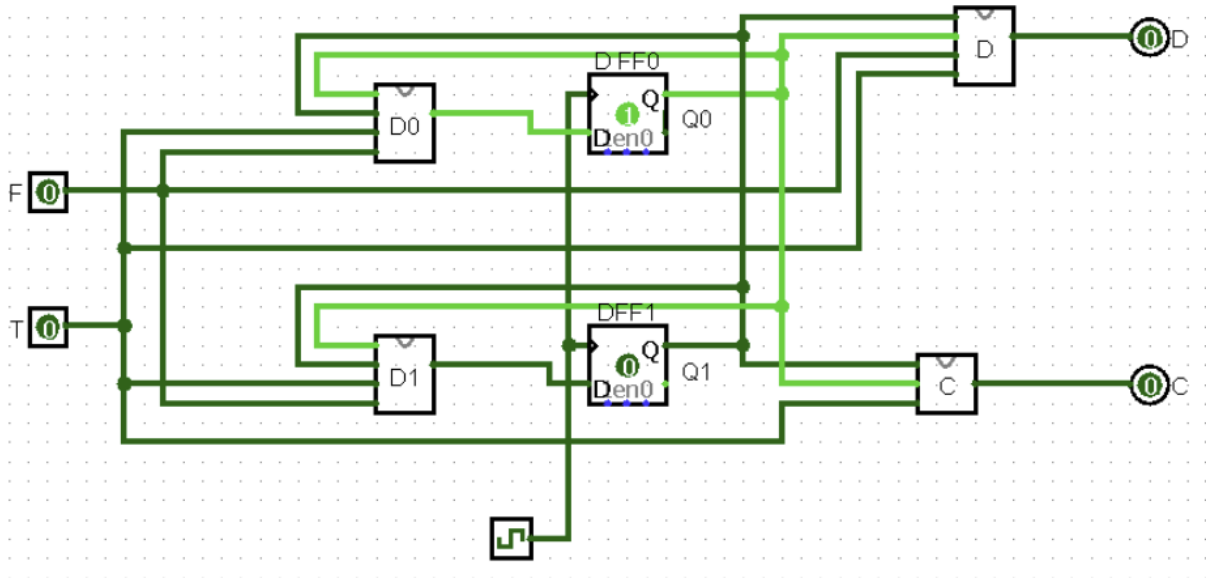
Input test 2 : 5,5,5,10

Step 1 : Set F = 1 [5,5,5,10]



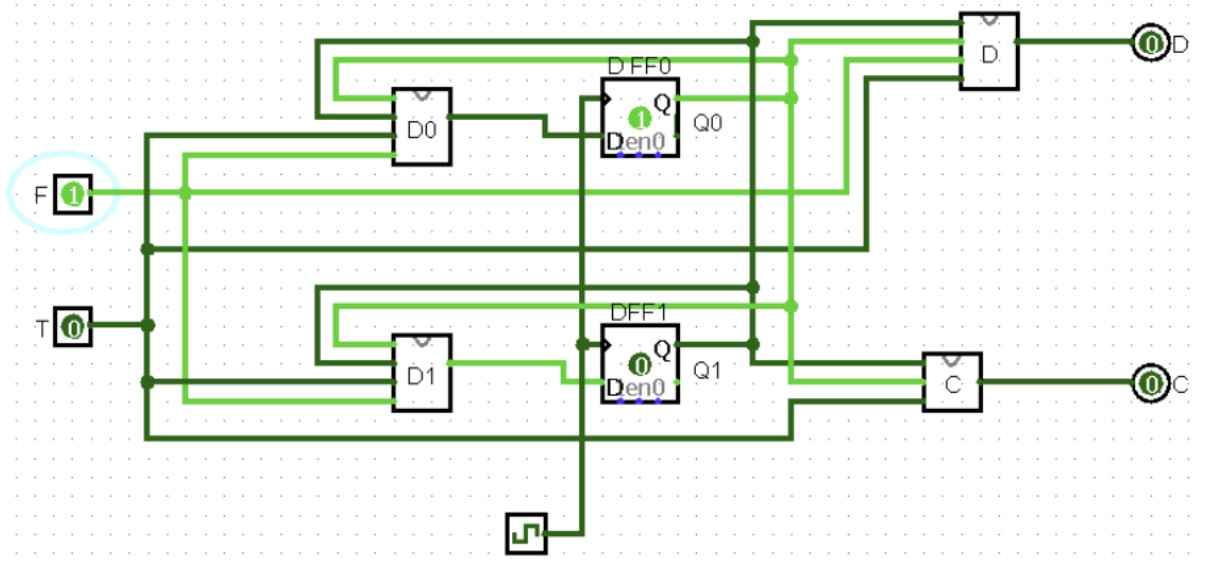
➢ C = 0 , D = 0. Machine takes no action.

Step 2 : Toggle clock then reset F.



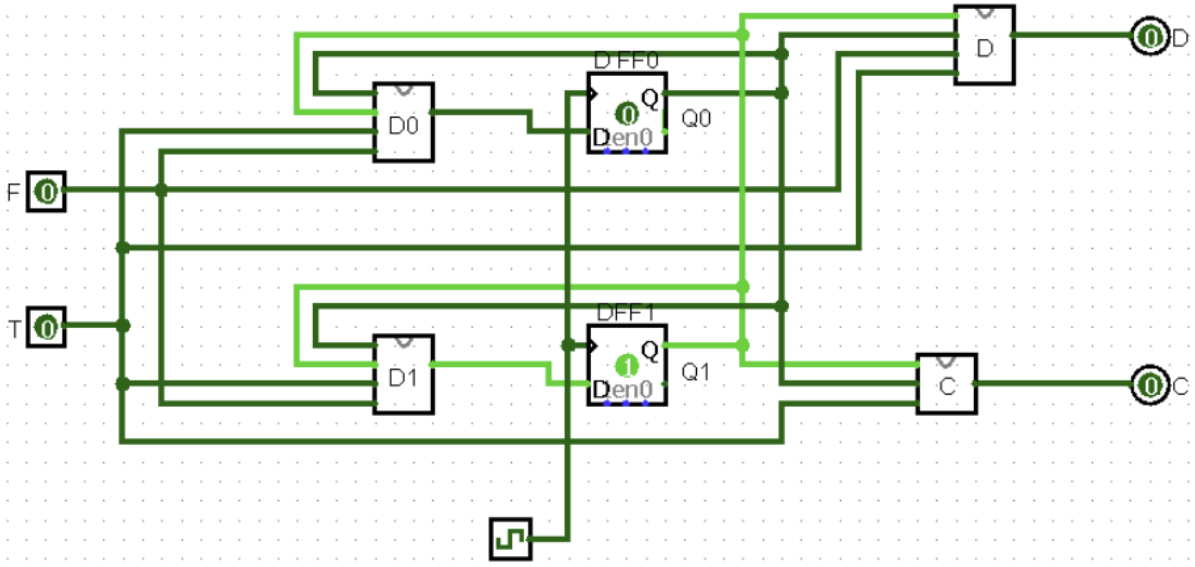
➢ Since $Q_1Q_0 = 01$, circuit is in state S1.

Step 3 : Set F = 1 [5,5,5,10]



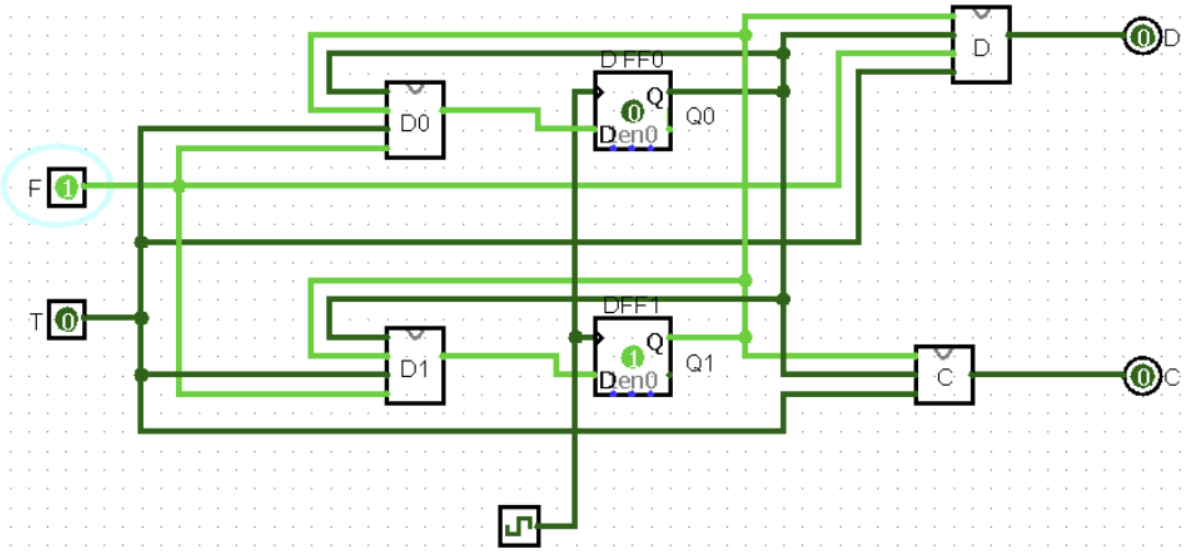
➢ C = 0 , D = 0. Machine takes no action.

Step 4 : Toggle clock then reset F.



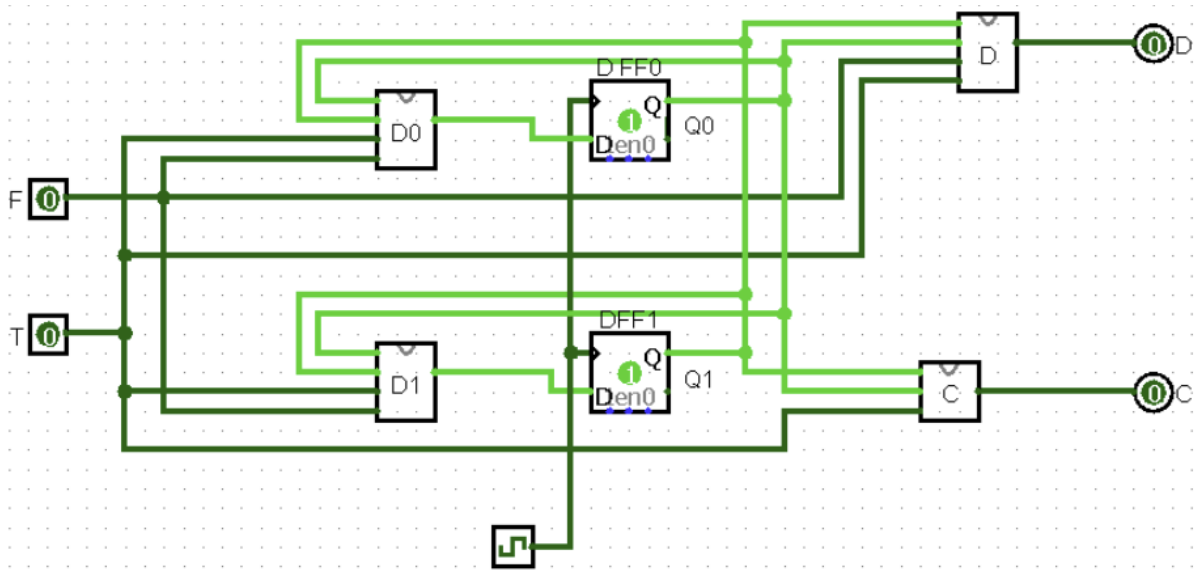
➢ Since $Q_1Q_0 = 10$, circuit moves to state S2.

Step 5 : Set F = 1 [5,5,5,10]



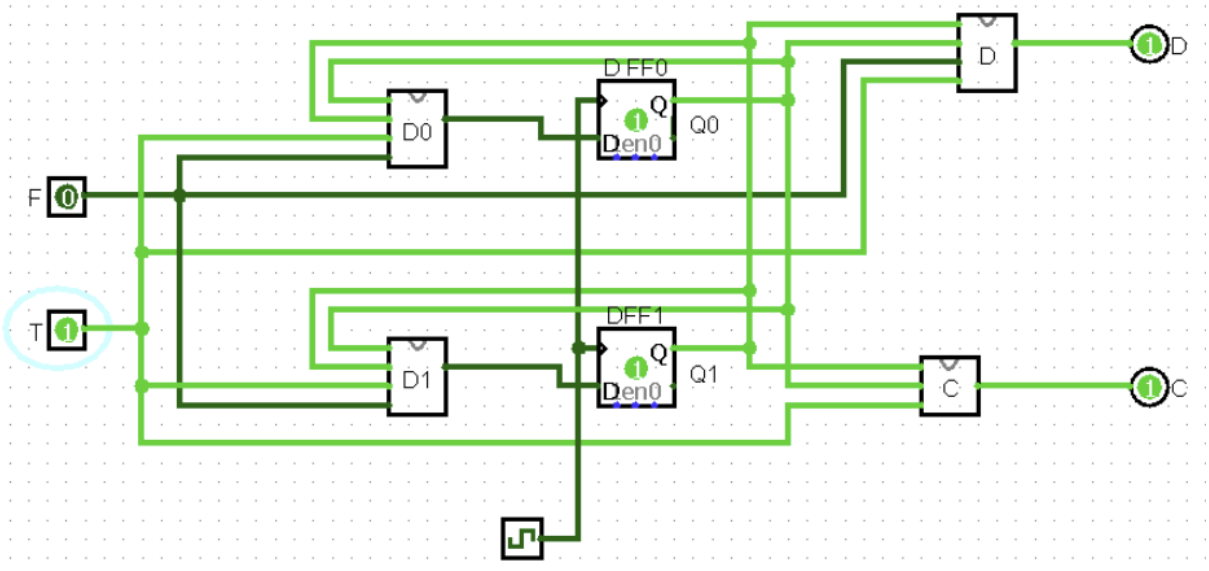
➢ C = 0 , D = 0. Machine takes no action.

Step 6 : Toggle clock then reset F.



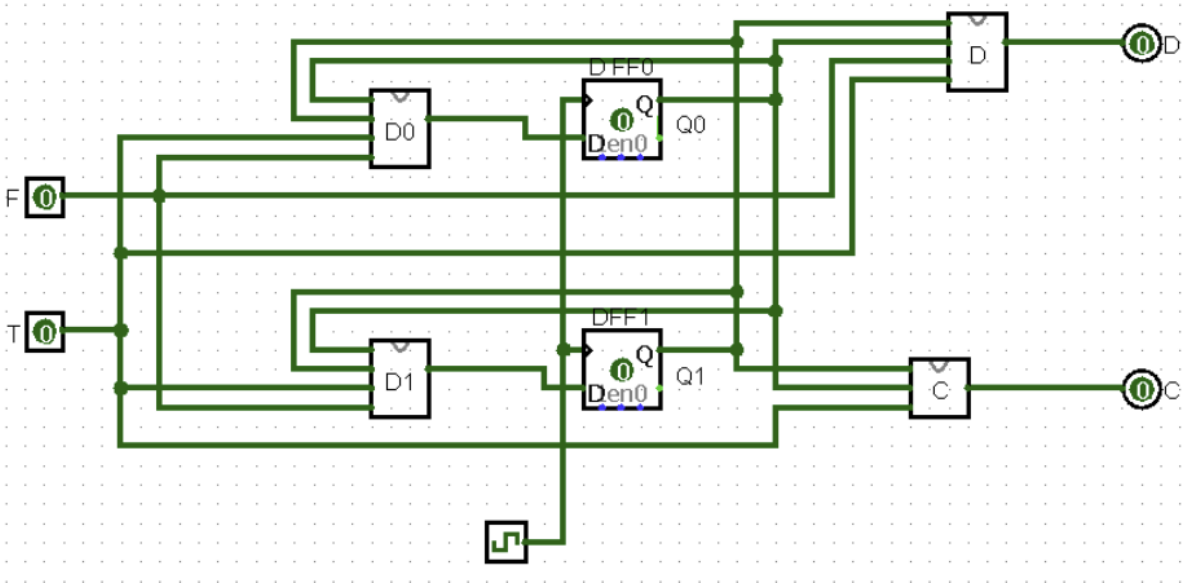
➢ Since $Q_1Q_0 = 11$, circuit moves to state S3.

Step 7 : Set T = 1 [5,5,5,10]



➢ C = 1 , D = 1. Machine must give drink and change.

Step 8 : Toggle clock then reset T.



Since $Q_1Q_0 = 00$, circuit moves to state S0.