## Pokhara University Faculty of Science and Technology

Course No.: CMP 262 Full marks: 100

Course title: Computer Architecture (3-1-1)

Pass marks: 45

Nature of the course: Theory & Practical Total Lectures: 45 hrs

Level: Bachelor - Program: BE (Computer)

### 1. Course Description

This course is designed to provide the knowledge of the evolution of computer architecture and the factors influencing the design of hardware and software elements of computer systems. It aims to provide an understanding of the design of processing unit and control unit architectures. This course introduces the concepts of instruction set design, processor processor organization, pipelining, cache and virtual memory organizations, I/O and interrupts, parallel processing and multicore computers.

#### 2. General Objectives

- To acquaint the students with the knowledge of computer architecture and associated processing, control unit and ALU unit of very simple central processing unit.
- To provide the knowledge of the functions of each element of memory hierarchy.
- To develop the skills in students to choose the appropriate Memory and Input Output organization used in real world computing systems.
- To acquaint the students with the knowledge of technology behind modern advanced computer architectures for parallel processing and multicore architecture.

#### 3. Methods of instructions

Lectures, Tutorials, Case Studies, Discussion, Readings and Practical Works.

#### 4. Content in details

	Specific objectives	Contents
(1)	<ul> <li>Understand the concepts of computer</li> </ul>	Unit 1 Introduction to Architecture [4 Hrs] U2 Marks 1.1.Brief overview of Computer organization and Architecture
	various addressing modes.	1.2.Hierarchy structure of computer system 1.3. Computer evolution and generations
	*IAS	1.4. Computer Components and Functions 1.5. Future Trends in Computer
		1.6. Review of Instruction sets. Addressing Modes and Instruction format

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(-	Understand the VHDL Programming	
	for simple operations.	operations [411rs] (8 Mayus)
		2.1 Register Transfer and RTL
		2.2.Micro Operation
		2.3 Data Transfer Micro Operations
	1	2.4 Arithmetic and Logical Operations 2 Program
		2.5 Shift Micro operations
	1	2.6 Introduction to HDL and VHDL
_		2.7 VIIDI programming for Adder, Mux, ALU
3	<ul> <li>Understand the functional units of</li> </ul>	Unit -3: Processor Organization [5 Hrs] (13 mores
•	CPU and their organization.	3.1CPU Organization/Structure
		3.2 Register Organization and Data paths
		3.3 Instruction Cycle(T states)
	1	3.4 Arithmetic and Logical Unit
		3.5 Design Principles for Modern Systems
$_{\odot}$	<ul> <li>Understand the design of Hardwired</li> </ul>	UNIT 4 Control Unit [5 Hrs] ( 14 Marks)
	and microprogrammed control units.	4.1 Control of the processor
		4.2 Hardwired Control Unit(Control unit inputs/logic)
		4.3 Microinstruction Format
	1	4.4 Micro Programmed Control Unit
		4.5 Architecture of Microprogrammed Control Unit
		4.6 Microinstruction Sequencing and Execution
		4.7 Application of Hardwired and Micro programmed
		Control Units
_		4.8 RISC and CISC Architecture
0	<ul> <li>Understand the representation of</li> </ul>	UNIT 5 Computer Arithmetic [7 Hrs.] (15 mares)
	binary numbers in signed and unsigned	5.1 Integer Representation
i	notation along with the algorithms	5.2 Integer Arithmetic
- 1	used for the basic arithmetic	5.3 Unsigned Binary Addition and Subtraction
- 1	operations.	5.4 Unsigned Binary Multiplication Algorithm
- 1	Farming	5.5 Booth Multiplication Algorithm
		5.6 Unsigned Binary Division Algorithm
		5.7 Floating Point Possessess
0 1	Understand the concents of pinclining	5.7 Floating Point Representation
ין ש	the concepts of pipelining	Unit 6: Pipelining [4 hrs] (8 marks) 6.1 Pipelining
- 1	for better performance.	6.2 Arishmania Promis
		6.2 Arithmetic Pipeline
- n   h	1 "	6.3 Instruction Pipeline
- 1		6.4 Conflicts in Instruction Pipelining and their
- 1		solutions
		6.5 RISC pipeline
-		6.6 Register Windowing and D.
	Review memory Hierarchy of	UNIT 7 Memory Organization [4 Hrs.] (2 marz)
	computer systems and understand the	7.1 Memory Hierarchy
100	nrinciples of cache moments to	7.2 Main Manager
	principles of cache memory to increase	7.2 Main Memory and Auxiliary Memory
		7.3 Associative Memory and Cache Memory 7.4 Cache mapping techniques- Direct, Associative
		7.4 Cache manning tools 1

# Block diagram -> pencil scale.

<ul> <li>Familiarize with IO interfaces and introduce various methods for improving I/O performances.</li> <li>Understand the concept of parallel processing and multi thread architecture in modern processors.</li> </ul>	<ul> <li>9.2 Parallelism In Uniprocessor system</li> <li>9.3 Multiprocessor System and their characteristics</li> <li>9.4 Flynn Classification</li> <li>9.5 Interconnection structures in Multiprocessors</li> <li>9.6 Vector processing and Array processing</li> <li>9.7 Introduction to Multithreaded Architecture</li> <li>Unit 10: Multi-core computer (4Hrs) [7] marks</li> </ul>
Prevalent new development in computer architecture: the use of multiple processors on a single chip	0.7 Introduction to Multithreaded Architecture