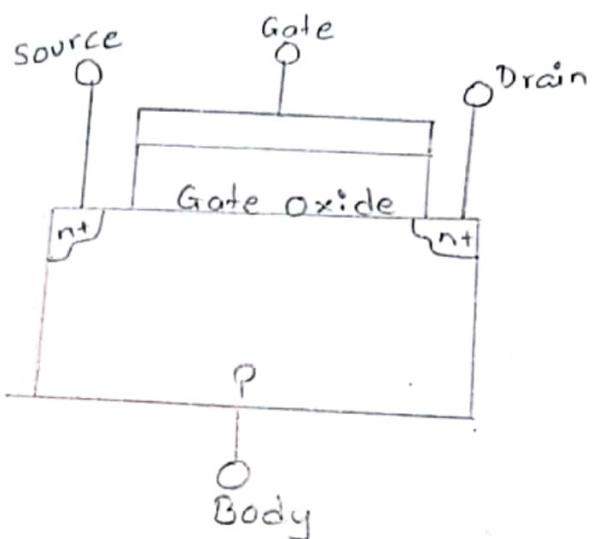
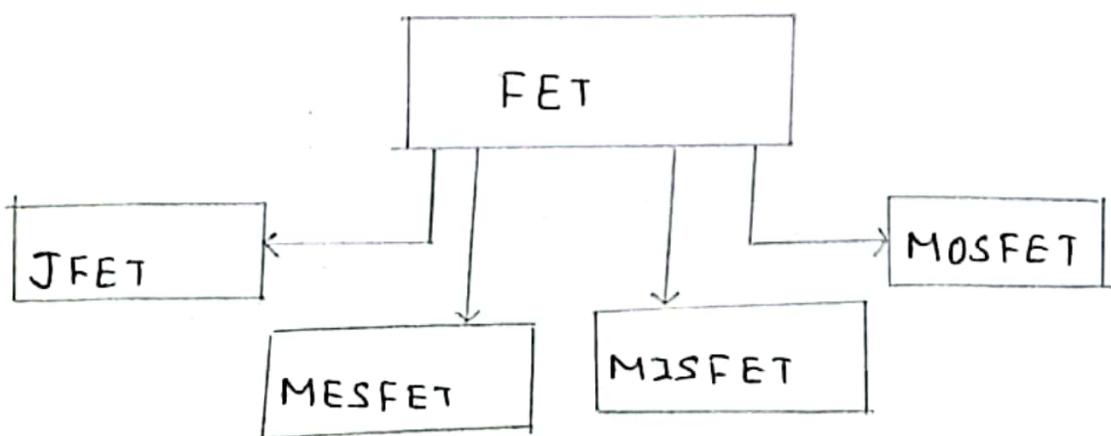


FET (Field Effect Transistor)

- It is a voltage controlled device
- It consists of three terminal
 - i) Gate
 - ii) Source
 - iii) Drain

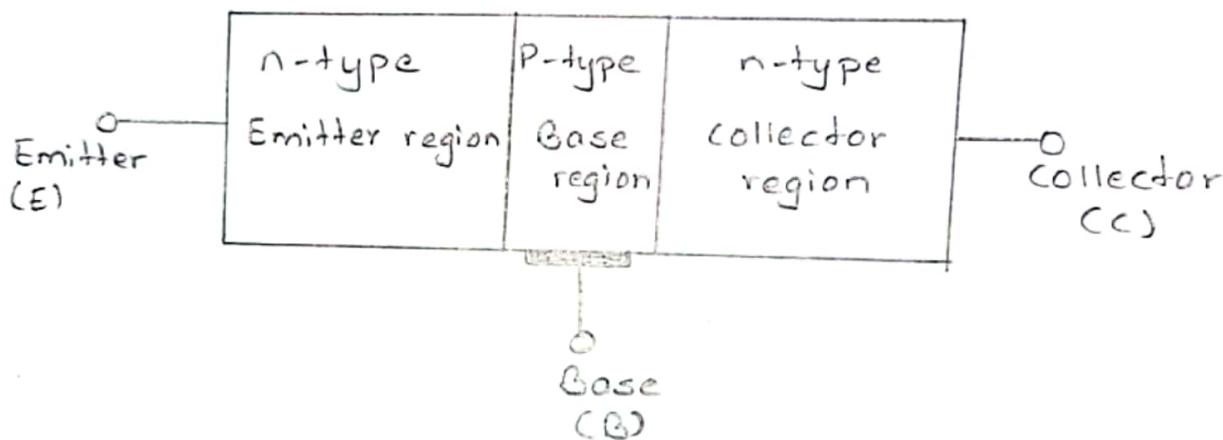


- They are preferred in High frequency and Low-voltage application.
- It is classified as four types.



BJT (Bipolar Junction transistor)

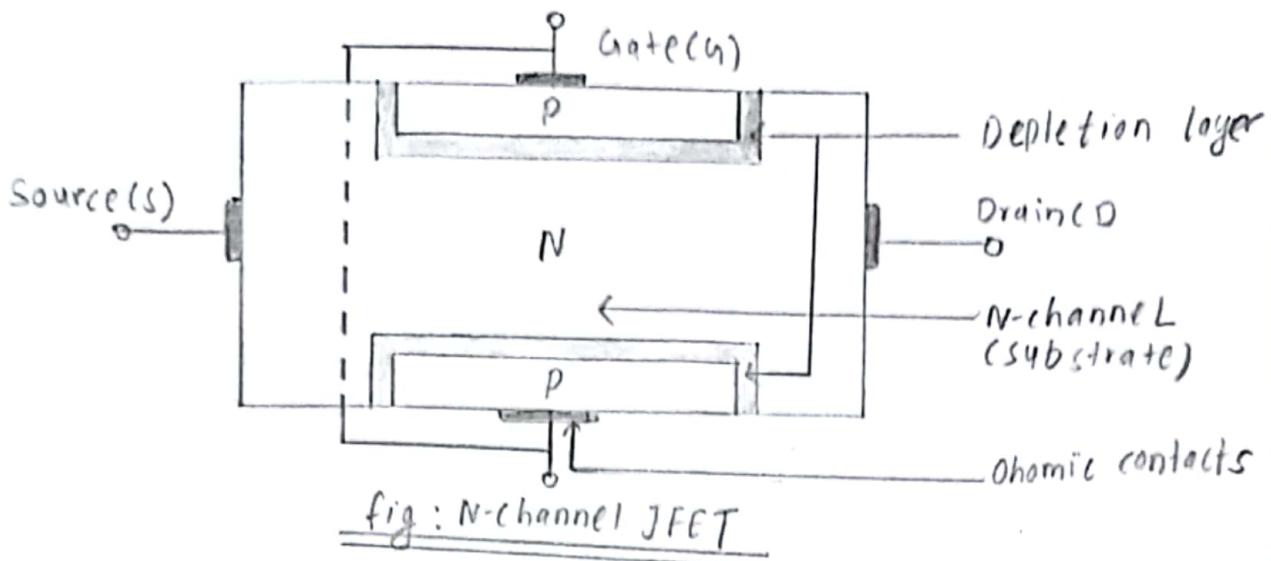
- It is three terminals current controlled active device. It is called Bipolar as it lies on the two types of charge carries
- BJT consist of a layer of p type si(or Ge) Sandwiched between two layer of n type Si (or Ge) called n-p-n Transistor.



1 Comparison between FET and BJT

Bipolar Junction Transistor	Field Effect Transistor
1) BJTs are preferred for low current applications.	FETs are preferred in low-voltage applications.
2) BJTs are current controlled. They require a biasing current to the base terminal for operation.	FETs are voltage-controlled. They only require voltage applied to the gate to turn the FET either on or off. They don't require a biasing current for operation.
3) BJTs offer greater gain at the output than FETs.	FETs' gains output gains are smaller than BJTs.
4) BJTs are larger in size and take more physical space than FETs.	FETs can be manufactured much smaller than BJTs.
5) They are cheaper to manufacture.	They are more expensive to manufacture.
6) They are less popular	They are more popular and widely used in commercial circuits today.
7) BJTs have low-medium input impedance.	No current flows through the gate, the input impedance of the FET is extremely large.
8) A BJT will consume more power in the on-state. It cannot switch with less than a 0.3V voltage drop.	FETs are preferred in load variations & have low power consumption.

CONSTRUCTION OF JFET



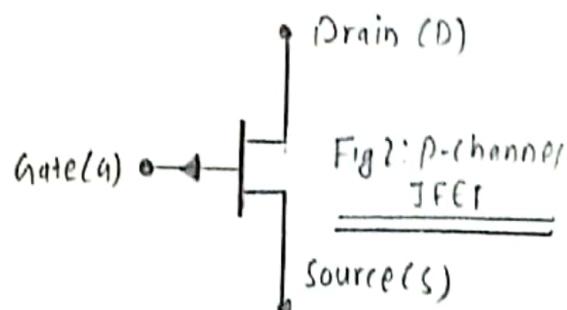
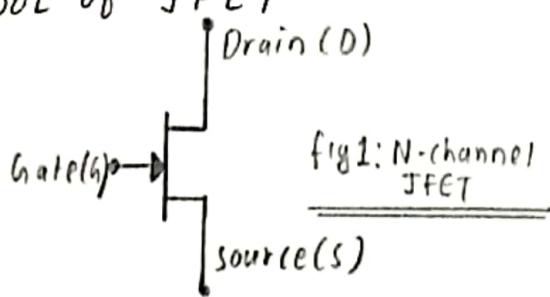
In a N-channel JFET, the substrate (base) is of N-type, and the gates are made of P-type, while in P-channel JFET, substrate is P-type and gate is of N-type. JFET is made of a long channel of semiconductor material of base layer. As a JFET is unipolar, N-type consists of electrons as conducting medium and P-channel consists of holes as medium. Ohmic contacts are provided at each end of semiconductor channels to form source drain connection.

Source: The terminal through which the majority charge carriers enter the channel, is called Source (S)

Drain : The terminal through which the majority charge carriers leaves the channel, is called Drain (D).

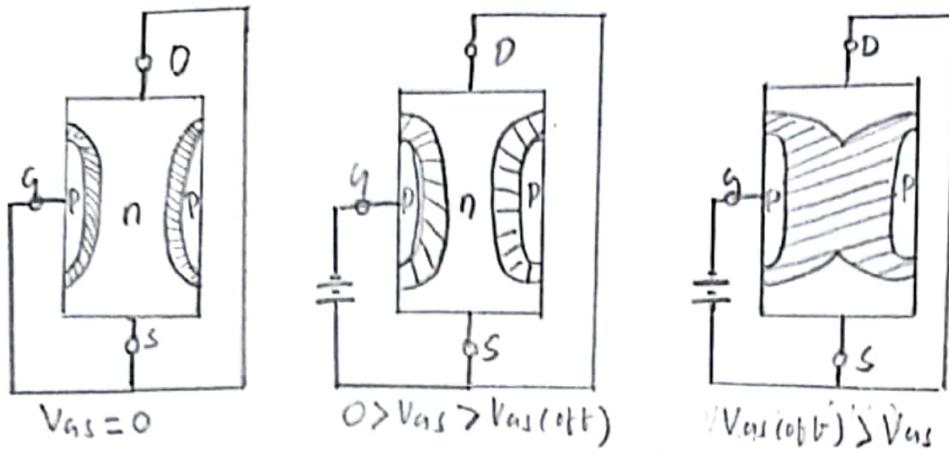
gate : The two internally connected heavily doped impurity regions to create two P-N junctions is called gate(G).

Symbol of JFET



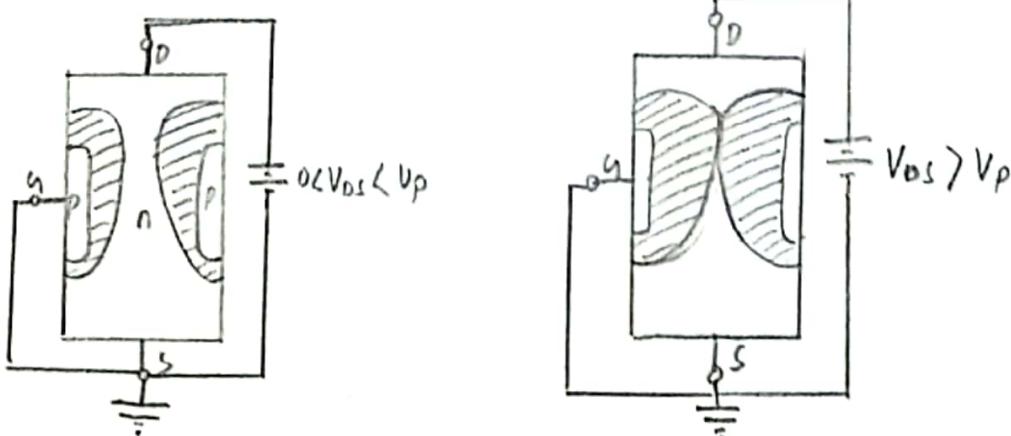
Theory of Operation

1) When gate-source voltage (V_{GS}) is applied ($V_{GS} < 0$) and drain-source voltage is zero i.e. $V_{DS} = 0$



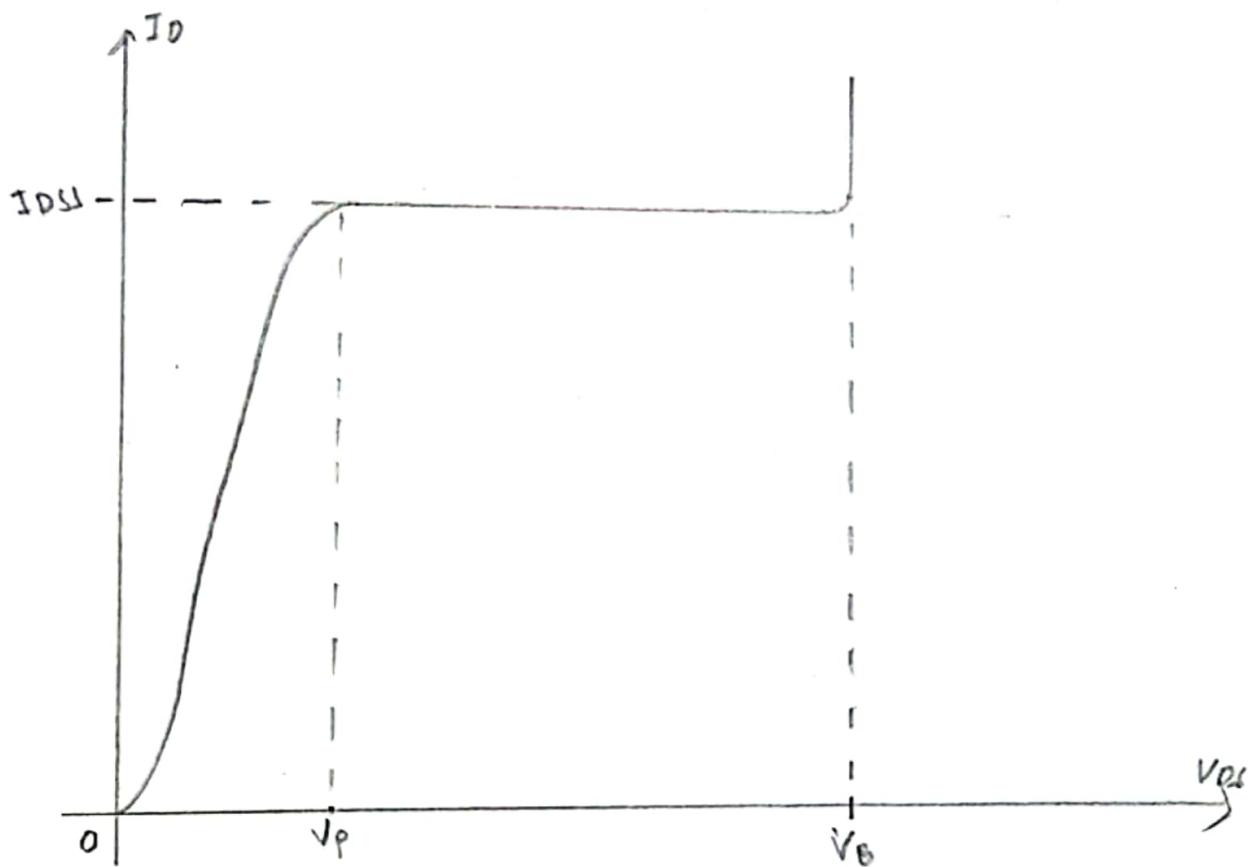
- When $V_{GS} = 0V$, two depletion layers and channels are formed normally.
- When V_{GS} increase negatively i.e. $0 > V_{GS} > V_{GS(\text{off})}$ [Here negatively because gate and source are reverse biased i.e. source is always at higher potential than gate so $V_{GS} = -ve$] depletion layer increase and channel width decrease.
- When $V_{GS(\text{off})} = V_{GS}$, the channel will be completely blocked so there is no flow of current between source(s) and Drain(D)

2) When gate-source voltage is zero ($V_{GS} = 0$) and drain source voltage is applied



- V_S is grounded zero (0) as source(s) is grounded so, $V_{DS}=0$.
 $V_D > 0$ so, depletion layer is wider towards the drain end.
- When V_{DS} increases i.e. $0 < V_{DS} < V_P$, depletion layer towards drain gradually increases and drain current also increases in the beginning
- When $V_{DS} = V_P$ (pinch-off voltage) the channel is effectively closed and I_D remains constant from that point
- If V_{DS} is increased further, the current I_D remains constant only breakdown occurs, when I_D increases rapidly

Characteristic curve



$I_{DSS} = I_D$ saturation value

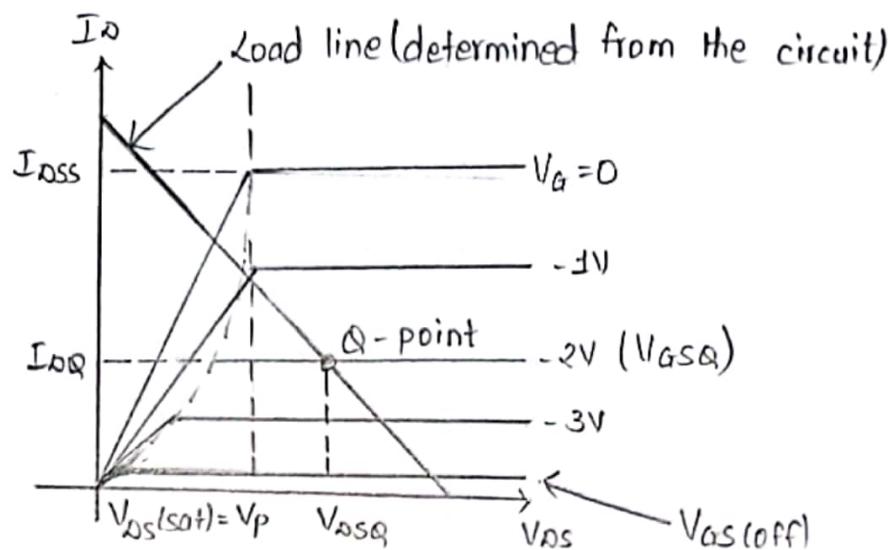
V_P = pinch-off voltage

V_B = Breakdown voltage

- When $V_{GS} = 0$ [Here V_{GS} is kept constant i.e. 0], $V_{DS} = 0$ then I_D is also zero
- When V_{DS} is increased, I_D increases linearly i.e. it follows Ohm's law.
- After increasing initially, I_D experiences some resistance. As V_D increases, the depletion layer becomes wider narrowing the channel, resisting the current flow.
- When $V_{DS} = V_P$ (pinch-off voltage), the I_D becomes nearly constant i.e. $I_D = I_{DSS}$
- If V_{DS} is further increased, I_D remains constant until V_{DS} reaches breakdown voltage (V_B) after which current rises rapidly.

Load line and Q-point

A loadline connects 2 points on the drain characteristics. One point is on the I_D axis and the other is on the V_{DS} axis. For a known V_{GS} , the intercept point between the load line and the drain curve can determine the operating/quiescent (Q) point and consequently, the I_{DQ} and V_{DSQ} .



The load line is used to analyze and design FET circuits. The slope of the load line is determined by the value of the load resistance, while the intercept of the y-axis is determined by the power supply voltage.

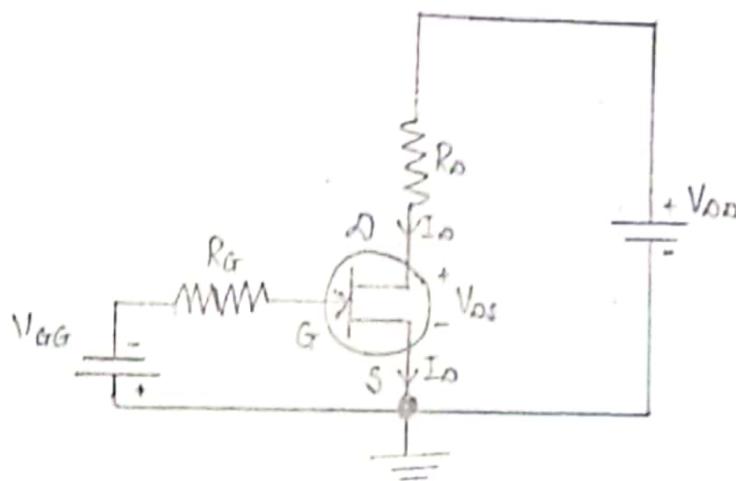
Biassing in a Field Effect Transistor(FET) refers to the process of applying a DC voltage to the gate terminal of the transistor in order to establish a stable operating point for the device.

The gate voltage controls the conductivity of the channel between the source and drain terminals of the FET. By applying a positive voltage to the gate terminal with respect to the source, the FET is turned on and current flows through the channel. Conversely, if a negative voltage is applied to the gate terminal, the FET is turned off and the channel current is minimized.

There are several methods of FET biasing, including:

Fixed Biasing:

In this method, a fixed voltage is applied to the gate terminal with respect to the source. This establishes a constant DC voltage across the channel and creates a stable operating point for the FET.



To determine the Q-point (I_{DQ} and V_{DSQ}), the relationship between the I_D and V_{DS} needs to be known.

looking at the output loop (loop 1 - drain characteristic):

$$-V_{DD} + I_D R_D + V_{DS} = 0$$

$$I_D = \frac{V_{DD} - V_{DS}}{R_D} = -\frac{1}{R_D} V_{DS} + \frac{V_{DD}}{R_D}$$

This expression is in the form of $y = mx + c$

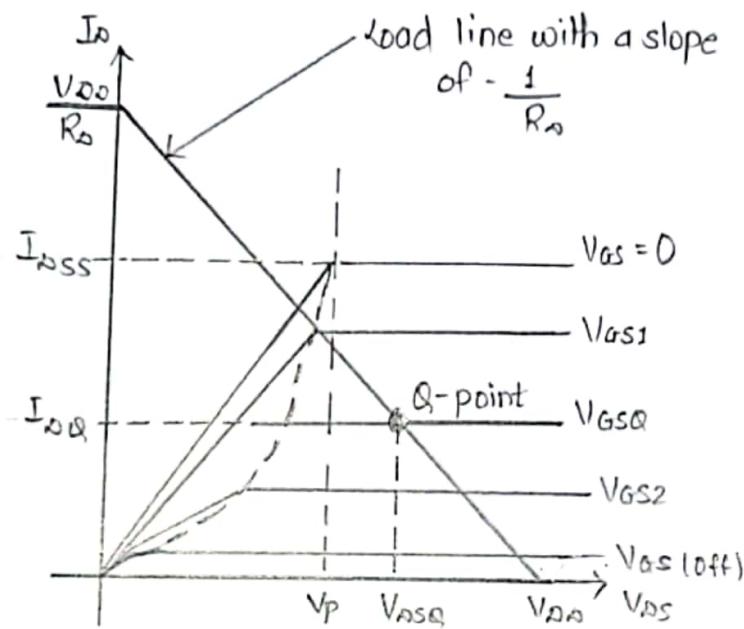
$$\text{Slope is } -\frac{1}{R_D} \text{ and } c = \frac{V_{DD}}{R_D}$$

If $I_o = 0$, $V_{DS} = V_{DD}$. Hence, the load line intersects the I_o axis at $\frac{V_{DD}}{R_o}$ and the V_{DS} axis at V_{DD} .

Slope is $-\frac{1}{R_o}$ and $c = \frac{V_{DD}}{R_o}$. At $I_o = 0$, $V_{DS} = V_{DD}$.

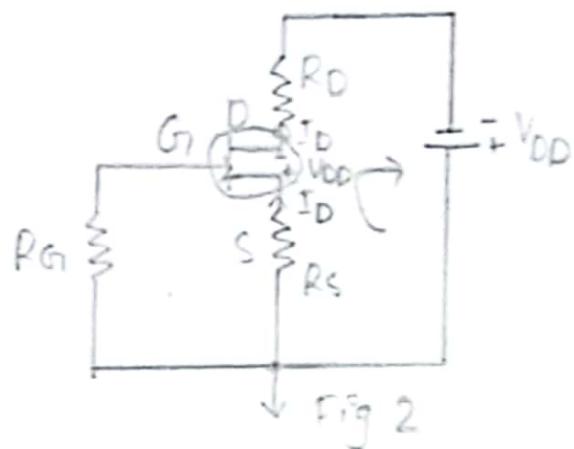
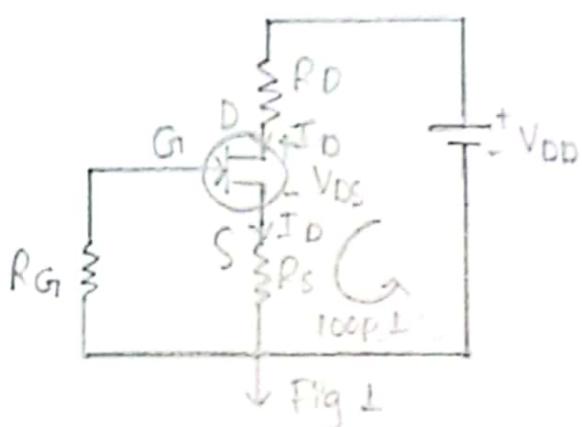
Hence, the load line intersects the I_o axis at $\frac{V_{DD}}{R_o}$ and

the V_{DS} axis at V_{DD} . Once V_{DSQ} is known, I_{DSQ} and V_{GSQ} can be determined.



Self-biasing

In order to operate in the saturation region, (hence as an amplifier), G_1-S of the JFET needs to be reverse biased. To obtain this condition, the V_{GS} has to be negative for the n-channel JFET and positive for the p-channel JFET. The following topologies will enable the mentioned condition to be achieved without the need of an external voltage to be connected to the G_1 . Due to this capability, this topology is called self biasing circuit.



In Fig 1:

$$-V_{DD} + I_D R_D + V_{DS} + I_D R_S = 0$$

$$I_D R_D + V_{DS} + I_D R_S = V_{DD}$$

$V_s = I_D R_S$ is positive

Since $I_{G_1} \approx 0$ then $V_{R_{G_1}} \approx 0$. Hence $V_{G_1} = 0$

Since $V_{G_1} = 0$ and V_{G_1} is positive, $V_{GS} = V_{G_1} - V_s = \text{negative}$.

So, then n-channel is properly biased as an amplifier.

$$V_{GS} = -V_s = -I_D R_S$$

$$R_S = \frac{V_s}{I_D}$$

In fig 2:

$$I_D R_S + V_{SD} + I_D R_D - V_{DD} = 0$$

$$I_D R_S + V_{SD} + I_D R_D = V_{DD}$$

Since $I_D R_S$ is positive and $0 - V_S = I_D R_S$, $V_S = -I_D R_S$.

Therefore, V_S is negative.

Since $I_{Gn} \geq 0$ then $V_{GS} \approx 0$. Hence $V_G = 0$.

Since $V_G = 0$ and V_S is negative, $V_{GS} = V_G - V_S = \text{positive}$. So the p-channel is properly biased as an amplifier.

$$V_{GS} = -V_S = I_D R_S$$

$$R_S = \frac{V_{GS}}{I_D} \cdot \text{For both n and p channel JFET, } R_G = |V_{GS}| / I_D.$$

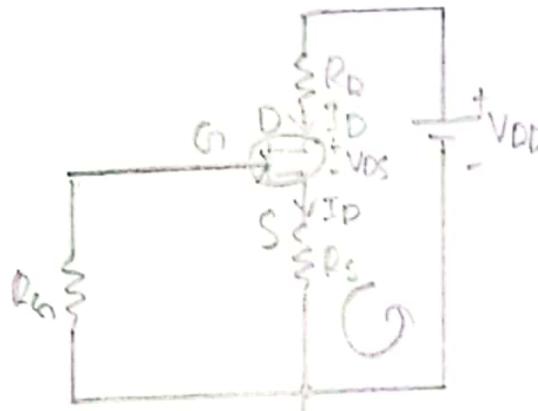
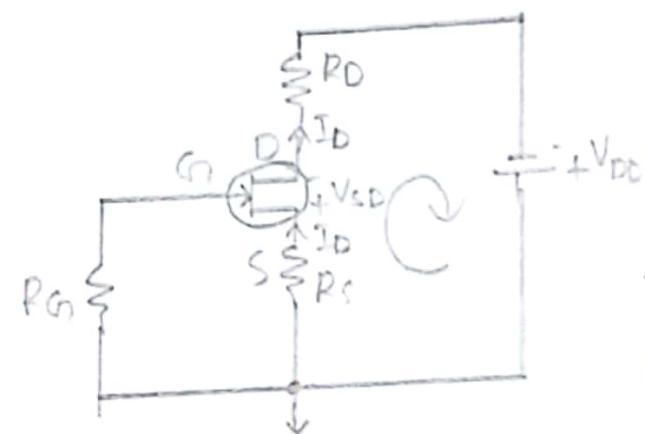


Fig: n-channel JFET

In the JFET, majority carriers are moving from S to D.

In the n-channel JFET, V_{DD} is positive to attract the electrons to move from S to D. Conventional current flow is opposite to the flow of electron. Hence, the direction of current is from D to S.

In the p-channel JFET, V_{DD} is negative to attract the holes to move from S to D. Conventional current flow is the same as the flow of holes. Hence, the direction of current is from S to D.



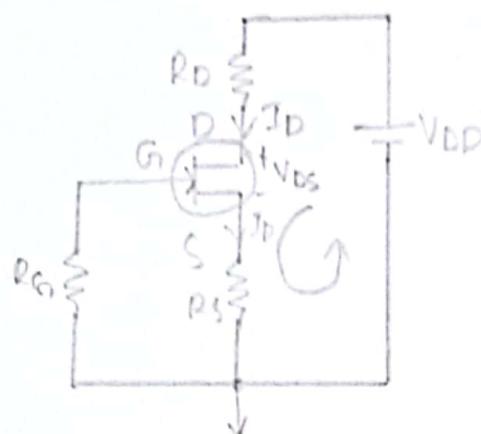
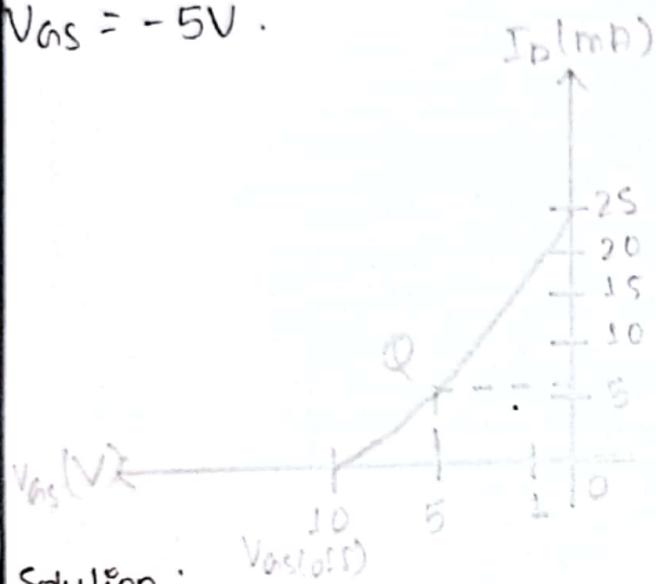
Determining the operational point of the self-biasing JFET

2 ways:

1. Graphical method, ie from the transfer and drain characteristic
2. from calculation, ie using $I_D = I_{DSS} \left[1 - \frac{V_{GS}}{V_{GS(S)}} \right]^2$

Example:

Determine the R_S that is needed to self bias to n channel JFET that has the transfer characteristic curve as shown below at $V_{DS} = -5V$.

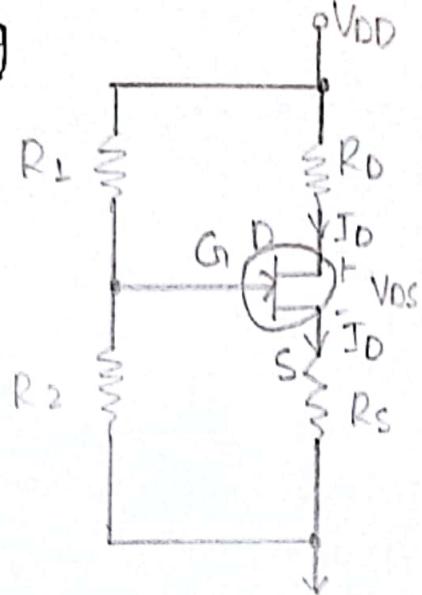


Solution:

From the graph, at $V_{GS} = -5V$, $I_D = 6.25\text{mA}$.

$$R_S = \frac{|V_{GS}|}{I_D} = \frac{5}{6.25} = 800\Omega$$

Voltage Division biasing



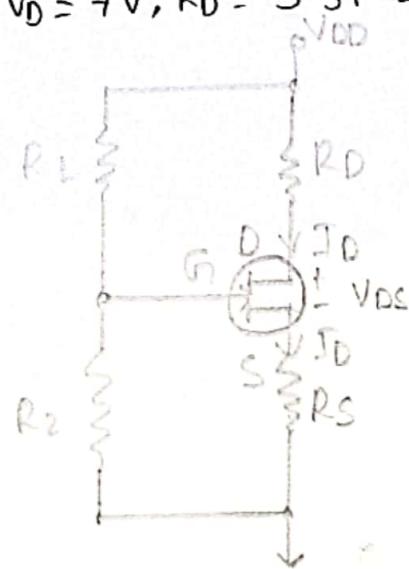
V_S has to be more positive than V_G to maintain the requirement of a reverse biased G-S.

$$V_S = I_D R_S$$

$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD}$$

Example

Determine I_D and V_{GS} for the following voltage division biased JFET. Given $V_{DD} = 12V$, $V_D = 7V$, $R_D = 3.3k\Omega$, $R_S = 1.8k\Omega$, $R_1 = 6.8M\Omega$ and $R_2 = 1M\Omega$



Solution:

$$I_D = \left(\frac{V_{DD} - V_D}{R_D} \right) = \left(\frac{12 - 7}{3.3k} \right) = 1.52mA$$

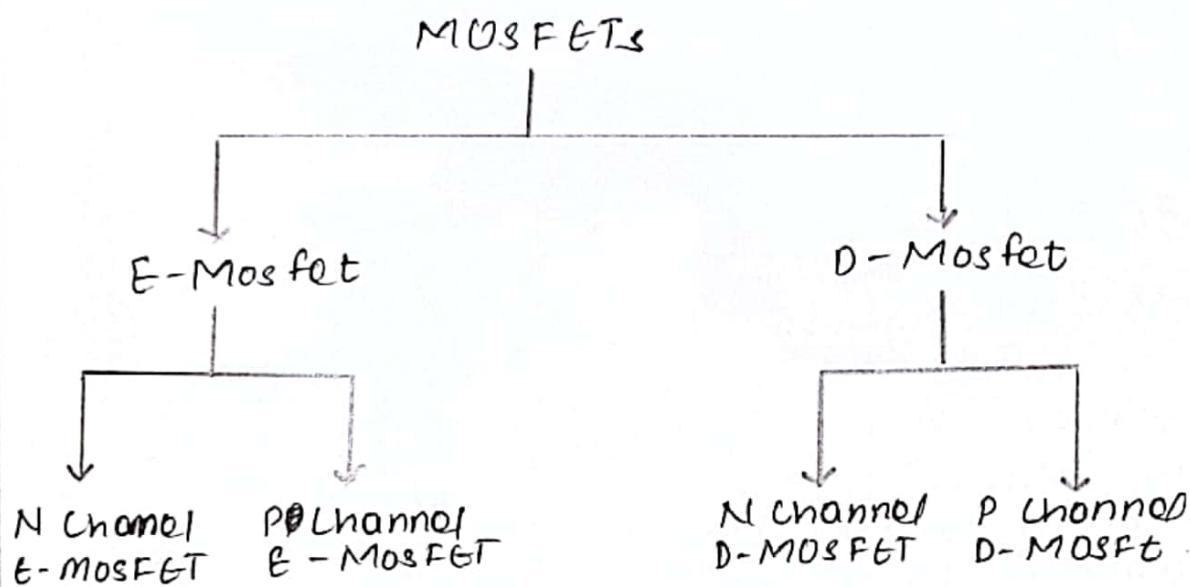
$$V_G = \left(\frac{R_2}{R_1 + R_2} \right) V_{DD} = \left(\frac{1M}{6.8M + 1M} \right) 12 = 1.54V$$

$$V_S = I_D R_S = 1.52mA \times 1.8k = 2.74V$$

$$V_{GS} = V_G - V_S = 1.54 - 2.74 = -1.2V$$

Metal Oxide Semiconductor Field Effect Transistor (MOSFET)

Metal oxide semiconductor field effect transistor (MOSFET) is a type of field effect transistor. In this type of FET the oxide layer insulates the gate electrode from the doped body and hence it is called metal oxide semiconductor field effect transistor.



Structure and Operation of Enhancement Type MOSFET

→ N-channel E- MOSFET
Structure

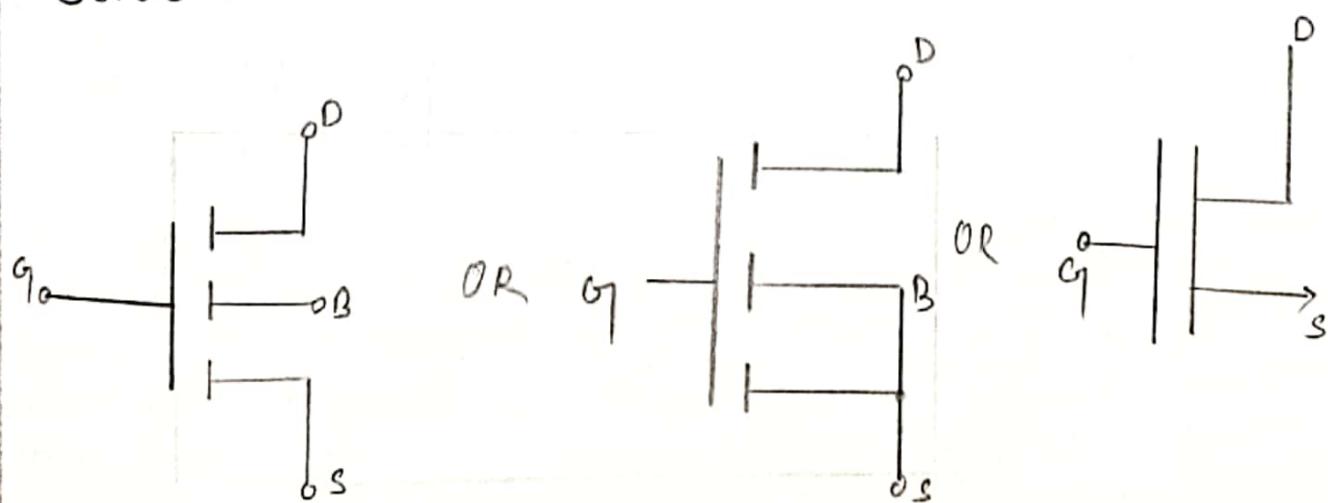


Fig: Symbol of n-channel Enhancement type MOSFET

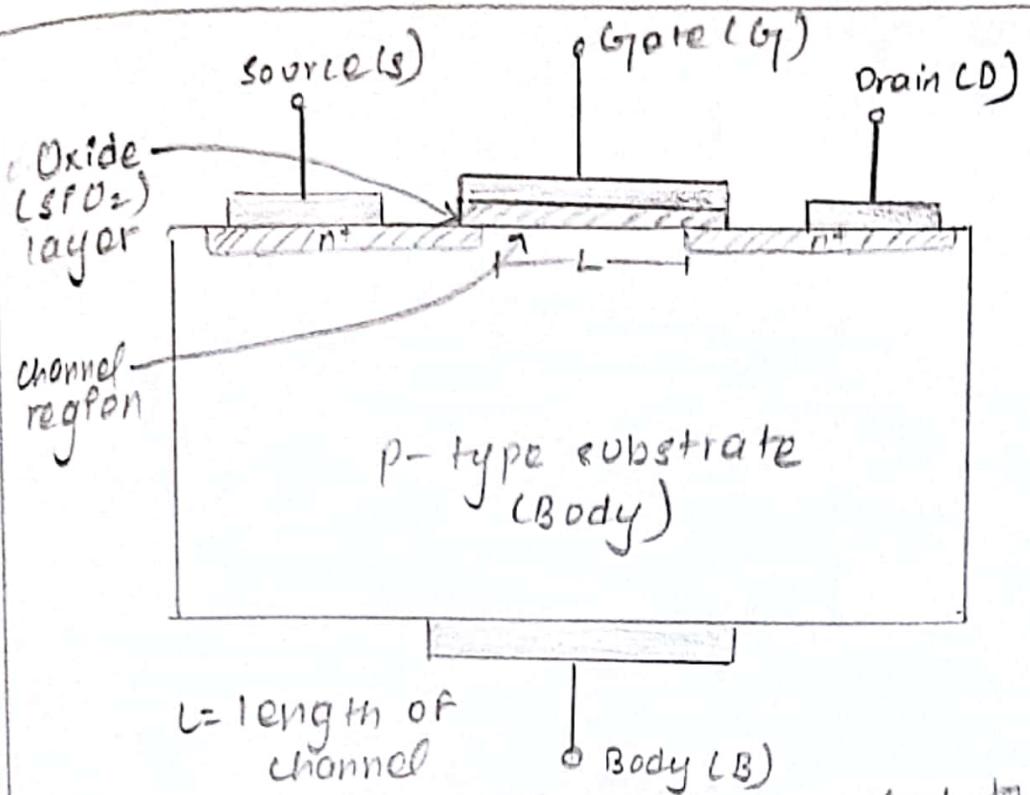


Fig: Body is internally connected to source and source is grounded.

The basic structure of enhancement type NMOSFET is shown in figure above. A slab of p-type substrate is formed, in which two heavily doped n-type regions (n^+ -source and n^+ -drain) are created. A thin ($\approx 0.1\text{ micrometers}$) layer of metal oxide (SiO_2), which is excellent electrical insulator, is formed covering the area between the source and drain regions. Metal contacts are made to drain regions to bring out for terminals of gate (G), source (S), drain (D) and substrate or body (B).

Another name for MOSFET is insulated gate -

Physical Operation:

With no bias voltage applied to the gate, two back-to-back diodes exist in series between drain and source present current conduction from drain to source when a voltage V_{DS} is applied. So, initially drain to source channel is at cut-off stage i.e. no conducting channel. When positive gate to source voltage (V_{GS}) is applied, channel starts to build up (as shown in figure below).

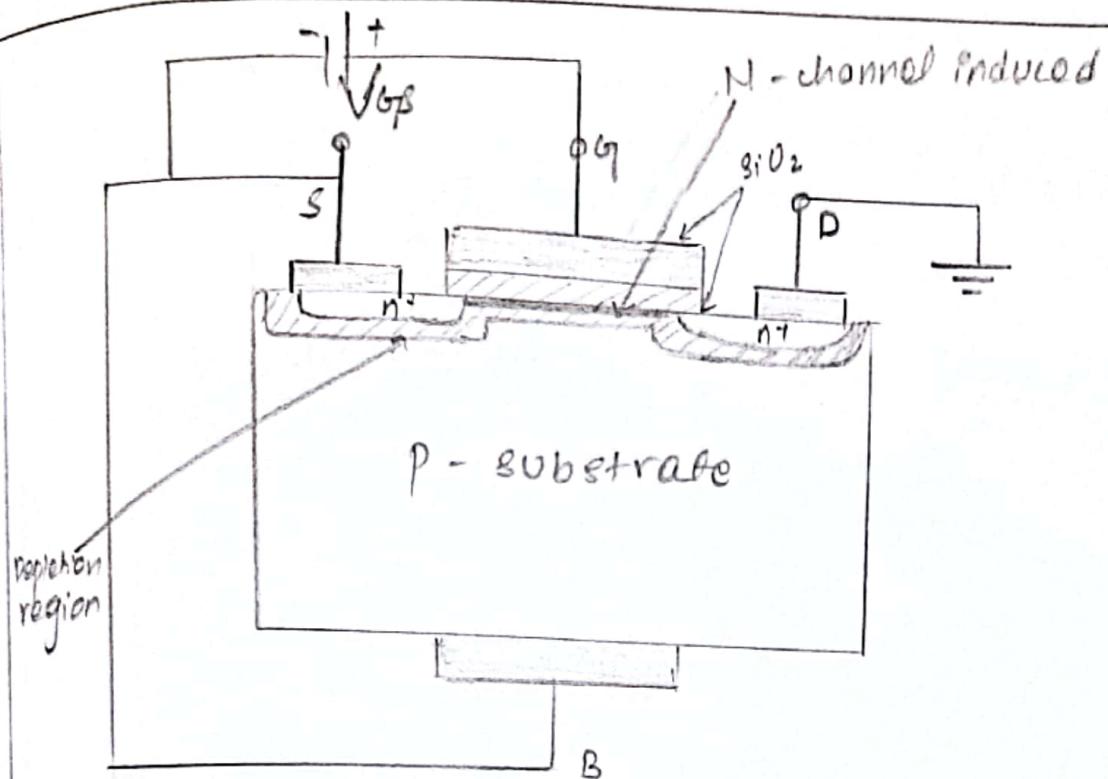


Fig : Body is internally connected to source and source is grounded.

Here, when V_{GS} is applied, positive voltage on gate causes free holes to be repelled from the substrate region under gate channel region. These holes are pushed downwards into the substrate, leaving behind populated bound negative charges. Also positive gate voltage attracts electrons from n^+ source and n^+ drain region into channel region. This sufficient accumulated electrons creates an ' n ' region connecting the source and drain regions.

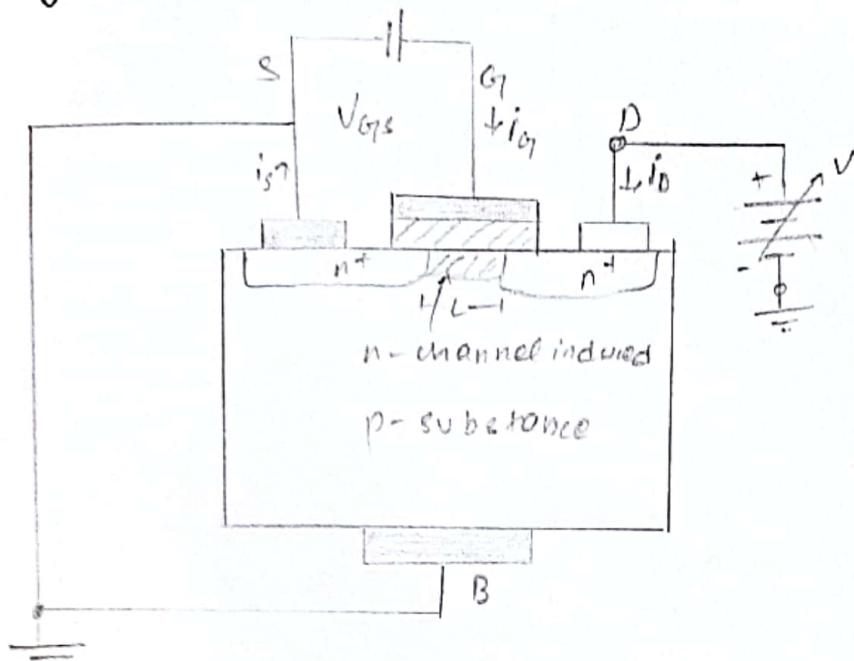
The induced n -region thus forms a channel for current flow from drain to source. This channel is created inverting the substrate surface from p-type to n-type hence is called inversion layer.

The value of V_{GS} at which a sufficient layer number of mobile electrons accumulate in the channel region to form a conducting channel is called threshold voltage (V_t). It is positive for n-channel MOSFET. i.e. when $V_{GS} \leq V_t$; channel is created or induced.

Thus, at $V_{GS} = V_t$; channel is at threshold of pinch off state i.e. at the point between ohmic region and pinch off region.

When $V_{GP} > V_t$ i.e. $(V_{GS} - V_{DS}) > V_t$ or, $V_{DS} \leq V_{GS} - V_t$; the channel is continuous and the conductance of the induced channel is proportional to excess gate voltage ($V_{GS} - V_t$) for small drain to source voltage. The EMOSFET operates in ohmic region.

When drain to source voltage V_{DS} is increased sufficiently so that is $V_{GS} > V_t$ (as shown in Figure below).



For this, V_{DS} appears as a voltage drop across the length of the channel (L) traveling along the channel from source (V_{DS}) to drain ($0V$). This result varying voltage between gate and the point along channel which is $V_{GS} - V_{DS}$ at the source end and $V_{GS} - V_{DS}$ at the drain end.

This creates non-uniform tapered shape channel because channel depth depends on this voltage. As V_{DS} increases, the channel becomes more taper and its resistance increases correspondingly. Thus the $i_D - V_{DS}$ curve ends, eventually, when V_{DS} is increased to the value that reduces the voltage between gate and channel at the drain end to V_t (i.e. $V_{GS} - V_{DS} = V_t$), channel depth at drain end decreases to almost zero and the channel is said to be pinched off. Increasing V_{DS} beyond this value has little (theoretically no) effect on channel shape and the current through channel remains constant. The drain current saturates at this value and the MOSFET is said to have entered the saturation region of operation. The region of $i_D - V_{DS}$

characteristic obtained for $V_{DS} < V_{DS,sat}$, is called the triode region.

* Describe the construction and working principle of MOSFET with the help of drain characteristics curve and mathematical expression.

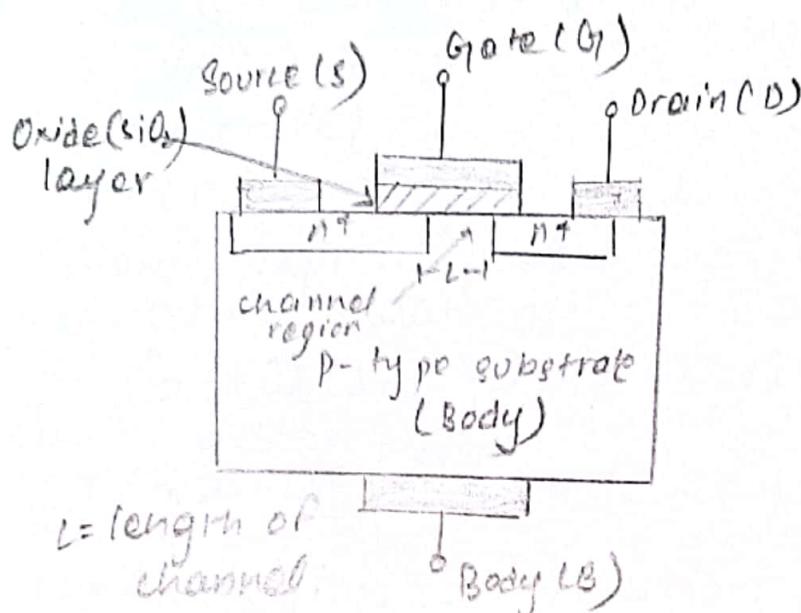


Fig: Construction of enhancement type N-MOSFET.

The basic construction of enhancement type n-MOSFET is shown in figure above. A slab of p-type substrate is formed in which two heavily doped n-type regions (nt-source and nt-Drain) are created. A thin ($1\text{--}2\mu\text{m}$) layer of metal oxide (SiO_2), which is excellent electrical insulator, is formed covering the area between the source and drain regions. Metal contacts are made of those regions to bring out of terminals: gate (G), source (S), drain (D) and substrate or body (B).

$$V_{DS} \geq (V_{GS} - V_t)$$

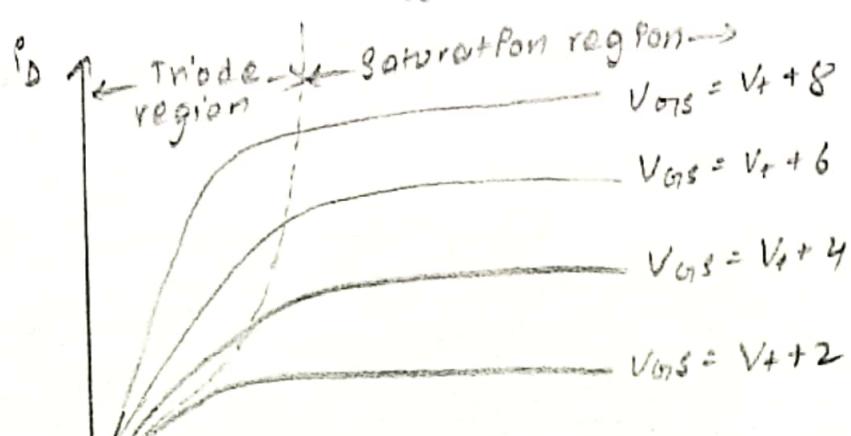


Fig: Drain characteristic curve of GMOSFET

The MOSFET is cut-off when $V_{DS} < V_t$. And to operate the MOSFET in the triode region.

We must produce a channel.

i.e when

$V_{DS} \geq V_t$; channel is induced.

when $V_{DS} > V_t$; channel is continuous for small V_{DS}

$$\text{or}, (V_{DS} - V_t) \geq V_t$$

$$\text{or}, V_{DS} \geq (V_t + V_t)$$

i.e MOSFET operates in ohmic region

The general expression for MOSFET is given by approximate equation,

$$I_D = K [2(V_{DS} - V_t) V_{DS} - V_{DS}^2] \quad \text{--- (1)}$$

where

$$K = \frac{1}{2} \mu n C_{OX} \left(\frac{W}{L} \right) = \text{device parameter.}$$

In ohmic region of operation V_{DS} is very small
so, V_{DS}^2 can be neglected.

Where,

μn = electron mobility in induced channel

C_{OX} = oxide capacitance unit area

L = length of channel

W = width of channel.

For eq 1 (1)

$$I_D = K [2(V_{DS} - V_t) V_{DS} - 0]$$

$$\text{or}, I_D = 2K (V_{DS} - V_t) V_{DS}$$

$$\text{or}, \frac{V_{DS}}{I_D} = R_{DS} = \frac{1}{2K(V_{DS} - V_t)}$$

When,

$V_{DS} < V_t$; the channel is pinched off.

i.e $V_{DS} \leq V_t$

or, $V_{DS} - V_t \leq 0$

$\therefore V_{DS} \geq V_{DS} - V_t$ (pinched off)

The boundary between the triode region and the saturation region is characterized by

$$V_{DS} = (V_{DS} - V_t) \quad (\text{Boundary})$$

Beyond this value of V_{DS} it does not increase.

$$\therefore I_D = I_{D(\text{sat})} = K [2(V_{DS} - V_t) V_{DS} - V_{DS}^2]$$

But,
 $V_{DS} = V_{GS} - V_t$

$$\therefore I_D(\text{sat}) = K [2(V_{GS} - V_t)(V_{GS} - V_t) - (V_{GS} - V_t)^2]$$
$$= K \{ (V_{GS} - V_t)^2 \}$$

$$\therefore I_D = I_{D(\text{sat})} = K \{ (V_{GS} - V_t)^2 \}$$

MOSFET

- ↳ Oxide layer insulates the gate electrode from the device, MOSFET.
- ↳ High I_OP Impedance than JFET & BJT; mostly used Transistor. (Ares, cheap, low power etc.)

* In Enhancement type no physical channel is present.

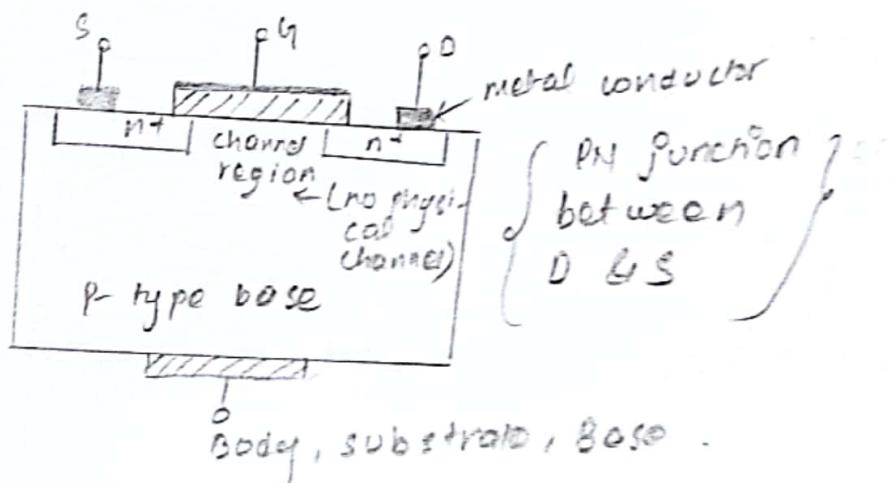
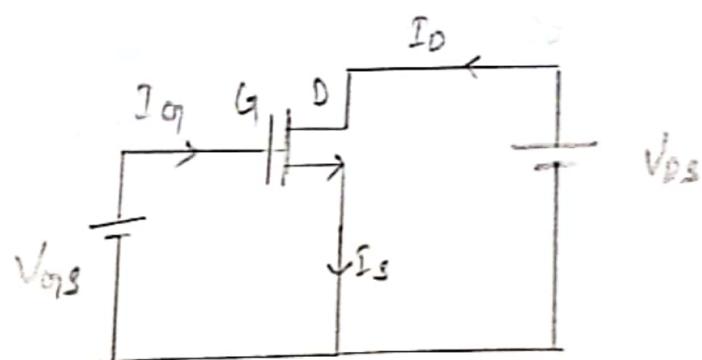


Fig. N-channel E-MOSFET

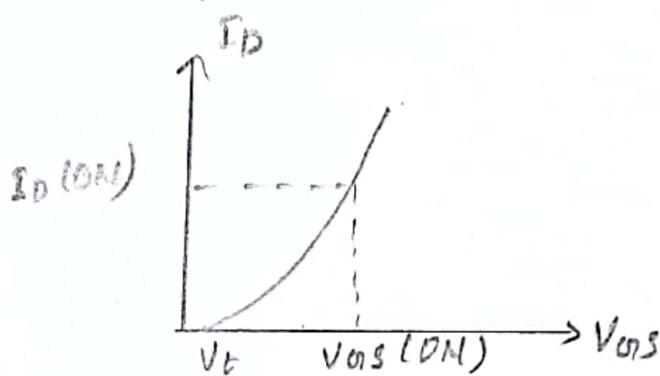
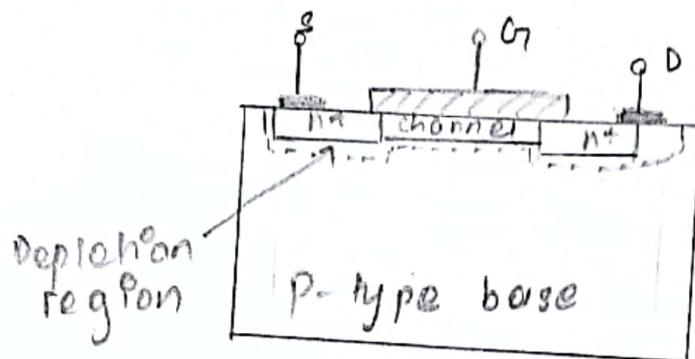


When $V_{GS} = 0$, no gate voltage, very high resistance between source and drain (no channel).

When $V_{GS} = +V_0$, the holes near the gate electrode are repelled and pushed down to the substrate and attract electrons from drain source and base also. Thus under gate electrode region a channel is formed called channel.

Due to due V_{GS} channel is formed between source and drain. The V_{GS} at which channel is formed between

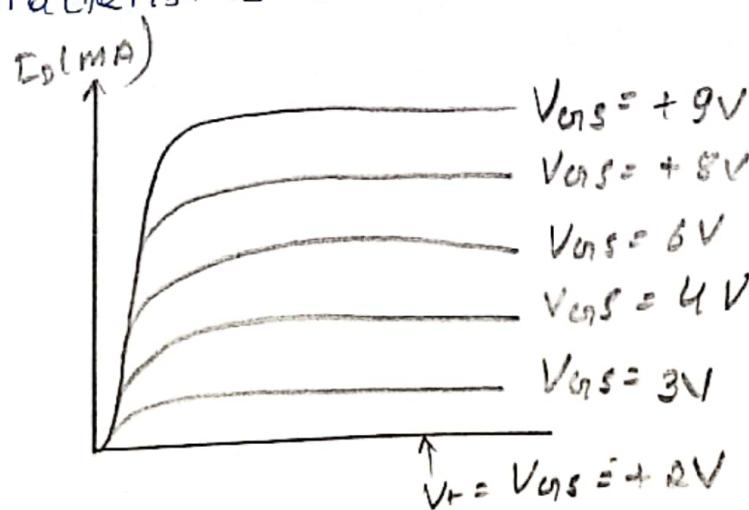
source and drain. P_S threshold voltage (V_T). Once channel is created current flow P_S controlled by V_{DS} .



Transfer characteristics of n-EMOSFET

$$I_{D(ON)} = K(V_{DS} - V_T)^2$$

Drain characteristics of N-channel EMOSFET



If $V_{DS} < V_T$, no drain current flows.

DEMOSFET:

(Depletion Enhancement metal oxide semiconductor field effect transistor)

1. What is DEMOSFET?

- DEMOSFET (Depletion enhancement metal oxide semiconductor field effect transistor) is a type of MOSFET that operates in both depletion and enhancement modes. In a DEMOSFET, the channel is initially depleted of carriers and then can be enhanced by applying a positive or negative gate voltage. DEMOSFETs are commonly used in analog circuits and power electronics applications.

2. Construction of Depletion type MOSFET:[N-channel]

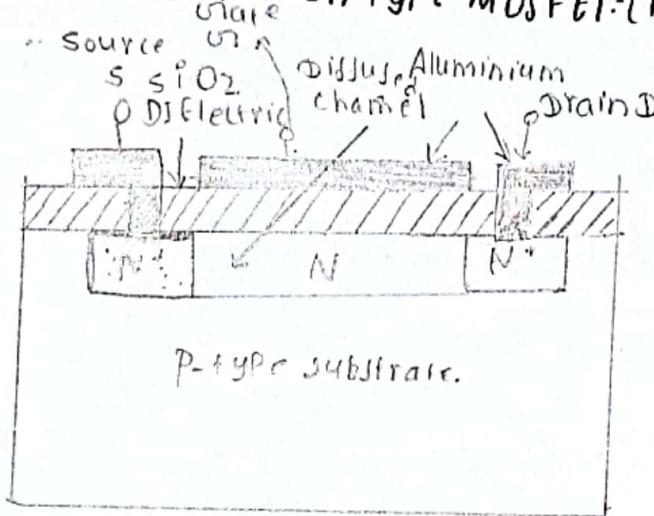


Fig: a N-channel DE-MOSFET structure.

Here, Fig a shows the construction of an N-channel DE-MOSFET. It consists of a lightly doped P-type substrate into which two blocks of heavily doped N-type material are diffused forming the source and drain. An N-channel is formed by diffusion between the source and drain. Now a thin layer of SiO₂ dielectric is grown over the entire surface and holes are cut through the SiO₂ layer to make contact with N-type blocks. The SiO₂ layer results in an extremely high input impedance of order of 10^{10} to $10^{15} \Omega$ for the device.

Construction of P-Channel MOSFET can be done just like of N-Channel DE-MOSFET, starting with N-type substrate and diffusing P-type drain and source blocks and connecting them internally by a P-doped channel region. It consists of a lightly doped N-type substrate into which two blocks of heavily doped P-type material are diffused forming the source and drain. A P-channel is formed by diffusion between the source and drain. Now a layer of SiO_2 is grown over the surface and it makes contact with P-type blocks.

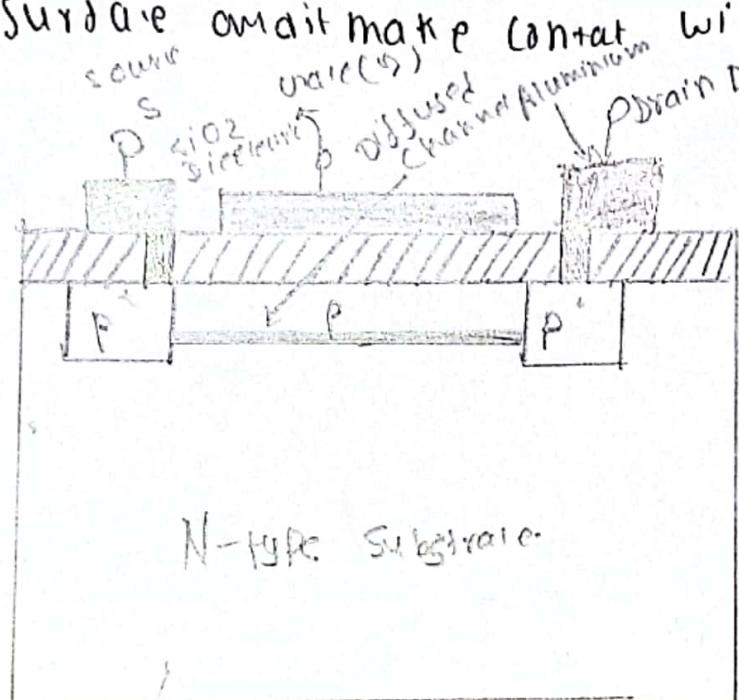


Fig 1: P-Channel DE-MOSFET Structure.

Operation of Depletion type MOSFET:

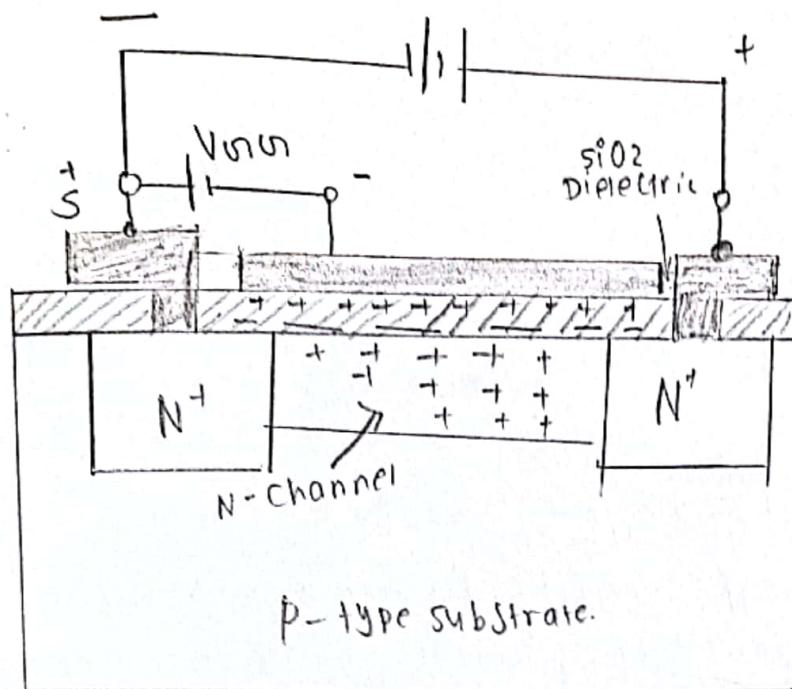


Fig b: Depletion mode operation:

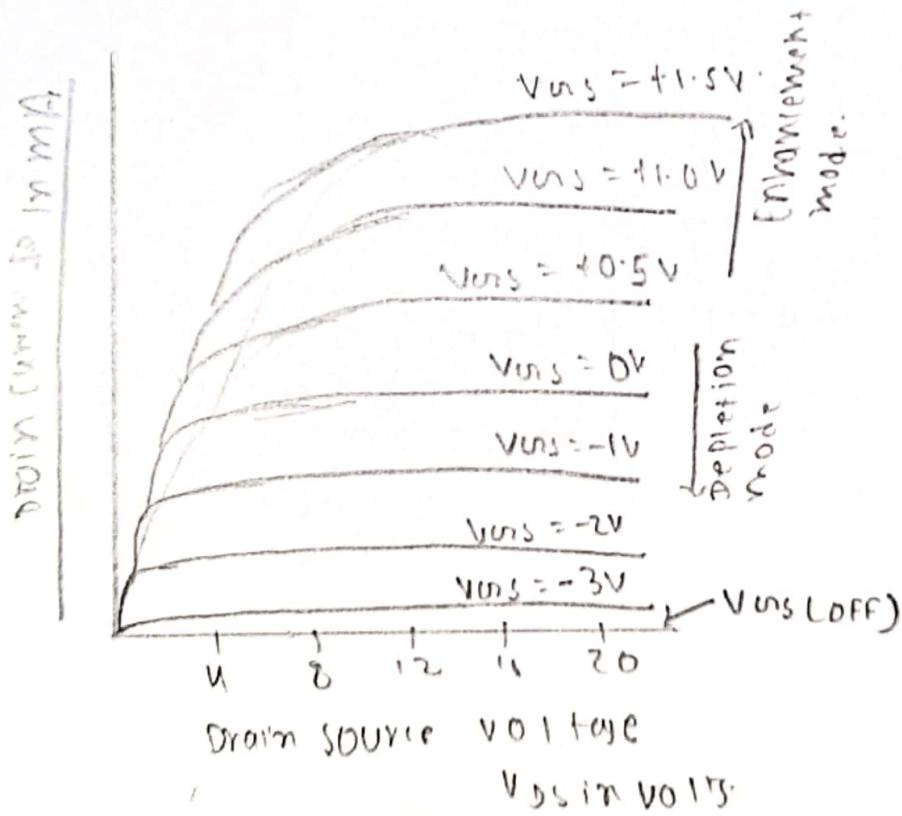
Here, the diffused channel N, the insulating dielectric SiO_2 layer and the metal layer of the gate forms a parallel plate capacitor. DE-MOSFET can be operated with either a positive or a negative gate. When gate is positive with respect to the source it operates in the enhancement mode and when the gate is negative w.r.t the source, as illustrated in fig b.

-When the drain is made +ve w.r.t source a drain current will flow even with zero gate potential and MOSFET is said to be operating in E-mode. In this mode of operation gate attracts the -ve charge carriers from the p-substrate to N-channel and thus reduces the channel resistance increases the drain current.
Gate [More Positive] = More drain current.

-When gate is made -ve w.r.t substrate gate repels some -ve charge carriers this creates a depletion region in the channel then channel resistance increases and drain current reduces. The more -ve the gate, lesser will be the drain current. Here too much negative gate voltage can pinch off the channel.

characteristics :-

typical drain characteristics for various levels of gate-source voltage of an n-channel MOSFET are shown in fig. The upper curves are for positive V_{GS} s and the lower curves are for negative V_{GS} s. the bottom drain curve is for $V_{GS} = V_{GS(OFF)}$ for a specified drain source voltage V_{DS} , $V_{GS(OFF)}$ is the gate source voltage at which drain current reduces to a certain specified negligibly small value, as shown in fig C. This voltage corresponds to the pinch off voltage V_P of JFET. For V_{GS} between $V_{GS(OFF)}$ and zero, the device operates in depletion mode while for V_{GS} exceeding zero the device operates in enhancement mode.



These drain curves again display an ohmic region, a constant current source region and a cut-off region. MOSFET has two major applications: a constant current source and a voltage variable resistor.

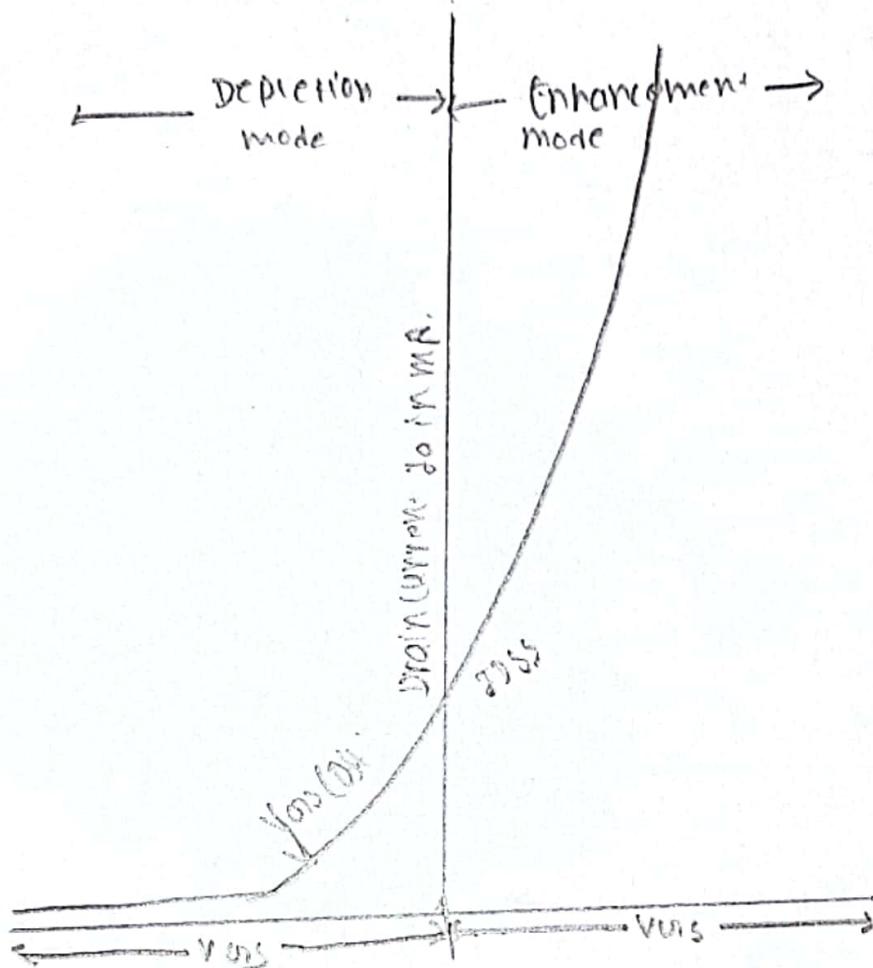


Fig d: Transfer characteristics Curve.

Fig d shows the transfer characteristics of an N-channel JFET. I_{dss} is drain current since the curve extends to right of origin I_{dss} is no longer the maximum possible drain current. Mathematically the curve is still part of a parabola and the same source law relation exists.

JFET (Junction Field Effect Transistor)

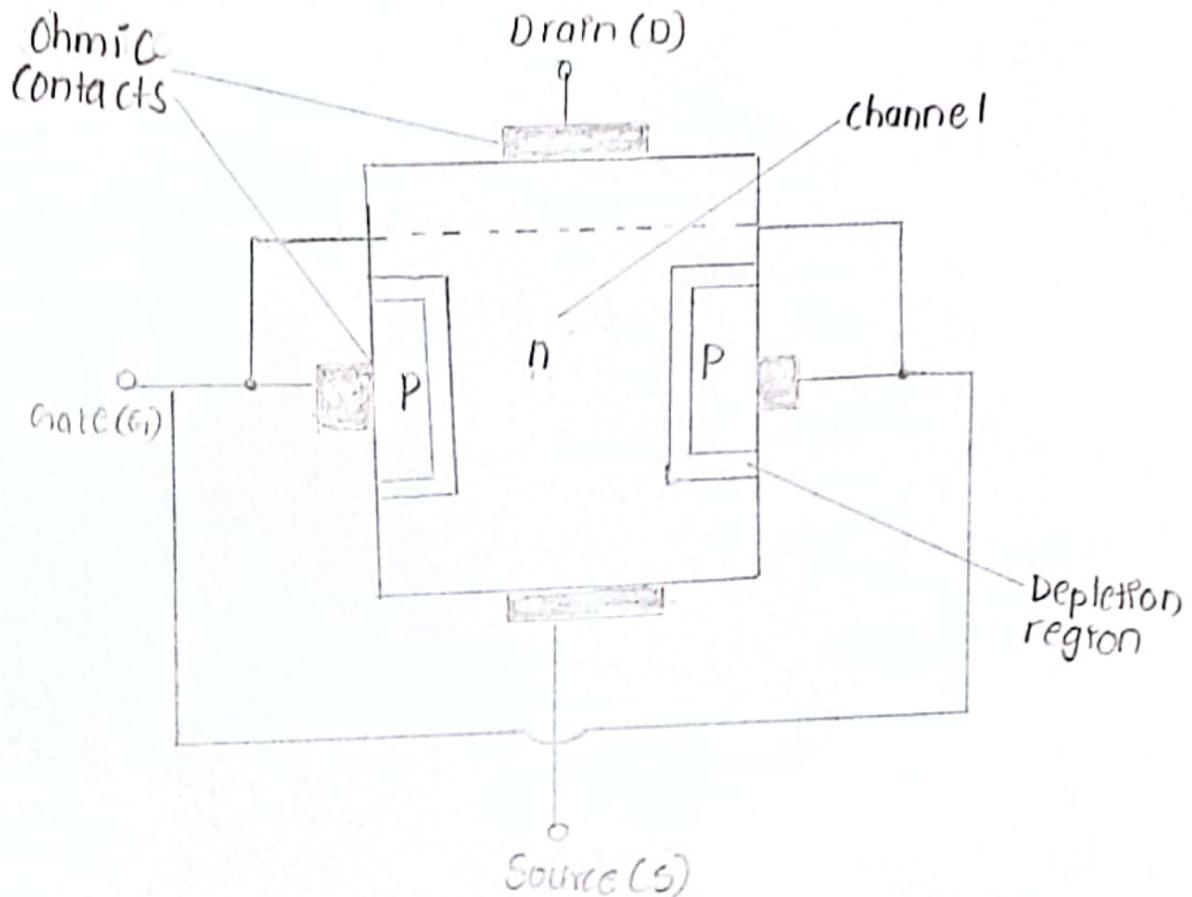


Fig: Construction of JFET

Source:- The terminal through which the majority carriers enter into the channel, is called the source terminal(s).

Drain:- The terminal through which the majority carriers leave from the channel is called the drain terminal (D).

Gate:- There are two internally connected heavily doped impurity regions to create two P-N junctions. These impurity regions are called the gate terminal(s).

channel: The region between the source and drain, sandwiched between the two gates ~~are~~ is called the channel.

* Types of JFET

- n-channel JFET
- p-channel JFET

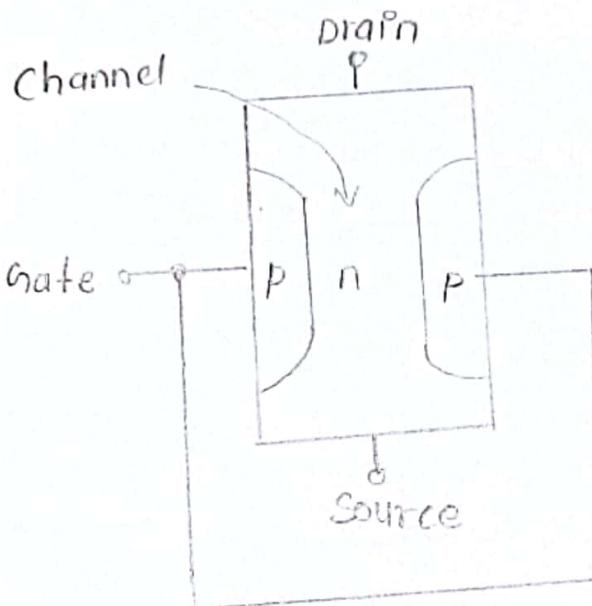


fig: n-channel JFET

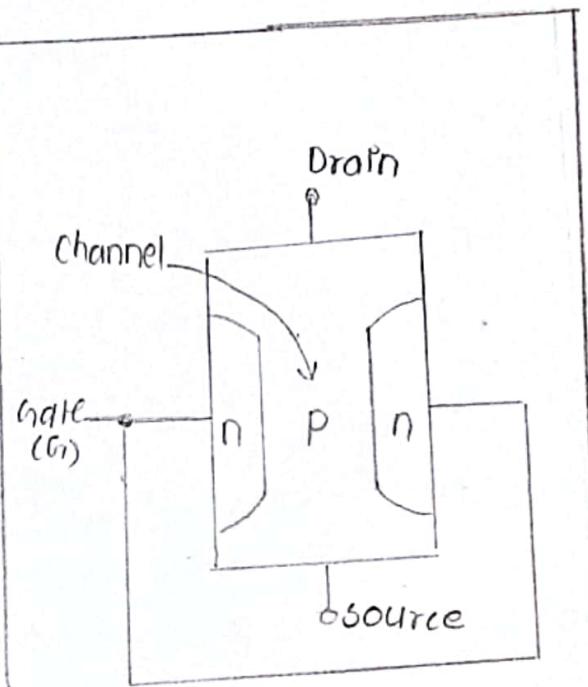


fig:- p-channel JFET

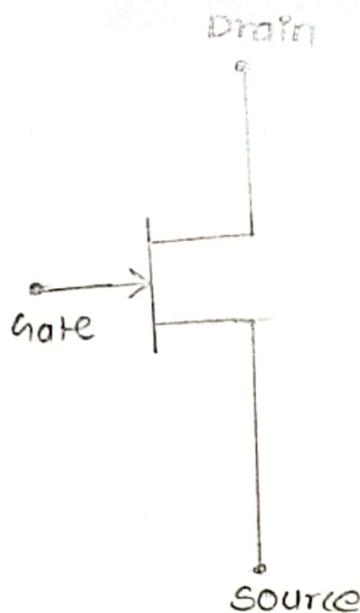


fig:symbol of n-channel JFET

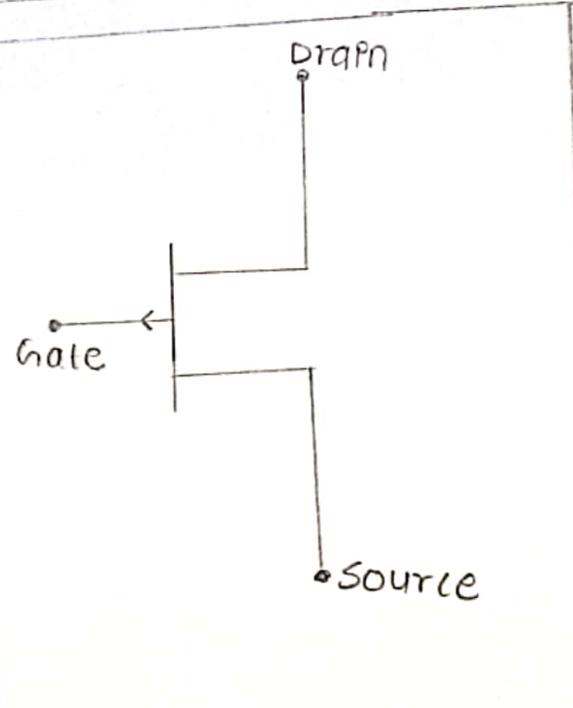


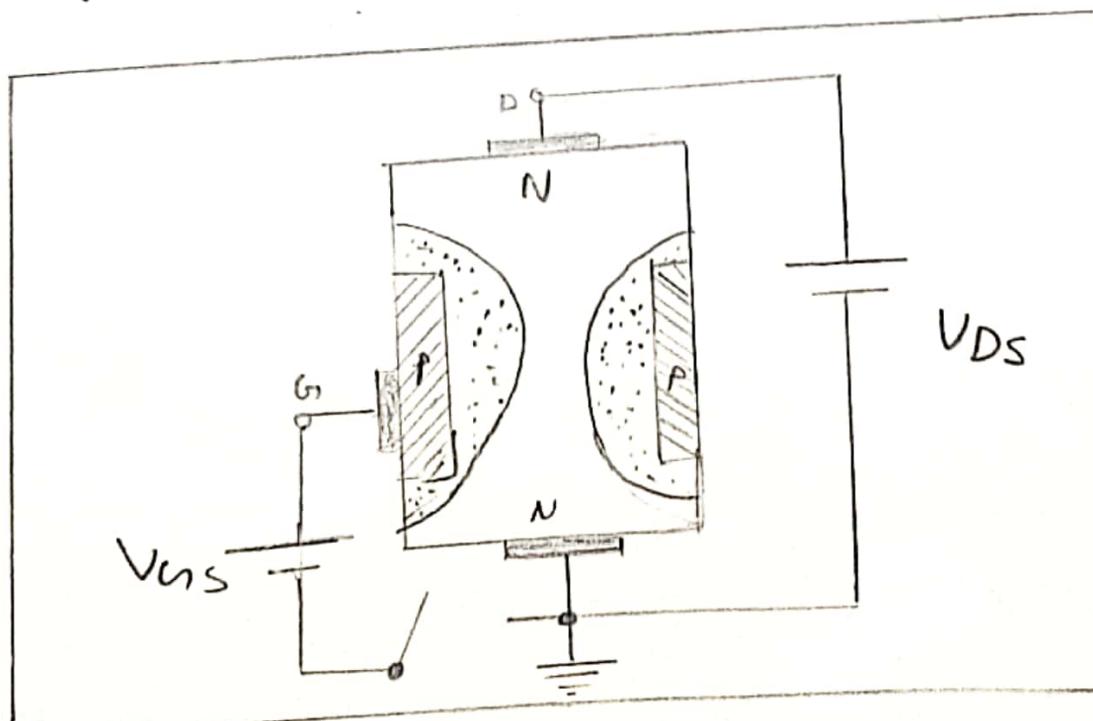
fig:symbol of p-channel JFET

Features of JFET

- JFET is a voltage controlled device i.e. Input voltage (V_{GS}) controls the output current (I_D).
- In JFETs, the width of a junction is used to control the effective cross sectional area of the channel through which current conducts.
- It is always operated with gate-source p-n junction in reverse bias.
- Because of reverse Bias it has high input impedance.
- In JFET the gate current is zero. i.e. $I_G = 0$

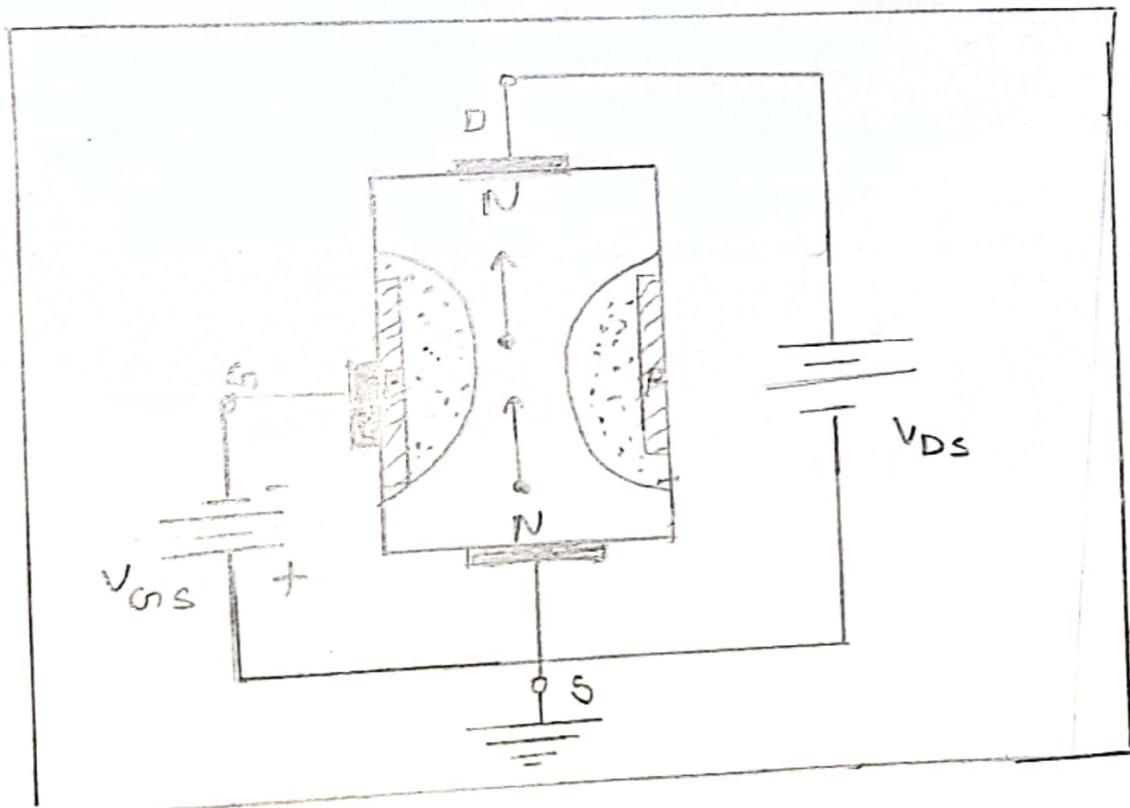
Operation of JFET

- When gate-source Voltage (V_{GS}) is applied and drain-source voltage is zero i.e. $V_{DS} = 0V$.
 - When $V_{GS} = 0V$, two depletion layers & channel are formed normally.
 - When V_{GS} increase negatively i.e. $0V > V_{GS} > V_{GS(\text{off})}$, depletion layer are also increase and channel will be decrease.
 - When $V_{GS} = V_{GS(\text{off})}$, depletion layer will touch each other and channel will totally removed. So no current can flow through the channel.



ii) When drain-source voltage (V_{DS}) is applied at constant gate-source voltage (V_{GS}):-

- Now reverse bias at the drain end is larger than source end and so the depletion layer is wider at the drain end than source end.
- When V_{DS} increases i.e. $0 < V_{DS} < V_p$, depletion layer at drain end is gradually increased and drain current ~~is also~~ also increased.
- When $V_{DS} = V_p$ the channel is effectively closed at drain ~~current~~ end and it does not allow further increase of drain current. So the drain current will become constant.



JFET characteristic Curve

- To start, suppose $V_{GS} = 0$
- Then, when V_{DS} is increased, I_D increases.
Therefore, I_D is proportional to V_{DS} for small values of V_{DS} .
- For larger value of V_{DS} , as V_{DS} increases, the depletion layer becomes wider, causing the resistance of channel increases.
- After the pinch-off voltage (V_p) is reached, the I_D becomes nearly constant (called as I_D maximum; I_{DSS} - Drain to source current with gate shorted).

I_D versus V_{DS} for $V_{GS} = 0V$.

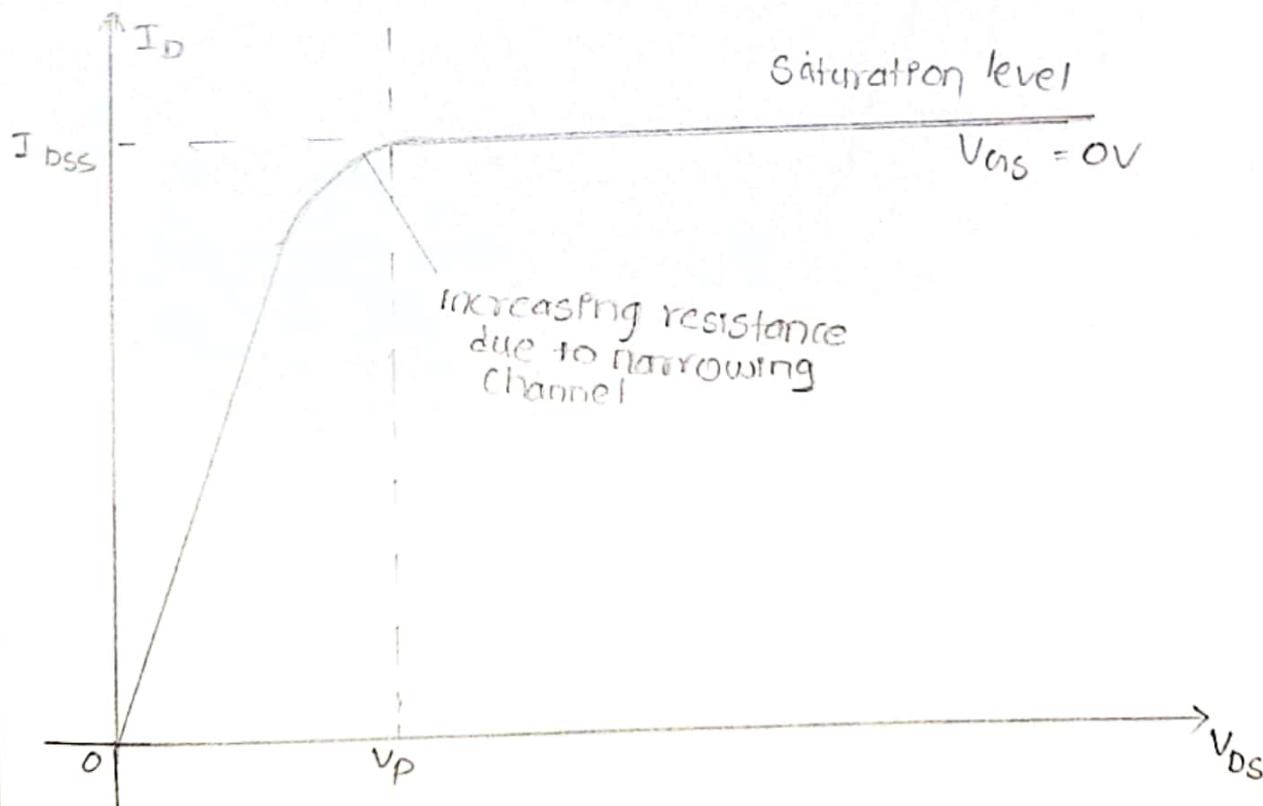


Fig:- JFET characteristic Curve.

Transfer characteristics:

→ In JFET, the relationship between V_{GS} (input voltage) and I_D (output current) is used to define the transfer characteristics. It is called as Shockley's Equation

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2 \quad V_P = V_{GS(\text{OFF})}$$

→ The relationship is more complicated (and not linear).

→ As a result, FET's are often referred to as square law devices.

→ Defined by Shockley's equation:

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P} \right)^2$$

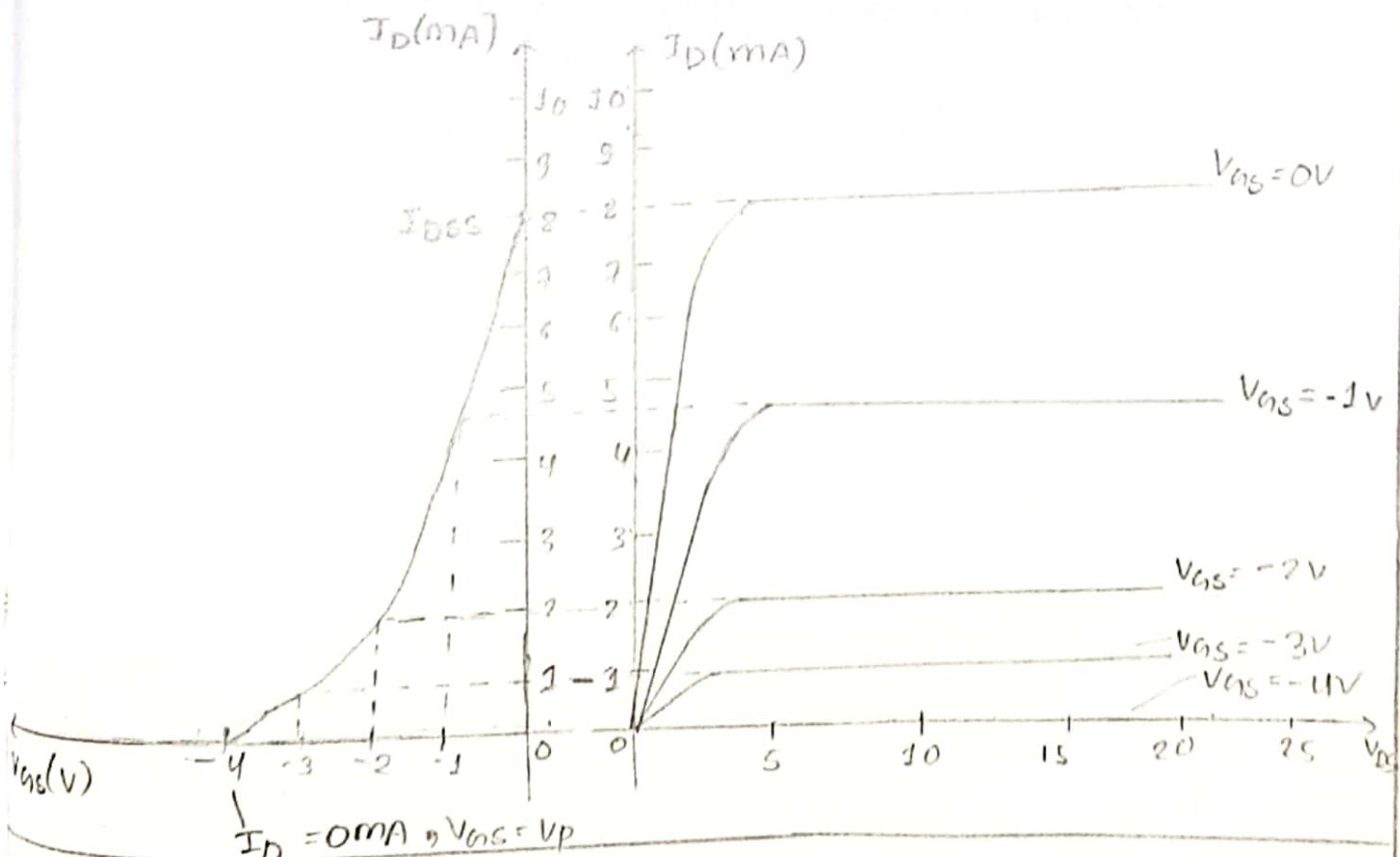
→ Relationship between I_D and V_{GS} .

→ Obtaining transfer characteristics curve axis point from Shockley:

→ When $V_{GS} = 0\text{V}$, $I_D = I_{DSS}$

→ When $V_{GS} = V_{GS(\text{OFF})}$ or V_P , $I_D = 0\text{mA}$

This curve shows the value of I_D for a given value of V_{GS} .



If Pg:- Transfer characteristics curve.

parameters of JFET

i) A.C drain resistance(r_d)

- It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in drain current (ΔI_D) at constant gate-source voltage i.e.

$$\text{a.c drain resistance, } r_d = \frac{\Delta V_{DS} \text{ at constant } V_{GS}}{\Delta I_D}$$

ii) Transconductance :- The control that the gate voltage has over the drain current is measured by transconductance g_F and is similar to the transconductance g_m of the tube. It may be defined as follows.

- It is the ratio of change in drain current (ΔI_D) to the change in gate-source voltage (ΔV_{GS}) at constant drain-source voltage i.e

$$\text{Transconductance}(g_F) = \frac{\Delta I_D}{\Delta V_{GS}} \text{ at constant } V_{DS}$$

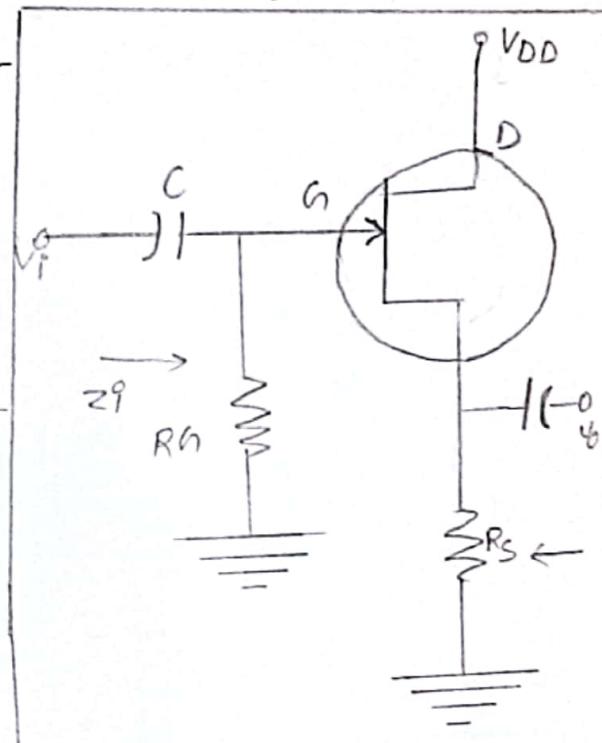
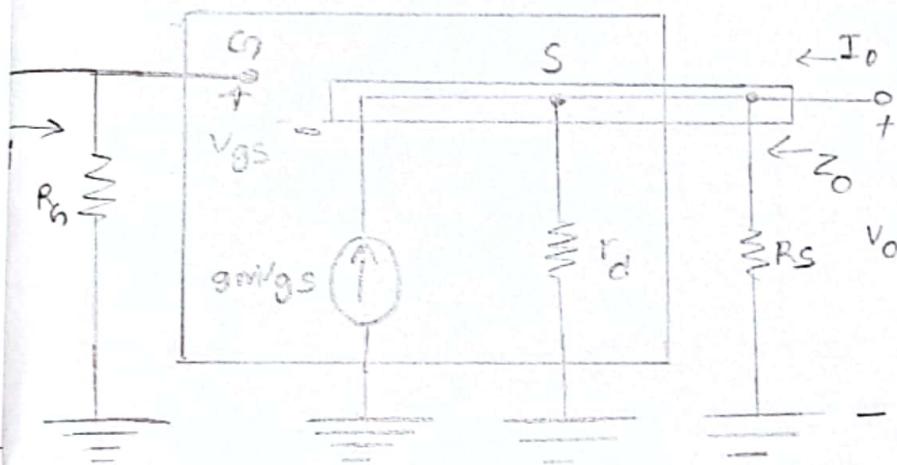
- The transconductance of a JFET is usually expressed either in mA/volt or microamperes/volt

iii) Amplification factor(μ): It is the ratio of change in drain-source voltage (ΔV_{DS}) to the change in gate-source voltage (ΔV_{GS}) at constant drain current i.e -

$$\text{Amplification factor}(\mu) = \frac{\Delta V_{DS}}{\Delta V_{GS}} \text{ at constant } I_D$$

Source Follower (common-Drain) circuit

- In a common-drain amplifier configuration, the input is on the gate, but output is from the source.
- There is no phase shift between input and output



Input impedance:

$$Z_i = R_g$$

Output impedance:

$$Z_o = r_d \parallel R_s \parallel \frac{1}{gm}$$

$$Z_o \approx R_s \parallel \frac{1}{gm} \quad | \quad r_d \geq 10R_s$$

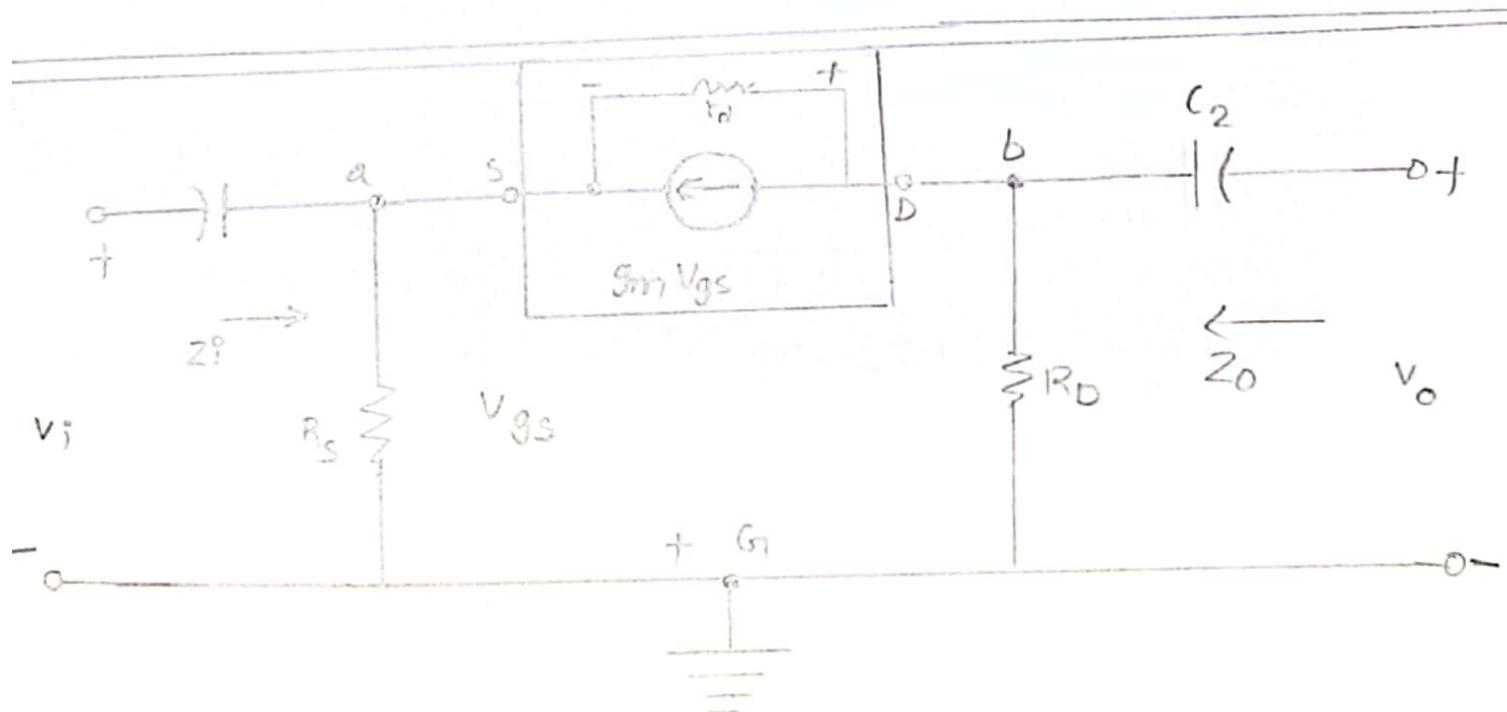
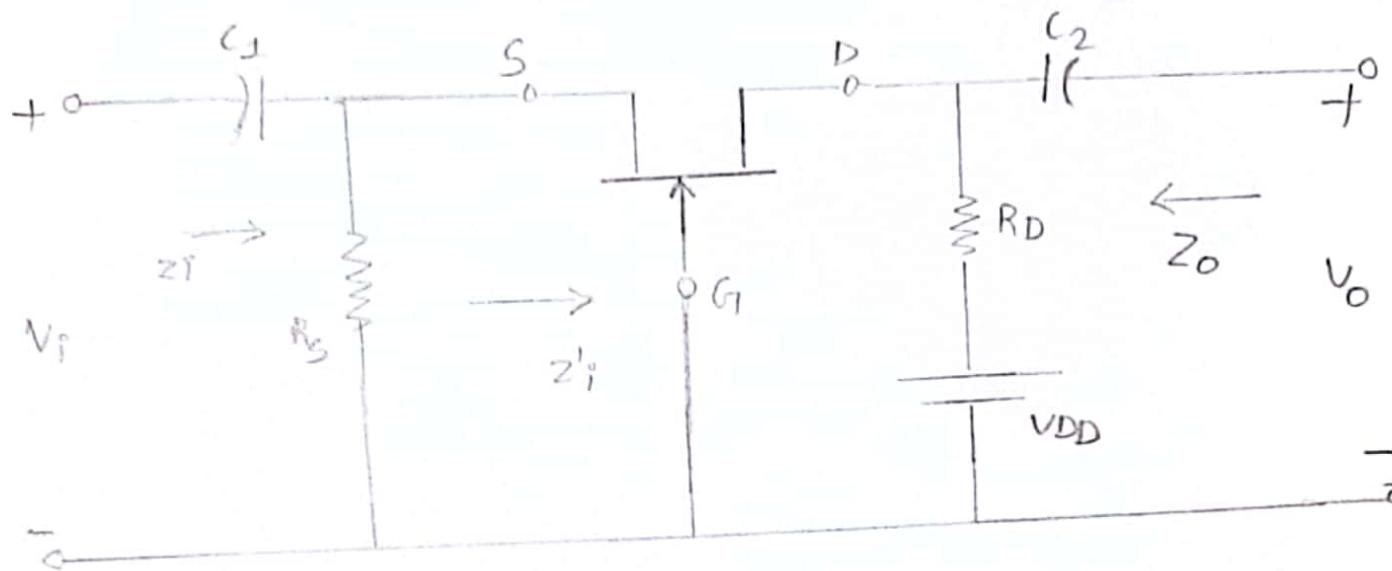
Voltage gain:

$$A_v = \frac{V_o}{V_i} = \frac{gm (r_d \parallel R_s)}{1 + gm (r_d \parallel R_s)}$$

$$A_v = \frac{V_o}{V_i} = \frac{gm R_s}{1 + gm R_s} \quad | \quad r_d \geq 10$$

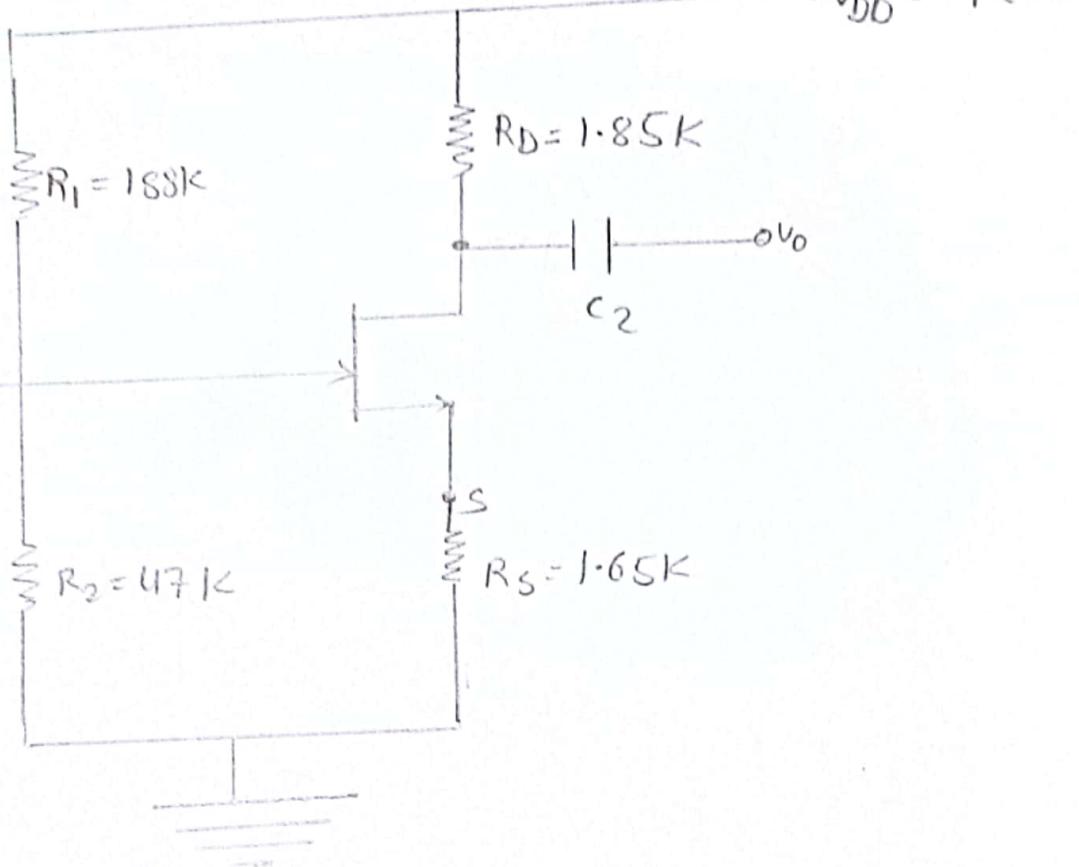
Common-Gate (CG) circuit :

- The Input is on the source and the output is on the drain.
- There is no phase shift between input and output.



problems

For the following Figure $V_P = -5V$, $I_{DSS} = 18mA$, Find I_D and V_{DS} .



Solⁿ,

$$V_G = \frac{R_2}{R_1+R_2} V_{DD} = \frac{47}{47+188} \times 20 = 4V$$

$$\therefore V_{GS} = V_G - V_S = 4 - I_D (1.65 \times 10^3)$$

$$V_{GS} = 4 - 1650 I_D \quad \text{--- (1)}$$

Also,

We know that,

$$I_D = I_{DSS} \left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$\text{or, } I_D = 18 \times 10^{-3} \left(1 + \frac{4-1650}{5}\right)^2$$

$$\text{or, } 1960 \cdot 2 I_D^2 - 22 \cdot 384 I_D + 0.05832 = 0 \quad \text{--- (2)}$$

Now, solving the equation we get,

$$I_D = 7.4mA \text{ or } 4mA$$

For 4mA,

$$V_{DS} = 20 - 4 (1.85 + 1.65) \times 10^3$$

$$= 5.98V$$

$$\therefore V_{DS} \approx 6V$$

Test for pinch-off point.

$$V_{DS} - V_P = (4V - 4mA \times 1.65k) - (-5) = 2.4V$$

$$\therefore V_{DS} > V_{DS} - V_P$$

$$\therefore 6V > 2.4V$$

$$\therefore I_D = 4mA \text{ and } V_{DS} = 6V$$