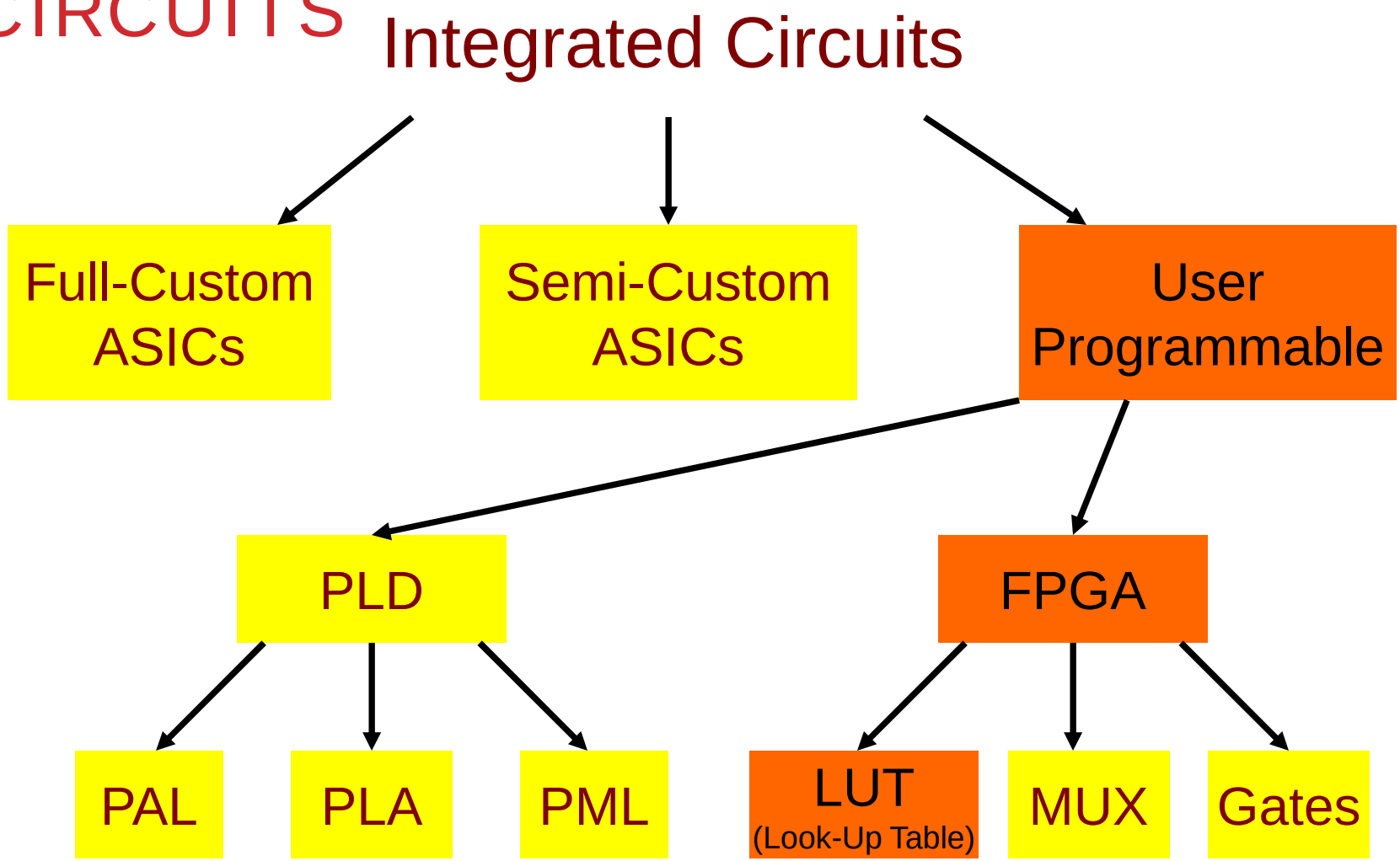
FPGA ARCHITECTURE AND DESIGN FLOW

AGENDA

- **Introduction to Programmable Logic**
- **CPLD - Working principle, Architecture, I/O Block, Macrocells, programming, features, examples.**
- **FPGA - Working principle, Architecture, I/O Block, CLB, embedded memory, clock management, DSP capability, programming, features, examples.**
- **Comparison of CPLD/FPGA Architecture**
- **PLD Design Flow**
- **Advantages of PLDs**
- **Prototyping Solutions**
- **Conclusion**

WORLD OF INTEGRATED CIRCUITS



PROGRAMMABLE LOGIC

Since the invent of PLD from 1980s with few gate count, they have grown into million gates, so as there usage in different applications.

Advantages like programmability and reconfiguration of PLDs has given ideas and shape to many applications.

Today's PLDs like FPGAs can compete with ASICs in terms of performance and gate counts.

From the time their use has increased in all sectors, like defense, consumer, multi media, communications, DSP, etc.

WHAT IS AVAILABLE ?

CPLD (Complex Programmable Logic Device) consists of multiple PLA blocks that are interconnected to realize larger digital systems.

FPGA (Field Programmable Gate Array) has narrower logic choices and more memory elements. LUT (Lookup Table) may replace actual logic gates.

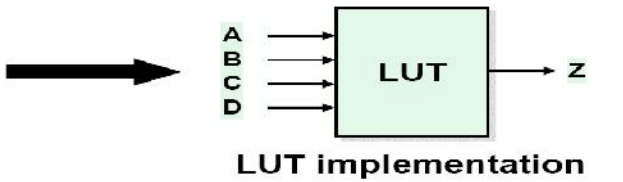
FPGA - WORKING PRINCIPLE (LUT)

Look-up table with N-inputs can be used to implement any combinatorial function of N inputs

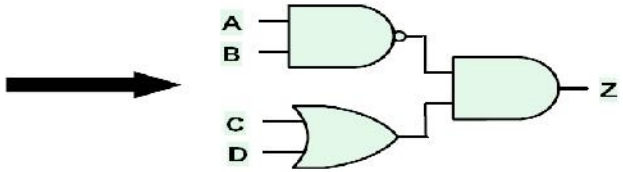
LUT is programmed with the truth-table

A	B	C	D	Z
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**1**
0	1	0	0	**0**
0	1	0	1	**1**
0	1	1	0	**1**
0	1	1	1	**1**
1	0	0	0	**0**
1	0	0	1	**1**
1	0	1	0	**1**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**0**
1	1	1	0	**0**

Truth-table



LUT implementation

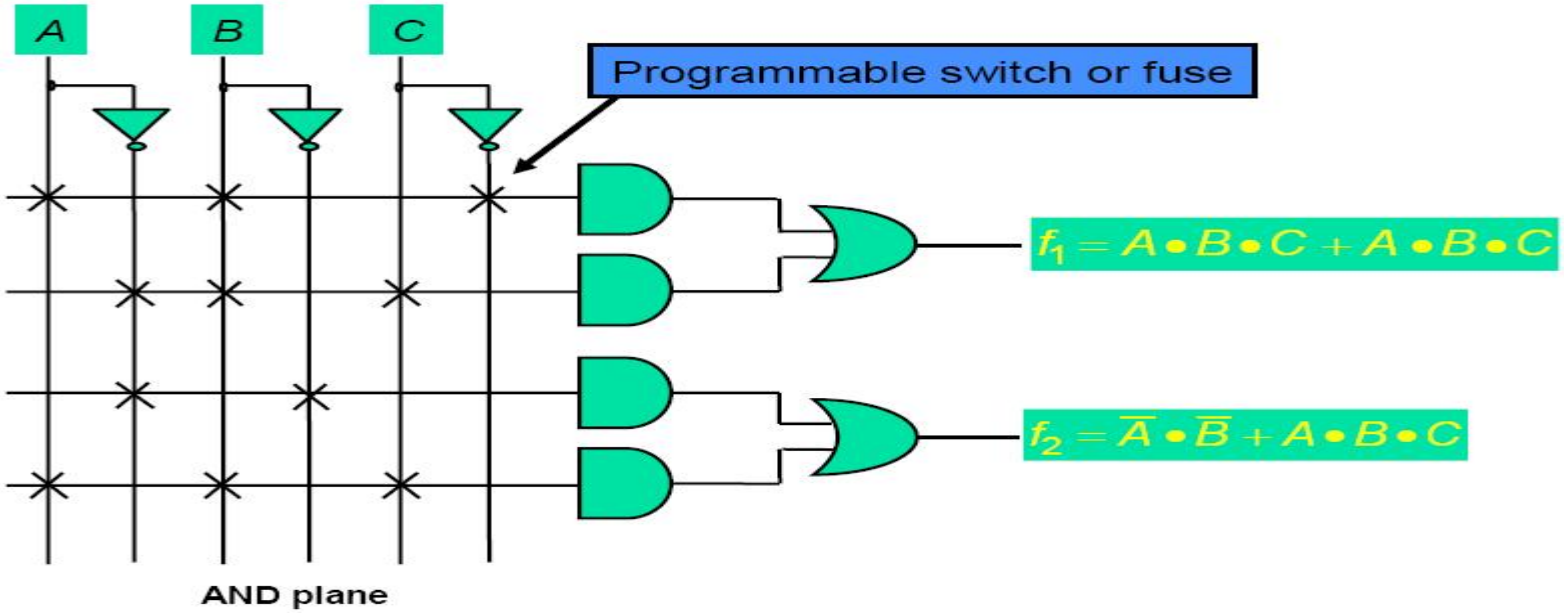


Gate implementation

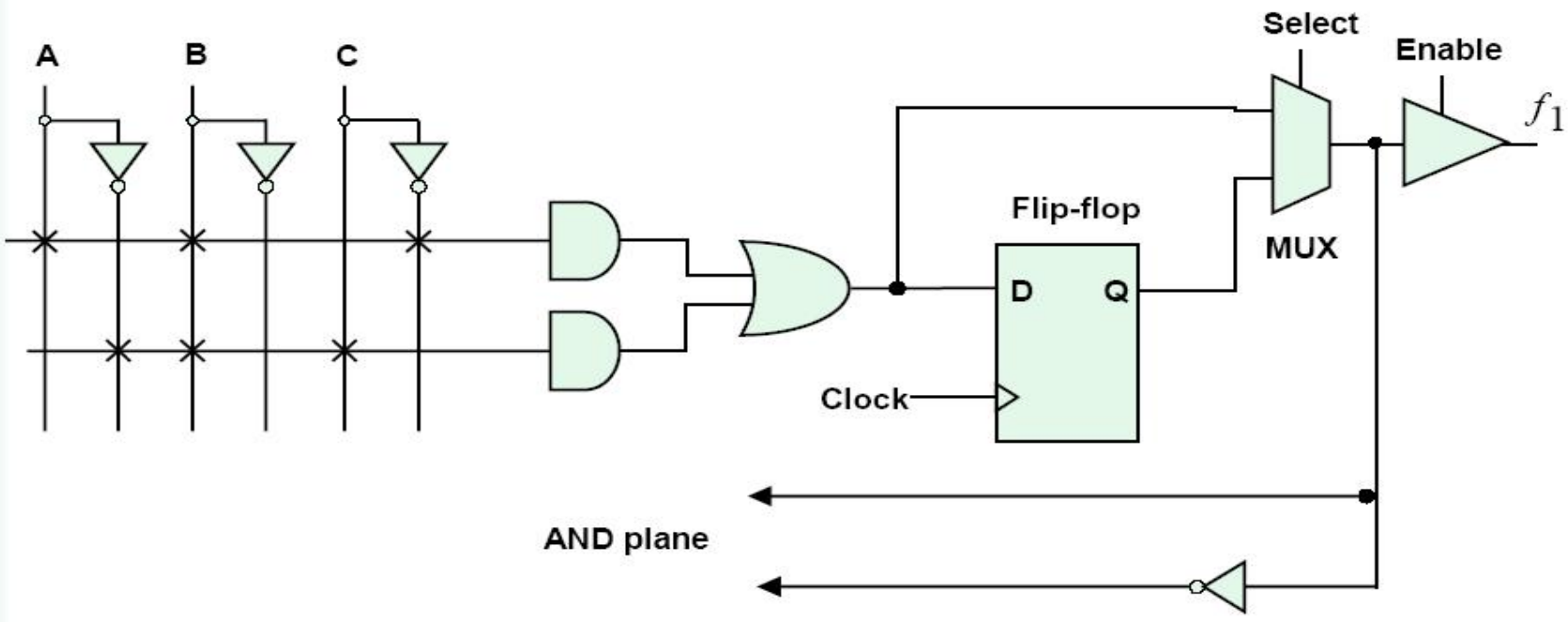
CPLD Architecture and Examples

CPLD – WORKING PRINCIPLE (SOP)

Programmable AND array followed by fixed fan-in OR gates

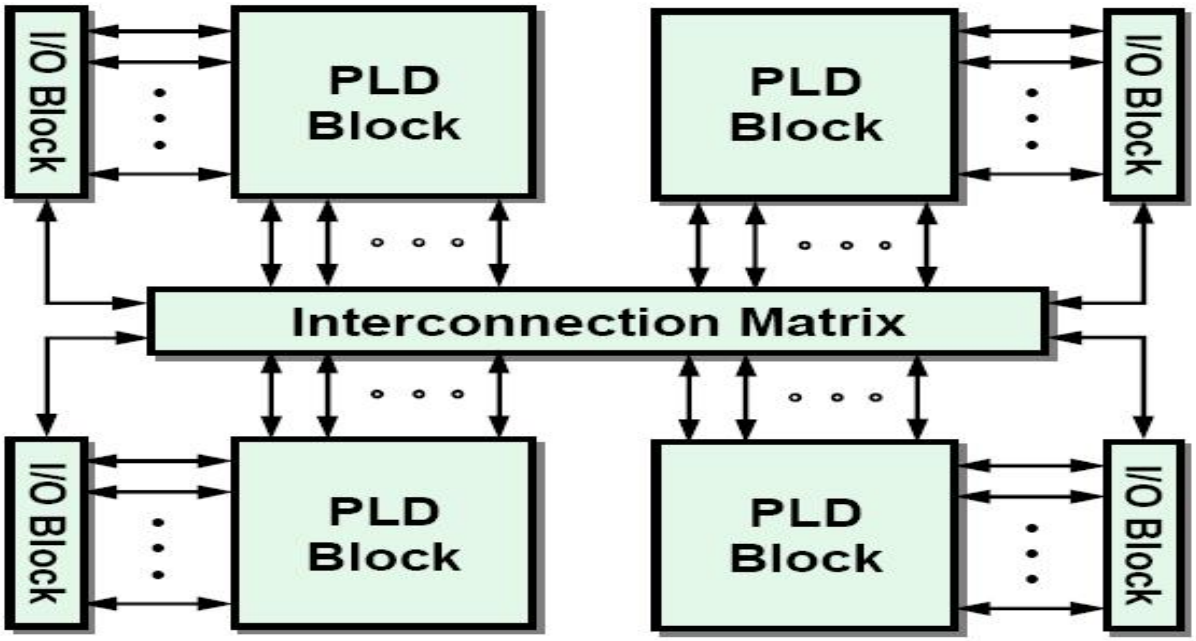


PLD - MACROCELL

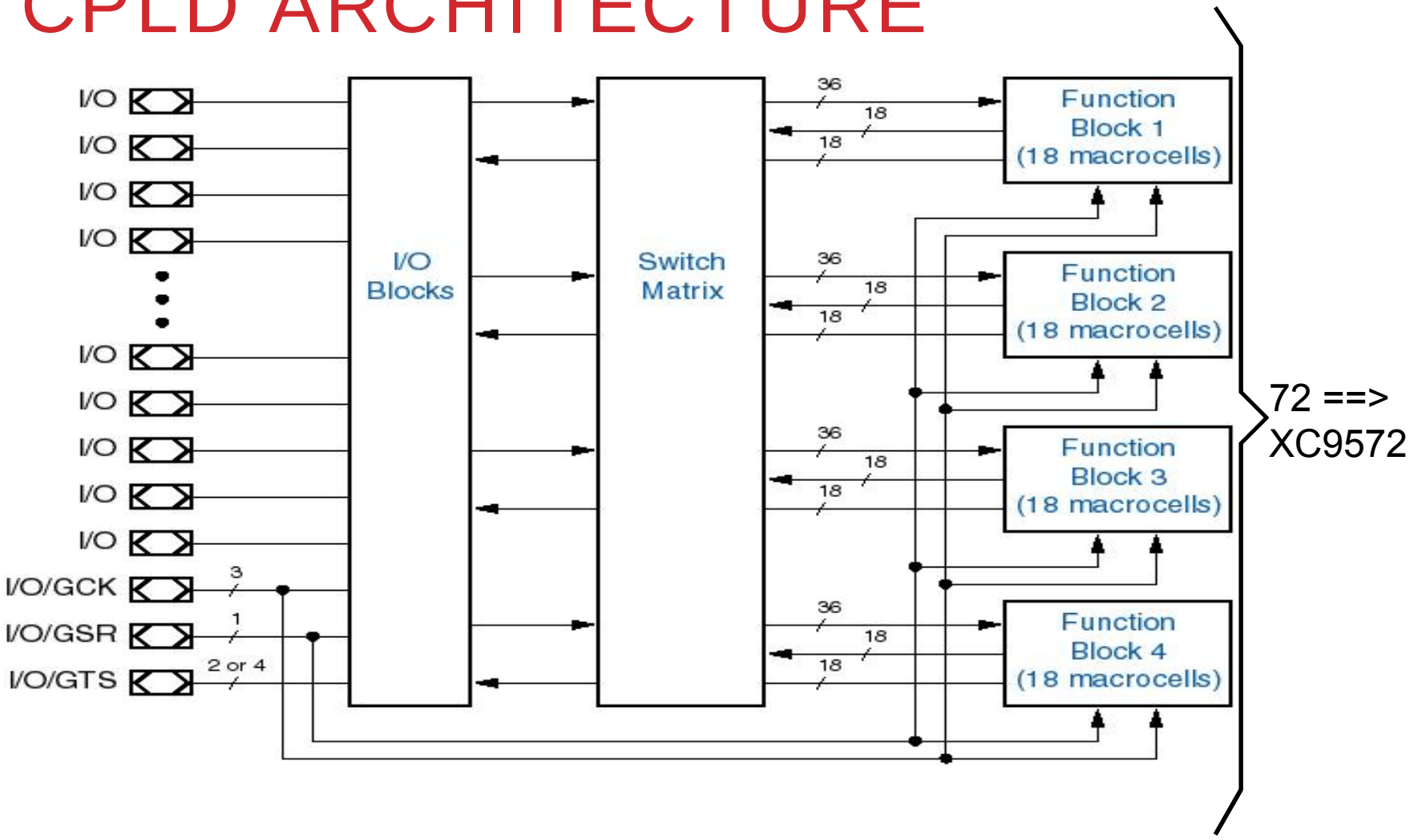


CPLD ARCHITECTURE

Integration of several PLD blocks with a programmable interconnect on a single chip



XILINX 9500-FAMILY CPLD ARCHITECTURE



ARCHITECTURE DESCRIPTION

Each XC9500 device is a subsystem consisting of multiple

- Function Blocks (FBs)
  - Provides programmable logic capability with 36 inputs and 18 outputs.
- I/O Blocks(IOBs)
  - The IOBs provide buffering for device inputs and outputs.
- Fast Connect switch matrix.
  - Connects all FB outputs and inputs signals to the FB inputs.

9500-SERIES MACROCELL (18 PER FB)

Set control

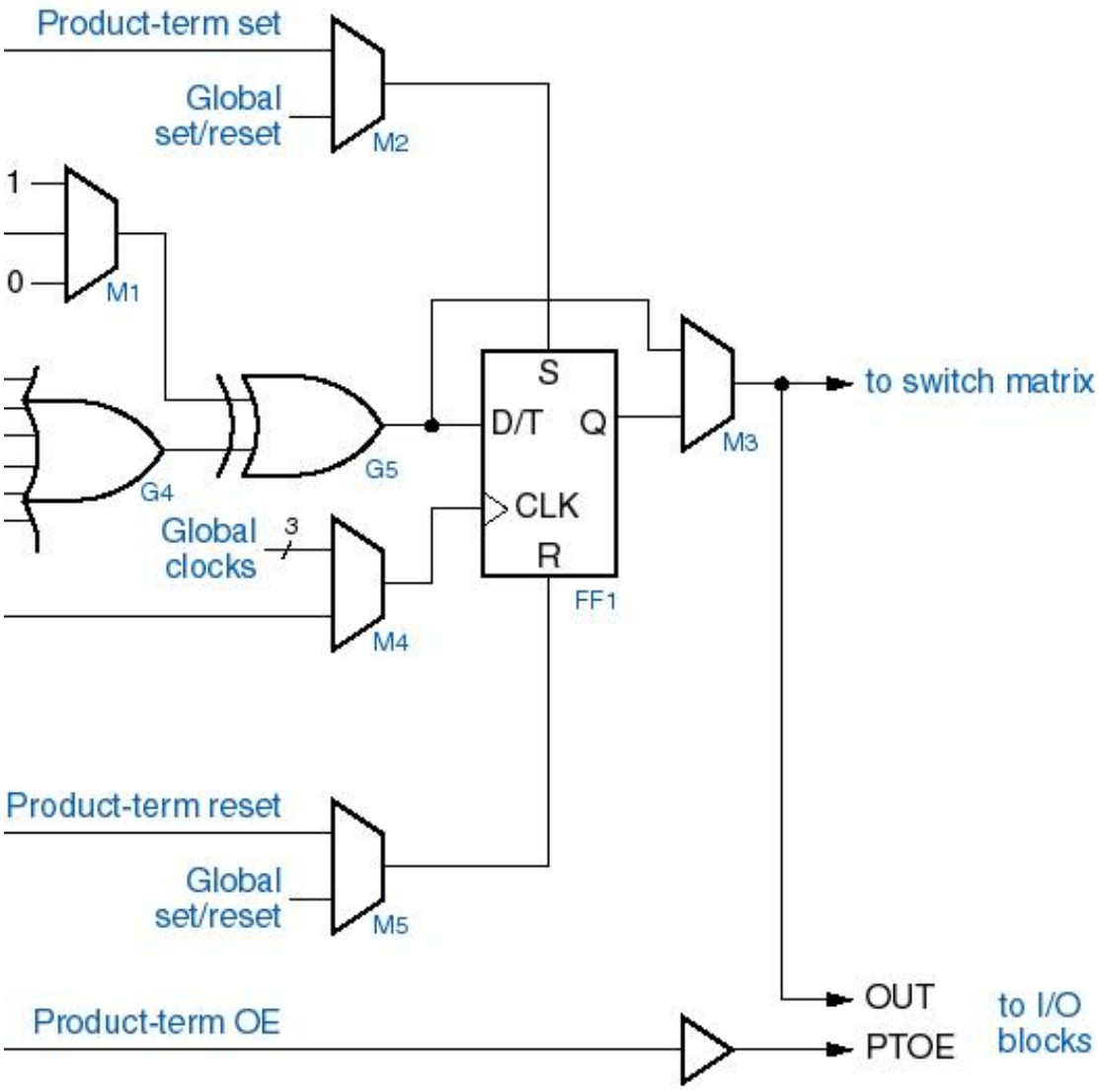
Programmable inversion or XOR product term

Up to 5 product terms

Global clock or product-term clock

Reset control

OE control



TECHNOLOGY USED

CPLD's are non-volatile devices, I.e retain the program after Power-off.

The EPROM, EEPROM, FastFlash are the non-volatile type of memory.

The FastFlash technology is used because of its advantage over the EEPROM.

- High Performance Logic Device.
- High Memory cell density
- Electrical erasable
- High reliability and endurance
- Fast device programming times

XILINX CPLD PRODUCT PORTFOLIO

CoolRunner-II

- **1.8V core**
- 1.5V - 3.3V I/O
- SSTL, HSTL, LVCMOS, LVTTL
- Lower power
  - DataGATE
- Clocking features
  - Clock Divide
  - CoolCLOCK
  - DualEDGE

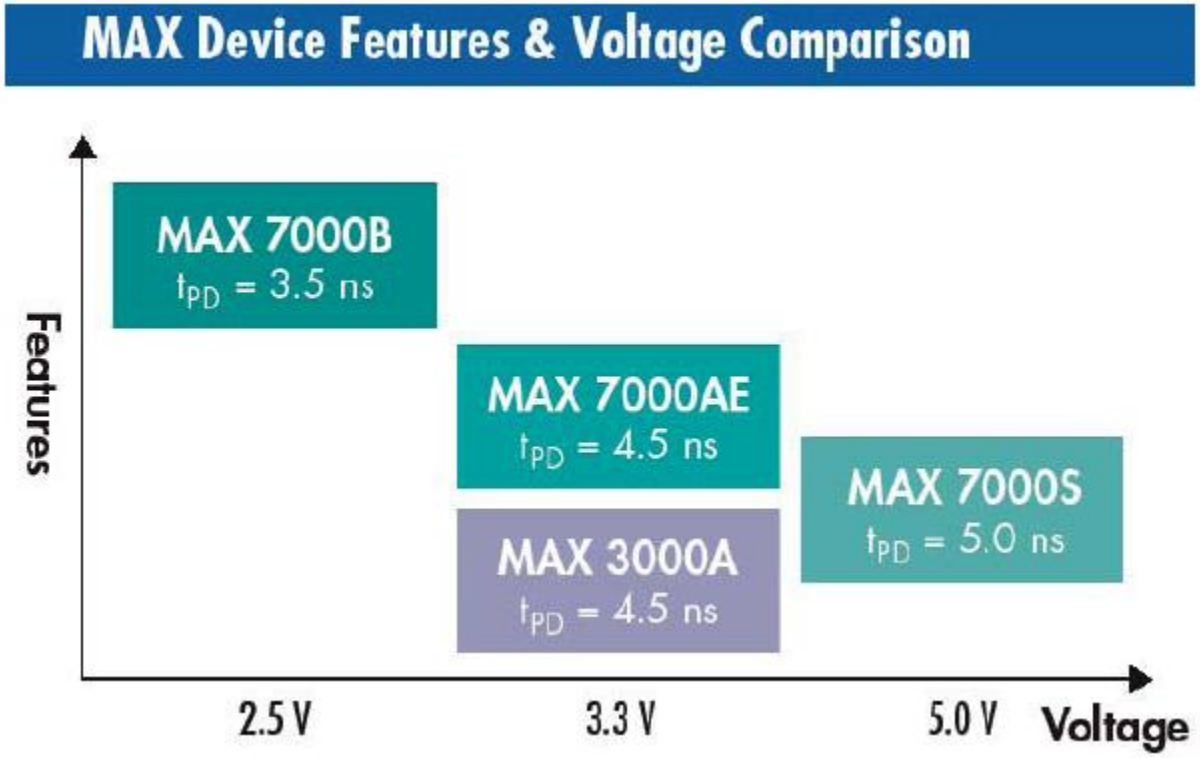
- **2.5V core**
- 1.8V - 3.3V I/O
- LVCMOS, LVTTL
- I/O Banking

XPLA3 CoolRunner

- **3.3V core**
- 2.7V - 5V I/O
- LVCMOS, LVTTL
- Low power
  - Fast Zero Power

- **3.3V core**
- 2.5V - 5.0V I/O
- LVCMOS, LVTTL

ALTERA CPLD PRODUCTS



FPGA Architecture

XILINX VISION: RE-PROGRAMMABLE & FABLESS

- **Ross Freeman**
  - Inventor of the Field Programmable Gate Array
- **Promoted end-user programmability and flexibility at the expense of more transistors**
- **Understood the ultimate implications of Moore's Law**

- **Bernie Vonderschmitt**
  - Pioneer of the Fabless Semiconductor Industry
- **Challenged the assumption that semiconductor companies must be vertically integrated**
- **Fabless semi association now has more than 500 members**

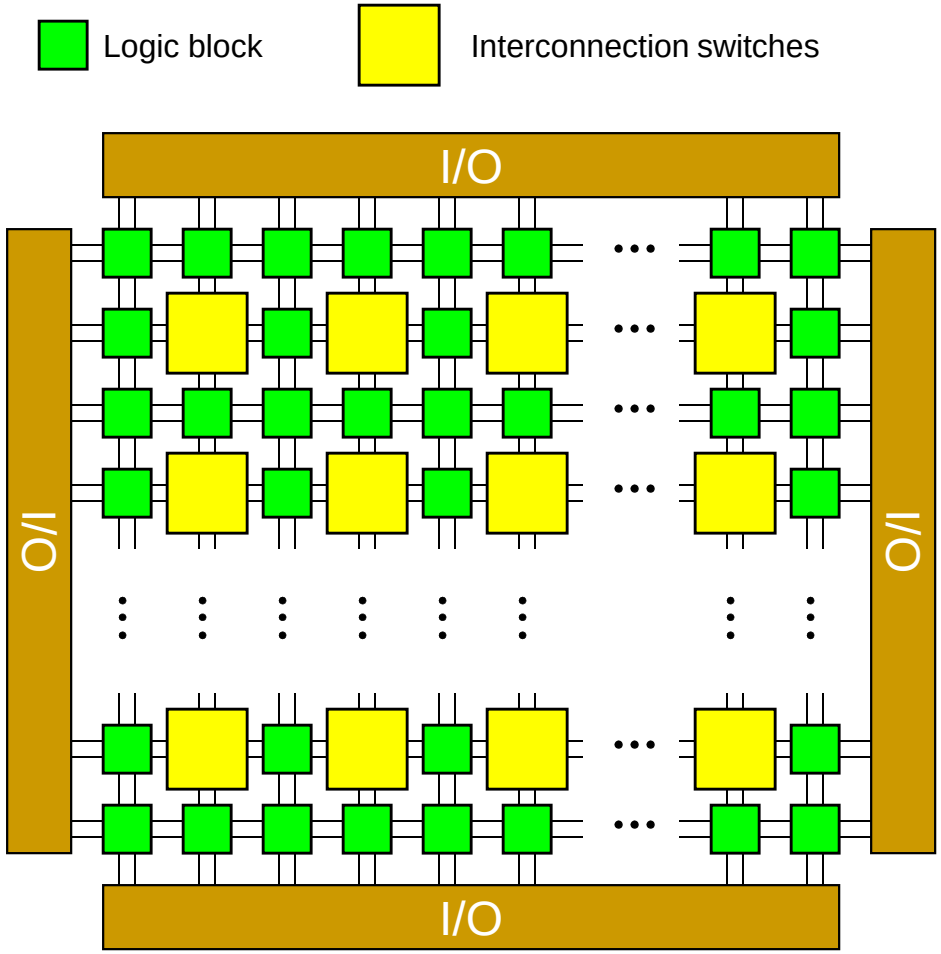
THE FPGA PROPOSITION

- **Xilinx was founded in 1984 on two revolutionary concepts:**
- **Post-fabrication re-programmability by end-users was more important than the cost of increased transistor count in Field Programmable Gate Arrays**
- **A semiconductor company does not need to own an integrated circuit fabrication plant**

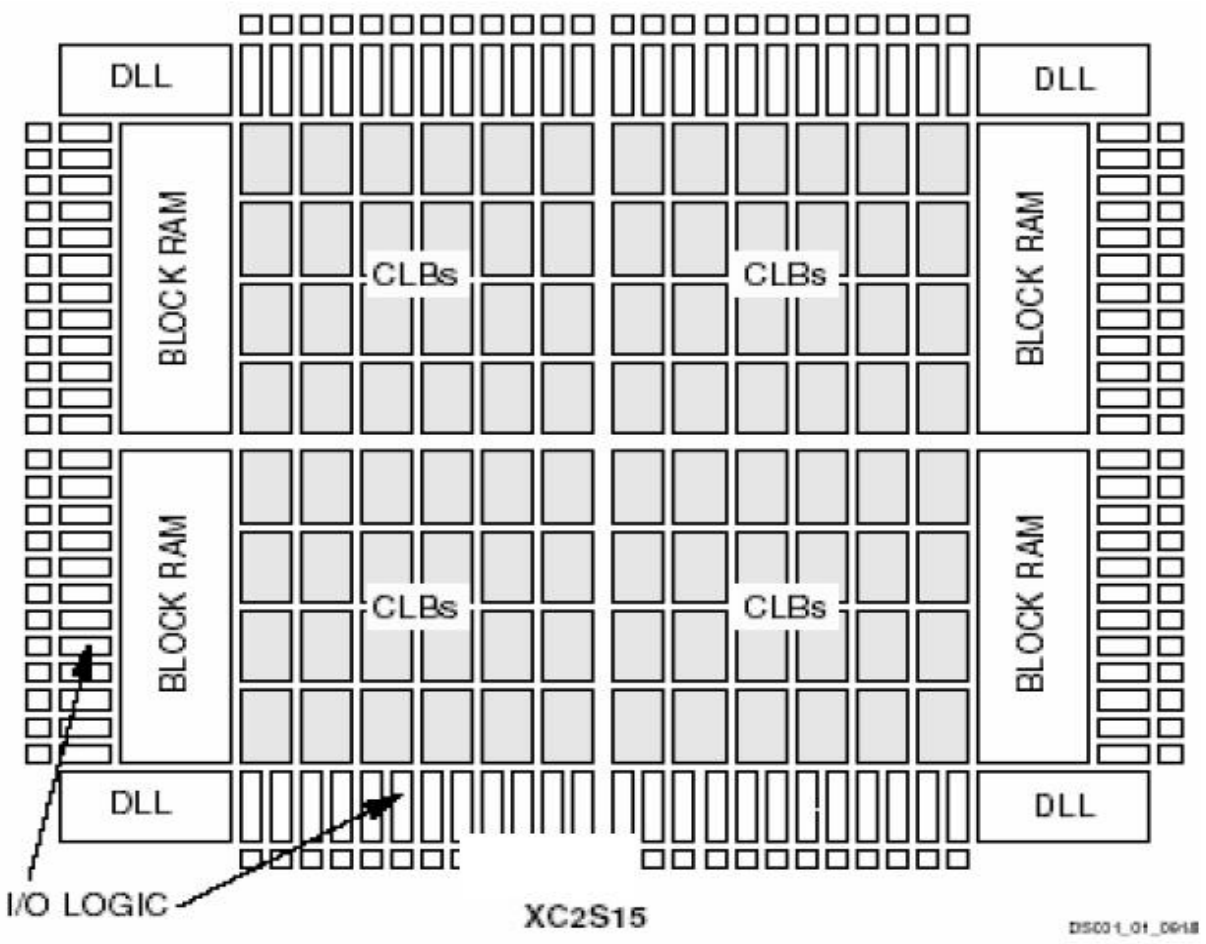
WHAT IS AN FPGA ?

FPGA building blocks:

- **Programmable logic blocks Implement combinatorial and sequential logic**
- **Programmable interconnect Wires to connect inputs and outputs to logic blocks**
- **Programmable I/O blocks Special logic blocks at the periphery of device for external connections**



FPGA BLOCK DIAGRAM



OTHER FPGA BUILDING BLOCKS

- **Clock distribution**
- **Embedded memory blocks**
- **Special purpose blocks:**
  - DSP blocks:
    - Hardware multipliers, adders and registers
  - Embedded microprocessors/microcontrollers
  - High-speed serial transceivers

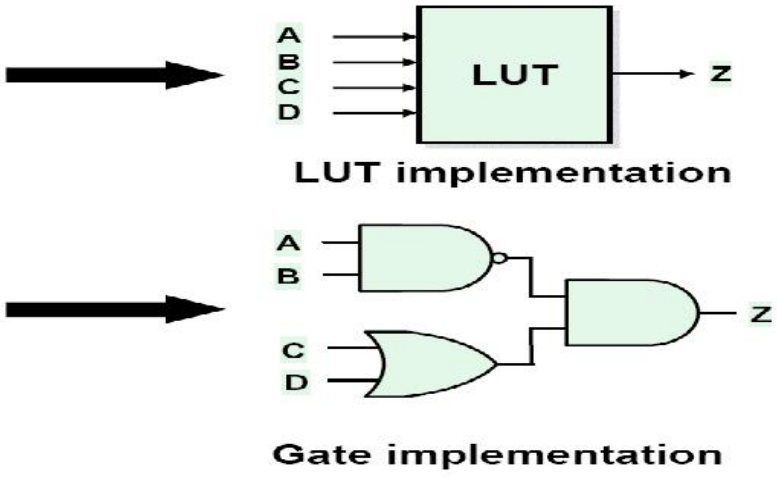
FPGA - WORKING PRINCIPLE (LUT)

Look-up table with N-inputs can be used to implement any combinatorial function of N inputs

LUT is programmed with the truth-table

A	B	C	D	Z
0	0	0	0	**0**
0	0	0	1	**1**
0	0	1	0	**1**
0	0	1	1	**1**
0	1	0	0	**0**
0	1	0	1	**1**
0	1	1	0	**1**
0	1	1	1	**1**
1	0	0	0	**0**
1	0	0	1	**1**
1	0	1	0	**1**
1	0	1	1	**1**
1	1	0	0	**0**
1	1	0	1	**0**
1	1	1	0	**0**

Truth-table

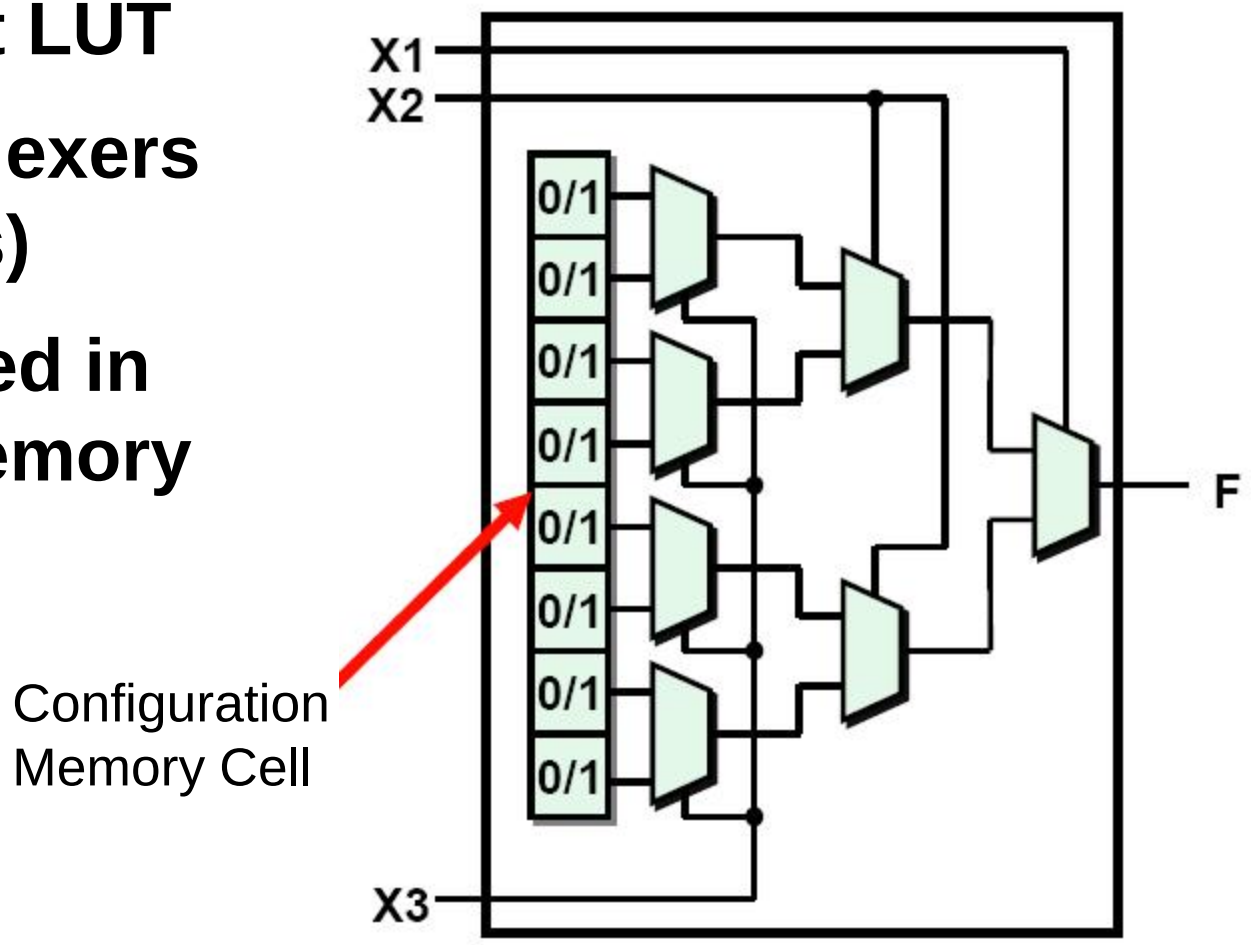


MUX BASED LUT

Example: 3-input LUT

Based on multiplexers (pass transistors)

LUT entries stored in configuration memory cells



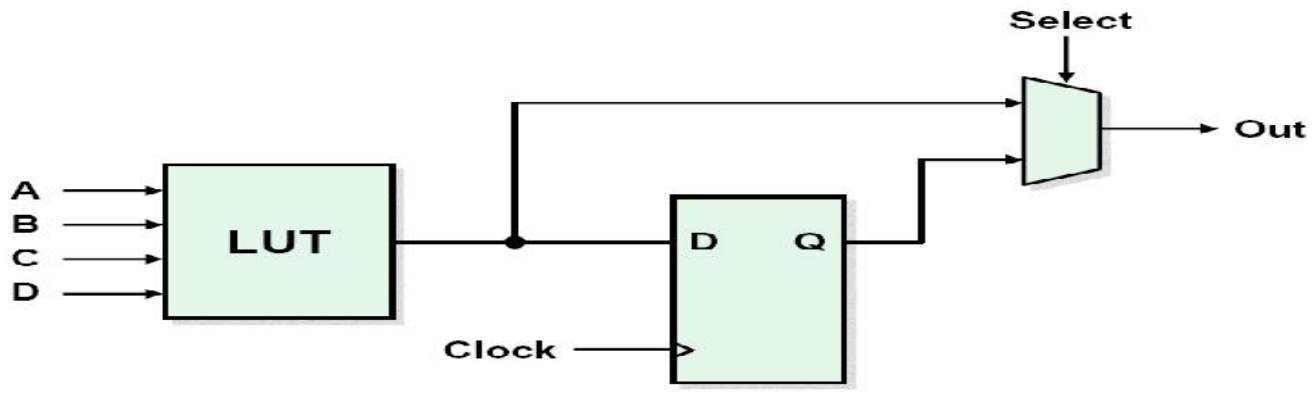
FPGA – BASIC LOGIC ELEMENT

LUT to implement combinatorial logic

Register for sequential circuits

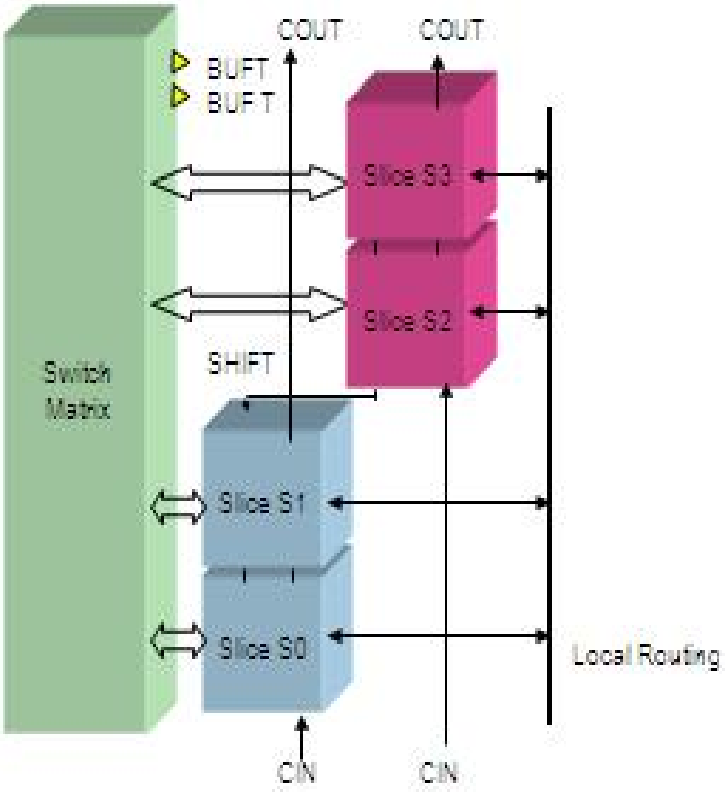
Additional logic (not shown):

- Carry logic for arithmetic functions
- Expansion logic for functions requiring more than 4 inputs



LOGIC RESOURCES

- **Slices contain logic resources and are arranged in two colums**
- **A switch matrix provides access to general routing resources**
- **Local routing provides connection between slices in the same CLB, and it provides routing to neighboring CLBs**



Virtex-II CLB contains four slices

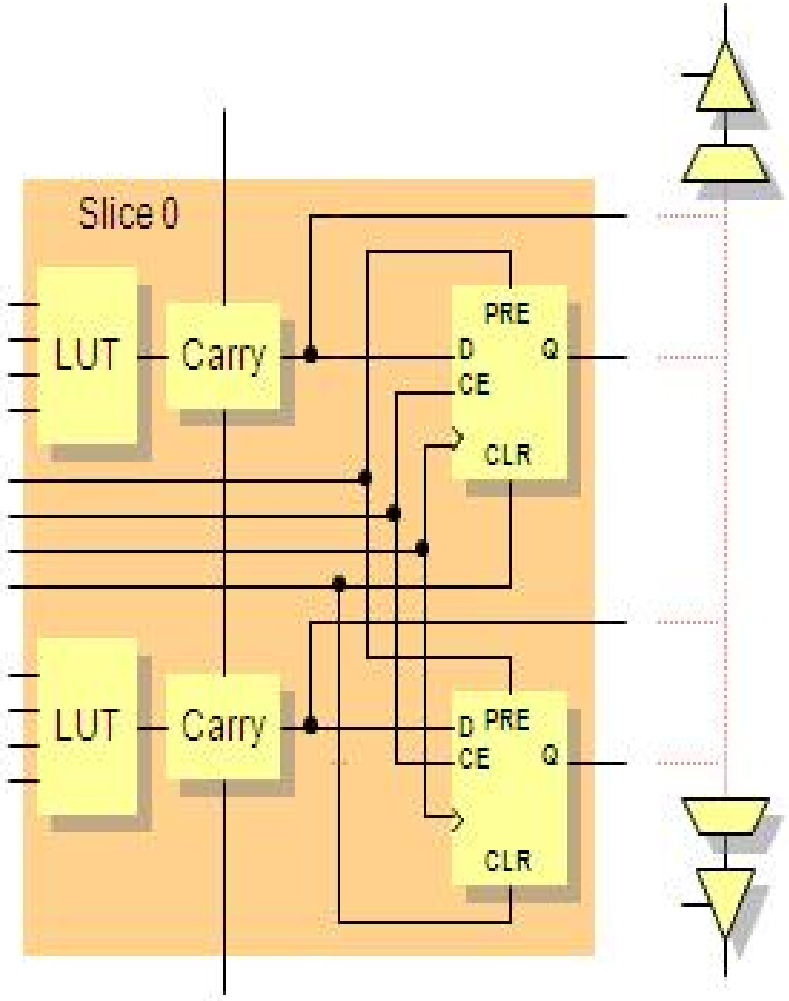
LOGIC RESOURCES

Each slice has four outputs

- Two registered outputs, two non-registered outputs
- Two BUFTs associated with each CLB, accessible by all 16 CLB outputs

Carry logic runs vertically, up only

- Two independent carry chains per CLB



MEMORY RESOURCES

Distributed RAM:

Synchronous write

Asynchronous read

- Accompanying flip-flops can be used to create synchronous read

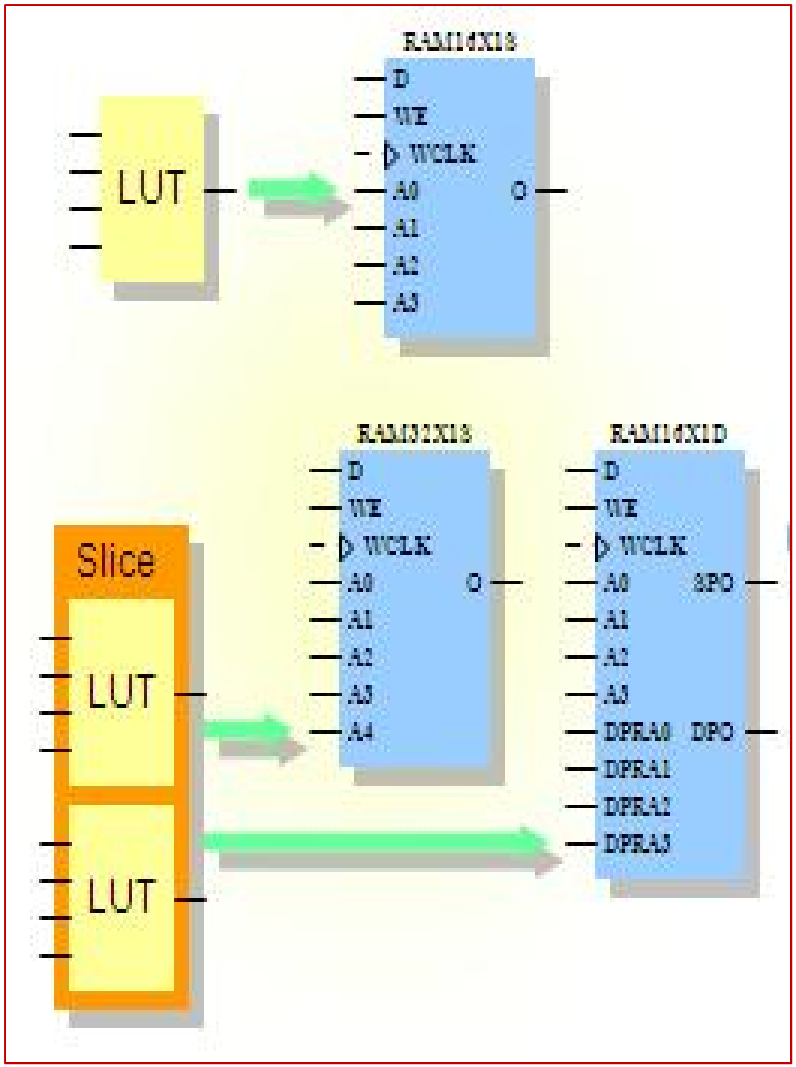
RAM and ROM are initialized during configuration

- Data can be written to RAM after configuration

Emulated dual-port RAM

- One read/write port
- One read-only port

1 LUT = 16 RAM bits



Block RAM:

Up to 3.5 Mb of RAM in 18-kb blocks

- Synchronous read and write

True dual-port memory

- Each port has synchronous read and write capability
- Different clocks for each port

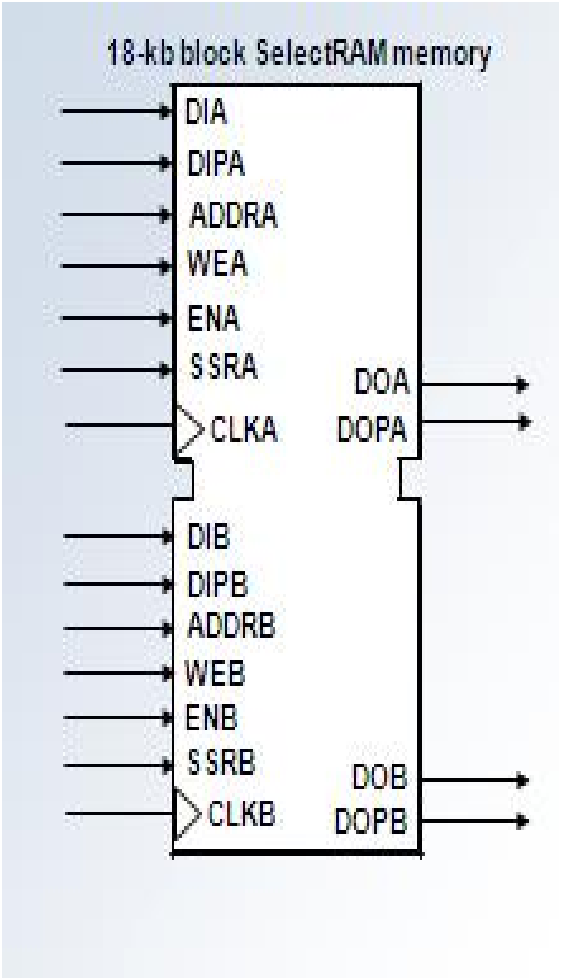
Supports initial values

Synchronous reset on output latches

Supports parity bits

- One parity bit per eight data bits

Situated next to embedded multiplier for fast multiply-accumulate operations



CLOCK RESOURCES :DCM

Up to twelve DCMs per device

- Located on the top and bottom edges of the die
- Driven by clock input pads

DCMs provide the following:

- Delay-Locked Loop (DLL)
- Digital Frequency Synthesizer (DFS)
- Digital Phase Shifter (DPS)

Up to four outputs of each DCM can drive onto global clock buffers

- All DCM outputs can drive general routing

FPGA VENDORS & DEVICE FAMILIES

Xilinx

- Virtex -7/Kintex 7 Ultrascale+ - 16nm, FinFET node based
- Virtex -7/ Kintex 7 Ultrascale – High performance serial I/O and bandwidth and logic capacity
- Zynq – All Programmable SoC FPGA
- Virtex-II/Virtex-6: Feature-packed high-performance SRAM-based FPGA
- Spartan 3/3E/3A: low-cost feature reduced version
- CoolRunner: CPLDs

Altera

- Arria Series – High performance and feature rich FPGAs
- Stratix Series
  - High-performance SRAM-based FPGAs
- Cyclone Series
  - Low-cost feature reduced version for cost-critical applications
- MAX Series FPGAs
  - non-volatile integration & advanced processing capabilities in a low-cost, single chip small form factor programmable logic device

Actel

- Anti-fuse based FPGAs
  - Radiation tolerant
- Flash-based FPGAs

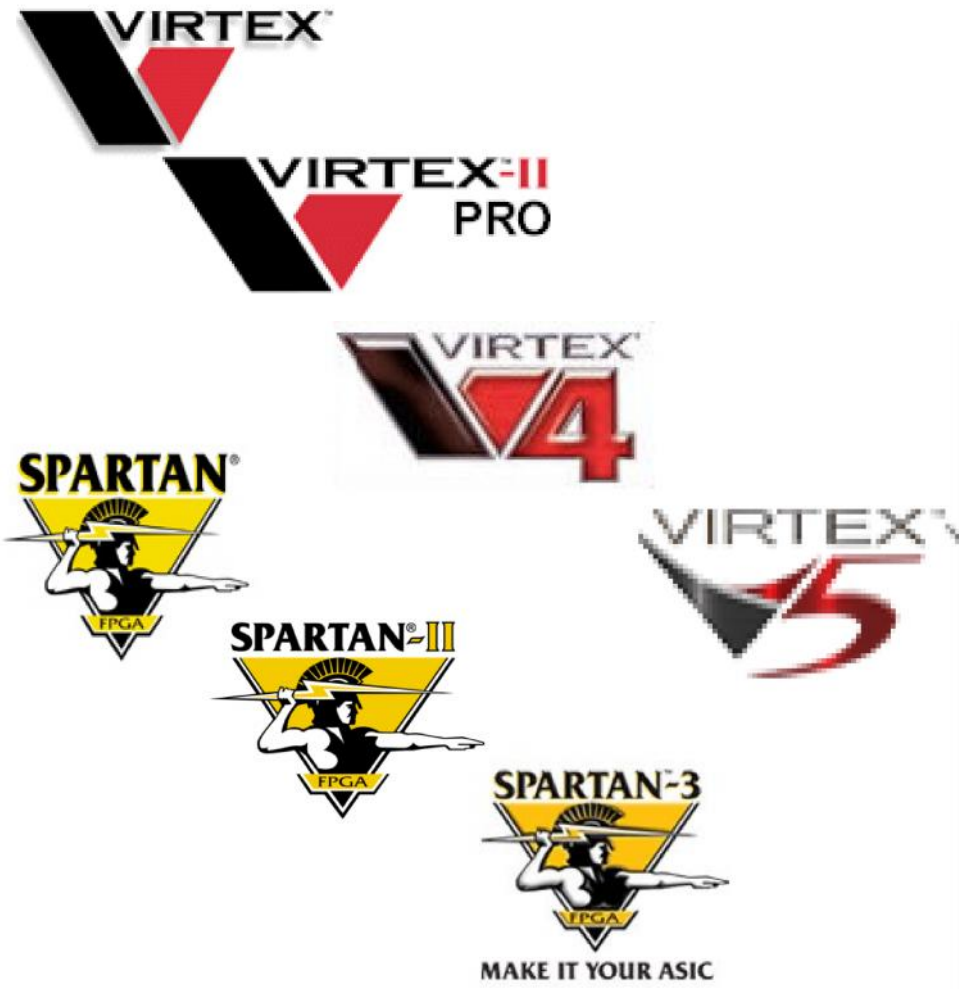
Lattice

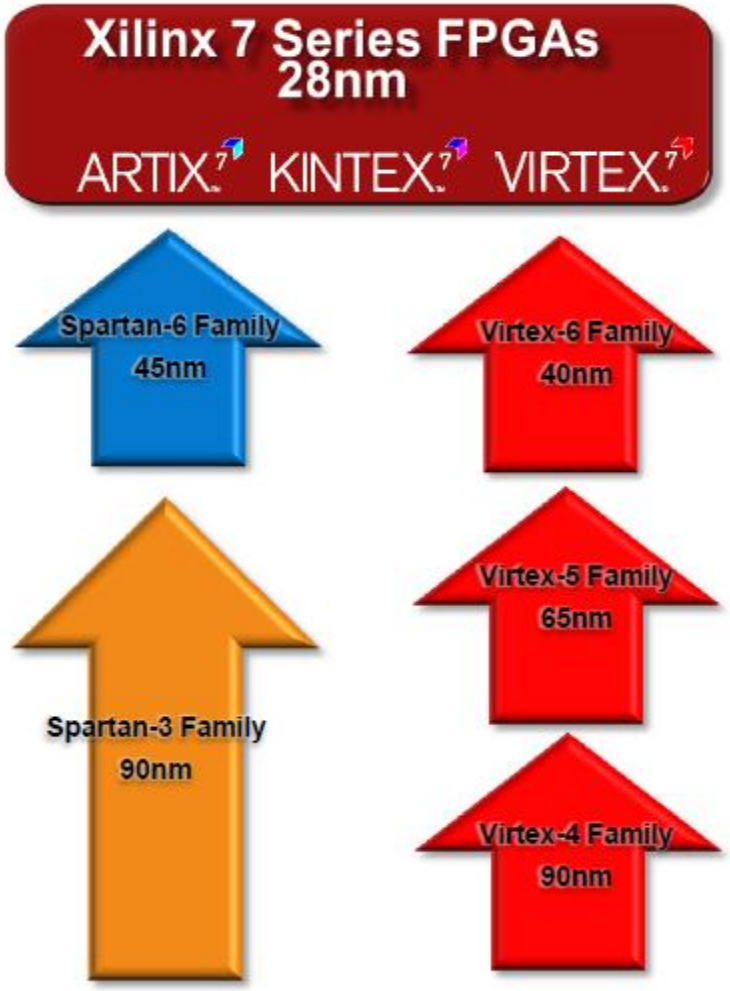
- Flash-based FPGAs
- CPLDs (EEPROM)

QuickLogic

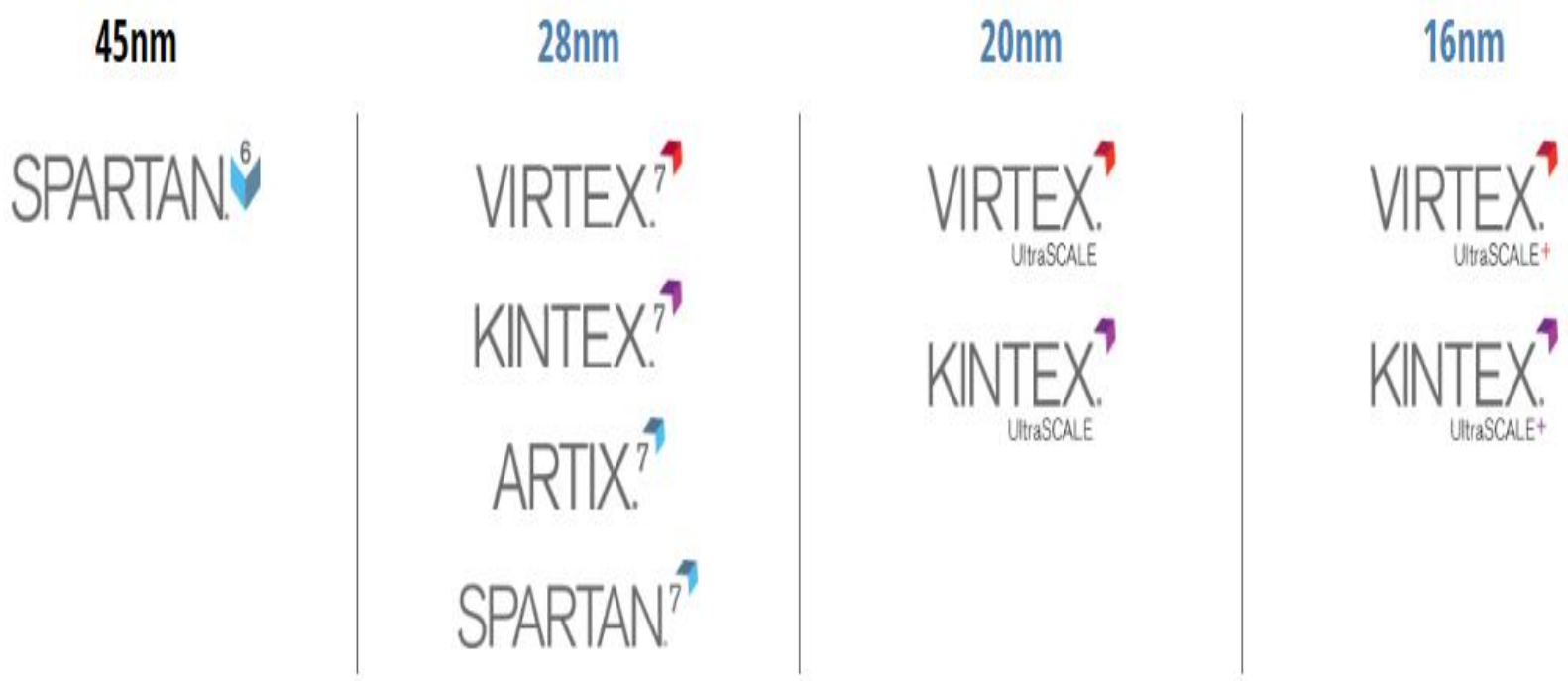
- ViaLink-based FPGAs

XILINX FPGA FAMILIES

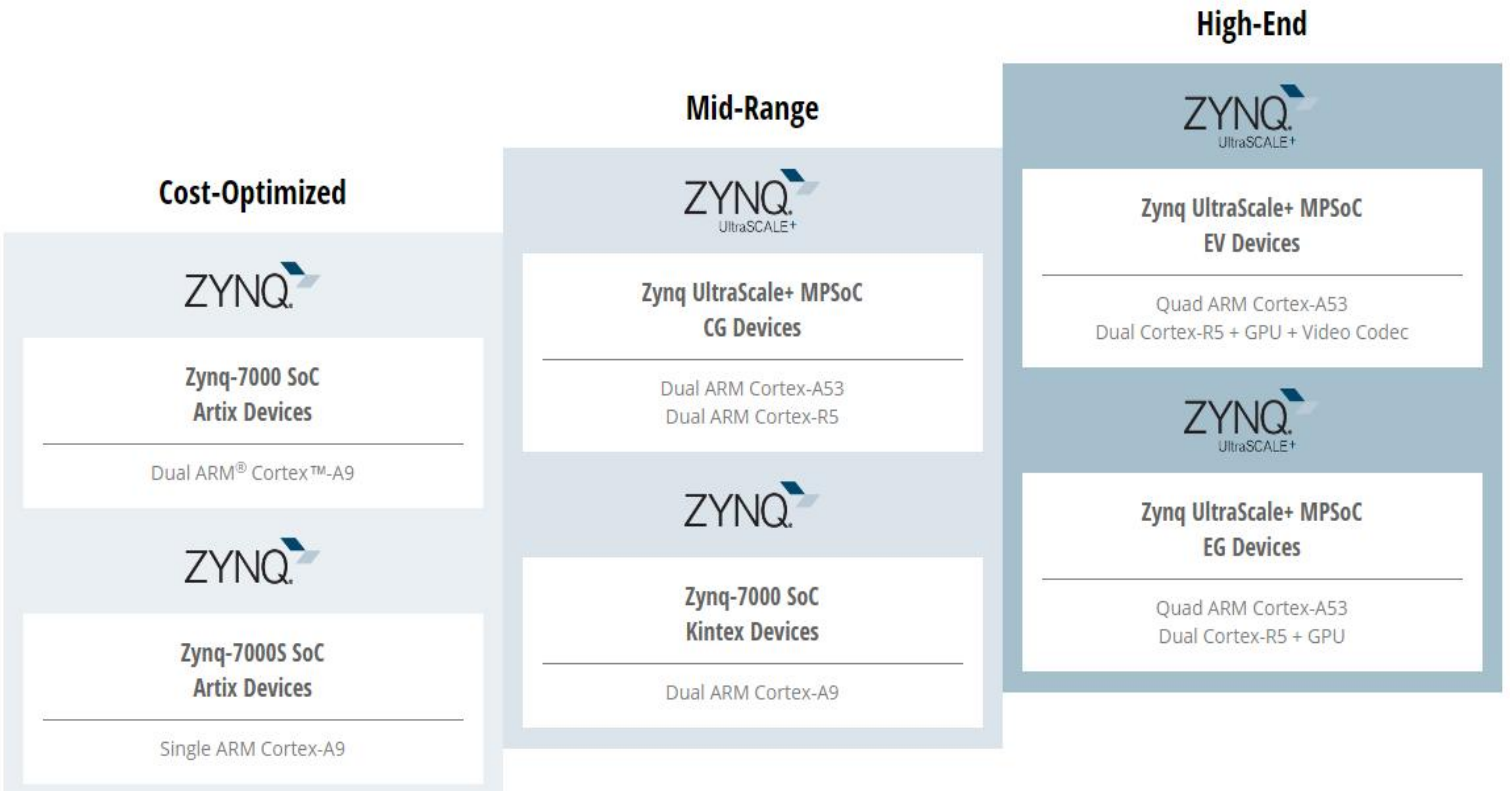




XILINX FPGA FAMILIES

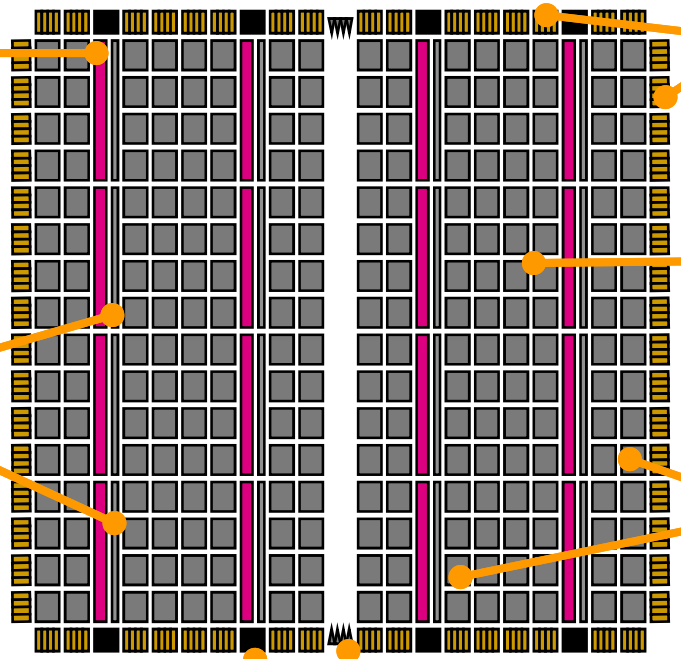


XILINX FPGA FAMILIES



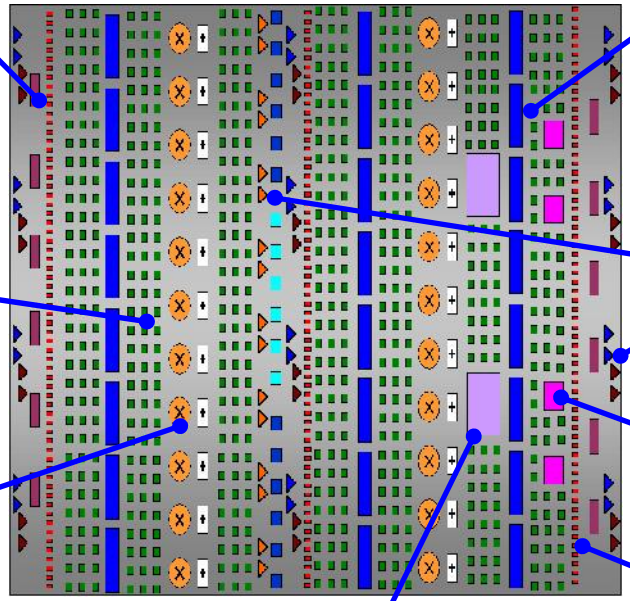
VIRTEX-II ARCHITECTURE

First FPGA Device to include embedded multipliers



- **Virtex™-II architecture's core voltage operates at 1.5V**

VIRTEX-4 ARCHITECTURE



RocketIO™ Multi-Gigabit Transceivers
622 Mbps–10.3 Gbps

Advanced CLBs
200K Logic Cells

XtremeDSP™ Technology Slices
256 18x18 GMACs

PowerPC™ 405 with APU Interface
450 MHz, 680 DMIPS

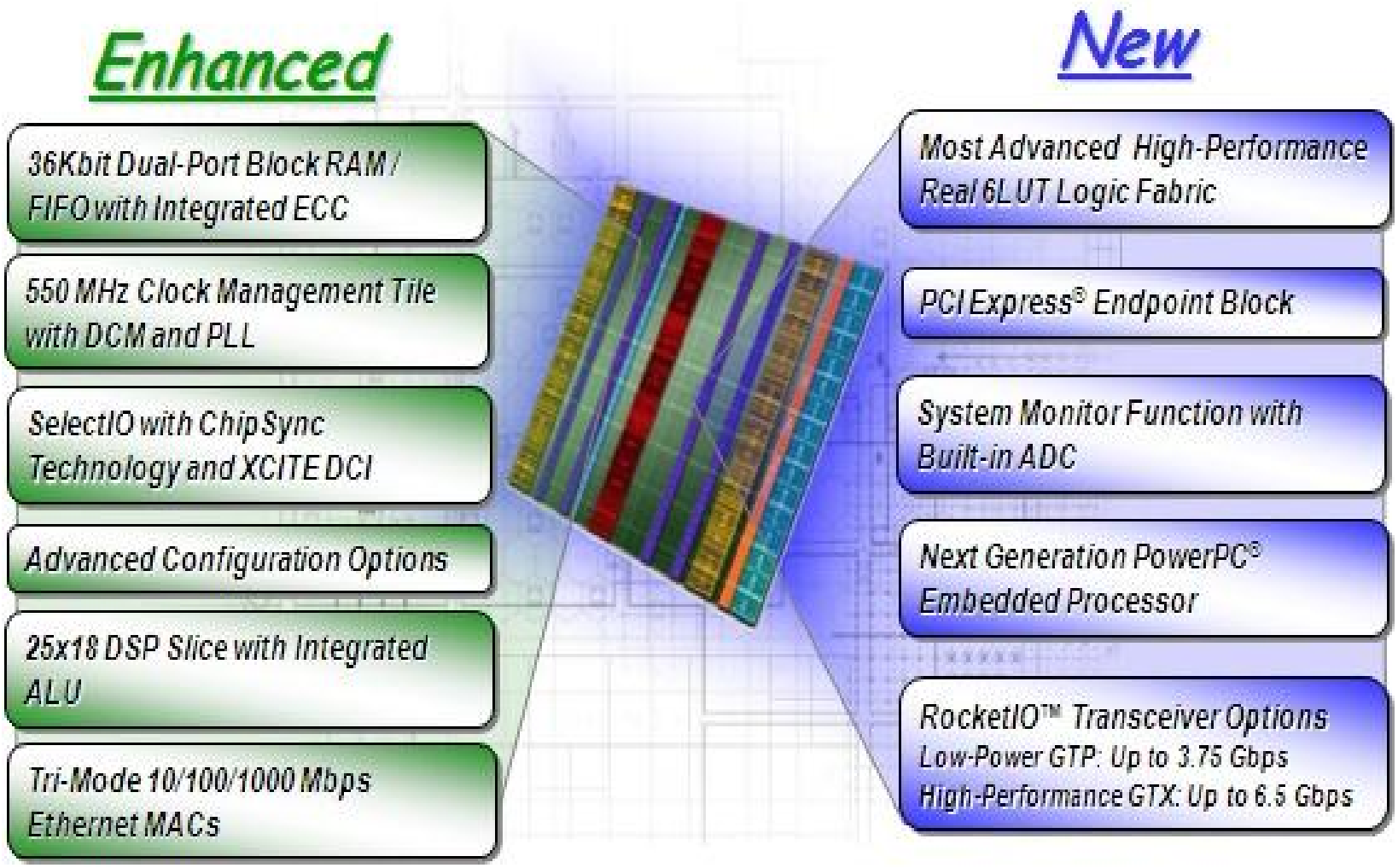
Smart RAM
New block RAM/FIFO

Xesium Clocking Technology
500 MHz

Tri-Mode Ethernet MAC
10/100/1000 Mbps

1 Gbps SelectIO™
ChipSync™ Source synch, XCITE Active Termination

VIRTEX-5 ARCHITECTURE

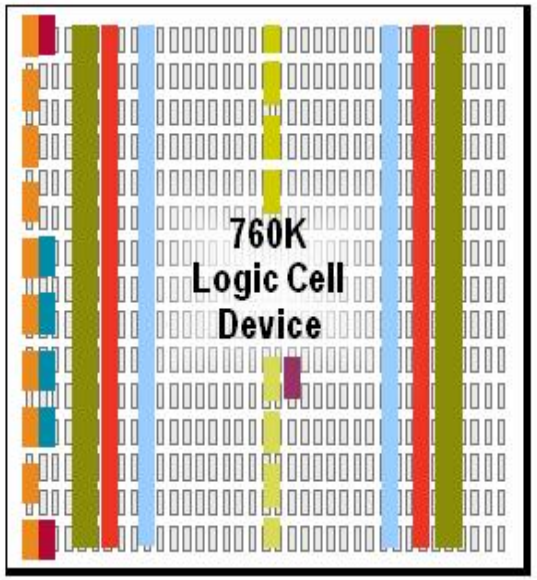


LATEST DEVICES FROM XILINX

- Virtex-6 Family
- Spartan-6 Family
- Virtex-7 Family
- Ultrascale
- Ultrascale+
- Zynq – All Programmable SoC

ARCHITECTURE

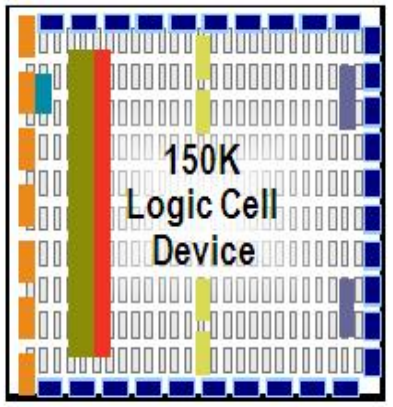
Virtex-6 FPGAs



Common Resources

- LUT-6 CLB
- BlockRAM
- DSP Slices
- High-performance Clocking
- Parallel I/O
- HSS Transceivers*
- PCIe® Interface

Spartan-6 FPGAs



- FIFO Logic
- Tri-mode EMAC
- System Monitor
- Hardened Memory Controllers
- 3.3 Volt compatible I/O

VIRTEX-6 FPGA FAMILY BENEFITS

Achieve a one speed-grade performance gain with second-generation ExpressFabric™ technology, 600MHz clocking technology and performance-tuned IP blocks

Build high-bandwidth interfaces for DDR3 memory with flexible SelectIO™ technology

Accelerate DSP performance with DSP48E1 slices

Advanced 40nm process, architecture, tools, and system level optimizations reduce core power by 30%

Low-voltage option increases power savings by 50% without significant performance penalties

Enhanced SelectIO technology reduces I/O power by up to 50%

VIRTEX® PRODUCT & PROCESS EVOLUTION

Delivering Balanced Performance, Power, and Cost

SPARTAN-6 FPGA FAMILY BENEFITS

Increase system performance with efficient, dual-register 6-input LUT (look-up-table) logic structure

Implement PCI Express with integrated endpoint blocks

Get connected with up to 8 low power (150 mW per) 3.125 Gbps GTP serial transceivers

Support access rates of up to 800 Mbps using integrated memory controllers

Build DSP applications using low-power 250 MHz DSP48A1 slices with 18 x 18 multipliers

Use multi-voltage, multi-standard SelectIO™ banks with low cost HSTL and SSTL memory interfaces

Clock management tiles, each consisting of 2 DCMs and 1 PLL

1000 MHz clocking

VIRTEX-7 FPGA FAMILY

Virtex®-7 FPGAs are optimized for advanced systems requiring the highest performance and highest bandwidth connectivity.

The Virtex-7 family delivers 2x higher system performance and 50% lower power consumption than previous generation FPGAs.

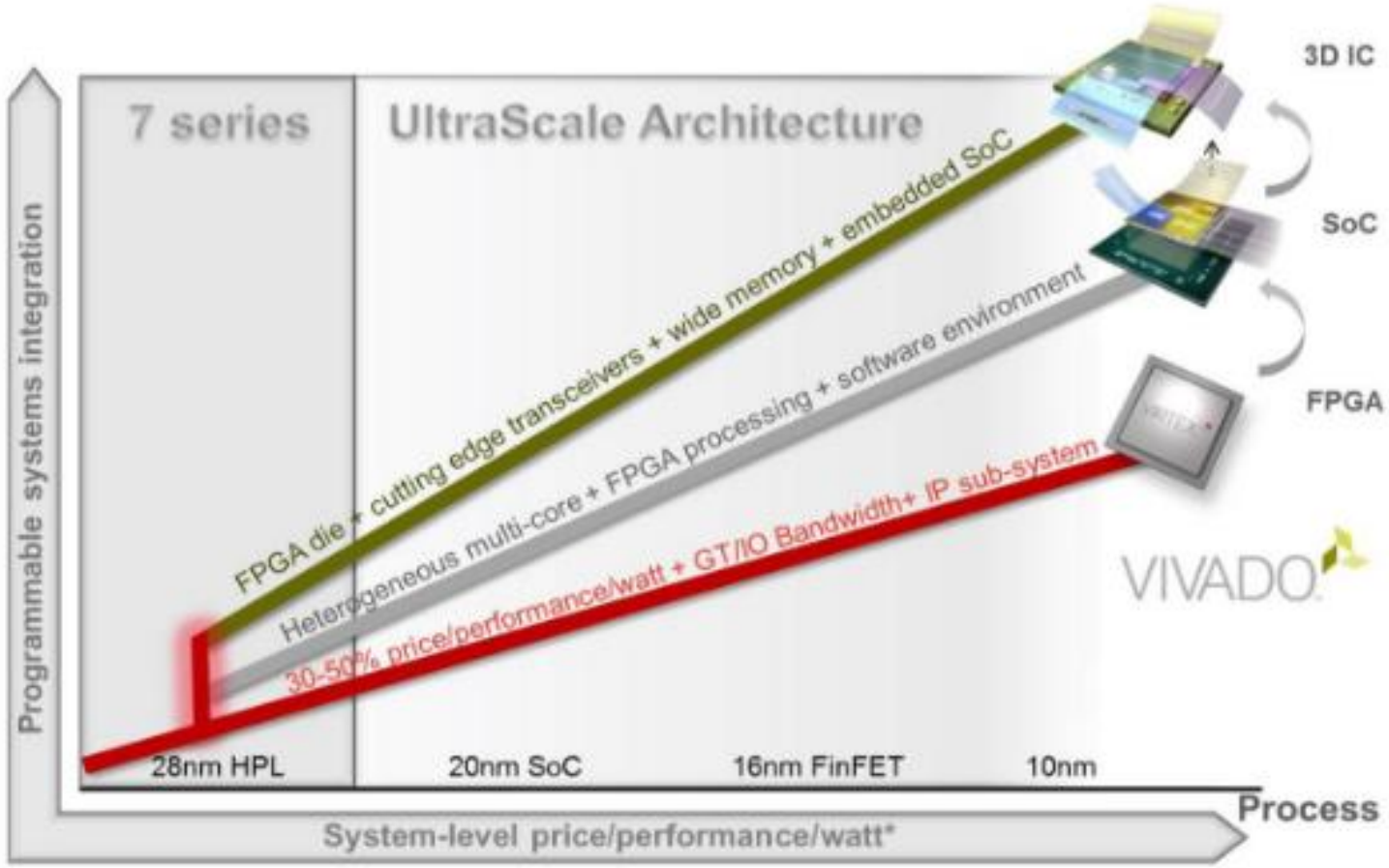
Delivering up to 2 million logic cells, 85Mbits of internal memory, 6.7 Tera-MACS DSP throughput, 2.8 Tb/s serial bandwidth, and fully integrated Agile Mixed Signal capability

Virtex-7 FPGAs are ideally suited for highest performance wireless, wired, and broadcast infrastructure equipment, aerospace and defense systems, high-performance computing, as well as ASIC prototyping and emulation.

UNIFIED XILINX FPGA FAMILY ARCHITECTURE

Series 7 Family	Artix	Kintex	Virtex
Market	Lowest Power & Cost	Best Price/Performance	Highest System Performance
Logic Cells	20K - 355K	30K - 410K	285K - 2,000K
Memory Kbits	720 - 12,060 Kbits	2,340 - 28,620 Kbits	14,760 - 64,800 Kbits
DSP Slices	40 - 700	120-1,540	700 - 3,960
Max Transceivers	3.75 Gbps	6.6 Gbps 10.3 Gbps	10.3 Gbps 13.1 Gbps 28.0 Gbps
External Memory Performance	800 Mbps	2,133 Mbps	2,133 Mbps
Max Select IO	450	500	1200
Select IO Voltages	3.3V and below	3.3V and below 1.8V and below	3.3V and below 1.8V and below
Relative Static Power	.5x	1.0x	1.0x
Relative Performance	.65x	1.0x	1.0x

ULTRASCALE AND ULTRASCALE+ FAMILY



* *System level combines unit with BOM cost*

Comparison of CPLD/FPGA Architecture

CPLD VS FPGA

Interconnect structure.

In-system performance.

Logic Utilization.

Applications.

INTERCONNECT STRUCTURE

CPLD uses a Continuous interconnect structure :

- Consists of metal lines of uniform length traverse the entire length and width of the device.
- Since the resistances and capacitances of all interconnect paths is fixed, delays between any two logic cells can be predictable.
- This minimizes the logic skew.

FPGA uses a segmented interconnect structure.

- Consists of matrix of metal interconnects that run throughout the device. Switch matrices or Antifuses join the ends of these segments allowing signals to travel between logic cells.
- Number of segments required to interconnect signals is neither constant nor predictable, so delays are not fixed or specified until place and route is Completed.

LOGIC UTILIZATION

Logic cells in most FPGA architecture have fine granularity, therefore more logic cells are required to implement a function in FPGA than in a CPLD.

Logic cells in FPGA can contain only small portion of a design, so a heavy burden is placed on its segmented interconnect structure.

As design complexity increases, the probability of routing conflicts also increases leading to lower FPGA device utilization.

Logic density in FPGA is less due to only 9 variables, where as CPLD has 36 variables available.

APPLICATIONS - FPGAS

FPGAs

- Basically register intensive applications.
- Data paths.
- Hardware Emulation.
- Image controller.
- Battery powered applications.
- Field-test equipments.
- Gate-array prototyping.

APPLICATIONS - CPLDS

CPLDs

- Basically combinatorial functions.
- Bus interfacings.
- Comparators.
- High-speed wide decoders.
- Large fast state micro controllers.
- High speed GLUE Logic.
- System video controller.
- PAL integration.

WHY TO GO FOR PLD'S ?

Flexibility.

In system programmability.

Less project development time.

Best prototyping solution.

Cost effective solutions.

Involves less risk.

Design security.

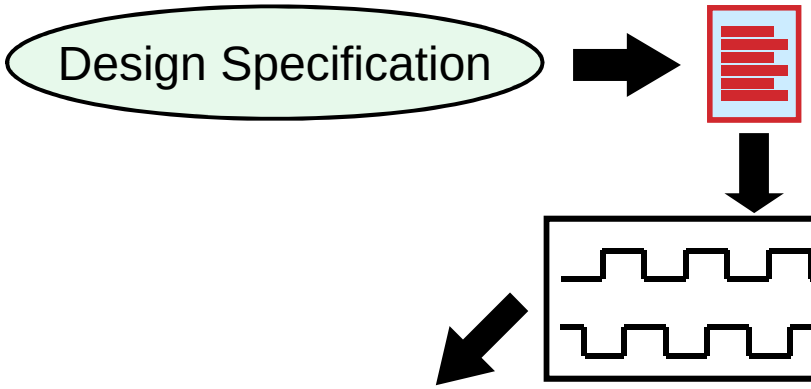
Consumes less board area.

Reconfigurable computing.

Best suits hardware verification for design.

FPGA Design Flow

FPGA DESIGN FLOW



Design Entry/RTL Coding

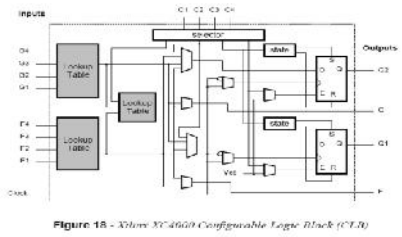
Behavioral or Structural Description of Design

RTL Simulation

- Functional Simulation
- Verify Logic Model & Data Flow (No Timing Delays)

Synthesis

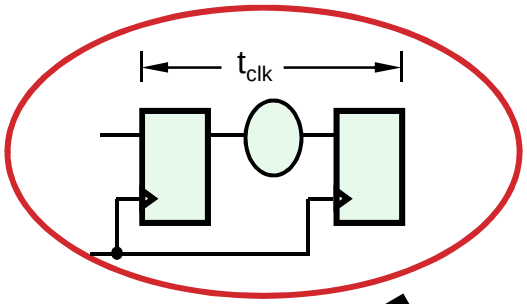
- Translate Design into Device Specific Primitives
- Optimization to Meet Required Area & Performance Constraints



Place & Route

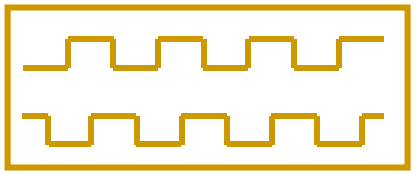
- Map Primitives to Specific Locations inside Target Technology with Reference to Area &
- Performance Constraints
- Specify Routing Resources to Be Used

FPGA DESIGN FLOW



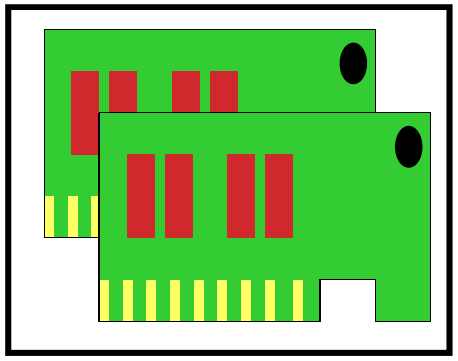
Timing Analysis

- Verify Performance Specifications Were Met
- Static Timing Analysis



Gate Level Simulation

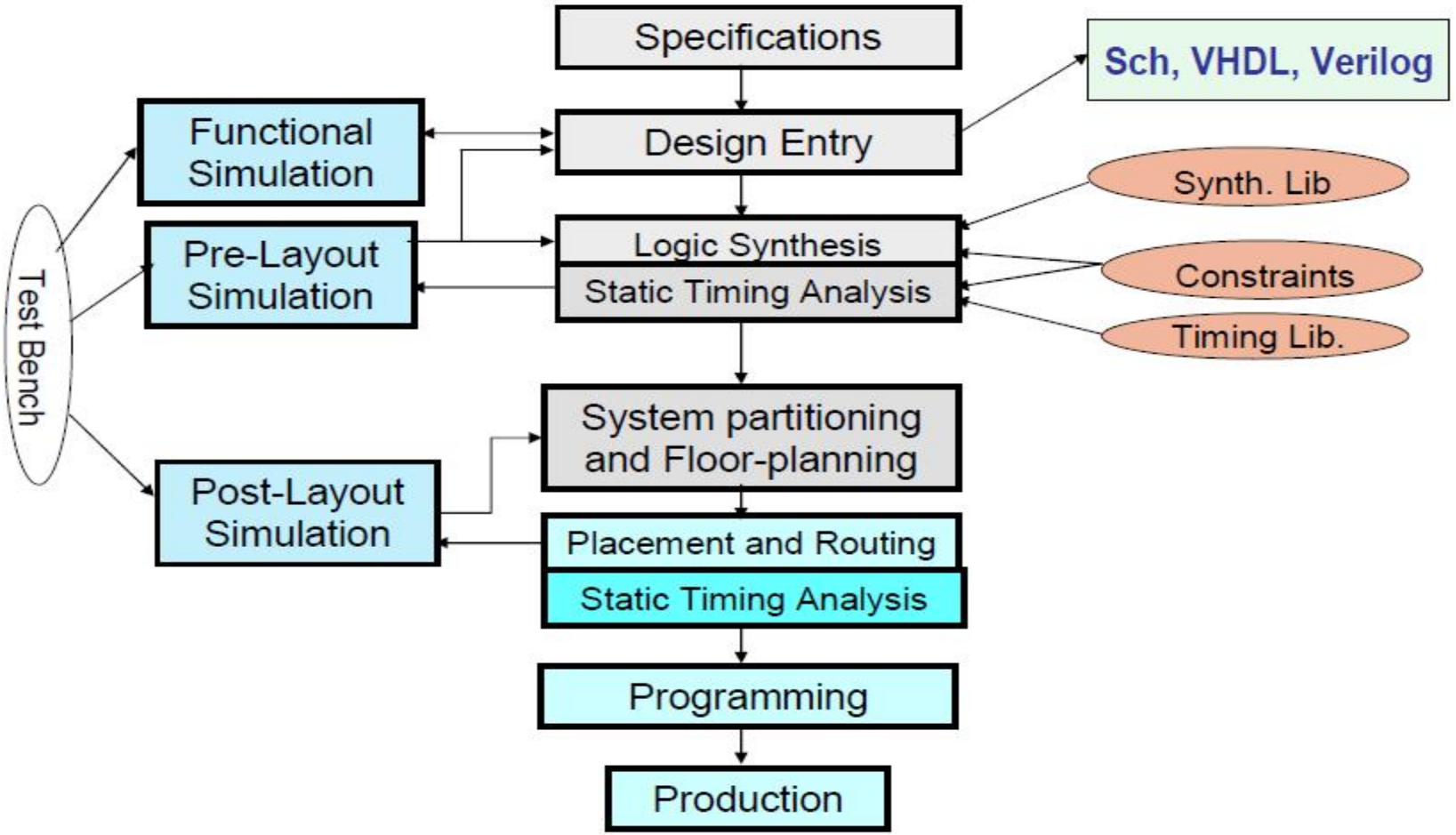
- Timing Simulation
- Verify Design Will Work in Target Technology



Program & Test

- Program & Test Device on Board

DESIGN FLOW

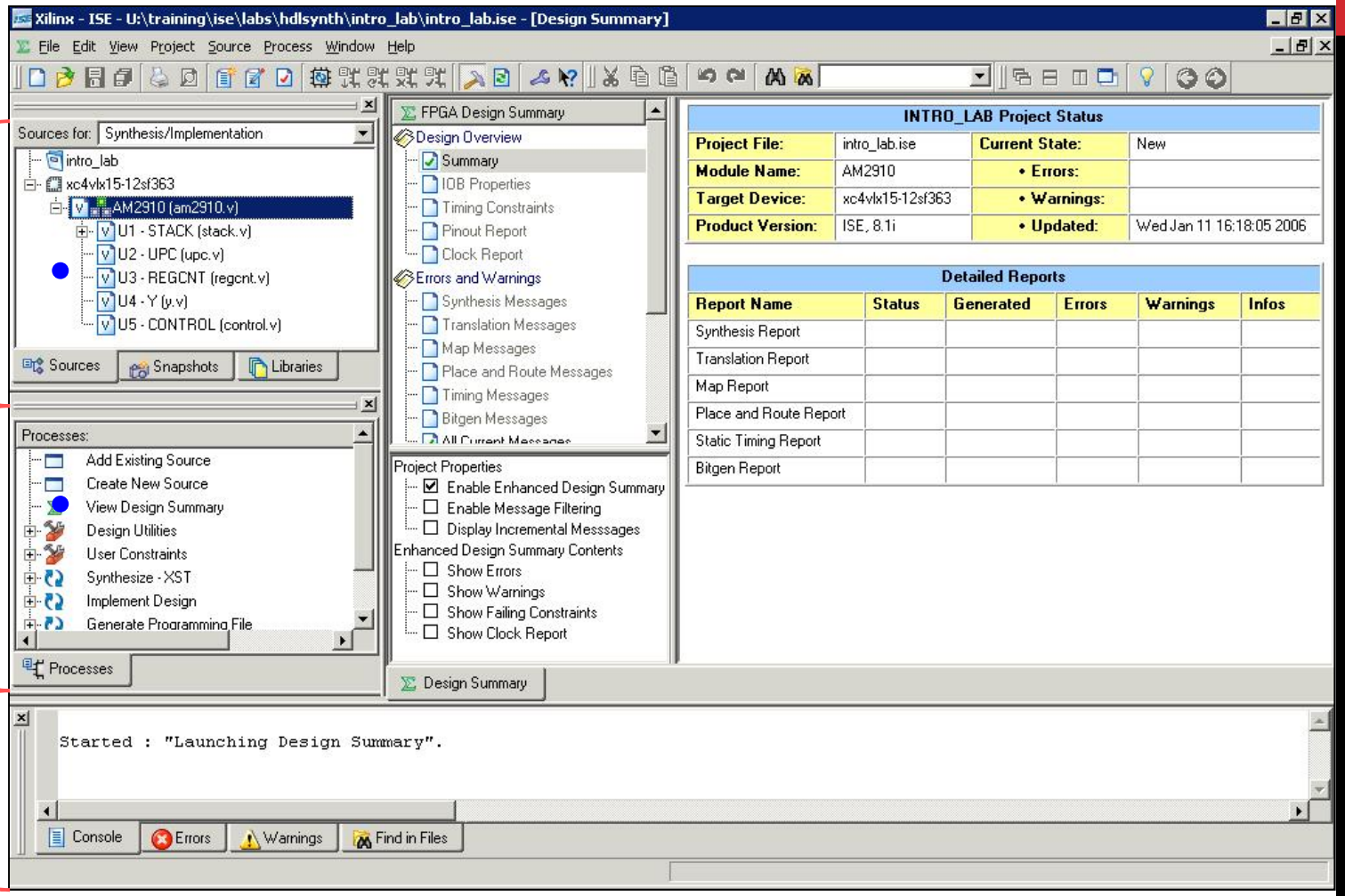

Specifications
Sch, VHDL, Verilog
Functional Simulation
Design Entry
Synth. Lib
Pre-Layout Simulation
Logic Synthesis
Constraints
Static Timing Analysis
Timing Lib.
Test Bench
System partitioning and Floor-planning
Post-Layout Simulation
Placement and Routing
Static Timing Analysis
Programming
Production

XILINX - PROJECT NAVIGATOR

Sources in project

Processes for source

Message Console



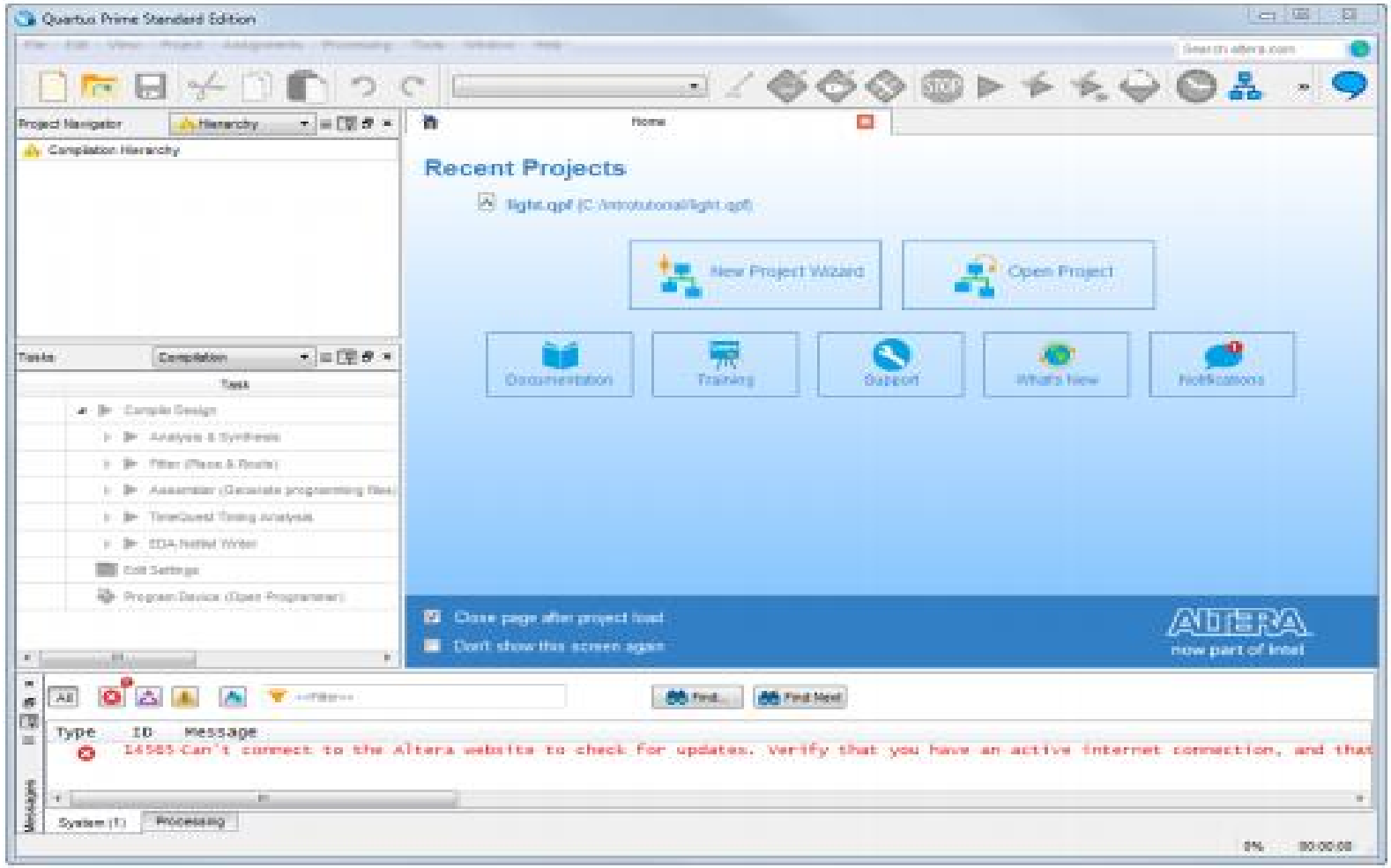
ALTERA QUARTUS II

Fully integrated design tool

- Multiple design entry methods
  - Text-based: VHDL, Verilog, AHDL
  - Built-in schematics editor
- Logic synthesis
- Place & route
- Simulation
- Timing & power analysis
- Create netlist for timing simulation
- Device programming

XILINX VIVADO

ALTERA QUARTUS PRIME



CONCLUSION

- **PLDs have transformed the way product are designed today.**
- **PLDs are now in our daily life.**
- **Advantages and Applications of PLDs are endless.**
- **HDL Languages offers fast way of design and development Using PLD.**