KHYATI KIYAWAT

khyati@virginia.edu | Khyati Kiyawat

INTERESTS

Computer Architecture, Processing-In-Memory(PIM), HW Accelerators, Energy-efficient Computing

EDUCATION

University of Virginia, VA, USA *2022 - present*
Ph. D. Student, Department of Computer Science GPA: 3.87/4.0
Advisor: Prof. Kevin Skadron

Indian Institute of Technology Roorkee, India *2016 - 2020*
B. Tech, Department of Electronics and Communication GPA: 9.23/10.0

ONGOING RESEARCH

My research focuses on designing and leveraging PIM architectures to provide energy-efficient solution to memory-bound workloads. Currently, I am

- Designing an energy-efficient PIM-DIMM system leveraging chiplet integration to accelerate GenAI workloads.
- Modeling a bit-serial subarray-level PIM architecture (Sieve) proposed for *k-mer* pattern matching on an FPGA-emulation framework (PiMulator). This work focuses on validating the simulation-based performance results of Sieve and extending PiMulator to model various PIM architectures, facilitating design space exploration.
- Accelerating filter operations in Online Analytic Processing (OLAP) database queries. Modeled energy consumption and area overhead associated with logic units placed inside DRAM. Implemented and compared the filter-scan performance on Alveo U280 FPGA.

PRESENTATIONS

- **Khyati Kiyawat**, Sergiu Mosanu, Mircea Stan, and Kevin Skadron.
  Open-Source Processing-In-Memory(PIM) Architecture Design through FPGA Emulation: A Case Study Modeling Sieve. *Open-Source Computer Architecture Research Workshop at ISCA, 2023. [OSCAR'23]*
- Akhil Shekar, Lingxi Wu, Kevin Gaffney, Martin Prammer, Helena Caminal, Yimin Gao, **Khyati Kiyawat**, Ashish Venkat, Jose Martinez, Jignesh Patel, and Kevin Skadron.
  Membrane: PiM-based OLAP Database Accelerator. *PRISM Annual Review, UCSD, 2023.*

INDUSTRIAL EXPERIENCE

Processor Architecture Research Intern | Intel, India *May 2024 - Jan 2025*
- Designed a framework for tensor tracking in GenAI workloads on Xeon Processors.

Front-end Design Verification Engineer | Texas Instruments, India *July 2020 - July 2022*
- Verified SoC integration of registers, communication peripherals, and co-processors for C2000 real-time MCUs.
- Handled critical silicon debugs for functional test patterns on Automatic test equipment.

Digital Electronics Intern | Texas Instruments, India *May 2019 - July 2019*
- Standardized memory-mapped register types and designed a Perl-based flow to auto-generate RTL for any IP.

RESEARCH PROJECTS

Scale-free Hyperbolic CORDIC Architecture | IIT Roorkee, India *Aug. 2019 - Nov. 2021*
- *Advisor:* Prof. Bishnu P Das, ECE Department
- Designed a low-latency CORDIC architecture to compute $\sinh$ and $\cosh$ functions with desired precision.

Power optimization of RISC-V PULPino | Nagoya University, Japan *Dec. 2019 - Feb. 2020*

- *Advisor:* Prof. Tohru Ishihara, Graduate School of Informatics
- Proposed a real-time Minimum Energy Point tracking method by analyzing power consumption on RISCV-based PULPino processor and observed at most 3.1% energy loss.

Image Processing based fish seed counting | IIT Bombay, India *May 2018 - July 2018*

- *Advisor:* Prof. Maryam S Baghini, VLSI Design Lab
- Proposed a novel data-acquisition apparatus to create a training dataset for a crowd-counting-based CNN model.

TEACHING AND MENTORING

Graduate Teaching Assistant | University of Virginia, USA *Fall 2023, Spring 2024, Spring 2025*

- Computer Systems and Organization I, (CS 2130), Computer Systems and Organization II (CS 3130), Memory Systems (CS 6501)

Engineering Grad School Mentor Program | University of Virginia, USA *April 2025 - Present*

- Mentoring an undergraduate student for Grad School Applications.

Rise Together | Charlottesville, Virginia *Oct. 2023 - May 2024*

- Mentoring high-school students in the US and helping them with college application and transition process.

Student Mentorship Programme | IIT Roorkee, India *Aug. 2018 - May 2020*

- Mentored a group of freshers to foster their development and prompt adjustment to the institute's culture.

AWARDS AND ACHIEVEMENTS

- Selected to participate in *Computing Research Association-Widening Partition (CRA-WP) Grad Cohort Workshop for Women*, San Francisco, USA, 2023.
- Awarded with *UVA Engineering Distinguished Fellowship 2022* given to the top Ph.D. applicants.
- Qualified as Semi-finalist in *Swadeshi Microprocessor Challenge 2020-21* to build a RISC-V based prototype for autonomous emergency distress system in automobiles.
- Recipient of *Honda Y-E-S Award 2018* awarded to students showing research potential in sustainable technology and also selected for Y-E-S Plus Scholarship 2019 to undergo an internship in Japan.
- Awarded with *1988 Batch Award 2017* given to one undergraduate student based on the academic merit.

SERVICES

Artifact Evaluation | ISCA *2024, 2025*

- Artifact Evaluation Committee member

Systems Interest Group (SIG) | University of Virginia *Nov. 2022 - May 2024*

- Initiated a cross-departmental forum, orchestrating regular meetings to foster in-depth discussions on cutting-edge research in computer systems, architecture, and networks among faculties and graduate students.

Unnat Bharat Abhiyan | IIT Roorkee *Sep. 2016 - May 2018*

- Contributed to the Govt. of India's initiative, leveraging the technical expertise of IITs to drive rural development.
- Selected as a key participant and developed skills in project management and community outreach.

PUBLICATIONS

- Anu Verma, **Khyati Kiyawat**, Bishnu P. Das, Pramod K. Meher.
  An Efficient Scaling-Free Folded Hyperbolic CORDIC Design Using a Novel Low-Complexity Power-of-2 Taylor Series Approximation. *IEEE Transactions on Very Large Scale Integration (TVLSI), 2023. [IEEE]*
- **Khyati Kiyawat**, Yutaka Masuda, Jun Shiomi and Tohru Ishihara.
  Real-Time Minimum Energy Point Tracking Using a Predetermined Optimal Voltage Setting Strategy.
  IEEE Computer Society Annual Symposium on VLSI (ISVLSI), 2020. [IEEE]