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# TRX_024_007

24-GHz Highly Integrated IQ Transceiver

## Data Sheet

| Status: | Date: | Author: | Filename: | |
|---|---|---|---|---|
| Final | 2019-11-13 | Silicon Radar GmbH | Datasheet_TRX_024_007_V1.5 | |
| Version: | Product number: | Package: | Marking: | Page: |
| 1.5 | TRX_024_007 | QFN20, 3 × 3 mm² | TRX007<br>YYWW | 1 of 16 |

# Version Control

| Version | Changed section | Description of change | Reason for change |
|---|---|---|---|
| 1.0 | Product name | Changed from TRX_024_07 to TRX_024_007 | New procedure for product nomenclature |
| | Status | From preliminary to final data sheet | Product released to serial production |
| | Max Ratings | ESD integrity updated | New test results |
| 1.1 | Specification | Spec data revised | Routinely revision |
| 1.2 | Specification | IQ imbalance and thermal resistance values changed | Correction |
| 1.3 | Overview | Typos fixed | Routinely revision |
| | Electrical Characteristics | Level of logic input specified | Correction |
| | Measurements Results | Diagram TX power vs. Temperature added<br>Description of analog behavior of inputs d0 – d3 added | New test results |
| 1.4 | 3.2 Pin Description | Table 1: LNA-gain control input voltage corrected | Correction |
| | 6.2 Power Cycling | Application hint added | Update |
| | 6.4 Evaluation Kit | Reference to Silicon Radar’s evaluation kit *SiRad Easy*® | Update |
| | 7 Meas. Results | Figure 10: Name of x-axis corrected,<br>Figure 12: Name of data series corrected | Correction |
| 1.5 | 4.4 Electrical Chars | Transmitter output power $P_{TX}$ now specified at condition $f_{TX}$ = 24.15 GHz | Correction |
| | 7 Measurements Results | Figure 19 ‘TX Power vs. Frequency at Various … ‘ added | Enhancement |

# Table of Contents

# 1 Features


- Radar transceiver for 24-GHz ISM band
- Single supply voltage of 3.3 V
- Fully ESD protected device
- Low power consumption of 300 mW in continuous operating mode
- Transmitter with power control in two steps
- Receiver with homodyne quadrature mixers
- Low-noise amplifier (LNA) with gain control
- Integrated low phase noise push-push VCO
- Divider division ratio 1:8 (1:32 available in TRX_024_006)
- Single ended TX output
- Single ended RX input
- QFN20 leadless plastic package $3 \times 3\,mm^2$
- Pb-free, RoHS compliant package
- IC is available as bare die as well

## 1.1 Overview

The IC is an integrated transceiver circuit for the 24-GHz ISM band in the frequency range 24.0 GHz – 24.25 GHz. It includes a low-noise amplifier (LNA) with gain control, quadrature mixers, a poly-phase filter, a voltage controlled oscillator with band switching and a divide-by-8 circuit. The transmitter can be powered down if TX_EN pin is supplied with 0 V. The gain of the receiver can be digitally controlled by Vct pin: Vct = 3.3 V sets the receiver in high gain mode, Vct = 0 V sets the receiver in low gain mode. The output power of the transmitter can be controlled by the pwr1 input. The IC is fabricated in SiGe BiCMOS technology.

Beside the TRX_024_007, an IC variant with a divider division ratio of 1:32 is available as TRX_024_006.

## 1.2 Applications

The TRX_024_007 can be used in wireless communication systems and in radar systems for the ISM band from 24.0 GHz to 24.25 GHz and for UWB applications between 23 GHz and 26 GHz.

# 2 Block Diagram

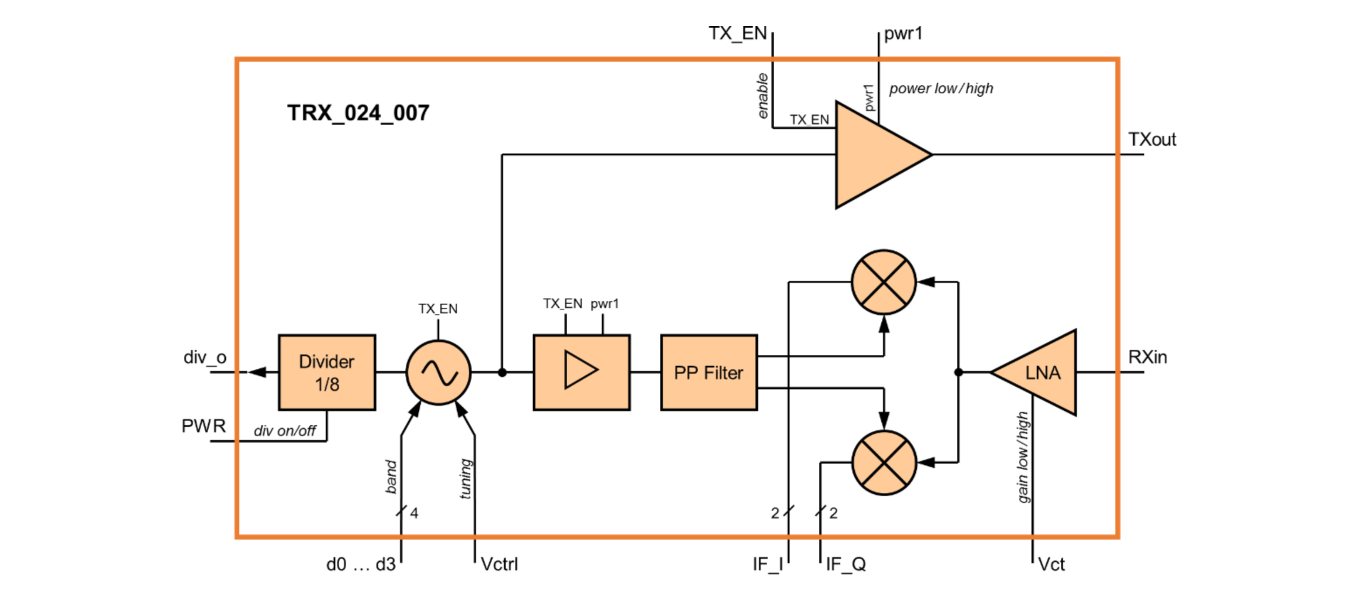


Figure 1 Block Diagram

# 3 Pin Configuration

## 3.1 Pin Assignment

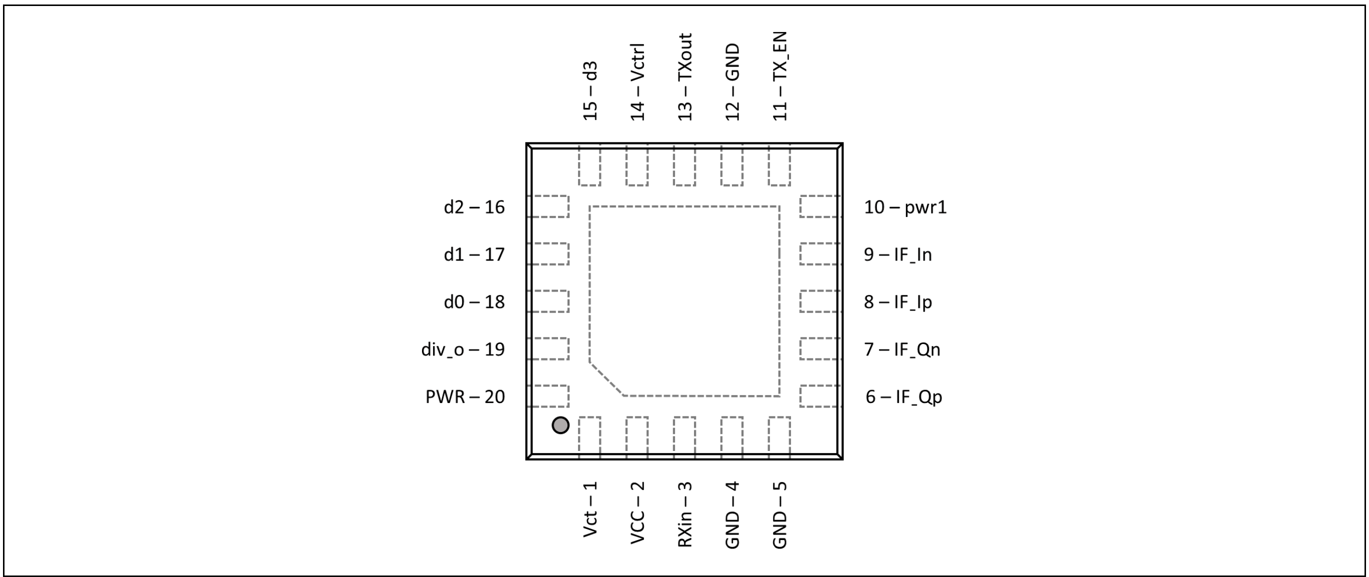


Figure 2 Pin Assignment (QFN20, Top View)

## 3.2 Pin Description

Table 1 Pin Description

| Pin | | Description |
|---|---|---|
| No. | Name | |
| 1 | Vct | LNA gain control input, with internal 100-kΩ pull-up resistor: 3.3 V – high gain mode, 0 – low gain mode |
| 2 | VCC | Supply voltage |
| 3 | RXin | RF input, 50 Ω |
| 4, 5 | GND | Ground |
| 6 | IF_Qp | IF outputs, DC coupled, external AC coupling capacitors required |
| 7 | IF_Qn | |
| 8 | IF_Ip | |
| 9 | IF_In | |
| 10 | pwr1 | Power-amplifier gain control input with internal 100-kΩ pull-up resistor: 3.3 V – $P_{OUT\_MAX}$ , 0 – $P_{OUT\_MAX}$ - 4 dB |
| 11 | TX_EN | TX enable input, high active, with internal 100-kΩ pull-up resistor: 3.3 V – enable, 0 – off |
| 12 | GND | Ground |
| 13 | TXout | Transmitter output, 50 Ω |
| 14 | Vctrl | VCO tuning voltage input |
| 15 | d3 | VCO band switching inputs, each input with internal 120-kΩ pull-down resistor |
| 16 | d2 | |
| 17 | d1 | |
| 18 | d0 | |
| 19 | div_o | Divider output, 50 Ω, DC coupled, external decoupling capacitor required (min. 100 pF) |
| 20 | PWR | Divider enable input, with internal 100-kΩ pull-up resistor: 3.3 V – enable, 0 – off |
| (21) | GND | Exposed die attach pad of the QFN package, must be soldered to ground |

# 4 Specification

## 4.1 Absolute Maximum Ratings

Attempted operation outside the absolute maximum ratings of the device may cause permanent damage to the device. Actual performance of the device is only given within the operational specifications, not at absolute maximum ratings.

Table 2 Absolute Maximum Ratings

| Parameter | Symbol | Min | Max | Unit | Condition / Remark |
|---|---|---|---|---|---|
| Supply voltage | $V_{CC}$ | | 3.6 | V | to GND |
| DC voltage at RF pins | $V_{DCRF}$ | 0 | 2 | mV | IC provides low ohmic circuit to GND for TXout and RXin |
| Junction temperature | $T_J$ | | 150 | °C | |
| Storage temperature range | $T_{STG}$ | -65 | 150 | °C | |
| DC voltage at control inputs | $V_{CTL}$ | -0.3 | $V_{CC}$ + 0.3 | V | d0, d1, d2, d3, Vctrl, pwr1, TX_EN, PWR |
| Input power into pin RFin | $P_{IN}$ | | 0 | dBm | |
| ESD robustness | $V_{ESD}$ | | 500 | V | Class 1A, Note 1 |

Note 1 According to ESDA/JEDEC Joint Standard for Electrostatic Discharge Sensitivity Testing, Human Body Model Component Level, ANSI/ESDA/JEDEC JS-001-2011

## 4.2 Operating Range

Table 3 Operating Range

| Parameter | Symbol | Min | Max | Unit | Condition / Remark |
|---|---|---|---|---|---|
| Ambient temperature | $T_A$ | -40 | 85 | °C | |
| Supply voltage | $V_{CC}$ | 3.13 | 3.47 | V | (3.3V ± 5%) |
| DC voltage at control inputs | $V_{CTL}$ | 0 | $V_{CC}$ | V | d0, d1, d2, d3, Vctrl, Vct, pwr1, TX_EN, PWR |

**Note: Do not drive input signals without power supplied to the device.**

## 4.3 Thermal Resistance

Table 4 Thermal Resistance

| Parameter | Symbol | Min | Typ | Max | Unit | Condition / Remark |
|---|---|---|---|---|---|---|
| Thermal resistance, junction-to-ambient | $R_{thja}$ | | | 75 | K/W | Four-layer PCB according to JEDEC standard JESD-51 |

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## 4.4 Electrical Characteristics

$T_A$ = -40 °C to +85 °C unless otherwise noted. Typical values measured at $T_A$ = 25 °C and $V_{CC}$ = 3.3 V.

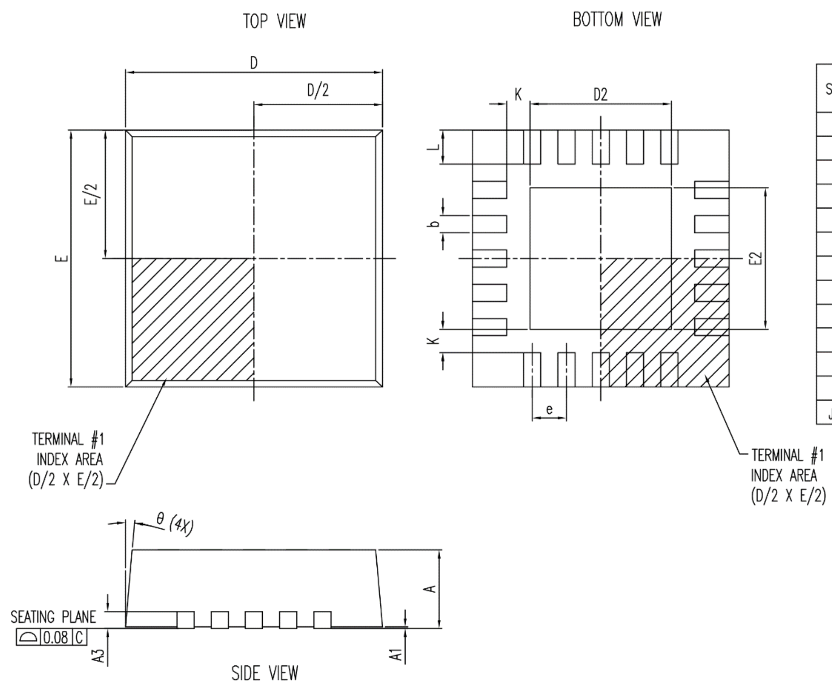
Table 5 Electrical Characteristics

| Parameter | Symbol | Min | Typ | Max | Unit | Condition / Remark |
|---|---|---|---|---|---|---|
| **DC Parameters** | | | | | | |
| Supply current consumption | $I_{CC}$ | 80 | 89 | 100 | mA | TX, divider enabled |
| Control input voltage, low level | $V_{IN\_L}$ | 0 | | 0.3 × $V_{CC}$ | V | Inputs TX_EN, pwr1, PWR and Vct |
| Control input voltage, high level | $V_{IN\_H}$ | 0.7 × $V_{CC}$ | | Vcc | V | |
| **Transmitter Section TX** | | | | | | |
| Transmitter start frequency | $f_{TX}$ | 22.3 | 22.8 | 23.3 | GHz | |
| Transmitter stop frequency | | 25.9 | 26.4 | 26.9 | GHz | |
| Divider division ratio | $D_{div\_o}$ | | 8 | | | Note 1 |
| Divider output frequency | $f_{div\_o}$ | 2.79 | | 3.36 | GHz | |
| Tuning voltage VCO | $V_{ctrl}$ | 0 | | 3.3 | V | |
| Tuning slope VCO (Vctrl) | $\Delta f_{TX}/\Delta V_{ctrl}$ | | 220 | | MHz/V | Only Vctrl swept |
| Number of adjustable frequency bands | | | 16 | | | d0 - d3: VCO band switching, Note 1 |
| Pushing VCO | $\Delta f_{TX}/\Delta V_{CC}$ | | 135 | | MHz/V | f = 24.15 GHz |
| Phase noise | $P_N$ | -105 | -102 | | dBc/Hz | at 1 MHz offset |
| Output impedance | $Z_{TXout}$ | | 50 | | Ω | |
| Transmitter output power | $P_{TX}$ | 2.5 | 4 | 6 | dBm | |
| Adjustable range output power | $P_{TX\_ADJ}$ | 0 | | 4 | dBm | pwr1 = 0 / 3.3 V |
| Divider output power | $P_{div\_o}$ | -9 | -8.5 | -8 | dBm | Note 2 |
| Spurious power | $P_{Sp-}$ | | -40 | | dBm | $f_{TX}$ - $f_{div}$ |
| | $P_{Sp+}$ | | -43 | | dBm | $f_{TX}$ + $f_{div}$ |
| Harmonics power | $P_{Ha12}$ | | -46 | | dBm | 12 GHz |
| | $P_{Ha48}$ | | -40 | | dBm | 48 GHz |
| **Receiver Section RX** | | | | | | |
| Receiver frequency | $f_{RX}$ | 22.3 | | 26.9 | GHz | |
| Receiver input impedance | $Z_{RXIN}$ | | 50 | | Ω | |
| Number of adjustable gain modes | | | 2 | | | Adjustable LNA gain control |
| Gain high gain mode | | | | 18 | dB | $V_{ct}$ = 3.3 V |
| Gain low gain mode | | | | 11 | dB | $V_{ct}$ = 0 |
| IF frequency range | $f_{IF}$ | 0 | | 200 | MHz | |
| IF output impedance | $Z_{OUT}$ | | 470 | | Ω | Differential |
| IQ amplitude imbalance | | -1 | | 1 | dB | |
| IQ phase imbalance | | -10 | | 10 | deg | |
| Noise figure, high gain mode | | | 4 | | dB | Simulated |
| Noise figure, low gain mode | | | 6 | | dB | (double side band at $f_{IF}$ = 1 MHz) |
| Input compression point | 1dB ICP | -20 | | -13 | dBm | |

Note 1 See also chapter 'Measurement Results', Figure 10 and 11.
Note 2 Divider output is loaded with 50 Ω, DC coupled, external decoupling capacitor ≥ 100 pF required.

# 5 Packaging

## 5.1 Package Dimensions

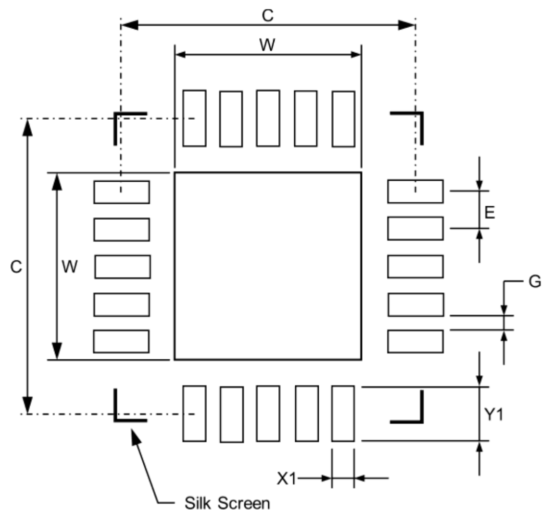



| SYMBOL | DIMENSION IN MM | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.80 | 0.90 | 1.00 |
| A1 | 0 | 0.02 | 0.05 |
| A3 | 0.20 REF. | | |
| D | 3.00 BASIC | | |
| D2 | 1.50 | 1.65 | 1.80 |
| E | 3.00 BASIC | | |
| E2 | 1.50 | 1.65 | 1.80 |
| e | 0.40 BASIC | | |
| b | 0.15 | 0.20 | 0.25 |
| L | 0.30 | 0.40 | 0.50 |
| K | 0.20 | | |
| θ | 0° | | 14° |
| JEDEC | REFERENCE MO-220 | | |

Figure 3 Outline Dimensions of QFN20, 3 × 3 mm², 0.4 mm Pitch

IC Weight: 0.235 g (typ.)

## 5.2 Package Footprint




| Dimension Limits in mm | | min | nom | max |
|---|---|---|---|---|
| Contact Pitch | E | | 0.4 BSC | |
| Contact Pad Width | W | | | 1.8 |
| Contact Pad Spacing | C | | 3.0 | |
| Contact Pad Width | X1 | | 0.2 | |
| Contact Pad Length | Y1 | | | 0.7 |
| Distance Between Pads | G | 0.20 | | |

Figure 4 Recommended Land Pattern

## 5.3 Package Code

| | |
|---|---|
| Top-Side Markings | TRX007<br>YYWW |

## 5.4 Qualification Test

Table 6 Reliability and Environmental Test

| Qualification Test | JEDEC Standard | Condition | Pass / Fail |
|---|---|---|---|
| MSL3 | J-STD-020E | Reflow simulation 3 times at 260°C | pass |

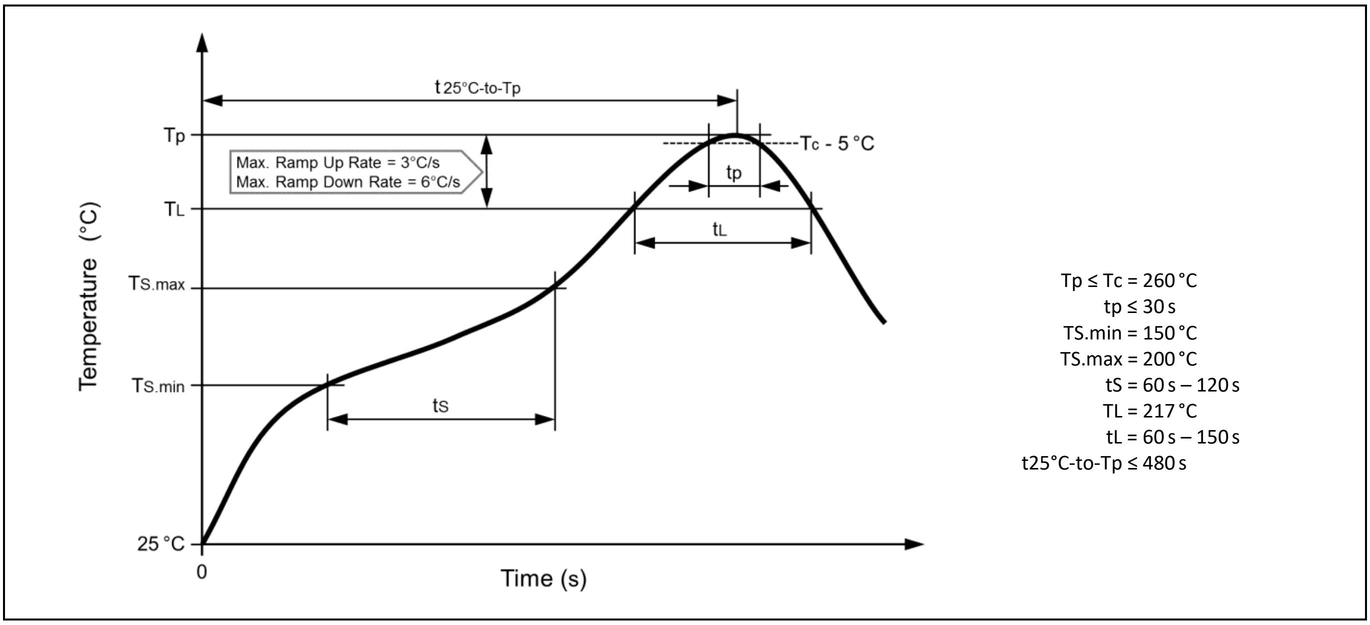



Figure 5 Reflow Profile for Pb-Free Assembly according to JEDEC Standard J-STD-020E

# 6 Application

## 6.1 Application Circuit Schematic

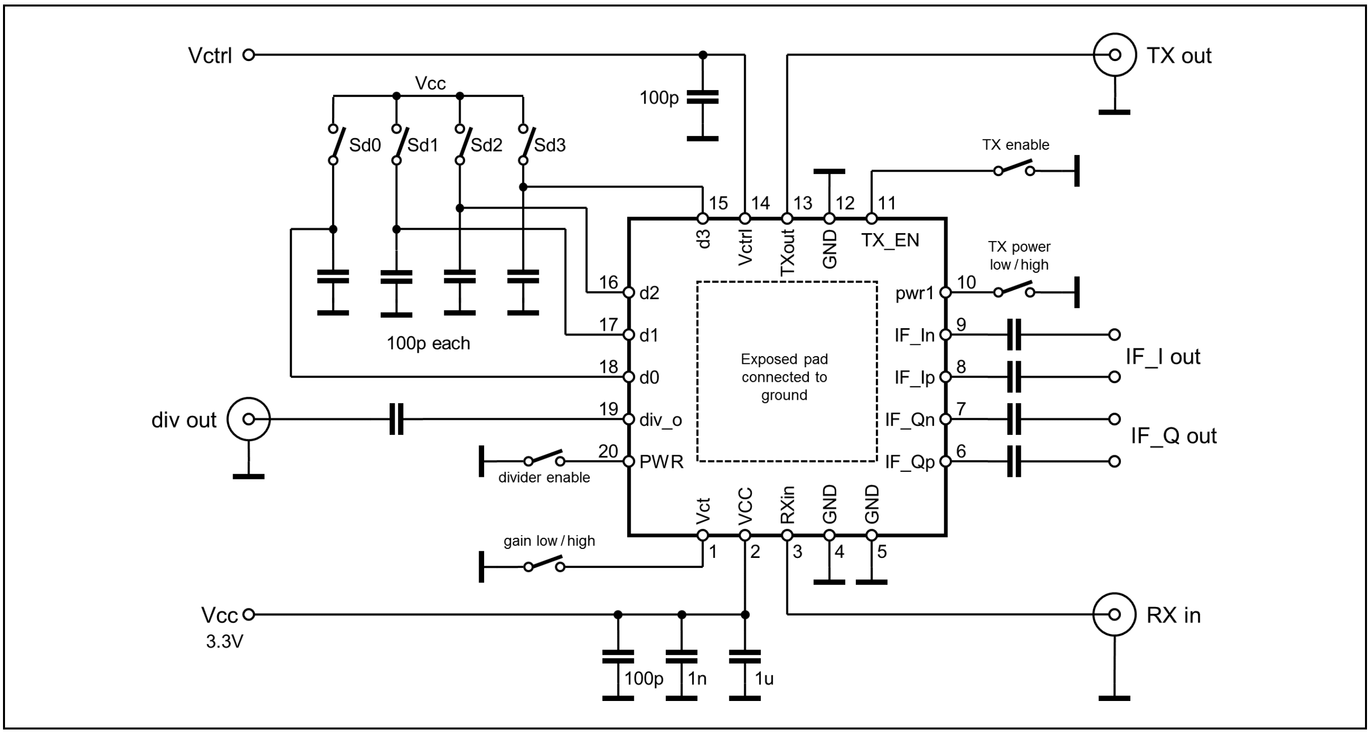



Figure 6 Application Circuit for Band Switching

## 6.2 Power Cycling

It is possible to reduce power consumption by power cycling the radar front end. Rapid power cycling with voltage rise times between 10 and 100 µs is possible. At power-up, it must be ensured that no input signal is driven high before the supply voltage is stable. At power-down, all input signals must be pulled low before the supply voltage is switched off.

## 6.3 Evaluation Board

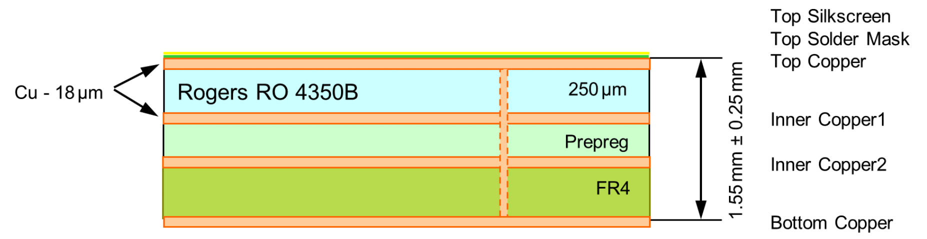



Figure 7 Evaluation Board Stack-up

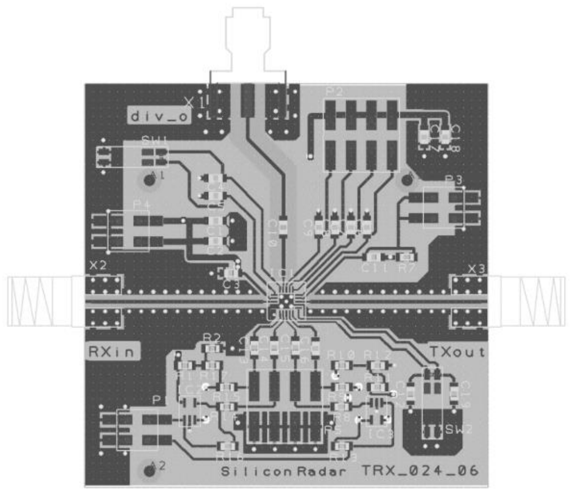



Figure 8 Evaluation Board Layout Including Via Holes (50 mm × 50 mm, Top View)

## 6.4 Evaluation Kit

For a quick and easy start into radar development Silicon Radar offers *SiRad Easy®*. It is an evaluation board system for many of our integrated IQ transceivers with antennas in package or on PCB. It comes with a reference hardware and provides a complete design environment which can be configured via a browser-based graphical interface. Its rich functionality and the open communication protocol make it a versatile tool – also for enhanced development projects.
It features:

- Distance measurement
- Velocity measurement
- Frequency modulated continuous wave mode (FMCW)
- Continuous wave mode (CW)

For more information about the features of *SiRad Easy®* see:
https://www.siliconradar.com

## 6.5 Input / Output Stages

The following figures show the simplified circuits of the input and output stages. It is important that the voltage applied to the input pins never exceeds $V_{CC}$ by more than 0.3 V. Otherwise, the supply current may be conducted through the upper ESD protection diode connected at the pin.

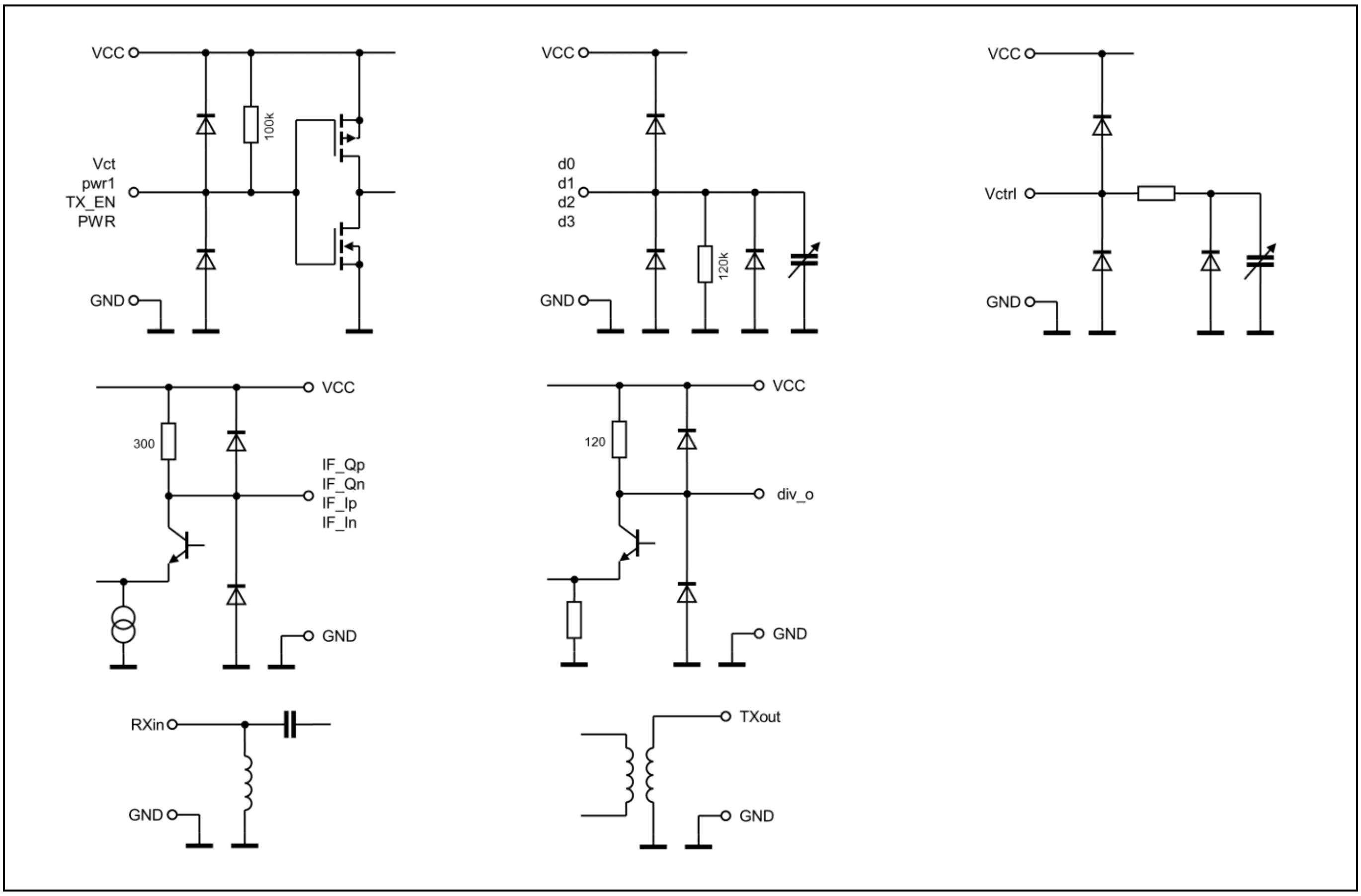



Figure 9 Equivalent I/O Circuits

# 7 Measurement Results

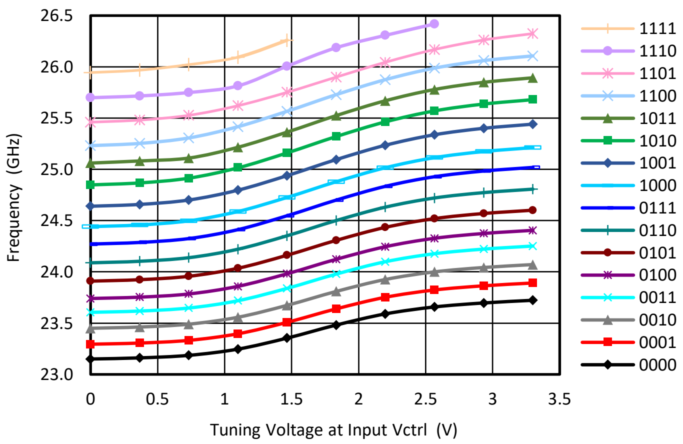



Figure 10 VCO Tuning with Band Switching (d0 - d3)

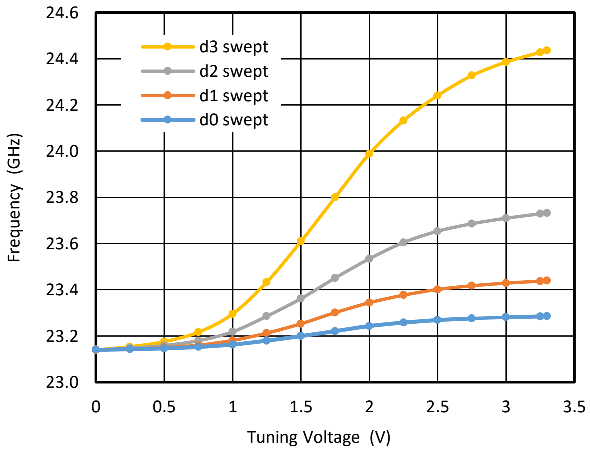



Figure 11 VCO Tuning, d3 - d0 swept, Vctrl = 0 = constant

VCO band switching inputs d3 to d0 can be used to switch the output frequency band as in Figure 10. As an example, input combination ‘0101’ with d3, d1 = 3.3 V and d2, d0 = 0 includes the 24-GHz ISM band. However, the designer should take into account that output frequency bands may shift from chip to chip (see Figure 12), and same switch settings may not give the same output band.
Note, VCO band switching inputs d0 - d3 are analog inputs and can be used to control the output frequency. The bandwidth of the switching inputs increases from d0 to d3. Any of these pins can be interconnected to each other and / or to pin Vctrl to use different bandwidth capabilities of the VCO.

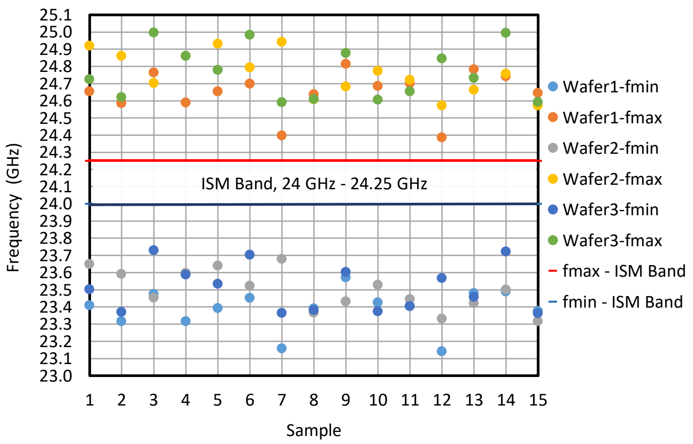



Figure 12 Output Frequency Range in Relation to ISM Band for Several Chips ($f_{min}$, $f_{max}$ measurement)

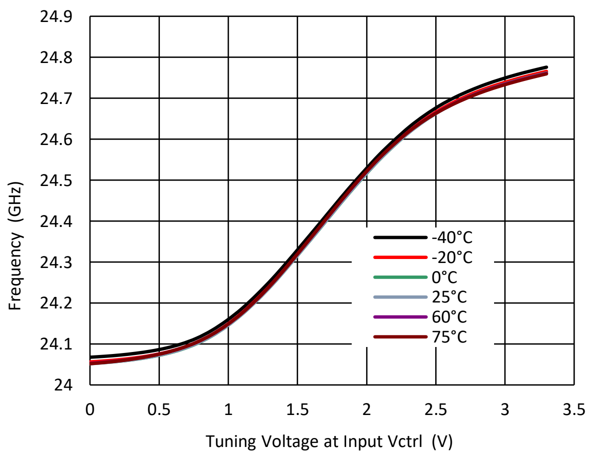



Figure 13 VCO Tuning at Various Temperatures (tuning voltage Vctrl)

The input settings for the measurement shown in Figure 12 are d3 = 0 (0 V), d2 = 1 (3.3 V). Inputs d0, d1, and Vctrl are interconnected and swept together.

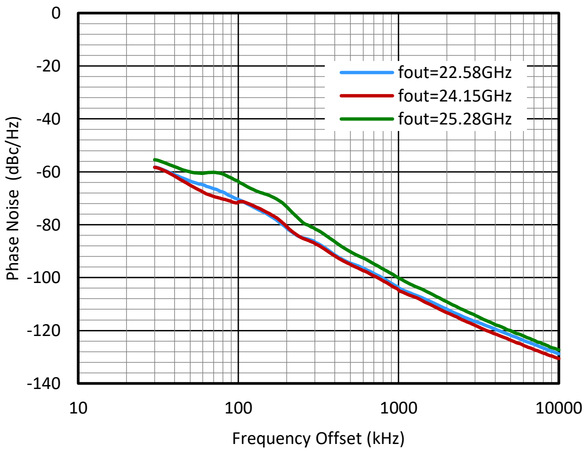



Figure 14 Phase Noise of the Free-Running VCO

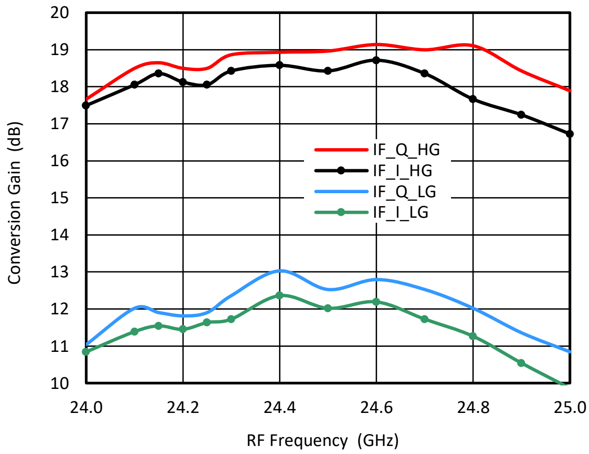



Figure 15 Conversion Gain of the Receiver in High-Gain and Low-Gain Mode

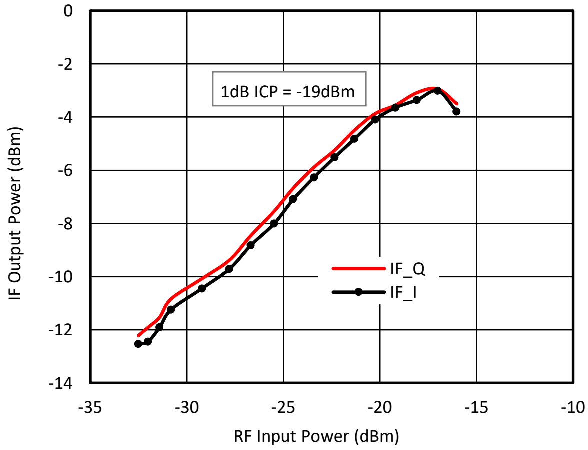



Figure 16 Conversion Gain of the Receiver in High-Gain Mode

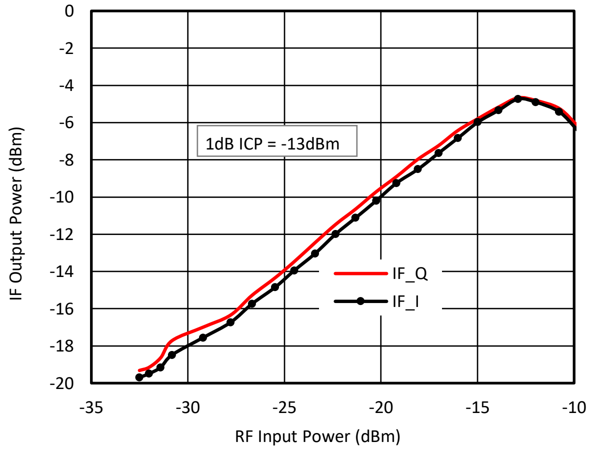



Figure 17 Conversion Gain of the Receiver in Low-Gain Mode

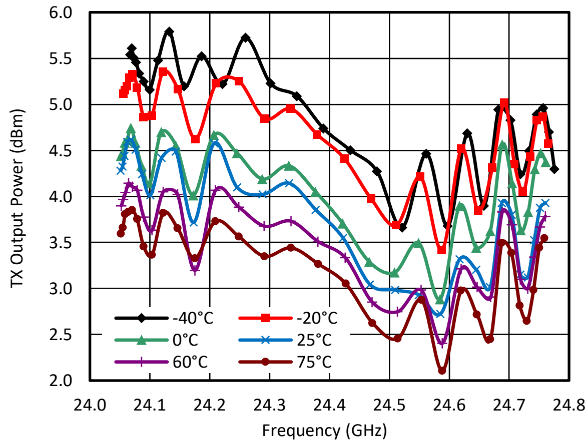



Figure 18 TX Power vs. Frequency at Various Temperatures

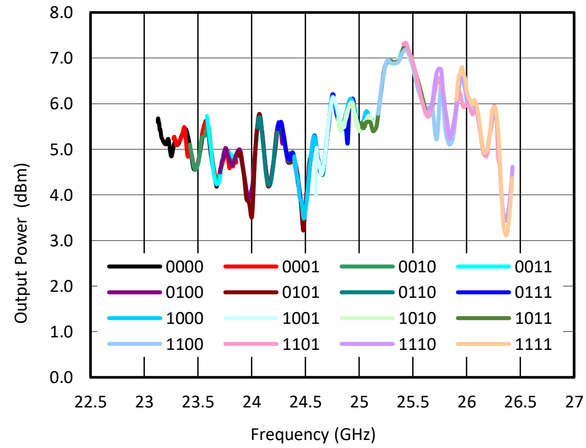



Figure 19 TX Power vs. Frequency at Various Control-Input Combinations

# Disclaimer