Prac5: Trigger Surround Cache

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I. Introduction

A Field Programmable Gate Array (FPGA) is an interconnected circuit that can be customized for specific applications. You can customize it using the coding language Verilog. In this lab, we will build a simple TSC Trigger Surround Cache using an ADC and a ring buffer memory device. ADC records an input analog signal and converts it to a digital signal. A ring buffer is a type of storage method where you have a fixed size storage, and you have two pointers - one pointer which is the head and one pointer which is the tail. The head points to the value you are going to read from, while the tail points to the value you are going to write to. The TSC must be able to communication with other devices using transfer protocols.

II. Design and Implementation

A. Hardware ans Software

This was run on a MacBook Pro computer using Iverilog. Additionally, gtkwave was used to monitor the wires.

B. TSC design overview

The TSC (Touch Sensing Controller) has a 3 bit state register, a 32-bit timer, a 32-bit TRIGGER_TM, and an internal ring buffer. It is connected to the ADC (Analog-to-Digital Converter) via a request (REQ), ready (RDY), and data (DAT) lines. Additionally, the TSC can communicate with other devices using triggered (TRD), Send Buffer (SBF), serial data (SD), and completed data (CD) registers and wires.

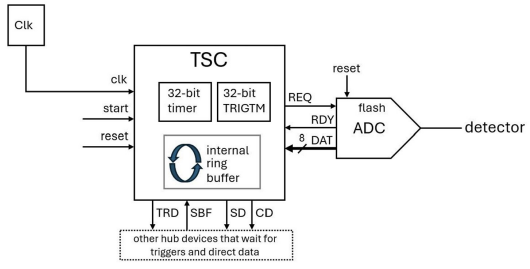

Fig. 1: Block diagram of the TSC

There is also an accompanying TSC_tb test bench which is used to initiate and test the TSC module.

C. CLock (clk)

A 1 THz clock signal is set up on clk wire in the TS_tb test bench.

1) State register: the st a register is a 3-bit register that has the folowing states:

- 000 Stop : Initial state used to wait for reset pin has been triggered.
- 001 ready State that is enter on the reset pin rising edge and it waits for the start pin rising edge.
- 010 Running State that is entered from ready state once the start pin rising edge is pulled hight.
- 011 Triggered State entered when the value read by the ADC is greater than the predetermined trigger value (TRIGVL).
- 100 IDLE This state is entered when a trigger event has occurred and the TSC is waiting for the start pin or SPF pins rising edge.
- 101 SENDING This state is entered from the IDLE state when the SFB pin gos high. It indicates that data is being sent.

2) Timer: The timer is incremented on the rising edge of the clock. When a trigger even occurs the timer si save in the TRIGTM register which is outputted to the test bench. The timer is reset if a transition into a running state occurs.

3) Ring Buffer: The ring buffer is an array uf 32 8-bit register. The tail pin index is named $\text{write}_prtandisInitialsettob11111andthetailindexisnamedread_ptrandi$

4) how the TSC intervacec with the ADC:

III. Testing and Validation

IV. Conclusion

This report shows that for multiplying small matrix sizes and counts, single-threaded matrix multiplication is faster, however, when the matrix sizes and counts are large enough, parallelized matrix multiplication becomes faster due to its overhead becoming negligible relative to its computation time.

The overheads for the parallel matrix multiplication program are the OpenCL setup overhead and kernel startup overhead, with the former being constant and the latter increasing linearly with matrix count.

Lastly, there is an unexplained decrease in speed up for small matrix sizes and matrix counts over 60 which is theorised to be caused by the matrix arrays allocation and transfer between the heap, stack and cache, however this hypothesis still requires further testing to confirm.