Design of a 2.45GHz CMOS Low-Noise Amplifier

By

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Project Report

Contents

Requirements

The final design needs to satisfy the following requirements

- f_0 = 2.45GHz
- Z_S = 50 Ohms
- Z_L = 50 Ohms
- $|S_{21}|$ >= 10dB
- $|S_{11}|$ =< -10dB
- $|S_{22}|$ =< -20dB
- NF =< 2.5dB
- IIP3 >= -7dBm
- P_{dc} =< 12mW
- V_{dd} =< 2.5V
- Source Power IIP3 = -30dBm

Design Limits

- Max Total Cap = 100pF
- Max Total Res = 100KOhms
- Max number of pins: 20
- Max bond wire length: 30 mm
- No On chip Inductors

Models

- SPICE nmos and pmos spreadsheets
- SPICE nnmos sub circuit
    - l_{min}=0.35 um
    - w_{min}=1.2 um

Extracting AC parameters

The first step in the design is extracting the key AC parameters from the provided HSPICE nmos model

Oxide capacitance (C_{ox})

$$C_{ox} = \frac{\epsilon_r \epsilon_0}{t_{ox}}$$ [1]

where $\epsilon_0 = 8.85 \times 10^{-12} F/m$ and $\epsilon_r = 3.97$. From nmos model thickness of the oxide is given as $t_{ox} = 7.8 \times 10^{-9} m$. It concludes:

$$C_{ox} = 4.51 \times 10^{-3} F/m^2$$

Optimal width (W_{opt})

Using the technique of power constrained noise matching, the optimal width of the input transistor (M1) can be found using the following equation

$$W_{opt} = \frac{1}{3(2\pi f_0) L_{eff} C_{ox} R_s}$$

where $R_s = 50\Omega$ and L_{eff} is for our case the minimum allowable gate length for this process: $L_{eff} = 0.35\mu m$

This results in:

$$W_{opt} = 274.6\mu m$$

Gate-Source capacitance (C_{gs})

An estimate of the gate source capacitance can be found using the following equation:

$$C_{gs} = \frac{2}{3} W L C_{ox} + W C_{gd0}$$

Assuming $W = W_{opt} = 274.6\mu m$ and $L = L_{eff} = 0.35\mu m$ and $C_{gd0} = 3.6 \times 10^{-10} F/m$

from nmos model:

$$C_{gs} = 387.6fF$$

Minimum transconductance (g_m)

Two factors limit the transconductance of the design, Noise Figure (NF) and Total Gain ($|S_{21}|$)

Noise figure consideration

As illustrated by H. Fukui[2] and T. Lee[3]

$$F_{min} \approx 1 + 2.3\left[\frac{\omega}{\omega_T}\right]$$

and

$$\omega_T = \frac{g_m}{C_{gs}}$$

which may be rewritten as

$$g_m = \frac{4.6\pi f_0 C_{gs}}{F_{min} - 1}$$

assuming

$$NF \leq 2.5dB \Rightarrow F_{min}^{max} = 1.78$$

then we have

$$g_m^{min_{NF}} = 17.6mS$$

Which is the minimum g_m required to achieve NF of 2.5dB.

Total Gain Consideration

Since the gain primarily depends on G_m and R_{out}, it is prudent to ensure that the required gain can be achieved with a reasonable output resistance. This is done using the analysis below where R_{load} = R_{source} = 50 Ohm. This is a significant assumption, specifically since it ignores the output resistor; however, it does provide a very rough estimate of a minimum gm.

To a good approximation, the transconductance of the cascode stage is the same as that of the single transistor stage. It will be multiplied by the quality factor of the input RLC tank (Q_{in}) formed by L_g , C_{gs} , and L_s; therefore, the effective transconductance of the cascode equals:

$$G_m = \frac{\omega_T}{2\omega_0 R_s}$$

where $|S_{21}|^2$ is defined as the ratio of the power delivered to the load to the available power at the source. it can be written in terms of G_m as:

$$|S_{21}|^2 = \frac{I_0^2 R_L}{\frac{V_s^2}{4R_s}} = \left(\frac{\omega_T}{\omega_0}\right)^2 = \left(\frac{g_m}{2\pi f_0 C_{gs}}\right)^2$$

or

$$g_m = 2\pi f_0 C_{gs} |S_{21}|$$

Therefore, to achieve $|S_{21}|$ requirement:

$$g_m^{min_{S21}} = 18.9mS$$

Note that $g_m^{min_{S21}} > g_m^{min_{NF}}$ resulting in

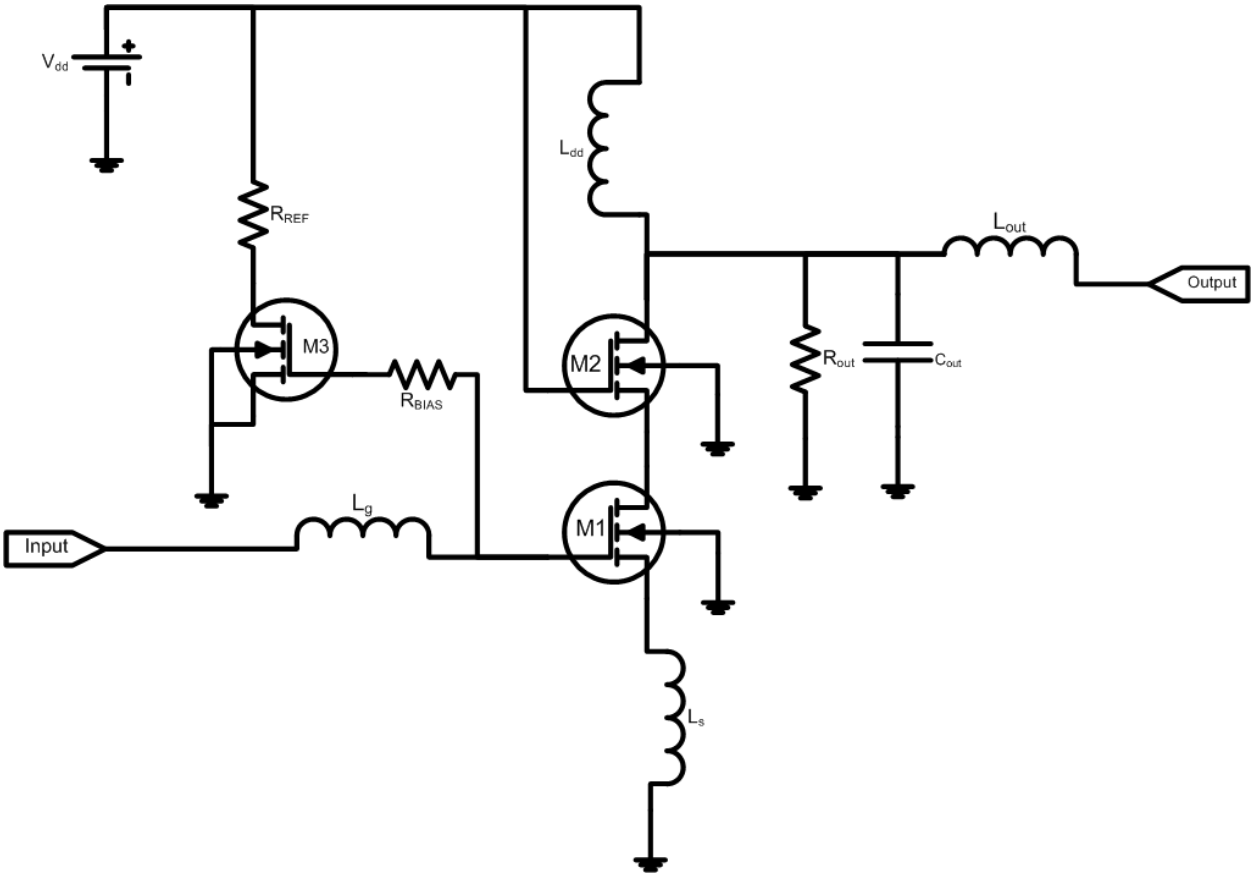
$$g_m > 18.9mS$$

and

$$\omega_T > 48.7Grps$$

Initial Design

Because the application is narrow band, we can tune out the output capacitance to increase gain. The cascode topology is used to increase the isolation between input and output improving gain and noise figure. A current mirror transistor is used to bias the main transistor. R_{BIAS} is chosen large compared to the input impedance so its noise contribution is negligible.



DC Bias (R_{BIAS} and R_{REF})

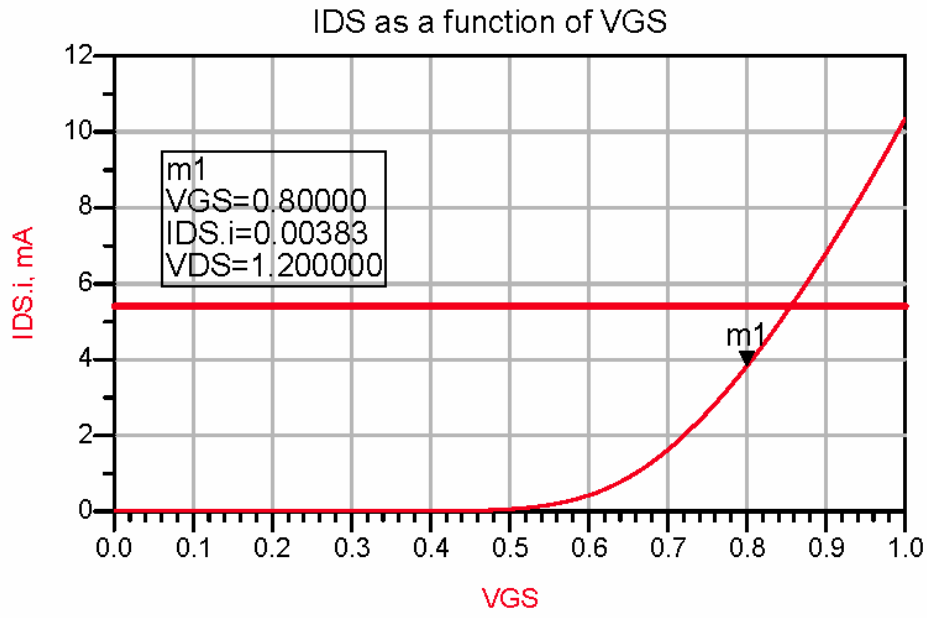
In order to achieve the highest linearity, V_{dd} and P_{dc} are chosen as the max allowable values: V_{dd} = 2.5V and P_{dc} = 12mW. This gives a max bias current of I_{dd} = 4.32mA (Assuming 90% of current is used by M1 and 10% by M3). The active bias circuit consists of transistor M3 and impedance R_{BIAS} and R_{REF}. Also, in order to reduce the additive power consumption of the bias circuit, the width of MOSFET M3 is chosen to be one tenth of the width of M1[4], $W_{M3} = 27.5\mu m$.

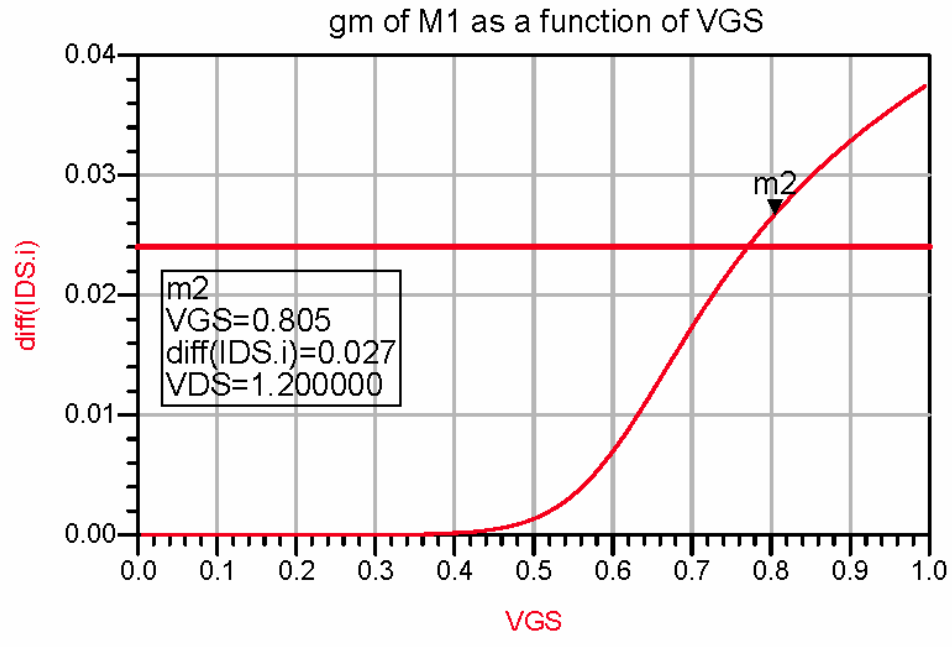
From the previous analysis, we require that M1 be biased such that gm is greater than 20 mS (19 mS plus 1 mS margin) and Ids less than 4.3 mA. From the below plots we let

Vg=.8V, which gives gm=27mS and Ids=3.8mA.

In order to apply .8V to the gate we require a 1.7V drop across R_{REF}. Since the current is about .45mA, we let $R_{REF} = 3.75k\Omega$.

Since no current flows through R_{BIAS} its value is not critical as long as it is large compared to the system impedance of 50 OHM. For this design we let $R_{BIAS} = 20k\Omega$.





Note: Vds=1.2mV

Source Inductance (L_s)

To satisfy the S_{11} requirement, the following analysis is used:

$$|S_{11}|<-10dB \Rightarrow \left|\frac{Z_{in}-Z_s}{Z_{in}+Z_s}\right|<\frac{1}{10^{0.5}} \Rightarrow 26\Omega<Z_{in}<96\Omega$$

Also, when the input circuit is operating at its resonant frequency the input impedance is

$$(Z_{in})_{f_0}=\omega_T L_s \Rightarrow L_s=\frac{(Z_{in})_{f_0}}{\omega_T}$$

which results in:

$$L_s=1.03nH$$

This inductance can be achieved by four 1mm bond wires (L_S=1nH, R_S=0.2Ohm, C_{pad}=320fF). Note that the mutual inductance between these four bond wires is not considered in this calculation. To reduce the mutual inductance, these bond wires need to be routed orthogonally.

Gate Inductance (L_g)

In order for the input to resonate at 2.45 GHz, the following analysis is used:

$$\omega_0=\frac{1}{\sqrt{(L_g+L_s)C_{gs}}} \Rightarrow L_g=\frac{1}{(2\pi f_0)^2 C_{gs}}-L_s$$

which calculates to:

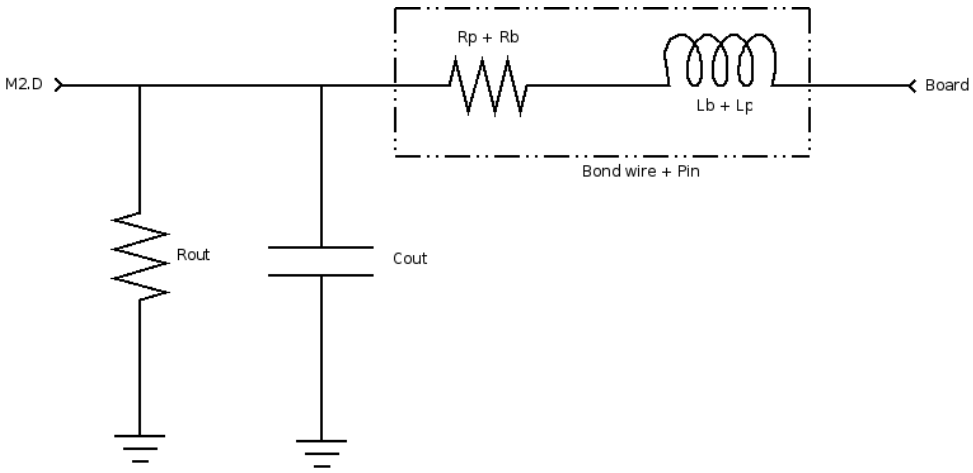
$$L_g=9.9nH$$

Which can be achieved by one 7mm bond wire (L_g=10nH, R_g=2Ohm, C_{pad}=80fF).

Output matching

The cascode topology has a very high output impedance; which can be assumed opened compared to 50 Ohm. In order to achieve the required gain, R_{out} is added to the drain of M2. Also C_{out} and the 5 mm output bond wire are used in an L-match topology to match the

output to a 50 Ohm load ($|S_{22}|$ < -20dB or VSWR < 1.22).



From the definition of S21, we know:

$$|S_{21}|>10dB \Rightarrow A_v>5$$

from the IV plot we also know:

$$g_m = 27.5mS$$

Simple circuit theory tells us that the voltage gain is approximately the product of gm and Rout:

$$A_v = g_m R_{out} \Rightarrow R_{out} = \frac{A_v}{g_m}$$

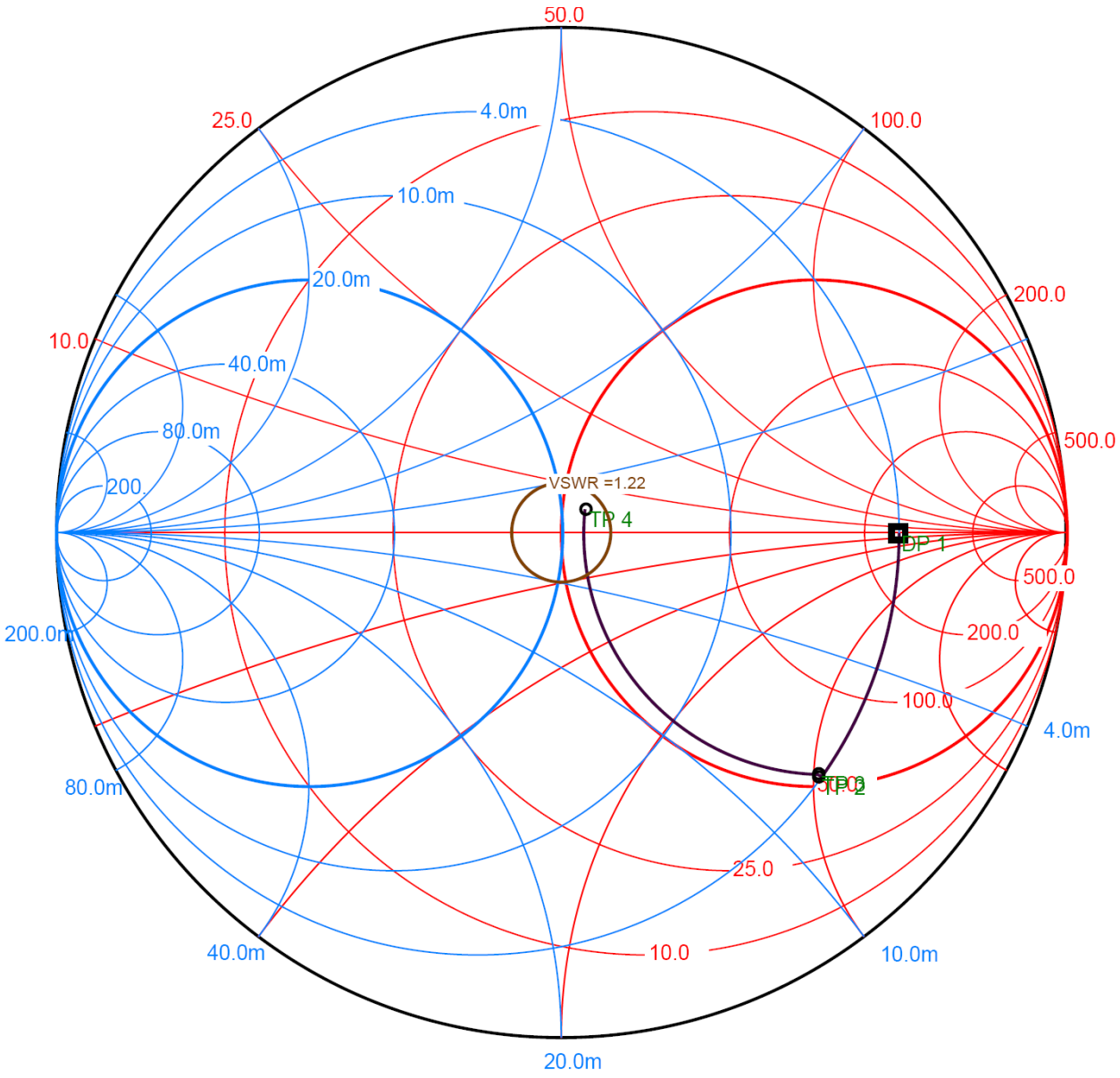
This leads to the requirement that in order to have adequate gain the output resistance needs to be at least 185 Ohm:

$$R_{out} = 185\Omega$$

Using Smith chart matching techniques, we determine the value of the output capacitor as well as the bond wire inductance needed to match the output to 50 Ohm.

$$C_{out} = 500fF$$

$$L_{out} = 5nH$$



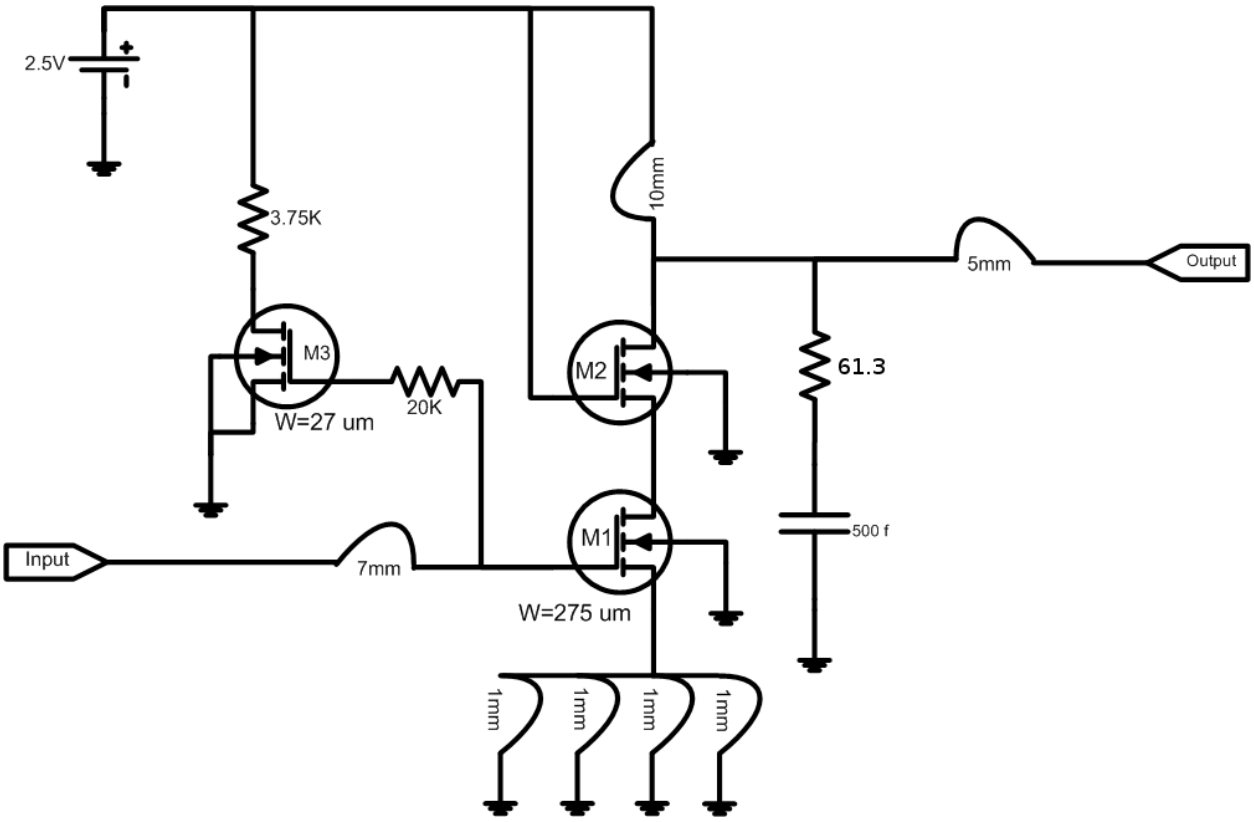
These values can be verified by using the standard L-match equations with a Q value of 1.64 (This results in L=5.3 nH and C=577 fF).

If there is no DC block, R_{out} will dissipate power and decreases the current to bias M1 resulting in a lower g_m. To address this issue we use a Parallel to Series transformation to transfer the parallel RC to series RC. This eliminates the need for a DC blocking cap for the resistor as well as reducing the value of the resistor to 61.3 Ohms

Drain Inductance (L_{dd})

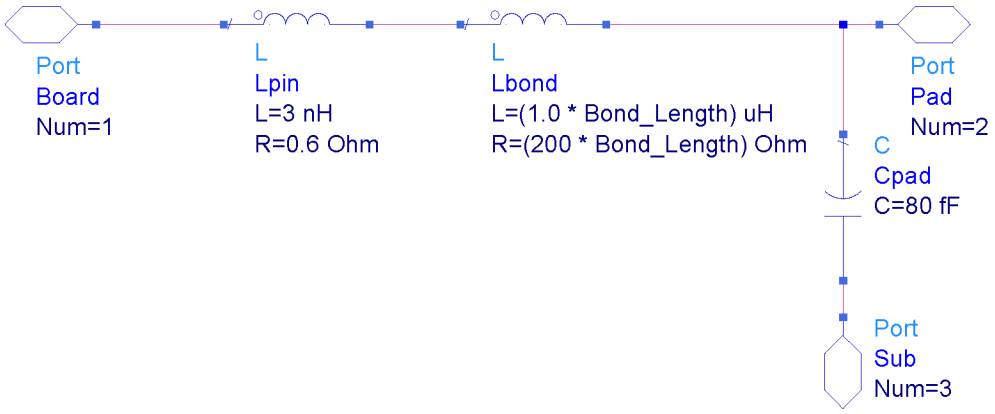
To maximize the gain, we need to maximize L_{dd}; however, there are restriction on total bond wire length. Due to the constraints, we assume one 10mm bond wire (L_{dd} = 13nH, R_{dd} = 2.6Ohm, C_{pad}=80fF) on the drain.

The following figure shows the summary of initial design.

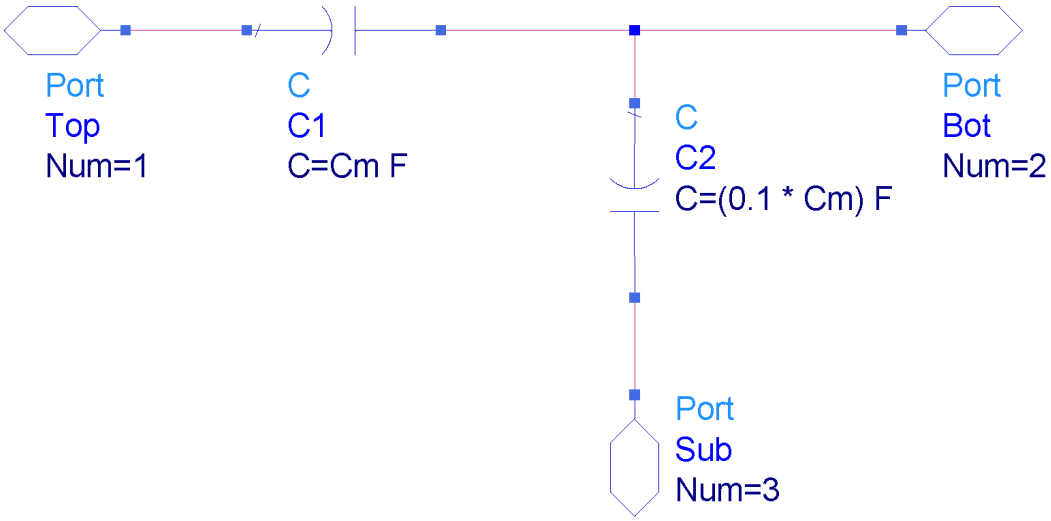


Simulation and Optimization

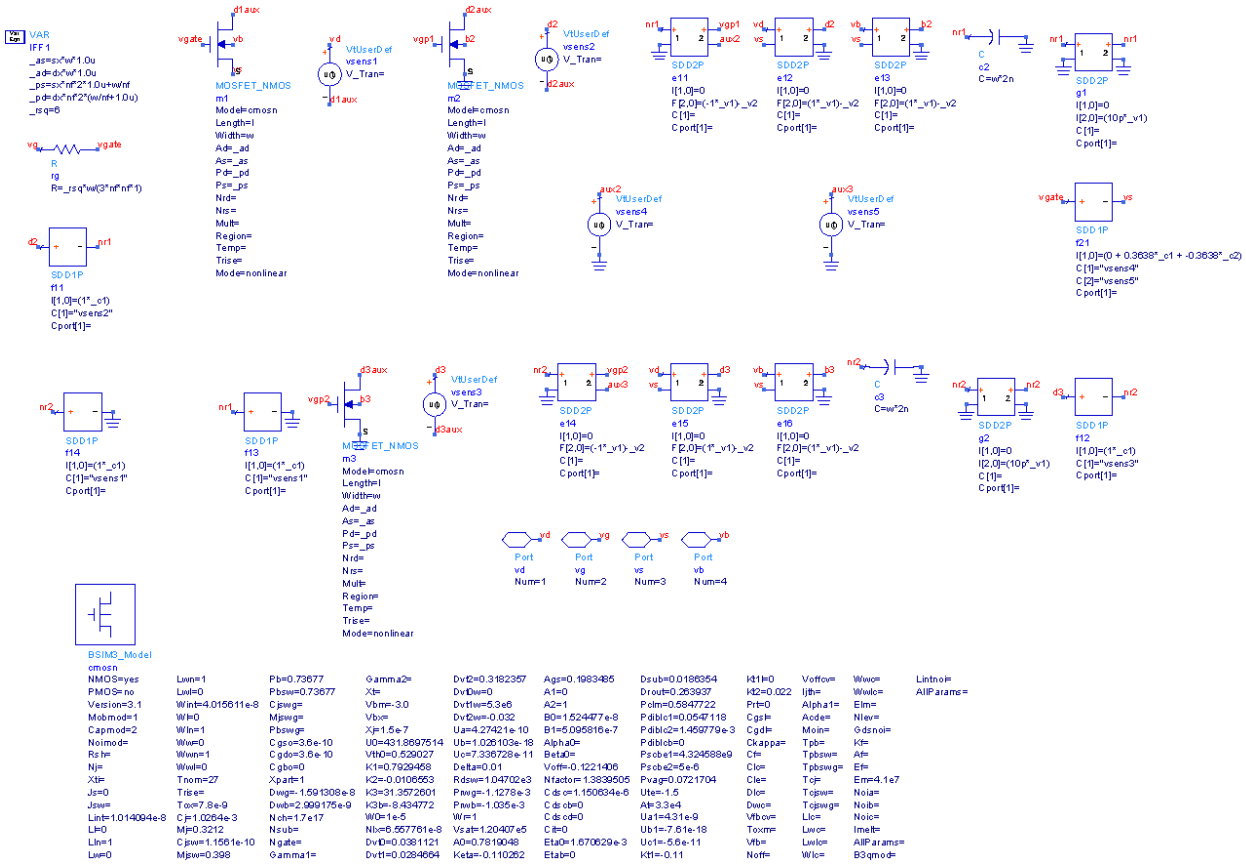
In the initial design process, we simplified the hand calculations by only focusing on the factors that have the most effect on the design; however, the final design needs to consider all the factors included in the models. To achieve this goal, the circuit had been modeled using Advance Design System (ADS). The HSPICE models for MMCAP, PIN (including bond wire) and NNMOS were imported[5] to ADS:



PIN Model in ADS



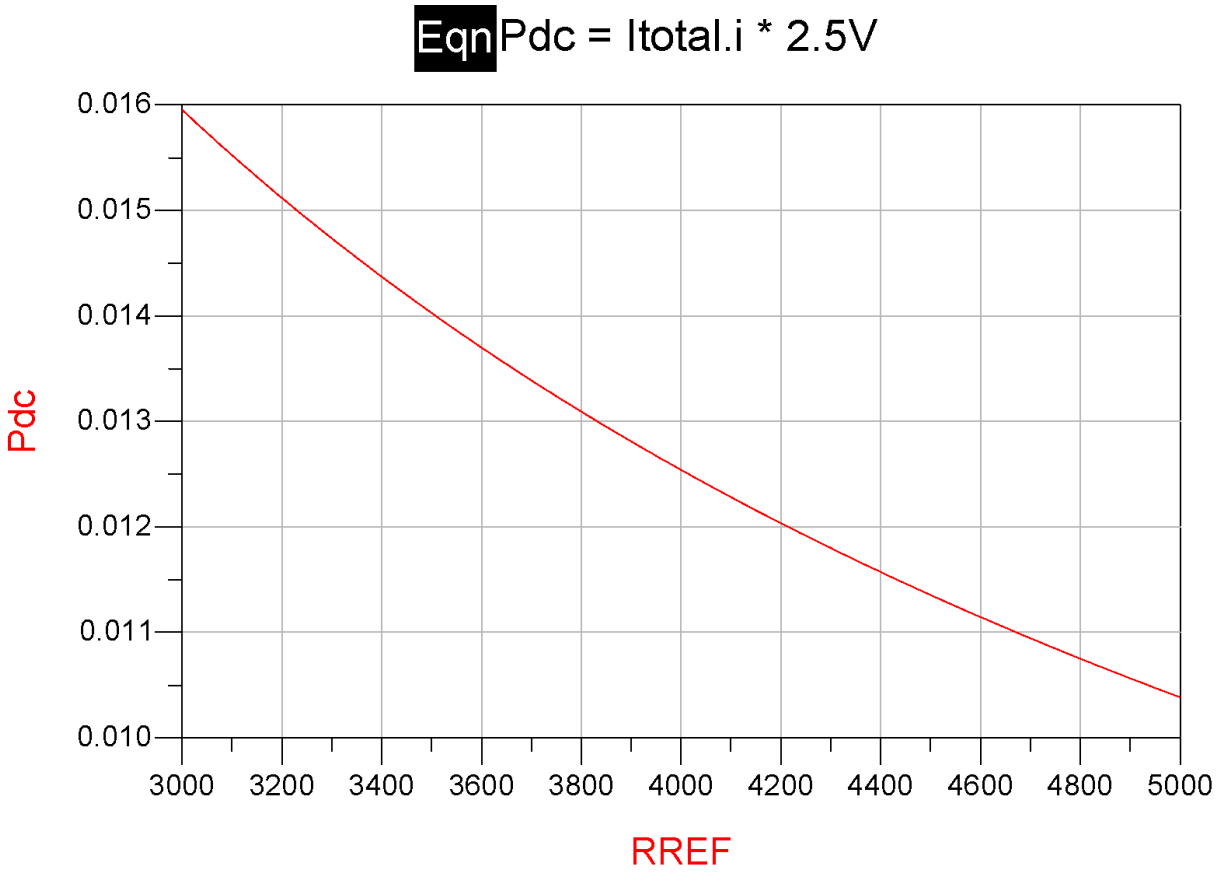
MMCAP Model in ADS



NNMOS Model in ADS

DC Bias (R_{REF})

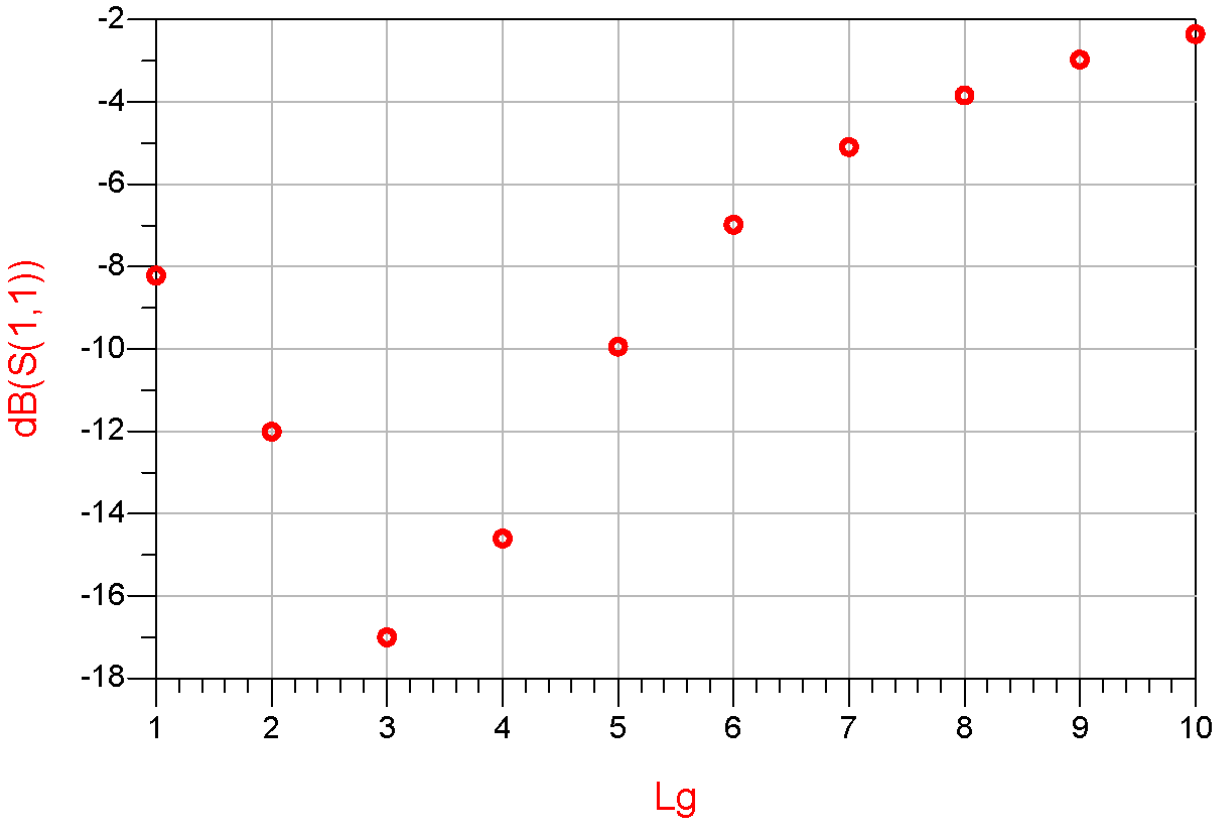
DC power consumption vs R_{REF} value was simulated to utilize the max allowed DC power; which in return maximizes gain and linearity and minimizes the noise. The graph helped to change R_{REF} to 4.4KOhms, which represents P_{DC} = 11.5mW.



Also, a 1mm bond wire connects the resistor to V_{dd} on the board. To use less bond wire, the gate of M2 is also connected to the same net, but in order to provide a better AC grounding, a 6pF mmcap to ground is added to M2 Gate.

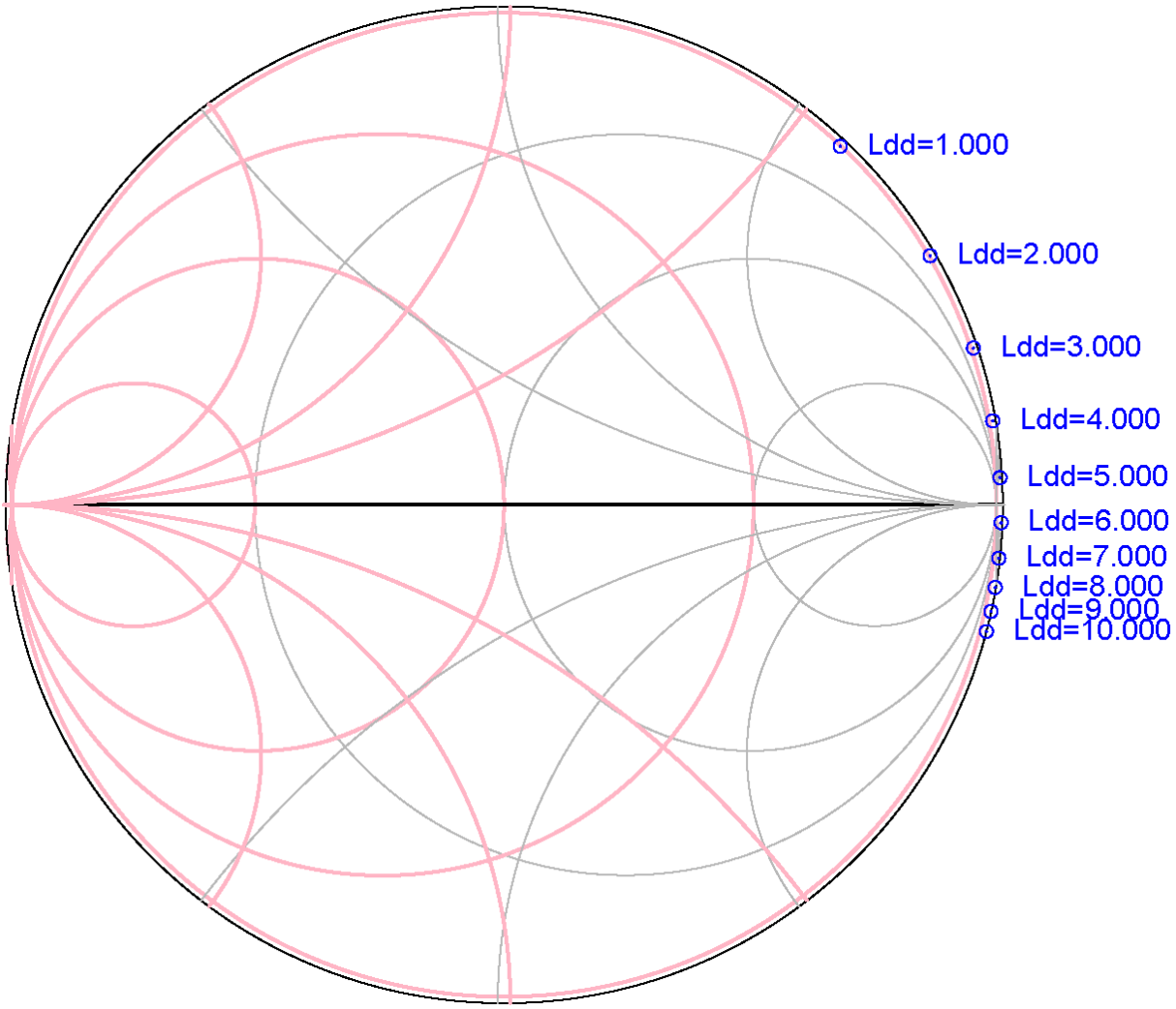
Gate bond wire length (L_g)

Due to the four 1mm bond wires on the source pin, the gate bond wire length had to be adjusted to optimize $|S_{11}|$



Drain supply bond wire length (L_{dd})

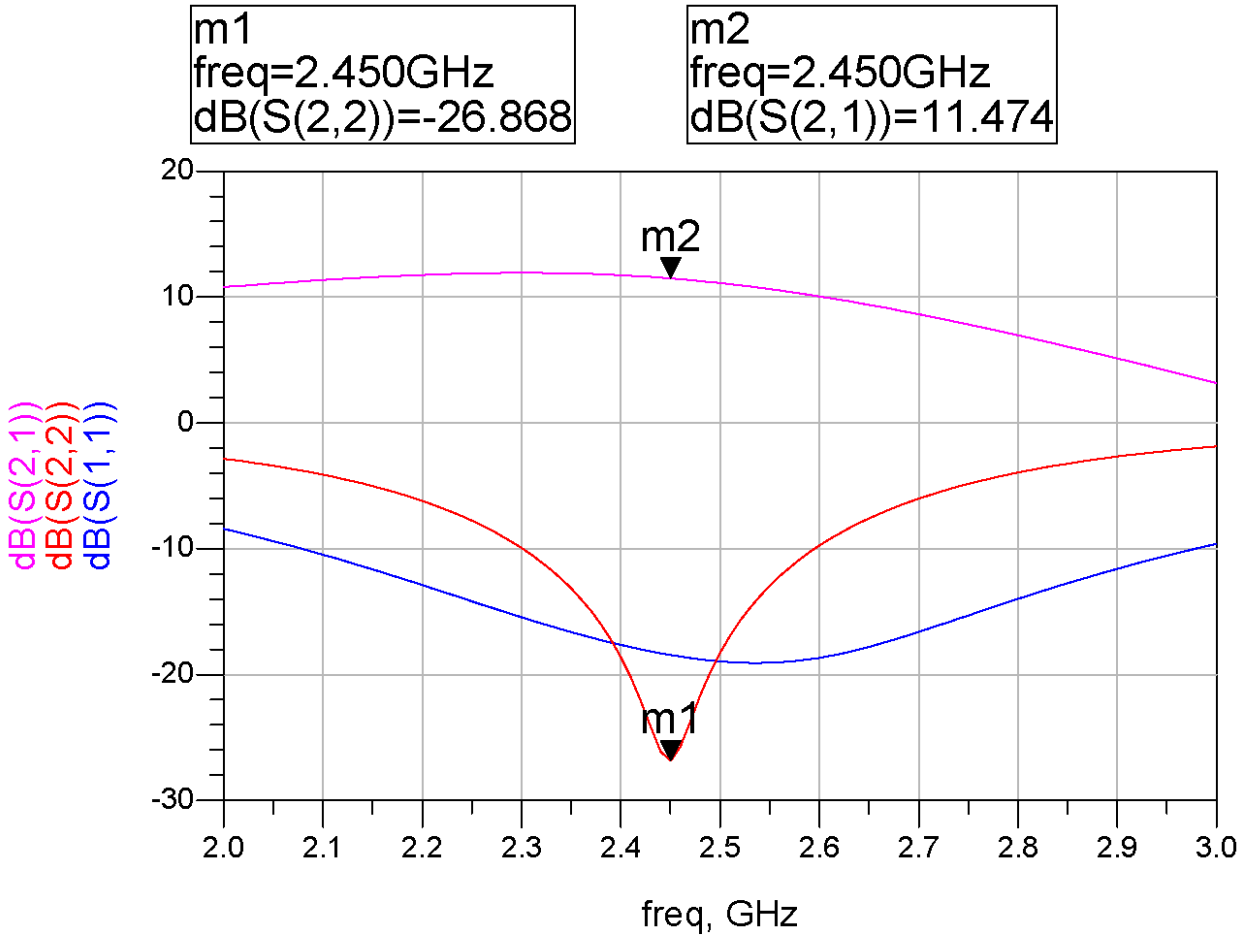
The impedance seen by the drain of M2 was swept vs L_{dd} which showed that the L_{dd} length can be reduced to 5mm to use less bond wire length while maintaining high impedance seen by the drain of M2.



Output network (R_{out}, C_{out} and output bond wire length)

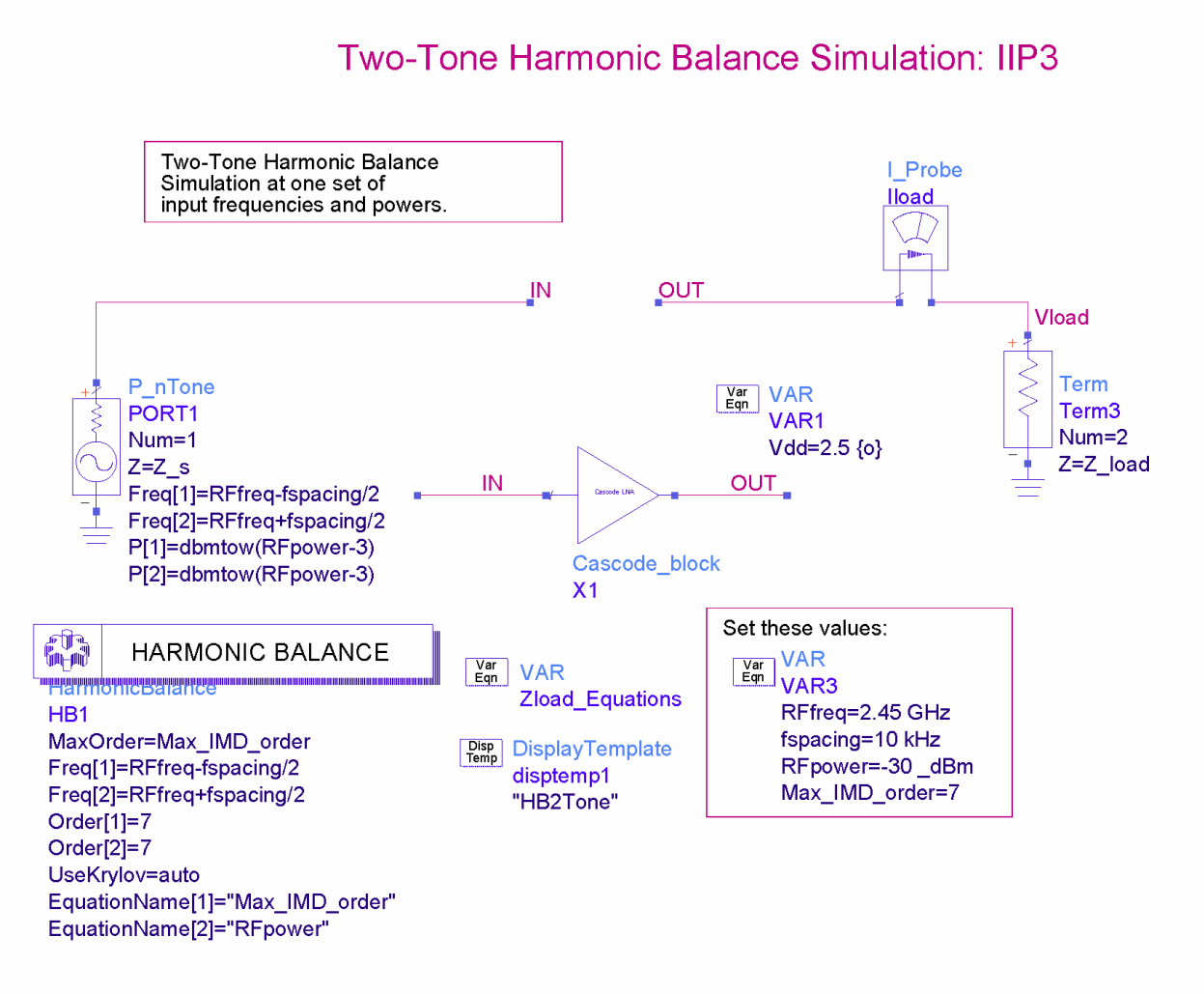
The ground pin of C_{out} is connected to C_b=6pF to provide an AC ground. S-parameter simulation showed that for a 5mm output bond wire with R_{out} = 61Ohm and C_{out} = 478fF, the following s-parameter values were obtained:

$|S_{22}|$ = -26dB and $|S_{21}|$ = 11.5dB.



Linearity

In order to measure the IIP3 a harmonic balance simulation was used. Per the specifications, the total input power was -30 dBm (-33 dBm per tone) with a spacing of 10kHz. The schematic elements needed for this simulation are shown below. The simulation shows an IIP3 of -4.8dBm, well within the specification of -7dBm.

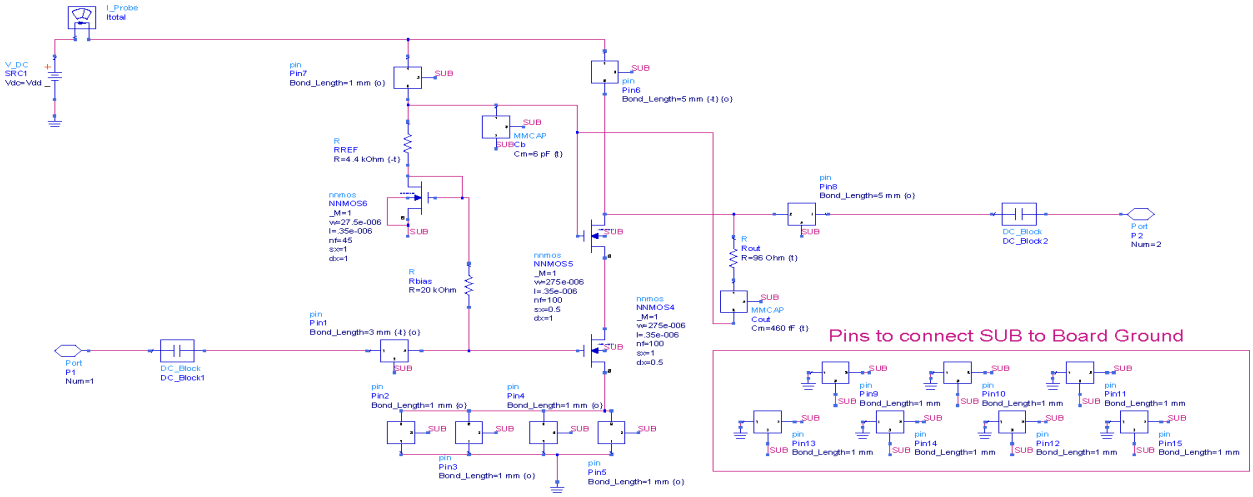


Ground to SUB Bond wires

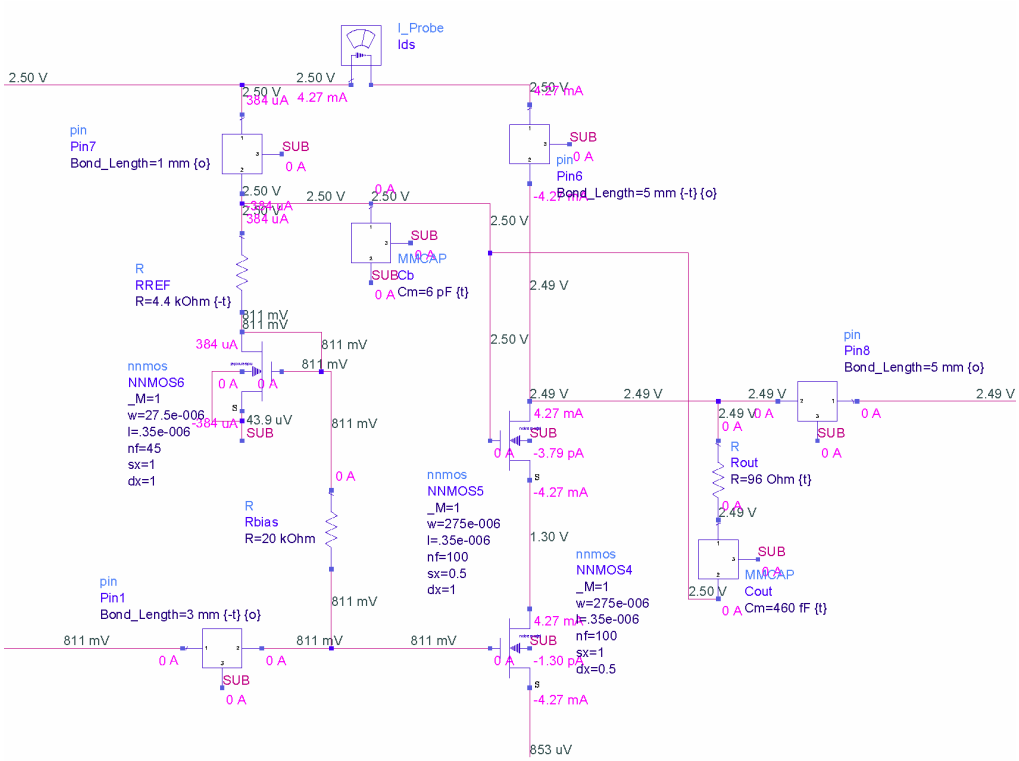
We also need to connect the SUB plane of the CMOS LNA to the ground of the board using bond wires. In order to minimize the parasitic between the board ground and SUB plane, multiple pins with shortest bond wire possible (1mm) are used to connect them together. Seven pins each with 1 mm bond wire are added to the design to connect SUB plane to board ground.

Final Design

After the whole circuit is put together, the output match was worse than -20dB, so R_{out} and C_{out} were modified to meet all the requirements (Please refer to Appendix). Bellow is the complete design:



Below are the critical areas of the design with the DC values annotated:



Variation from initial design

The following table shows a comparison between hand calculated and optimized values.

Component	Hand Calculation	Optimized
V_{dd}	2.5V	2.5V
R_{BIAS}	20K	20K
R_{REF}	3.75K	4.4K
W	275um	275um
Source bond wire	4 x 1mm	4 x 1mm
Gate bond wire	1 x 7mm	1 x 3mm
Drain bond wire	1 x 10mm	1 x 5mm
R_{out}	61	96
C_{out}	500 fF	460 fF
Output bond wire	1 x 5mm	1 x 5mm

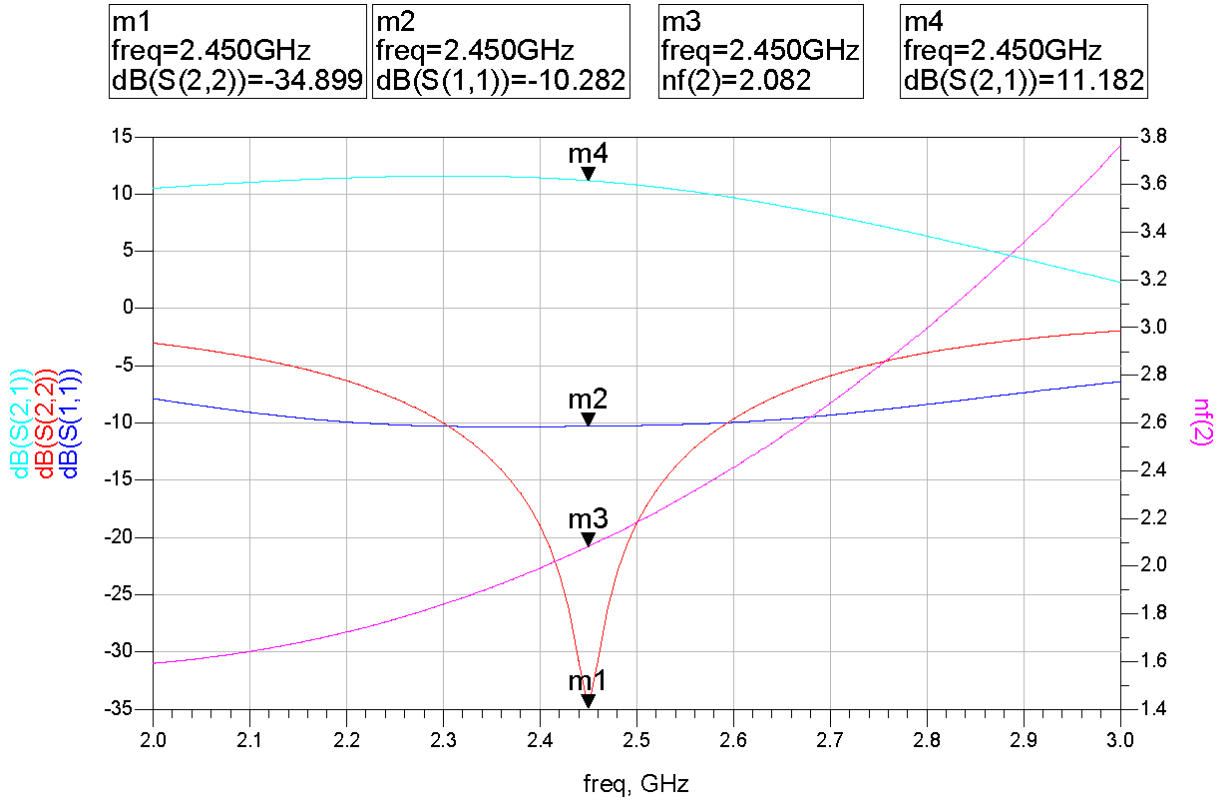
Performance

The following table shows the summary of the CMOS LNA performance at 2.45GHz compared with the design specifications.

	Specification	Achieved
P_{dc}	≤ 12mW	11.5 mW
$\|S_{11}\|$	≤ -10dB	-10.3dB
$\|S_{22}\|$	≤ -20dB	-34.9dB
$\|S_{21}\|$	≥ 10dB	11.2dB
IIP3	≥ -7dBm	-4.8dBm
NF	≤ 2.5dB	2.1dB
V_{dd}	≤ 2.5V	2.5V
Total Capacitance	≤ 100pF	6.46pF
Total Resistance	≤ 100K	24.4K
Total bond wire	≤ 30mm	25mm
No. of Pins	≤ 20	15

Appendix

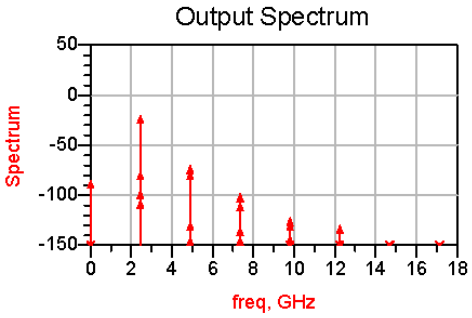
$|S_{11}|$, $|S_{22}|$, $|S_{21}|$ and Noise Figure

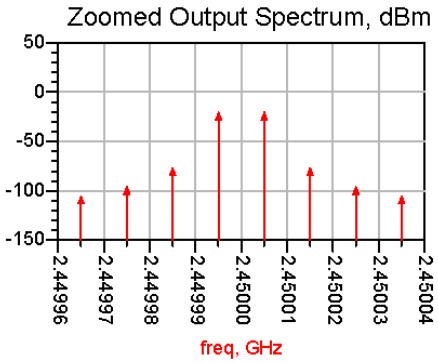


IIP3

Harmonic Balance Two-Tone Test

Use with HB2Tone Schematic Template





Fundamental Frequencies	Available Source Power Both Tones,dBm
2.449995 G 2.450005 G	-30.00

Fundamental Output Power, Both Tones,dBm	Transducer Power Gain
-18.855	11.145

Low and High Side Output TOI Points, dBm		Low and High Side Input TOI Points, dBm	
6.312	6.312	-4.833	-4.832

Low and High Side Output 5thOI Points, dBm		Low and High Side Input 5thOI Points, dBm	
-3.047	-3.045	-14.192	-14.190

These become invalid as the amplifier is driven into compression.
If the low and high side TOI points do not agree, try increasing the order of each tone and/or the maxorder.

References

[1] R. Jacob Baker "CMOS: circuit design, layout, and simulation", Wiley-IEEE Press; 2 edition, 2004

[2] Fukui, H., "Design of microwave GaAs MESFET's for broadband low noise amplifier," IEEE Transactions on Microwave Theory and Techniques, Vol. 27, No. 7, 1979.

[3] T. H. Lee, The Design of CMOS Radio Frequency Integrated Circuits, 2nd ed. Cambridge University Press, 2004.

[4] Xuan Chen, Quanyuan Feng, and Shiyu Li; "Design of a 2.5GHz Differential CMOS LNA" Progress In Electromagnetics Research Symposium, Cambridge, USA, July 2-6, 2008, page 203

[5] http://edocs.soco.agilent.com/display/ads2009/Creating+HSPICE+Compatible+Designs