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OTP Memory Specification

-for capacitive sensors

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1 Document control

1.1 Revision history

Revision history is handled by Aras.

1.2 References

Ref	Doc number	Rev	Title
1	13/210-AIC9003N	A	OTP Memory Design Specification Vienna platform
2	N/A	A	NeoFuse OTP description "NeoFuse Technology Introduction_SDDI Customers1 (002).pdf"
3	N/A	N/A	https://en.wikipedia.org/wiki/ASCII, section "ASCII printable characters"
4	N/A	N/A	S018GEFUSE_PIPO512B_datasheet, SMIC Macro Cell Data Sheet S018GEFUSE_PIPO512B
5	TSMC Electrical Fuse	Version 212A	TEF018G32X16PI33_C160215
6	Aras: 100022106	Version 0.453	Attopsemi AT128X8Z180MH0AA 128 x 8 Bits One Time Programmable Device SMIC 0.18µm 1.8V/3.3V Mixed Signal Process
7	N/A	Nov.22 2019	UMC design specification: Design_Spec_L153LM_eFuse_3p3V_v03.pdf

1.3 Terms and abbreviations

Term	Description
OTP	One Time Programmable memory. Memory that can be read several times, but programmed only once.
NVM	Non Volatile Memory. Information is retained during power-cycle. Can also be used for OTP.
FPC	Fingerprint Cards
CP test	Circuit Probe test. Functional test with dies still on the wafer.
MSB	Most significant Byte. Note upper case letters.
LSB	Least significant Byte. Note upper case letters.
msb	Most significant Bit. Note lower case letters.
lsb	Least significant Bit. Note lower case letters.

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2 Document introduction

2.1 Objective

This document serves as an index and an introduction to the use of OTP memories in the sensors and other chip products available from FPC
The OTP memory is divided into sections each containing different information. The formats of these sections are described in separate chapters, see the list of contents.
The product specific information is specified in a separate document together with the product. The product specific document refers to the specifications for each of the memory sections used by the product.

2.2 Usage

The OTP documentation for a product shall always refer to a released revision of each OTP section document.
The contents of a layout format cannot be changed once it is part of a released revision of the corresponding OTP section document. The reason for this is that the same layout format can be used by several products. Instead, a new layout format must be added with a new format ID.
To be able to release new revisions of the OTP section documents, it is allowed to indicate that a format ID is preliminary. Once it has been introduced in a production test, i.e. chips have been delivered using the format, it shall be permanent.

2.3 Information distribution

The OTP documentation structure contains information that is internal to FPC. However, details about the actual formats used for a specific product can be extracted and distributed to affected customers.

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3 OTP Memory

3.1 Main usage

The OTP memory is mainly intended to introduce the possibility to uniquely identify a sensor die. The memory is limited in size, so the amount of information to store in the memory must be selected with care.

3.2 OTP HW

Depending on foundry choice, different OTP IP is used.

3.2.1 Foundry provided OTP IPs

The OTP used by sensors manufactured at SMIC is described in ref [4], sensors manufactured at TSMC use OTP described in ref [5] and sensors manufactured at UMC use OTP described in ref [7].

3.2.1.1 Default value

Every OTP memory bit has a default value of “0” and may be changed to “1” with OTP write command. Any “0” bit can be changed to “1”, however it cannot be changed back to “0”. Any single bit shall not be written twice, writing a “1” twice may damage the sensor.

3.2.1.2 Data redundancy

Only one type of error needs to be considered; an OTP bit with value “1” may erroneous become a “0”. To mitigate this, the following simple error correction method is used:
OTP memory address space 0 to 31 is duplicated at address 32 to 63 (decimal address numbers), reducing the effective payload of the memory to 32 bytes (256 bits).
OTP write: OTP writes to OTP address X shall also written to OTP address X+32 (decimal).
OTP read: OTP read from OTP address X shall be bitwise OR with read from OTP address X+32 (decimal).

3.2.1.3 Data integrity check

The OTP memory data integrity shall be validated before OTP memory usage. The data integrity validation method uses the redundancy information described in Section 3.2.1.2.
Method:

i. Count bit errors by comparing OTP memory content at address X with OTP memory content at address X+32 (decimal).
ii. If a bit error is detected, re-read X and X+32 for the OTP memory byte with the detected bit error.
iii. OTP memory with all bits = “0” in the address range to be tested is classified as broken OTP memory.

The number of allowed bit errors will be product specific and are not detailed in this document.

3.2.2 Non foundry provided OTP IP

3.2.2.1 Attopsemi OTP IP

The I-Fuse OTP from Attopsemi is described in ref [6].
The Attopsemi I-fuse™ OTP memory is based on the irreversible mechanism of electro-migration. The programming mechanism is deterministic, controllable, and can be modeled precisely by physical laws. The OTP cell size is only 1/100 of the conventional e-fuse cells in the comparable CMOS technologies by using 1R1D cell instead of 1R1T. The D means “diode”, which is a source/drain junction diode of a PMOS device available in any CMOS processes. The effective IP size is also about half to one-third of the other

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OTP technologies because of small cell size and low overhead peripheral circuits. Unlike other OTP technologies, the I-fuse™ OTP memory only uses the convenient core and I/O voltages for program and read, i.e. 1.8V/2.5V/3.3V, so that the I-fuse™ is very easy to use. No needs to have large area and power hungry charge pumps.

3.2.2.2 eMemory OTP IP

The NeoFuse OTP from eMemory is described in ref [2].
NeoFuse is a small-form factor logic NVM technology with the advantages of low-power operation, high reliability and strong security. It provides non-volatile storage functions from 0.15um down to the leading 5nm FinFET technology node. The density supports a range of 64 to 4M bits.
For IP operations, NeoFuse provides a user-friendly interface and fully integrated OTP IP that minimizes design effort and circuit complexity when embedded as a NVM silicon IP. An internal charge pump is designed and embedded in the NeoFuse silicon IP to enable field programming capabilities. eMemory's proprietary ROM code conversion, NeoROM, can also be used to reduce programming costs once the program code is fixed.

3.3 OTP sections

The OTP memory can have up to 4 different sections depending on how the current chip is integrated into the target platform.
Detailed descriptions of the different sections are available in the following documents:

Table 1. Available memory sections

Section	Mandatory	Reference
Wafer	Yes	Chapter 5
Package	No	Chapter 6
Module	No	Chapter 7
Vendor specific	No	Product specific document

Each format has an ID to identify the mapping of the information. This format ID starts with 1 for each of the three sections Wafer, Package and Module.
All sections, except the vendor specific, start with a byte indicating the format ID.

3.3.1 Wafer

This section is mandatory in all chips from FPC containing an OTP.
The Wafer section contains information that uniquely identifies the chip, e.g. Lot ID, wafer ID, position on the wafer. There is also a possibility to store calibration information such as trimming of an oscillator.
The information here shall be generic so that the chips can be used for any purpose, e.g. both single and multiple chip packages.
The data in this section is normally written during the wafer test (CP test).

3.3.2 Package

This section is optional.
This section contains information about the package that the chip is mounted in. If the package contains more than one chip, the OTP can also contain information about the other chip(-s) in the package. The information shall be as generic as possible so that the package can be used for different types of assemblies.
The data in this section is normally written during the package test (Final Test).

3.3.3 Module

This section is optional.

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This section contains information about the module that the package is mounted in.
The data in this section is normally written during the module production test.

3.3.4 Vendor specific

This section is optional.
The vendor specific information is normally stored at the end of the available OTP memory. The size of the information is specified in the product specific documentation. The FPC software cannot be expected to parse this section of the memory and it will be regarded as raw binary data.
However, it is also possible to reserve some bytes inside the Wafer, Package or Module sections for vendor specific information. In that case, these bytes will be included in the size of the corresponding section. E.g. if the Package section contains 4 FPC bytes and 2 vendor bytes, the total size of the Package section will be 7 bytes (1 byte format ID + 4 FPC bytes + 2 vendor bytes).

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3.4 Memory utilization

The two msb (most significant bits) of the first byte of the Wafer section indicate if the Module and/or Package section of the OTP memory are used. The table below shows the possible combinations of the two bits:

Table 2. Coding of memory section usage.

Value (bit 7:6)	Description
00	All bytes following the Wafer section are either vendor specific or not yet used.
01	The Package section holds an FPC format. The remaining part of the memory is either vendor specific or not yet used. ***Note: FPC1268 may have Package section without setting this bit.***
10	The Module section holds an FPC format. **The Package section is not used (0 bytes).** The remaining part of the memory is either vendor specific or not yet used.
11	Both Package and Module sections are FPC format. Any remaining bytes are either vendor specific or not used.

The two msb of the first byte will be written when the information in the corresponding section is written, e.g. bit 7 is written when the Module information is written in the OTP memory.

The image below shows the different layout situations depending on the two first bits in the first byte.

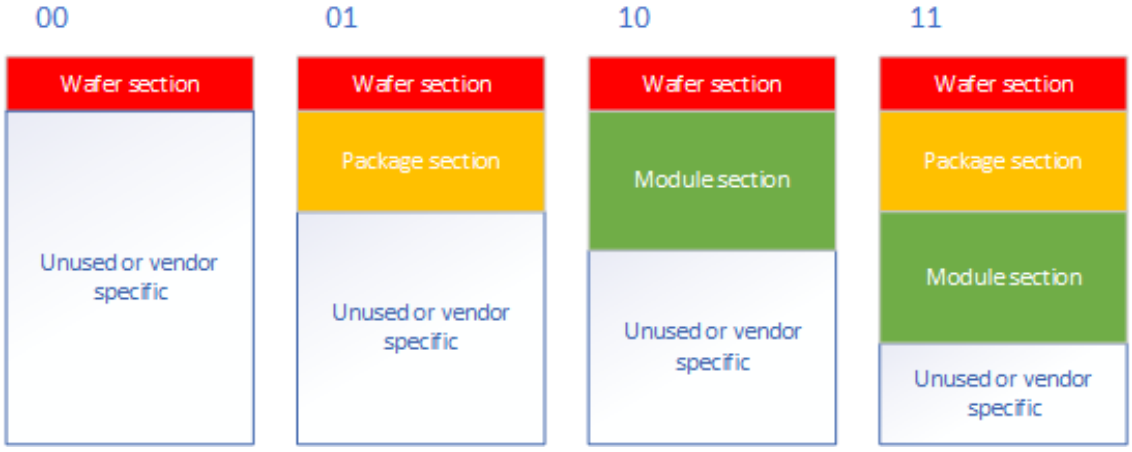

Figure 1. Available memory layout combinations

As the size of each section is specified by the format ID, it is possible to determine the size of the remaining part of the OTP memory.

3.5 Special handling of Module section in FPC1266 and FPC1268

The Module section of sensors with hardware ID 0x321 and 0x341 is always written with static placement at address 0x13 (20d) regardless of the presence of a Package section in the OTP memory. At the time of writing this means FPC1266, FPC1268, FPC1267. This will result in the following distribution of the data:

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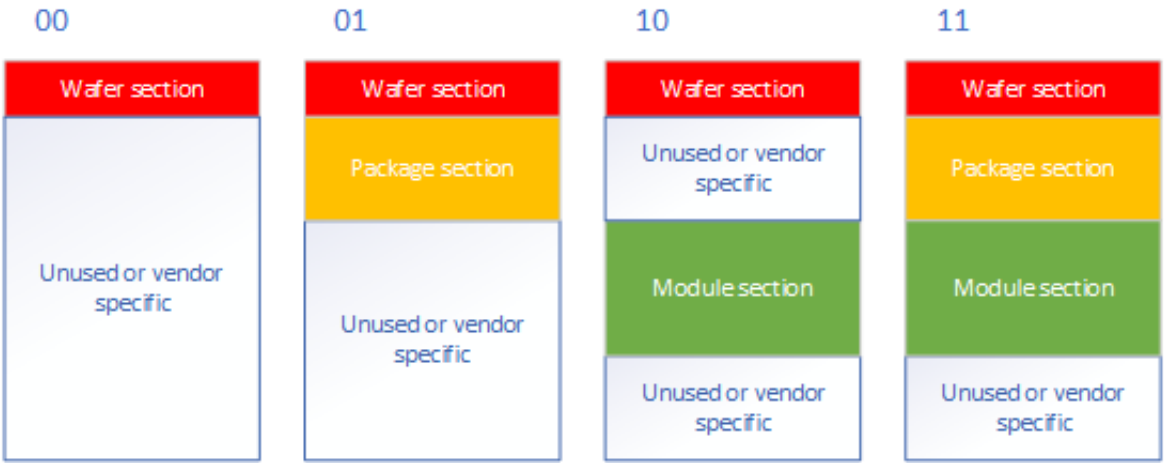

Figure 2. OTP layout for sensors with static placement of the Module section.

3.6 OTP memory size

The maximum size of the OTP memory differs between sensors intended for the mobile market and sensors intended for smartcard/IoT market. Sensors used for payment solutions will require security keys present in the OTP.

3.6.1 Mobile

Sensors intended for mobile market will require 256 bits (32 bytes) OTP memory size, legacy bytes only.

3.6.2 Embedded

Sensors intended for IoT market will require >256 bits OTP memory size, legacy bytes + security keys (MAC + ENC keys) etc.

3.6.3 Smartcard

Sensors intended for smartcard market will require >256 bits OTP memory size, legacy bytes + security keys (MAC + ENC keys) etc. Singen requires 1024 bits.

Table 3 lists the different sections of the Singen 1024-bit OTP memory.

Table 3. Singen 1024-bit OTP memory sections

Section	Address	Size	Read lock	Write lock	Content / Description
F	896 - 1023	128	Y	Y	Reserved for future security functionality
E	640 – 895	256	Y	Y	ENC-key K1
D	512 – 639	128	Y	Y	MAC-key K2
C	504 – 511	8	N	Y	Security Mode and Lock Enable bits*
B	256 – 503	248	N	N	Future Use for information storage
A	0 – 255	256	N	N	Legacy information (wafer, package, module)

**See Table 4 for detailed information*

- Read lock means that bits can't be read out via debug ports or API after lock has been enabled.

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- Write lock means that bits can be read out via debug ports or API, but not written after lock has been enabled.

Table 4. Security Mode, Size and Lock Enable Bit

Section C			
Byte Index	**Bit index**	**Internal index**	**Comment/Description**
63	511:510	7:5	Reserved
	508	4	ENC-key length. One bit. 0 – 128 bit key. 1 – 256 bit key
	507	3	Reserved
	506:505	2:1	Security Mode. Two bits. 00 – No security. 01 – Invalid 10 – Authentication only (MAC mode). 11 – Encryption and Authentication (EtM Mode)
	504	0	Lock bit. Prohibit write to section C to F Prohibit external read from section D to F

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4 Supplier information

4.1 Encoding of Lot ID

The Lot ID is used to specify the lot when the wafer was manufactured. The ID usually specifies the production plant and type of lot. There is also a running serial number. The format of the ID differs between different suppliers. The following sections describe the available suppliers and how their Lot ID are constructed. The encoding of the ID inside the OTP is also described.

4.1.1 SMIC

The Lot ID for SMIC contains 6 characters, e.g. DP6409

- 1st character: Production area, “D” for S1, “E” for Fab 4, “H” for Fab 7, and “S” for Fab 15
- 2nd character: Run type, “P” for pilot, “B” for probe card lot, “L” for Engineering lot, and “T” for research or technology develop lot, “0~9”&”A,E,F,G,H,J,K,M,N,Q,S,U,W” for general production lot
- 3rd to 6th character: Serial number, 0001 to W999 (exclude C, D, I, O, V, X, Y, Z in character 3).

For production lots, the serial number extends to also include the 2nd character:
00001 => …. => 09999 => 0A000 => 0A001 => … => 0W999 => A0000 => A0001 => … => AW999 => E0000 => E0001 => … => WW999 => after this the serial number will begin at 00001 again.

In the wafer section of the OTP, the Lot ID for SMIC will be encoded as follows:

Table 5. Encoding for SMIC lot ID.

Byte	Character	Encoding
1	1	8 bit printable ASCII
2	2	8 bit printable ASCII
3	3	8 bit printable ASCII
4-5	4-6	16 bit representation of numerical serial number (0 – 999), see example below. Byte 4 Most significant byte of the serial number. Byte 5 Least significant byte of the serial number.

Example:
The Lot ID DP6409 will be encoded as follows:

Table 6. Example of SMIC encoding.

Byte	Value	Meaning
1	0x44	“D”
2	0x50	“P”
3	0x36	“6”
4 5	0x01 (MSB) 0x99 (LSB)	409 (decimal)

4.1.2 TSMC

The Lot ID for TSMC contains 6 characters, e.g. “G0WG56”

- 1st character: fab, letter A-Z , “G” stands for TSMC Fab6
- 2nd character: lot type, letter A-Z or digit 0-9, “6” stands for engineering lot
- 3rd to 6th character: serial number, letter A-Z or digit 0-9

As the Lot ID for TSMC can contain letters (A-Z) in all positions, all characters (except the first) will be encoded as 7-bit printable ASCII. In order to fit into 5 bytes of memory, the TSMC Lot ID will be encoded as follows:

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Table 7. Encoding of TSMC lot ID.

Byte	Encoding
1	bit 7:4 fab ID (4 bits, see table below) bit 3:0 lot type (4 msb)
2	bit 7:5 lot type (3 lsb) bit 4:0 serial pos 1 (5 msb)
3	bit 7:6 serial pos 1 (2 lsb) bit 5:0 serial pos 2 (6 msb)
4	bit 7 serial pos 2 (lsb) bit 6:0 serial pos 3 (7 bits)
5	bit 7:1 serial pos 4 (7 bits) bit 0 spare

To save room, the fab ID is converted to a number between 1 and 15 according to the table below. The table will be extended when additional fabs are identified.

Table 8. Encoding of TSMC fabs.

Value	Fab	TSMC value
1	Fab 6	G
2	Fab 8	Q
3	Fab 10	H

Example:
The Lot ID “G0WG56” will be encoded as follows:

Table 9. Example of TSMC lot ID.

Character	Value
G	1 (see table above)
0	0x30
W	0x57
G	0x47
5	0x35
6	0x36

This results in the following byte values in the OTP memory map:

Table 10. Encoded bytes in the OTP

Byte	Value
1	0x16
2	0x15
3	0xE3
4	0xB5
5	0x6C

4.2 Package vendors

The following is a list of the available package vendors, and the ID used in the OTP memory to identify them.

Table 11. Available Package vendors

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Name	Value (Hex)
DreamTech	0x10
Crucialtec	0x11
Primax	0x12
O-Film	0x13
Mcnex	0x14
Huatian	0x15
SPIL	0x16
Hana Micron South Korea	0x17
Hana Micron Vietnam	0x18

4.3 Module vendors

The list of available module vendors is maintained by the Customer Projects team. The current set of module vendors are specified at the following location in the FPC Confluence:
https://fpc-confluence.fingerprint.local/confluence/display/CS/OTP+Write
(Nedcard?)

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5 OTP Wafer Memory Layout

This chapter defines the OTP memory layout of the Wafer section.

5.1 Format description

The first byte of the format specifies the format ID. The size of the format includes this first byte.
Important: The two msb (most significant bits) of the ID byte (bits 7-6) indicate if the Package and Module sections are used, see chapter 1-4.
Normally, the information in the Wafer section is written during CP test (Circuit Probe).

5.1.1 Wafer Format ID 63 Only vendor specific information

Size in bytes: 1
If the project decides that the entire OTP memory shall be dedicated to the vendor, the Wafer section will still need one byte to indicate that the information is not possible to parse by the FPC SW.

Section	Byte	Usage	Format
Admin	0	OTP Wafer layout format ID	bit 7:6 = 00 bit 5:0 = 111111

5.1.2 Wafer Format ID 00 0001

Size in bytes: 12
Chip ID is uniquely identified by the Lot ID, wafer coordinates, wafer ID and manufacturing date.
Wafer produced by SMIC:

Section	Address	Content
Admin	Byte 0, bit 5:0	**Layout format ID = 00 0001**
Wafer	Byte 1, bit 7:0	Lot ID, 3 first letters, ASCII char, e.g. “DAW” in “DAW591. 1st letter.
Wafer	Byte 2, bit 7:0	Lot ID, 3 first letters, ASCII char, e.g. “DAW” in “DAW591. 2nd letter.
Wafer	Byte 3, bit 7:0	Lot ID, 3 first letters, ASCII char, e.g. “DAW” in “DAW591. 3rd letter.
Wafer	Byte 4, bit 7:0	Lot ID, 3 last digits, binary number, e.g. 591 in “DAW591”. 8 bits together with row below, MSB part.
Wafer	Byte 5, bit 7:0	Lot ID, 3 last digits, binary number, e.g. 591 in “DAW591”. 8 bits together with row above, LSB part.
Wafer	Byte 6, bit 7:0	X-Coordinate.
Wafer	Byte 7, bit 7:0	Y-Coordinate.
Wafer	Byte 8, bit 7:3	Wafer ID (1-25).
Wafer	Byte 8, bit 2:0	OscHiTrim (3 MSB) @ functional mode
Wafer	Byte 9, bit 7:6	OscHiTrim (2 LSB) @ functional mode
Wafer	Byte 9, bit 5	Static, always ‘0’
Wafer	Byte 9, bit 4:0	OscLoTrim
Wafer	Byte 10, bit 7:1	Time stamp, year (binary, 0 = year 2000)
Wafer	Byte 10, bit 0	Time stamp, Month (MSB)
Wafer	Byte 11, bit 7:5	Time stamp, Month (3 LSB)
Wafer	Byte 11, bit 4:0	Time stamp, day

5.1.3 Wafer Format ID 00 0010

Size in bytes: 12
Chip ID is uniquely identified by the Lot ID, wafer coordinates, wafer ID and manufacturing date.
Wafer produced by TSMC.
Important: The coordinates for the die on the wafer are in 2-complementary format meaning that they can be negative if Origo is in the centre of the wafer.

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Section	Address	Content
Admin	Byte 0, bit 5:0	**Layout format ID = 00 0010**
Wafer	Byte 1, bit 7:4	fab ID (4 bits, see table in chapter 4.1.2 TSMC)
Wafer	Byte 1, bit 3:0	Lot ID, 5 last letters, ASCII char, e.g. “0WG56” in “G0WG56”. 1st letter
Wafer	Byte 2, bit 7:5	
Wafer	Byte 2, bit 4:0	Lot ID, 5 last letters, ASCII char, e.g. “0WG56” in “G0WG56”. 2nd letter
Wafer	Byte 3, bit 7:6	
Wafer	Byte 3, bit 5:0	Lot ID, 5 last letters, ASCII char, e.g. “0WG56” in “G0WG56”. 3rd letter
Wafer	Byte 4, bit 7	
Wafer	Byte 4, bit 6:0	Lot ID, 5 last letters, ASCII char, e.g. “0WG56” in “G0WG56”. 4th letter
Wafer	Byte 5, bit 7:1	Lot ID, 5 last letters, ASCII char, e.g. “0WG56” in “G0WG56”. 5th letter
Wafer	Byte 5, bit 0	Spare
Wafer	Byte 6	X coordinate on wafer, binary 2-complementary (range: -128 to 127)
Wafer	Byte 7	Y coordinate on wafer, binary 2-complementary (range: -128 to 127)
Wafer	Byte 8, bit 7:3	Wafer ID (range: 1-25)
Wafer	Byte 8, bit 2:0	Clock trim: oscHi (3 most significant bits) 5 bits 2-complementary (range -16 to 15)
Wafer	Byte 9, bit 7:6	oscHi (2 least significant bits)
Wafer	Byte 9, bit 5	oscLoFreq (bit value = 0)
Wafer	Byte 9, bit 4:0	oscLo , 5 bits 2-complementary (range -16 to 15)
Wafer	Byte 10, bit 7:1	Year (binary, year 2000 = 0)
Wafer	Byte 10, bit 0	Month (most significant bit)
Wafer	Byte 11, bit 7:5	Month (3 least significant bits)
Wafer	Byte 11, bit 4:0	Day

5.1.4 Wafer Format ID 00 0011

Size in bytes: 12

Chip ID is uniquely identified by the Lot ID, wafer coordinates, wafer ID and manufacturing date.

Wafer produced by UMC:

Section	Address	Content
Admin	Byte 0, bit 5:0	**Layout format ID = 00 0011**
Wafer	Byte 1, bit 7:0	Lot ID, 5 letters, ASCII char, “P1A23”. 1st letter.
Wafer	Byte 2, bit 7:0	Lot ID, 5 letters, ASCII char, “P1A23”. 2nd letter.
Wafer	Byte 3, bit 7:0	Lot ID, 5 letters, ASCII char, “P1A23”. 3rd letter.
Wafer	Byte 4, bit 7:0	Lot ID, 5 letters, ASCII char, “P1A23”. 4th letter.
Wafer	Byte 5, bit 7:0	Lot ID, 5 letters, ASCII char, “P1A23”. 5th letter.
Wafer	Byte 6, bit 7:0	X-Coordinate.
Wafer	Byte 7, bit 7:0	Y-Coordinate.
Wafer	Byte 8, bit 7:3	Wafer ID (1-25).
Wafer	Byte 8, bit 2:0	OscHiTrim (3 MSB) @ functional mode
Wafer	Byte 9, bit 7:6	OscHiTrim (2 LSB) @ functional mode
Wafer	Byte 9, bit 5	Static, always ‘0’
Wafer	Byte 9, bit 4:0	OscLoTrim
Wafer	Byte 10, bit 7:1	Time stamp, year (binary, 0 = year 2000)
Wafer	Byte 10, bit 0	Time stamp, Month (MSB)
Wafer	Byte 11, bit 7:5	Time stamp, Month (3 LSB)

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Wafer	Byte 11, bit 4:0	Time stamp, day

5.1.5 Wafer Format ID 00 0100

Size in bytes: 12
Chip ID is uniquely identified by the Lot ID, wafer coordinates, wafer ID and manufacturing date.
Wafer produced by Cansemi:

Section	Address	Content
Admin	Byte 0, bit 5:0	**Layout format ID = 00 0100**
Wafer	Byte 1, bit 7:0	Lot ID, 1 first letter, ASCII char, e.g. “D” in “D139999".
Wafer	Byte 2, bit 7:0	Lot ID, the 1st number, ASCII char, e.g. “1” in “D139999".
Wafer	Byte 3, bit 7:0	Lot ID, the 2nd number, ASCII char, e.g. “3” in “D139999"
Wafer	Byte 4, bit 7:0	Lot ID, the 4 last numbers, binary number, e.g. "9999" in “D139999”. 8 bits together with the row below, MSB part
Wafer	Byte 5, bit 7:0	Lot ID, the 4 last numbers, binary number, e.g. "9999" in “D139999”. 8 bits together with the row above, LSB part
Wafer	Byte 6, bit 7:0	X-Coordinate.
Wafer	Byte 7, bit 7:0	Y-Coordinate.
Wafer	Byte 8, bit 7:3	Wafer ID (1-25).
Wafer	Byte 8, bit 2:0	OscHiTrim (3 MSB) @ functional mode
Wafer	Byte 9, bit 7:6	OscHiTrim (2 LSB) @ functional mode
Wafer	Byte 9, bit 5	Static, always ‘0’
Wafer	Byte 9, bit 4:0	OscLoTrim
Wafer	Byte 10, bit 7:1	Time stamp, year (binary, 0 = year 2000)
Wafer	Byte 10, bit 0	Time stamp, Month (MSB)
Wafer	Byte 11, bit 7:5	Time stamp, Month (3 LSB)
Wafer	Byte 11, bit 4:0	Time stamp, day

5.1.6 Wafer Format ID 00 0101

Size in bytes: 12
Chip ID is uniquely identified by the Lot ID, wafer coordinates, wafer ID and manufacturing date.
Wafer produced by X-FAB:

Section	Address	Content
Admin	Byte 0, bit 5:0	**Layout format ID = 00 0101**
Wafer	Byte 1, bit 7:0	Lot ID, 1 first letter, ASCII char, e.g. “P” in “P12345".
Wafer	Byte 2, bit 7:0	Lot ID, the 1st number, ASCII char, e.g. “1” in “P12345".
Wafer	Byte 3, bit 7:0	Lot ID, the 2nd number, ASCII char, e.g. “2” in “P12345"
Wafer	Byte 4, bit 7:0	Lot ID, the 3rd number, ASCII char, e.g. “3” in “P12345"
Wafer	Byte 5, bit 7:0	Lot ID, the 2 last numbers, binary number, e.g. "45" in “P12345”
Wafer	Byte 6, bit 7:0	X-Coordinate.
Wafer	Byte 7, bit 7:0	Y-Coordinate.
Wafer	Byte 8, bit 7:3	Wafer ID (1-25).
Wafer	Byte 8, bit 2:0	OscHiTrim (3 MSB) @ functional mode
Wafer	Byte 9, bit 7:6	OscHiTrim (2 LSB) @ functional mode
Wafer	Byte 9, bit 5	Static, always ‘0’
Wafer	Byte 9, bit 4:0	OscLoTrim
Wafer	Byte 10, bit 7:1	Time stamp, year (binary, 0 = year 2000)
Wafer	Byte 10, bit 0	Time stamp, Month (MSB)
Wafer	Byte 11, bit 7:5	Time stamp, Month (3 LSB)

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Wafer	Byte 11, bit 4:0	Time stamp, day

5.1.7 Wafer Format ID 00 1001

Size in bytes: 13
Chip ID is uniquely identified by the Lot ID, wafer coordinates, wafer ID and manufacturing date. Wafer produced by SMIC one aditional byte for ASIC configuration data otherwise same format as Wafer Format ID 00 0001.

Section	Address	Content
Admin	Byte 0, bit 5:0	**Layout format ID = 00 1001**
Wafer	Byte 1-11	Same format as ID = 00 0001
Wafer	Byte 12, bit 7:6	Reserved for future Trim Values
Wafer	Byte 12, bit 5:1	OscHiTrim (Analog Frequency Scaling)
Wafer	Byte 12, bit 0	Reserved for future Trim Values

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6 OTP Package Memory Layout

This chapter defines the OTP memory layout of the Package section.

6.1 Package section formats

This section of the OTP is used both for packages containing only the sensor, and for SIP (System In Package) containing multiple chips, e.g. sensor and companion chip.
The first byte of each format specifies the format ID. The size of the format includes this first byte.
Important: When Package information is written to the OTP, bit 6 must be set to "1" in byte 0 of the OTP memory. This indicates to the FPC software that there is a Package section in the OTP memory.

6.1.1 Package Format ID 1

Size in bytes: 8
This format holds information about a SIP containing a sensor and a 2060 companion chip.
During SIP production, in addition to package related information, FPC2060 information is stored in the sensor OTP.

Section	Address	Content
Admin	Byte 0	**Layout format ID = 1**
FPC2060	Byte 1:5	LOT ID for TSMC, see chapter 1-4.
FPC2060	Byte 6	FPC2060 oscTrim (reserved for future usage) 4 bits 2-complementary (range -8 to 7)
Package	Byte 7	SIP package design version number (CPxx)

6.1.2 Package Format ID 2

Size in bytes: 3
This format is mainly used for FPC designed reference packages.

Section	Address	Content
Admin	Byte 0	**Layout format ID = 2**
Package	Byte 1, bit 7:1	Package vendor, see chapter 1-4
Package	Byte 1, bit 0	Package test result: 1 = Pass, 0 = Fail or Not tested
Package	Byte 2	FPC Package design version number (CPxx)

6.1.3 Package Format ID 3

Size in bytes: 5

Section	Address	Content
Admin	Byte 0	**Layout format ID = 3**
Package	Byte 1, bit 7:1	Package vendor, see chapter 1-4
Package	Byte 1, bit 0	Package test result: 1 = Pass, 0 = Fail or Not tested [1]
Package	Byte 2	FPC Package design version number (CPxx)
Package	Byte 3, bit 7:1	Year (binary, year 2000 = 0)
Package	Byte 3, bit 0	Month (most significant bit)
Package	Byte 4, bit 7:5	Month (3 least significant bits)
Package	Byte 4, bit 4:0	Day

1) Year, Month and Day is written first time the Package is tested regardless if test is "Pass" or not.
   0 = "Fail" if Year, Month and Day is written
   0 = "Not tested" if Year, Month and Day is not written

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6.1.4 Package Format ID 4

Size in bytes: 5
Format includes revision of Final Test program.

Section	Address	Content
Admin	Byte 0	**Layout format ID = 4**
Package	Byte 1, bit 7:4	Test program Major revision ID. Range 0-15
Package	Byte 1, bit 3:0	Test program Minor revision ID. Range 0-15
Package	Byte 2	Package design version number (CPxx)
Package	Byte 3, bit 7:1	Year (binary, year 2000 = 0)
Package	Byte 3, bit 0	Month (most significant bit)
Package	Byte 4, bit 7:5	Month (3 least significant bits)
Package	Byte 4, bit 4:0	Day

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7 OTP Module Memory Layout

This document defines the OTP memory layout of the Module section.

7.1 Module section revisions

This section of the OTP is used to store information about the module. For development and reference modules, more detailed information can be stored, e.g. coating type, revision of test equipment etc. The first byte of each format specifies the format ID. The size of the format includes this first byte.
Important: When Module information is written to the OTP, bit 7 must be set to "1" in byte 0 of the OTP memory. This indicates to the FPC software that there is a Module section in the OTP memory.

7.1.1 Module Format ID 1

Size in bytes: 5
This format is mainly intended for FPC designed reference modules.

Section	Address	Content
Admin	Byte 0	**Layout format ID = 1**
Module	Byte 1, bit 7:1	Module vendor, see chapter 4.3
Module	Byte 1, bit 0	Module test result: 1 = Pass, 0 = Fail or Not tested *1
Module	Byte 2, bit 7	Reserved for future usage
Module	Byte 2, bit 6:0	FPC Module design version number
Module	Byte 3, bit 7:1	Year (binary, year 2000 = 0)
Module	Byte 3, bit 0	Month (most significant bit)
Module	Byte 4, bit 7:5	Month (3 least significant bits)
Module	Byte 4, bit 4:0	Day

1) Year, Month and Day is written first time the Module is tested regardless if test is "Pass" or not.
   0 = "Fail" if Year, Month and Day is written
   0 = "Not tested" if Year, Month and Day is not written

7.1.2 Module Format ID 2

Size in bytes: 5

Section	Address	Content
Admin	Byte 0	**Layout format ID = 2**
Module	Byte 1, bit 7:1	Module vendor, see chapter 4.3
Module	Byte 1, bit 0	Module test result: 1 = Pass, 0 = Fail or Not tested *1
Module	Byte 2, bit 7:3	FPC Product variant (5-bit). See Appendix A
Module	Byte 2, bit 2:0	FPC Module design version number (3 most significant bits)
Module	Byte 3, bit 7:6	FPC Module design version number (2 least significant bits)
Module	Byte 3, bit 5	External sensor available: 1 = Available, 0 = Not available
Module	Byte 3, bit 4:1	Year (binary, year 2016 = 0) e.g. from year 2016 to 2031
Module	Byte 3, bit 0	Month (most significant bit)
Module	Byte 4, bit 7:5	Month (3 least significant bits)
Module	Byte 4, bit 4:0	Day

1) Year, Month and Day is written first time the Module is tested regardless if test is "Pass" or not.
   0 = "Fail" if Year, Month and Day is written
   0 = "Not tested" if Year, Month and Day is not written

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7.1.3 Module Format ID 3

Size in bytes: 7

Section	Address	Content
Admin	Byte 0	**Layout format ID = 3**
Module	Byte 1, bit 7:1	Module vendor, see chapter 4.3
Module	Byte 1, bit 0	Module test result: 1 = Pass, 0 = Fail or Not tested *2
Module	Byte 2, bit 7:4	FPC Product (4-bit). See tables in Appendix B
Module	Byte 2, bit 3:1	Coating type (3-bit). See table in Appendix C
Module	Byte 2, bit 0	Coating thickness in steps of 5um (7-bit) (most significant bit)
Module	Byte 3, bit 7:2	Coating thickness in steps of 5um (7-bit) (6 least significant bits)
Module	Byte 3, bit 1:0	Reserved for internal use
Module	Byte 4	Reserved for Sense Touch calibration data
Module	Byte 5, bit 7	Reserved for future use
Module	Byte 5, bit 6	Sidebuttons available: 1 = Available, 0 = Not available
Module	Byte 5, bit 5	External force sensor available: 1 = Available, 0 = Not available
Module	Byte 5, bit 4:1	Year (binary, year 2016 = 0) e.g. from year 2016 to 2031
Module	Byte 5, bit 0	Month (most significant bit)
Module	Byte 6, bit 7:5	Month (3 least significant bits)
Module	Byte 6, bit 4:0	Day

2) Year, Month and Day is written first time the Module is tested regardless if test is “Pass” or not.
0 = “Fail” if Year, Month and Day is written
0 = “Not tested” if Year, Month and Day is not written

Coating thickness is specified in steps of 5um:

Binary	Thickness
0000001	5um
0000010	10um
0000011	15um
…	
1111111	635um

7.1.4 Module Format ID X (Singen)

Size in bytes: 14

Section	Address	Content
Admin	Byte 0, bit 7:0	Format version. Set to X.
Module	Byte 1, bit 7:1	Module vendor, see chapter 4.3
Module	Byte 1, bit 0	Module test result: 1 = Pass, 0 = Fail or Not tested *1
Module	Byte 2, bit 7:0	LGA/SiP Batch, 5 first numbers, ASCII char, e.g. “27717” in “27717AA/57”. 1st number.
Module	Byte 3, bit 7:0	LGA/SiP Batch, 5 first numbers, ASCII char, e.g. “27717” in “27717AA/57”. 2nd number.
Module	Byte 4, bit 7:0	LGA/SiP Batch, 5 first numbers, ASCII char, e.g. “27717” in “27717AA/57”. 3rd number.
Module	Byte 5, bit 7:0	LGA/SiP Batch, 5 first numbers, ASCII char, e.g. “27717” in “27717AA/57”. 4th number.

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Module	Byte 6, bit 7:0	LGA/SiP Batch, 5 first numbers, ASCII char, e.g. “27717” in “27717AA/57”. 5ft number.
Module	Byte 7, bit 7:0	LGA/SiP Batch, 2 first letters, ASCII char, e.g. “AA” in “27717AA/57”. 1st letter.
Module	Byte 8, bit 7:0	LGA/SiP Batch, 2 first letters, ASCII char, e.g. “AA” in “27717AA/57”. 2nd letter.
Module	Byte 9, bit 7:0	LGA/SiP Batch, “/” letter, ASCII char, e.g. “AA” in “27717AA/57”.
Module	Byte 10, bit 7:0	LGA/SiP Batch, 2 last numbers, ASCII char, e.g. “57” in “27717AA/57”. 1st number.
Module	Byte 11, bit 7:0	LGA/SiP Batch, 2 last numbers, ASCII char, e.g. “57” in “27717AA/57”. 2nd number.
Module	Byte 12, bit 7:3	FPC Product variant (5-bit). See Appendix A
Module	Byte 12, bit 2:0	FPC Module design version number (3 most significant bits)
Module	Byte 13, bit 7:6	FPC Module design version number (2 least significant bits)
Module	Byte 13, bit 5	External sensor available: 1 = Available, 0 = Not available
Module	Byte 13, bit 4:1	Year (binary, year 2016 = 0) e.g. from year 2016 to 2031
Module	Byte 13, bit 0	Month (most significant bit)
Module	Byte 14, bit 7:5	Month (3 least significant bits)
Module	Byte 14, bit 4:0	Day

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Appendix A FPC Product Variants for Module Format ID 2

Table 1: Product variants for sensor HWID 0x0311, 0x0331, 0x0351

Binary	Variant
00001	FPC1262
00010	FPC1263
00011	FPC1264
00100	FPC1265
00101	FPC1261
00110	FPC1260

Table 2: Product variants for sensor HWID 0x0321, 0x0341

Note: FPC1268 is using Module Format ID = 1.

Binary	Variant
00001	FPC1266
00010	FPC1267
00110	FPC1260

Table 3: Product variants for sensor HWID 0x0B11, 0x0B21

Binary	Variant
00001	FPC1281-S
00010	FPC1281-G
00011	FPC1281-Z
00100	FPC1283

Table 4: Product variants for sensor HWID 0x0711, 0x0721

Binary	Variant
00001	FPC1075
00010	FPC1272-G
00011	FPC1272-Z

Table 5: Product variants for sensor HWID 0x0612, 0x0621

Binary	Variant
00001	FPC1028
00010	FPC1228-G
00011	FPC1228-Z
00100	FPC1229
00101	FPC1229-G175-SS (Single Supply)

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Appendix B FPC Products for Module Format ID 3

Previous curve products such as FPC1541-C & FPC1542-C share product ID 0001 with the flat products.
Product ID 0010 is added for the 1st curve product based on FPC1552 or new sensors.
Product ID 0011 is reserved for the 2nd curve product based on FPC1552 or new sensors.

Table 6: FPC products for HWID 0x0E11, 0x0E12, 0x0E22

Binary	Product
0001	FPC1291
0010	FPC1292
0011	FPC1293
0100	FPC1294

Table 7: FPC products for HWID 0x1011, 0x1021, 0x1012,0x1022,0x1013, 0x1023

Binary	Product
0001	FPC1511

Table 8: FPC products for HWID 0x1031

Binary	Product
0001	FPC1521

Table 9: FPC products for HWID 0x1811, 0x1821

Binary	Product
0001	FPC1541*

*FPC1541-S & FPC1541-C160 share product ID 0001.

Table 10: FPC products for HWID 0x1C12, 0x1C13,0x1F12

Binary	Product
0001	FPC1542*

*FPC1542-S & FPC1542-C160 share product ID 0001.

Table 11: FPC products for HWID 0x1E21,0x1E22

Binary	Product
0001	FPC1552*
0010	FPC1552-C170-R55**
0011	FPC1552-C170-R45***

*FPC1552-S & FPC1552-S160 share product ID 0001
**Product ID 0010 for Haiti, main radius 5.5mm
***Product ID 0011 for Haiti, main radius 4.5mm

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Appendix C Printable ASCII table

ASCII printable table, defined in ref[3].

Table 12: Printable ASCII table

Dec	Hex	Glyph
32	20	(space)
33	21	!
34	22	"
35	23	#
36	24	$
37	25	%
38	26	&
39	27	'
40	28	(
41	29	)
42	2A	*
43	2B	+
44	2C	,
45	2D	-
46	2E	.
47	2F	/
48	30	0
49	31	1
50	32	2
51	33	3
52	34	4
53	35	5
54	36	6
55	37	7
56	38	8
57	39	9
58	3A	:
59	3B	;
60	3C	<
61	3D	=
62	3E	>
63	3F	?

Dec	Hex	Glyph
64	40	@
65	41	A
66	42	B
67	43	C
68	44	D
69	45	E
70	46	F
71	47	G
72	48	H
73	49	I
74	4A	J
75	4B	K
76	4C	L
77	4D	M
78	4E	N
79	4F	O
80	50	P
81	51	Q
82	52	R
83	53	S
84	54	T
85	55	U
86	56	V
87	57	W
88	58	X
89	59	Y
90	5A	Z
91	5B	[
92	5C	\
93	5D	]
94	5E	^
95	5F	_

Dec	Hex	Glyph
96	60	`
97	61	a
98	62	b
99	63	c
100	64	d
101	65	e
102	66	f
103	67	g
104	68	h
105	69	i
106	6A	j
107	6B	k
108	6C	l
109	6D	m
110	6E	n
111	6F	o
112	70	p
113	71	q
114	72	r
115	73	s
116	74	t
117	75	u
118	76	v
119	77	w
120	78	x
121	79	y
122	7A	z
123	7B	{
124	7C	|
125	7D	}
126	7E	~

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