
VLSI LAB REPORT | 2024

# (CO3098) LSI logic design

## Floating-point ALU
## Synthesis and LEC report

**Submitted to: Mr. Huynh Phuc Nghi**

Submitted by: To Hoang Phong - 2112012
Vu Huynh Tan Phat - 2114391

Ho Chi Minh University of Technology (HCMUT)

The faculty of Computer Science and Engineering

| | |
|---|---|
| Author | Group 1 |
| Date | 2024/04/08 |
| Version | 1 |

# Contents

**1 Synthesis** **3**
1.1 Synthesis result: Area . . . . . 3
1.2 Synthesis result: qor . . . . . 4
1.3 Synthesis result: Time . . . . . 5
1.4 Schematic . . . . . 7

**2 LEC** **7**

# 1 Synthesis

Because FP_ALU is a combinational circuit, we need to insert registers (flip-flops) between input signals and logic gates, and create a clk signal. The following diagram will illustrate the synthesis circuit:

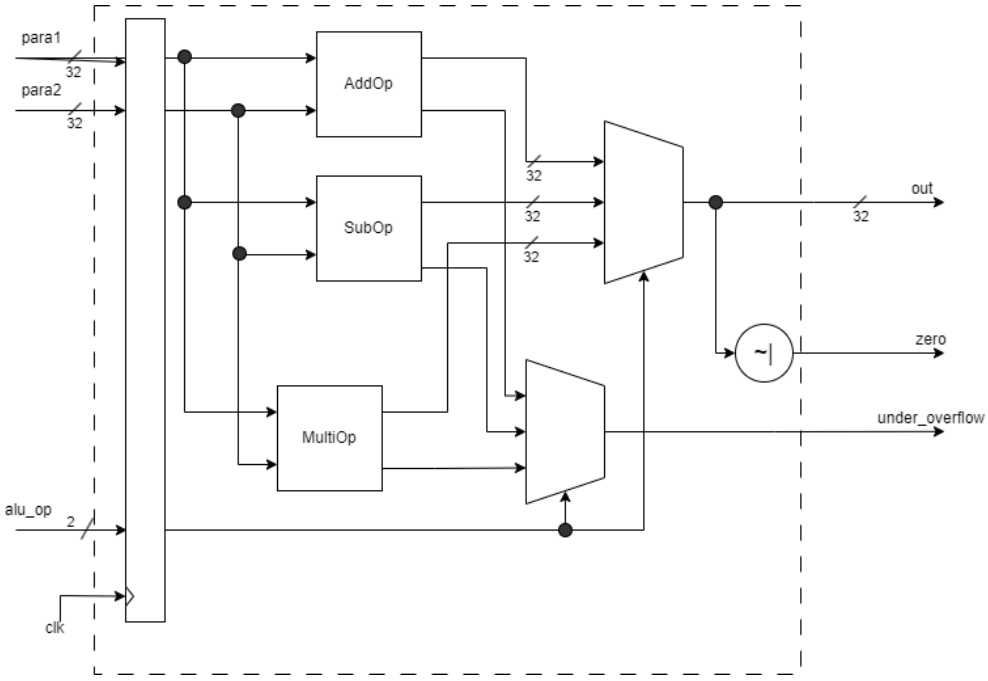


Figure 1: The synthesis circuit

## 1.1 Synthesis result: Area

```
[l01group3@ktmt LAB1]$ cat reports_Apr17-10\:06\:22/final_area.rpt
============================================================
  Generated by:           Genus(TM) Synthesis Solution 19.13-s073_1
  Generated on:           Apr 17 2024  10:09:46 am
  Module:                 FP_ALU_SYN
  Technology libraries:   slow_1v0
                          pll 0.0
                          CDK_S128x16 0.0
                          CDK_S256x16 0.0
                          CDK_R512x16 0.0
                          physical_cells
                          slow_1v0
                          pll 0.0
                          CDK_S128x16 0.0
                          CDK_S256x16 0.0
                          CDK_R512x16 0.0
                          physical_cells
  Operating conditions:   slow
  Interconnect mode:      global
  Area mode:              physical library
============================================================

  Instance  Module  Cell Count  Cell Area  Net Area   Total Area
------------------------------------------------------------------
FP_ALU_SYN              4647  13001.455  6040.296    19041.750
[l01group3@ktmt LAB1]$
```

Figure 2: The area for circuit

The cell area takes 13001.455$\mu m^2$ and the net area takes 6040.296$\mu m^2$. In total, this circuit area takes 19041.750$\mu m^2$. This is result after inserting registers (flip-flops) so the result of original circuit would be a little smaller.

### 1.2 Synthesis result: qor

```
================================================================

Timing
--------

Clock   Period
--------------
clk    15000.0


  Cost    Critical         Violating
 Group   Path Slack  TNS     Paths
-------------------------------------
clk            0.1   0.0         0
default    No paths   0.0
-------------------------------------
Total                0.0         0

Instance Count
--------------
Leaf Instance Count             3439
Physical Instance count            0
Sequential Instance Count        100
Combinational Instance Count    3339
Hierarchical Instance Count        0

Area
----
Cell Area                       8701.831
Physical Cell Area              0.000
Total Cell Area (Cell+Physical) 8701.831
Net Area                        4808.677
Total Area (Cell+Physical+Net)  13510.508

Runtime                         0.0 seconds
Elapsed Runtime                 270 seconds
Genus peak memory usage         1081.83
Innovus peak memory usage       no_value
Hostname                        localhost
```

Figure 3: Quality of Result

After many time synthesis, the clock 15ns will result in the most qualified result, which is 0.1ps critical path slack. The area also has changes. The cell area takes 8701.831$\mu m^2$ and the net area takes 4808.677$\mu m^2$. In total, this circuit area takes 13510.508$\mu m^2$.

### 1.3 Synthesis result: Time

There were 50 paths in general, so we only displayed 3 paths with the minimum slack. To read others, please click on this

```
Path 1: MET (0 ps) Late External Delay Assertion at pin zero
         Group: clk
    Startpoint: (R) para2_ff_reg[7]/CK
         Clock: (R) clk
      Endpoint: (R) zero
         Clock: (R) clk

                  Capture       Launch
     Clock Edge:+   15000            0
      Src Latency:+     0            0
      Net Latency:+     0 (I)        0 (I)
          Arrival:=   15000            0

     Output Delay:-    7500
    Required Time:=    7500
     Launch Clock:-       0
        Data Path:-    7500
            Slack:=       0

Exceptions/Constraints:
  output_delay            7500           bound_flasher_gate.s_line_10

#-------------------------------------------------------------------------------------------------------------
#             Timing Point               Flags    Arc    Edge    Cell      Fanout Load Trans Delay Arrival Instance
#                                                                            (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------
  para2_ff_reg[7]/CK                     -       -      R     (arrival)      66    -     0     -       0    (-,-)
  para2_ff_reg[7]/Q                      -       CK->Q  R     DFFHQX8         7 35.0    83   268     268    (-,-)
  g18089/Y                               -       A->Y   F     CLKINVX4        1  6.9    45    52     321    (-,-)
  g17976__5115/Y                         -       B->Y   R     NOR2X4          2 11.7   113    73     394    (-,-)
  g35750/Y                               -       A1N->Y R     AOI2BB1X4       1  9.9   106   149     544    (-,-)
  g17851__5115/Y                         -       A->Y   F     NAND2X8         2 11.1    80    85     629    (-,-)
  g18692/Y                               -       A->Y   R     INVX3           1  6.9    49    52     681    (-,-)
  g17838__5526/Y                         -       B->Y   F     NOR2X4          1 10.2    64    49     730    (-,-)
  g17831__6417/Y                         -       B->Y   R     NOR3X8          1  8.5   108    89     819    (-,-)
  g17827__2346/Y                         -       A->Y   F     NOR2X6          1 10.0    57    68     888    (-,-)
  g17826__2883/Y                         -       B->Y   R     NOR2X8          2 25.3   125    81     969    (-,-)
  g17823/Y                               -       A->Y   F     CLKINVX12       3 28.0    64    73    1042    (-,-)
  g17822/Y                               -       A->Y   R     CLKINVX20       9 47.2    50    47    1089    (-,-)
  g17813/Y                               -       A->Y   F     CLKINVX12      10 40.2    68    55    1143    (-,-)
  g18381__1705/Y                         -       B->Y   R     NOR2BX2         1  6.8   129    88    1232    (-,-)
  g35742/Y                               -       B0->Y  F     AOI21X4         3 10.7   129    79    1311    (-,-)
```

Figure 4: Time path from para2_ff_reg[7] to zero

Description: We have slack = 0, which means that the design is critically working at the desired frequency in this path.

```
  g31832__5107/Y                          -       B->Y   F     NAND2X6        2  8.7    84    76    7172    (-,-)
  g31810__3680/Y                          -       B->Y   R     NOR2X4         1  8.4    92    74    7245    (-,-)
  g31807__5526/Y                          -       B->Y   F     NAND2X6        1  8.5    82    75    7320    (-,-)
  g31801__5477/Y                          -       B->Y   R     NOR2X6         1  8.4    72    63    7383    (-,-)
  g31795__2883/Y                          -       B->Y   F     NAND2X6        1  6.9    72    64    7447    (-,-)
  g31794__9945/Y                          -       B->Y   R     NOR2X4         1  3.9    58    53    7500    (-,-)
  zero                                    -       -      R     (port)         -    -     -     0     7500    (-,-)
#-------------------------------------------------------------------------------------------------------------------



Path 2: MET (108 ps) Late External Delay Assertion at pin out[14]
         Group: clk
    Startpoint: (R) para2_ff_reg[7]/CK
         Clock: (R) clk
      Endpoint: (R) out[14]
         Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   15000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   15000            0

     Output Delay:-    7500
    Required Time:=    7500
     Launch Clock:-       0
        Data Path:-    7392
            Slack:=     108

Exceptions/Constraints:
  output_delay             7500           bound_flasher_gate.s_line_8_80_1

#-------------------------------------------------------------------------------------------------------------------
```

Figure 5: Time path from para2_ff_reg[7] to out[14]

Description: We have slack $= 108 > 0$, which means that the design is meeting the timing and still it can be improved in this path.

```
  g36625/Y                                -       B->Y   F     NOR2X1         1  4.8   111   131    6888    (-,-)
  g36579/Y                                -       AN->Y  F     NOR3BX4        1  7.1    76   132    7020    (-,-)
  g31955__35354/Y                         -       A0->Y  R     OAI21X4        1  5.4   119    78    7098    (-,-)
  g31930__9315/Y                          -       B->Y   F     NAND2X2        1  6.2   139   111    7209    (-,-)
  g31882__2802/Y                          -       A->Y   F     CLKAND2X6      2 12.5    55   128    7338    (-,-)
  g34614/Y                                -       A->Y   R     INVX1          1  3.9    68    55    7392    (-,-)
  out[14]                                 -       -      R     (port)         -    -     -     0     7392    (-,-)
#-------------------------------------------------------------------------------------------------------------------



Path 3: MET (111 ps) Late External Delay Assertion at pin out[13]
         Group: clk
    Startpoint: (R) para2_ff_reg[7]/CK
         Clock: (R) clk
      Endpoint: (R) out[13]
         Clock: (R) clk

                    Capture       Launch
       Clock Edge:+   15000            0
      Src Latency:+       0            0
      Net Latency:+       0 (I)        0 (I)
          Arrival:=   15000            0

     Output Delay:-    7500
    Required Time:=    7500
     Launch Clock:-       0
        Data Path:-    7389
            Slack:=     111

Exceptions/Constraints:
  output_delay             7500           bound_flasher_gate.s_line_8_81_1

#-------------------------------------------------------------------------------------------------------------------
#              Timing Point                Flags    Arc    Edge    Cell      Fanout Load Trans Delay Arrival Instance
#                                                                              (fF)  (ps)  (ps)   (ps)  Location
#-------------------------------------------------------------------------------------------------------------------
  para2_ff_reg[7]/CK                      -       -      R     (arrival)      66    -     0     -       0    (-,-)
  para2_ff_reg[7]/Q                       -       CK->Q  R     DFFHQX8         7 35.0    83   268     268    (-,-)
  g18089/Y                                -       A->Y   F     CLKINVX4        1  6.9    45    52     321    (-,-)
  g17976__5115/Y                          -       B->Y   R     NOR2X4          2 11.7   113    73     394    (-,-)
```

Figure 6: Time path from para2_ff_reg[7] to out[14]

Description: We have slack $= 111 > 0$, which means that the design is meeting the timing and still it can be improved in this path.

### 1.4 Schematic

## 2 LEC

In designs to be compared, first the key points are identified. The key points are the points whose value will be compared in the LEC mode to determine the equivalency. These may include the input and output ports of modules. Once key points are identified, mapping is done between the designs so that the corresponding points get mapped. Those which get mapped are the mapped points

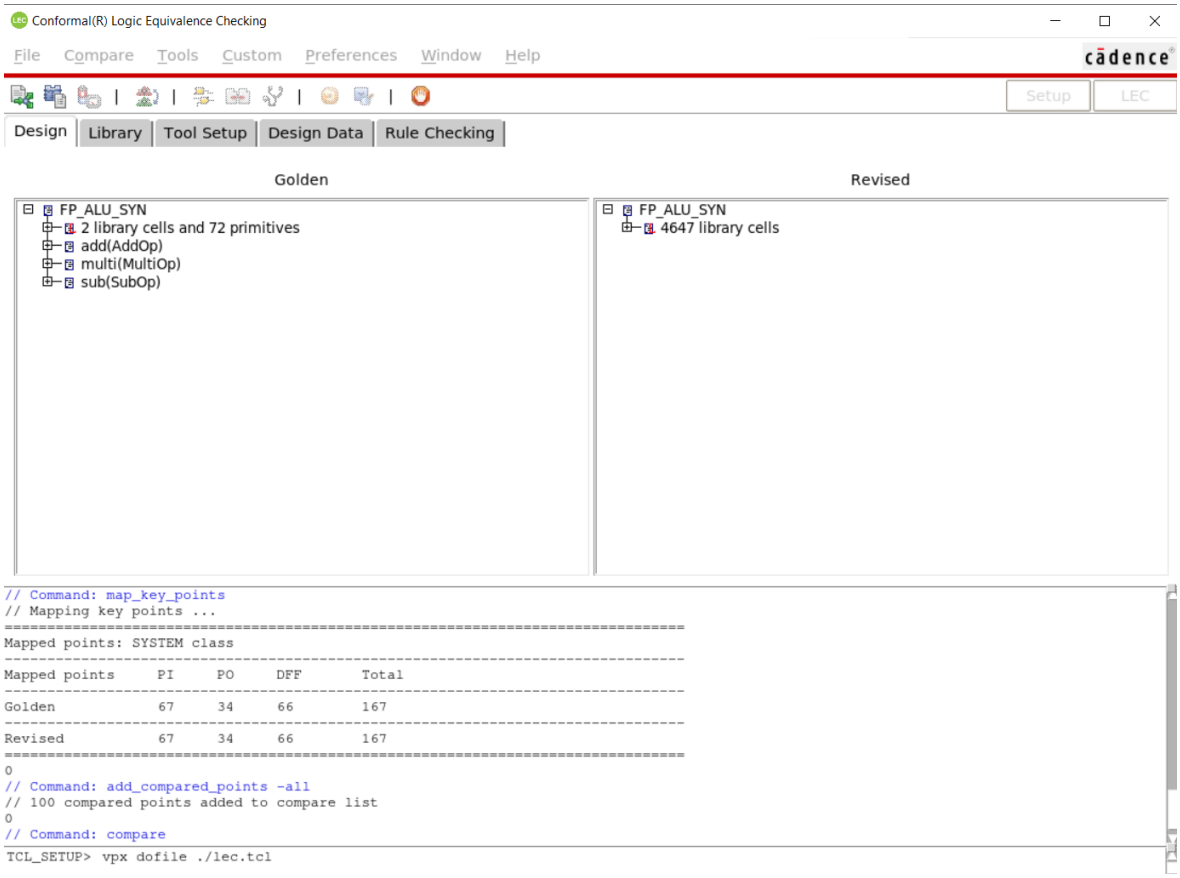


Figure 7: Logic Equivalence checking of the circuit

Description: There was no non-equivalent point after LEC. All the key points of golden and revised design have been compared and there was no unmapped point after this process.