VLSI LAB REPORT | 2024

(CO3098) LSI logic design

Floating-point ALU
Layout report

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1 Cell-based method P&R

In this project, we use the cell-based method P&R (placement and routing). It means we will ultilize CMOS to layout basic logic gates (inverter, nand, nor, etc) and then create more complex gates (full adder, half adder, mux, etc) based on truth table, formula, and basic gates.

Library preparation for layout

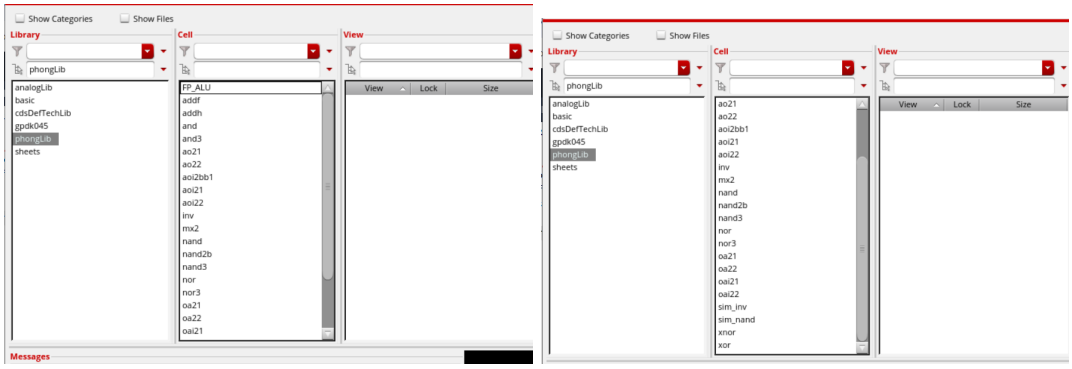

Figure 1: Library

The above figure shows all cells we made during the project, from CMOS-based gates (inv, nand, etc) to complex gates (addf, addh, mx2, aoi22, etc), and FP_ALU contains layout files of this project. Because of the time limitation, we just simulated inverter and nand gate.

Layout, DRC, LVS and simulation result of nand gate

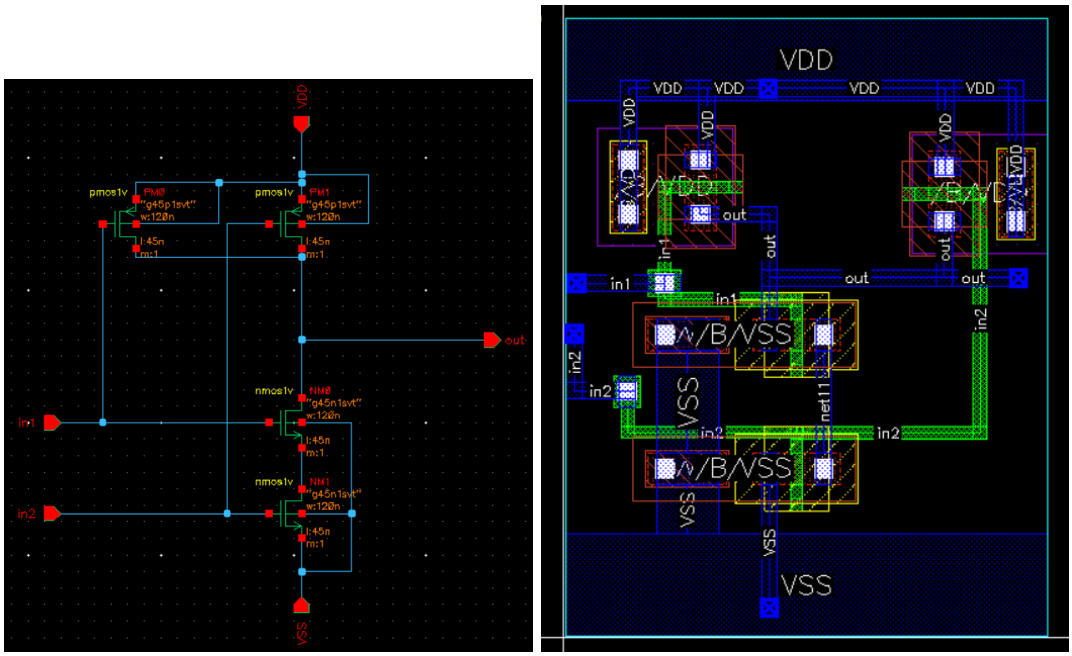

Figure 2: NAND schematic and layout

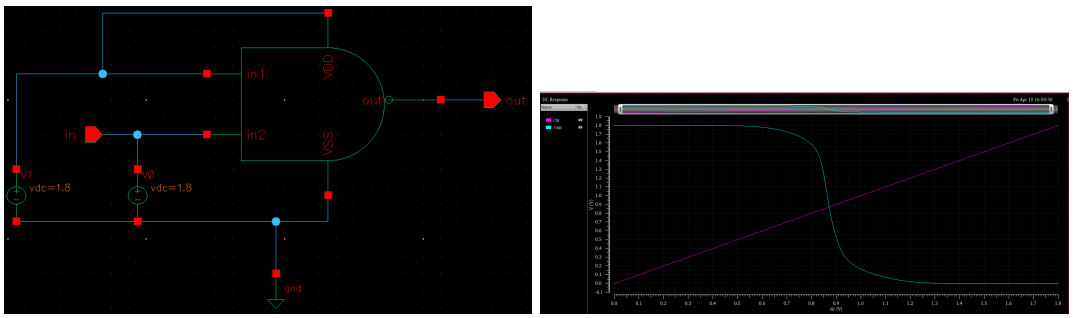

Figure 3: NAND simulation schematic and plot

Note: To facilitate the simulation process, we set an input pin to VDD (1 in logic) and another pin to a linear source. We also used two probes, one for input and one for output to observe changes of them.

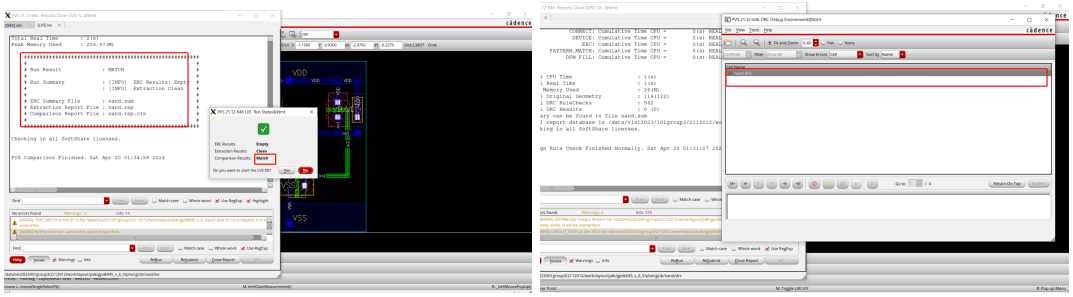

Figure 4: NAND lvs and drc check

Note: There was no error in lvs and drc check.

The similar method was used in other gates, except for simulation steps

2 Result

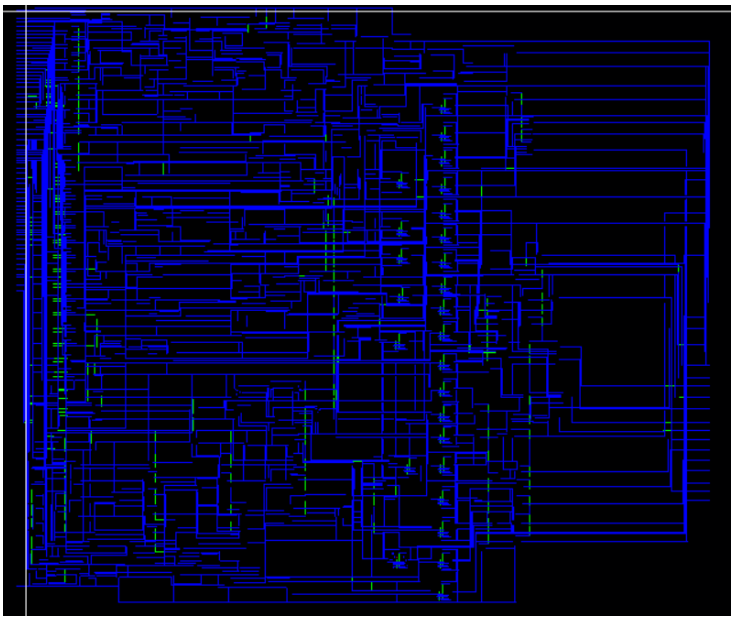

Figure 5: FP_ALU layout

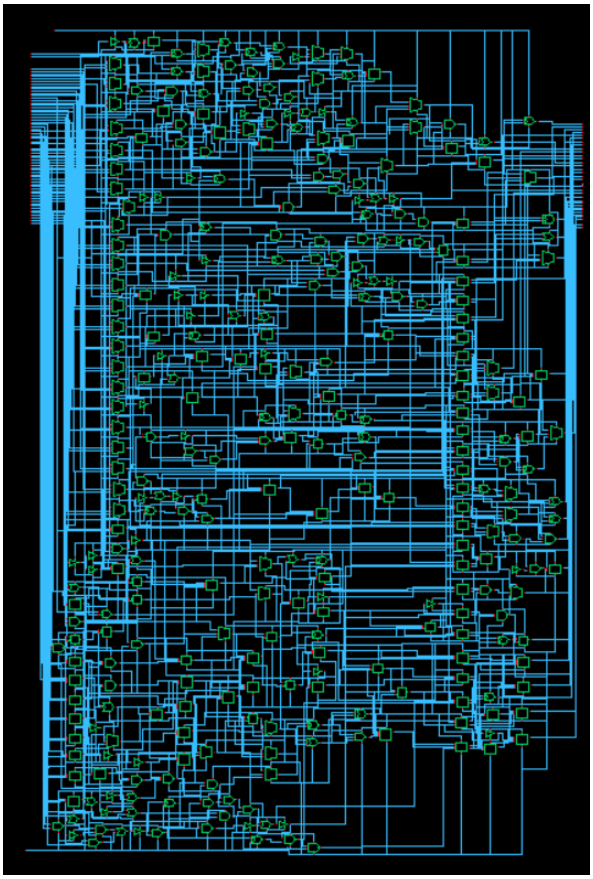

Figure 6: FP_ALU schematic

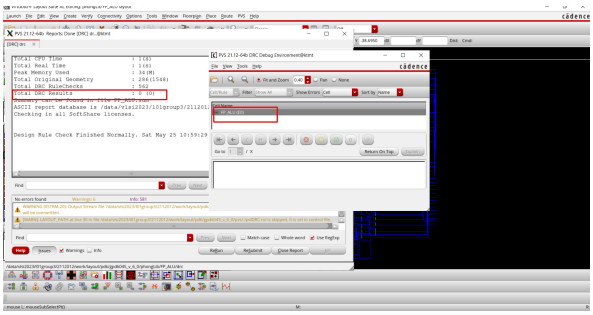

Figure 7: FP_ALU drc

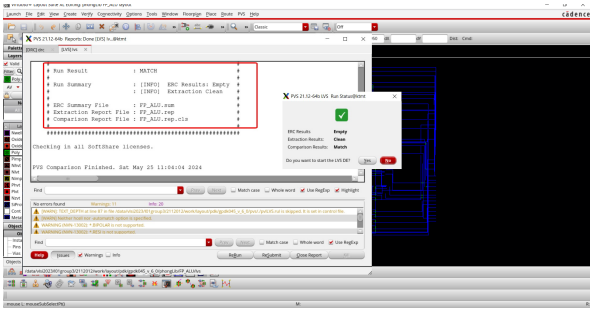

Figure 8: FP_ALU lvs

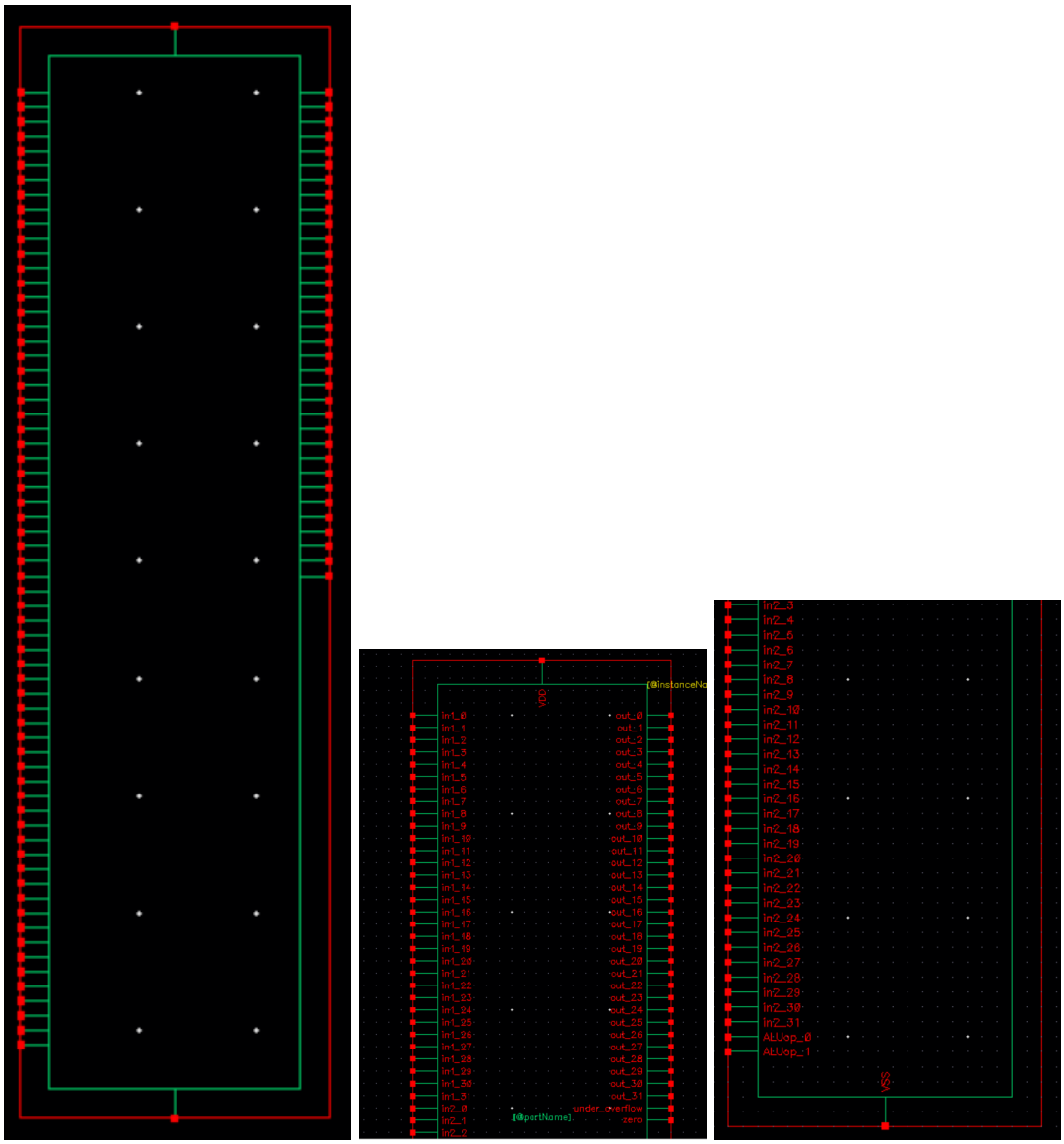

Figure 9: FP_ALU symbol