Volume-1 Chapter-1 (Old Question)

October 2024

1. **Q1.** *P*, *Q*, and *R* are propositions. It is known that the truth value of proposition *P* is true, and the values of both the propositions "(not *P*) or *Q*" and "(not *Q*) or *R*" are true. Which of the following is a combination of the truth values of *Q* and *R*? Here, *X* or *Y* represents the logical sum of *X* and *Y*, and not *X* represents the negation of *X*.

	Q	*R*
a)	False	False
b)	False	True
c)	True	False
d)	True	True

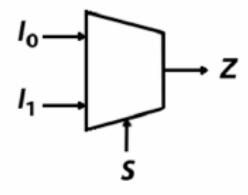
2. Q9. When the CPU needs data, it first accesses the cache memory. When the data is not available in the cache memory, the CPU accesses the main memory. If the miss ratio is 0.2 and the access times for cache memory and main memory are as shown below, what is the approximate average memory access time in ns for the CPU? Here, there are only cache memory and main memory for the CPU, the access time for main memory includes the time to confirm whether the data is available in cache memory, and the overhead time for the cache management can be ignored.

Access destination	Access time (ns)
Cache Memory	75
Main Memory	1500

a) 315 b) 360 c) 1,215 d) 1,260

3. **Q10.** Which of the following is the appropriate purpose of defragmentation of hard disks?
a) To access disk files faster and more efficiently
b) To clean up temporary and junk files
c) To delete IBG (interblock gap) and increase capacity
d) To protect disk drives from physical failures

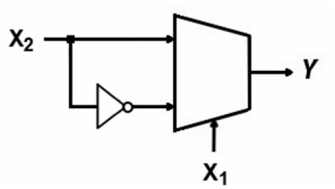
4. Q16. A graphical symbol for the 2-to-1 MUX (multiplexer) and its truth table are shown in the figure below. The MUX has two data inputs (I0, I1), one select-line (S) and one output (Z). If the select line is S=0, then the output Z is switched to input I_0, whereas if a select line is S=1, then the output Z is switched to input I_1.

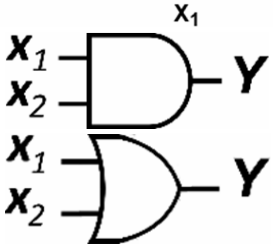


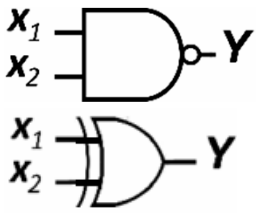
S	Z
0	I_0
1	I_1

Truth Table

Which of the following is a logic gate that is equivalent to the circuit implemented with the 2-to-1 MUX below?



a) 

b) 

c)

d)

5. Q17. Audio signals are recorded using 8-bit samples at a sampling rate of 11,000 times per second. When a flash memory of 512 × 106 bytes is used, what is the maximum recording time of such data in minutes?
a) 77 b) 96 c) 775 d) 969

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1. **Q1.** What is the decimal representation of the hexadecimal number 123.4?
a) 83.25 b) 83.5 c) 291.25 d) 291.5

2. **Q2.** Five people are sitting at a table in a restaurant. Two of them ordered coffee, and the other three ordered tea. The waiter forgets who ordered what and puts the drinks in a random order for the five persons. What is the probability that every person gets the correct drink?
a) 1/30 b) 1/20 c) 1/10 d) 3/10

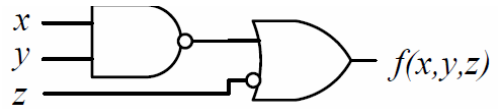
3. **Q9.** When an HDD has the specifications below, what is the average access time for an HDD to transfer 1 MB of data in ms? Here, the average access time can be calculated as the sum of the average seek time, controller overhead, rotational latency, and transfer time. Other overheads can be ignored.

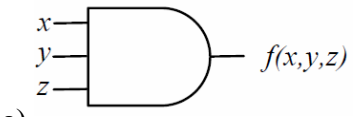
Average seek time	4 ms
Controller overhead	1.25 ms
Rotation speed	5,000 rpm
Transfer rate	60 MB/s

a) 21.93 b) 26.67 c) 27.92 d) 33.92

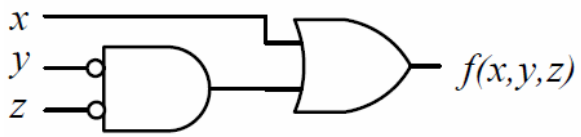
4. **Q10.** Which of the following is the port that can theoretically connect up to 127 peripheral devices, controlled by a PC?
a) Displayport b) HDMI c) SATA d) USB

5. Q16. Which of the following is equivalent to the circuit below?





a)



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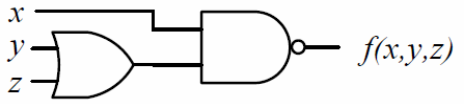
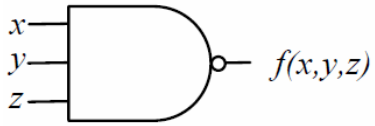


c)



d)

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6. **Q2.** *n* is a binary integer represented in two's complement. Which of the following operations get the value 7 × *n* using only bit shifting and an addition or subtraction operation?
a) Shift *n* 2 bits to the left, then add *n* to the result.
b) Shift *n* 2 bits to the left, then subtract *n* from the result.
c) Shift *n* 3 bits to the left, then add *n* to the result.
d) Shift *n* 3 bits to the left, then subtract *n* from the result.

7. **Q3.** A parking lot has 10 parking spaces in a row, and 7 cars are parked at random parking spaces. What is the probability that the three empty places are adjacent to each other?
a) 1/90 b) 1/72 c) 1/15 d) 1/12

3. Q4. What is the sum of two binary fractions 1.0101 and 1.0111 expressed in decimal form?
a) 2.5 b) 2.75 c) 2.875 d) 2.9375

4. Q11. In a CPU, which of the following is a special register that contains *the address of the next instruction* to be fetched?
a) Accumulator b) Index register
c) Instruction register d) Program counter

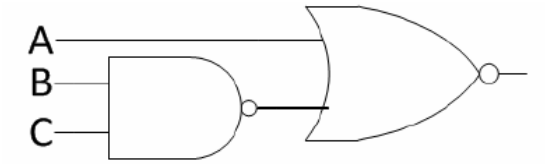
5. Q12. Which of the following is an appropriate CPU operation associated with cache memory?
a) When a cache hit occurs, the CPU fetches data from ROM.
b) When a cache hit occurs, the CPU fetches data from the main memory.
c) When a cache miss occurs, the CPU fetches data from the cache memory.
d) When a cache miss occurs, the CPU fetches data from the main memory.

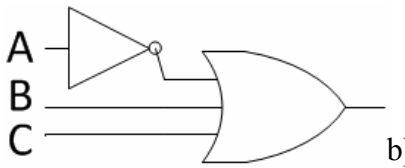
6. Q13. Which of the following is a computer architecture in which a processor executes the *same instruction on multiple data*?
a) MIMD b) MISD c) SIMD d) SISD

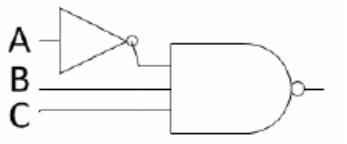
7. Q20. Which of the following is a sequential circuit that has *two stable states*?
a) Adder circuit b) Capacitor

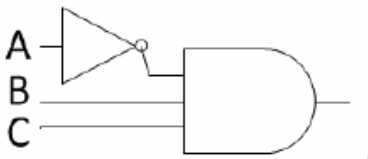
c) Flip-flop d) NAND gate

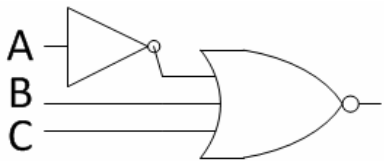
8. Q21. Which of the following is equivalent to the logic circuit shown below?



a) 

b) 

c) 

d) 

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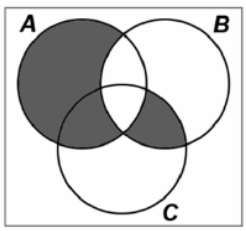
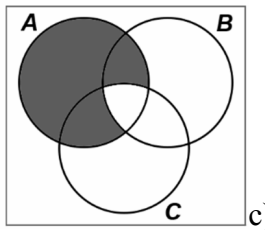
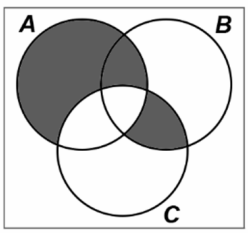
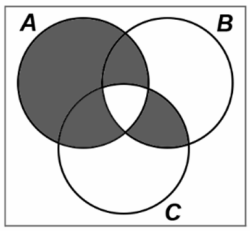
9. **Q1.** Which of the following is a Venn diagram that represents the set below?

$$(A \cap \bar{C}) \cup (A \cap \bar{B} \cap C) \cup (\bar{A} \cap B \cap C)$$

a) 

b) 

c) 

d) 

10. Q2. When the hexadecimal value ABCD in a 32-bit register is logically shifted right by two bits, which of the following is the resulting value in hexadecimal?
a) 2AF3 b) 6AF3 c) AF34 d) EAF3

11. **Q3.** What is the probability that at least three coins land heads up when four unbiased coins are tossed simultaneously?
a) 1/4 b) 5/16 c) 3/8 d) 5/8

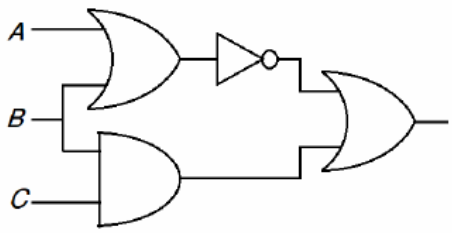
12. **Q4.** Random(*n*) is a function that returns an integer of 0 or more and less than *n* with a uniform probability. When the series of procedures below is run on the integer type variables *A*, *B*, and *C*, what is the probability that the value of *C* will be 0?
A = Random(10)
B = Random(10)
C = *A*−*B*
a) 1/100 b) 1/20 c) 1/10 d) 1/5

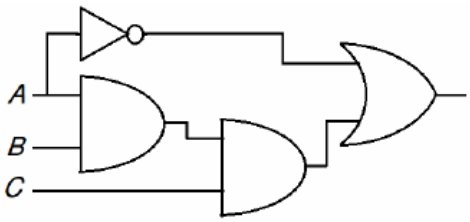
13. Q12. Which of the following is classified as an internal interrupt?
a) Interrupt caused by an abnormal power condition, such as a momentary loss of commercial power supply
b) Interrupt caused by performing a divide-by-zero operation
c) Interrupt caused by the completion of input or output
d) Interrupt caused by the occurrence of a memory parity error

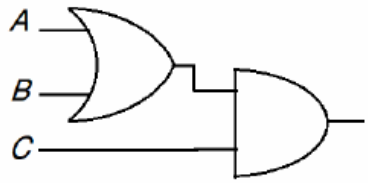
14. Q13. Which of the following is the technique that minimizes the number of write operations to the main memory by updating the data only in the cache memory and updating into the main memory later?
a) Overlay b) Write back c) Write protected d) Write through

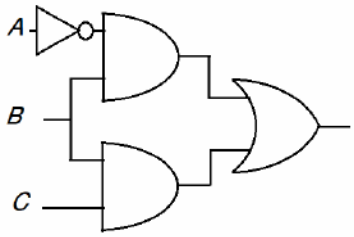
15. **Q14.** Which of the following is an appropriate description of a 3D printer's function?
a) It detects the shape of three-dimensional objects and produces output of 3D data.
b) It functions by pushing the pins of a high temperature printing head onto heat-sensitive paper.
c) It makes three-dimensional objects using methods such as fused filament fabrication.
d) It projects computer graphics onto uneven three-dimensional objects such as buildings and furniture.

16. Q20.
20. Which of the following is the logic circuit that is equivalent to the logical expression $\bar{A}BC + AC$?

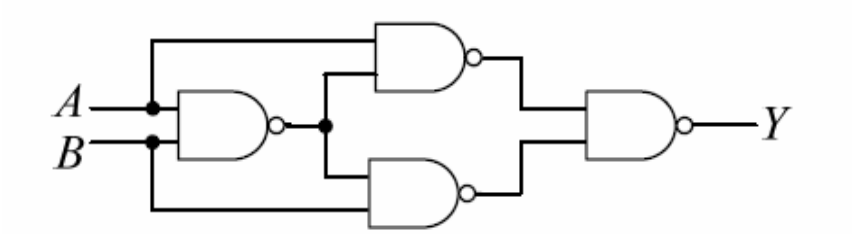
a)


b)


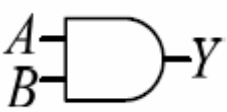
c)


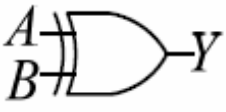
d)


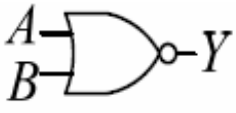
17. Q21. Which of the following is the logic gate that is equivalent to the logic circuit shown below?



a) 

b) 

c) 

d) 

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18. Q1. For an 8-bit binary integer, which of the following sets the least significant bit to 1 while leaving the other bits unchanged?
a) Perform bitwise AND operation with 00000001.
b) Perform bitwise NAND operation with 11111110.
c) Perform bitwise OR operation with 00000001.
d) Perform bitwise XOR operation with 00000001.

19. **Q2.** Which of the following is an appropriate explanation of the loss of significance?
a) It occurs when the result of an operation exceeds the maximum handle limit and raises an exception.
b) It occurs when two nearly equal floating-point numbers are subtracted to produce a result of unacceptably reduced significant digits.
c) It refers to a rounding error that occurs when the part smaller than the least significant digit of the result is rounded off, up, or down in floating-point operations.
d) It refers to the case when two floating-point numbers are added, but the less significant digits of either one do not affect the result.

20. **Q3.** When two dice are rolled, what is the probability that the sum of the dice is 5? Here, the two dice are fair and independent.
a) 1/18 b) 1/12 c) 1/9 d) 1/6

21. **Q6.** There are three (3) blue balls and four (4) green balls in a box. When two balls are randomly taken out from the box, what is the probability that both are blue?
a) 2/49 b) 1/15 c) 1/7 d) 9/49

22. **Q11.** There is a 32-bit microprocessor with 32-bit external data bus, driven by 64 MHz input clock, and the processor takes 8 input clock cycles to complete 1 bus cycle. What is the theoretical maximum data transfer rate in megabytes per second (MB/s) for the external data bus of the processor?
a) 3 b) 32 c) 256 d) 320

23. Q12. There is a computer that has an average instruction execution time of 20 nanoseconds. What is the performance of this computer in MIPS?

a) 5 b) 10 c) 20 d) 50

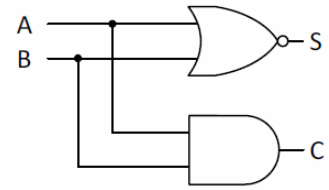
24. Q13. There is a disk drive that has a capacity of 8 GB. The drive has five (5) platters with two (2) surfaces: 10,000 tracks per surface and 200 sectors per track. How many bytes are in each sector? Here, 1 GB is 1,000,000,000 bytes.
a) 100 b) 200 c) 400 d) 800

25. Q14. Which of the following is a memory device that stores programs or data in factories and only has the read operation for the stored programs or data?
a) DRAM b) Flash memory c) Mask ROM d) SRAM

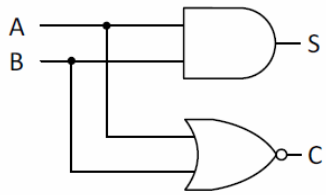
26. Q20. A half adder is a logic circuit that performs the addition of two single-bit binary numbers and outputs the sum and carry. The truth table of a half adder is shown in the table below. Which of the following is an appropriate logic diagram of the half adder?

Inputs		Outputs	
A	B	C (Carry)	S (Sum)
0	0	0	0
0	1	0	1
1	0	0	1
1	1	1	0

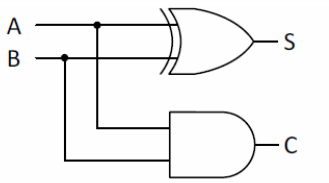
a)



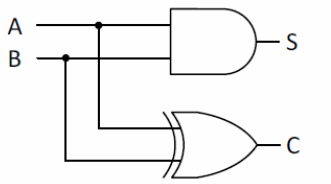
b)



c)



d)



27. Q22. Which of the following uses a flip-flop circuit in a memory cell?
a) DRAM b) EEPROM c) SDRAM d) SRAM

28. Q23. For a given decimal data, the check digit is calculated with the method below and is appended to the original data. When the given data is 7394, what is the result? Here, the weight is 1234 and the base number is 11.
(1) For each digit of the data, calculate the product with the digit at the same radix of the weight and calculate the sum of these products.
(2) Calculate the remainder after the division of the sum by the base number.
(3) Subtract the remainder from the base number and let the last digit of the result be the check digit.
a) 73940 b) 73941 c) 73944 d) 73947

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29. a

Q1. For logical variables A and B, which of the following is equivalent to the NOR operation on A and B? Here, $A + B$, $A \cdot B$, and $\bar{A}$ are OR, AND, and NOT operations on the corresponding variables, respectively.

a) $\bar{A} \cdot (A + \bar{B})$ b) $\bar{A} \cdot (\bar{A} + \bar{B})$ c) $B \cdot (A + \bar{B})$ d) $\bar{B} \cdot (\bar{A} + \bar{B})$

30. Q2. For non-negative integer A, which of the following has the same value as (A mod 32) + 64? Here, mod, +, AND, and OR are remainder-after-division, arithmetic addition, bitwise-AND, and bitwise-OR operators, respectively.
a) (A AND 31) OR 64 b) (A AND 32) OR 32
c) (A OR 31) AND 64 d) (A OR 64) AND 32

31. Q11. Which of the following is the average cycles per instruction (CPI) of a computer that can execute 1 billion instructions per second at a clock rate of 2.4 GHz?
a) 0.04 b) 0.12 c) 2.4 d) 25

32. Q12. What is the approximate average access time in milliseconds (ms) of a magnetic disk with the specifications shown in the table below? Approximate average access time is the sum of average seek time, track-to-track seek time, and average rotational delay. Here, the controller overhead can be ignored.

Average seek time	7.5 ms
Track to track seek time	1.2 ms
Rotational speed	7,200 rpm

a) 11.67 b) 12.87 c) 15.83 d) 25.

33. Q13. Which of the following is the list that contains A through D sorted starting with the shortest effective access time of the main memory?

	Cache memory			Main memory
	Does the system have cache memory? (yes/no)	Access time (nanoseconds)	Hit rate (%)	Access time (nanoseconds)
A	No	-	-	15
B	No	-	-	30
C	Yes	20	60	70
D	Yes	10	90	80

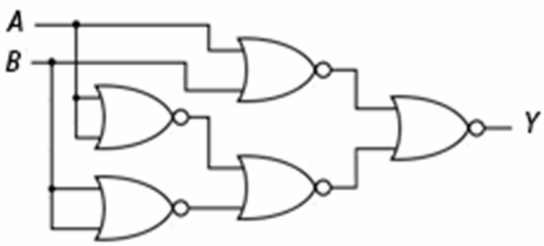
a) *A*, *B*, *C*, *D* b) *A*, *D*, *B*, *C*
c) *C*, *D*, *A*, *B* d) *D*, *C*, *A*, *B*

34. Q14. A 12-point character is to be displayed on a 96-dpi display in bitmap. How many dots is the height of a square font? Here, 1 point is 1/72 inch.

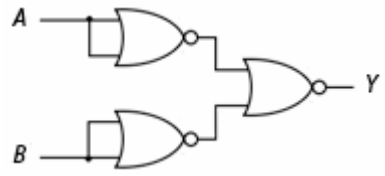
a) 8 b) 9 c) 12 d) 16

35. Q21. Which of the following is the Exclusive-NOR logic function that is implemented with two-input NOR gates? d

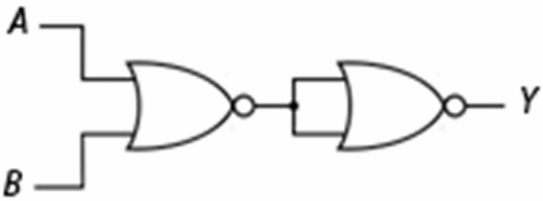
a)



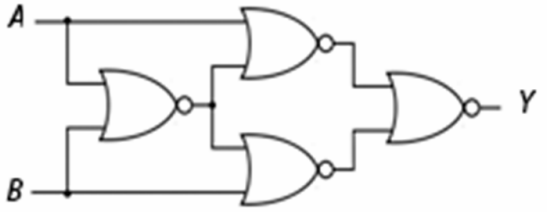
b)



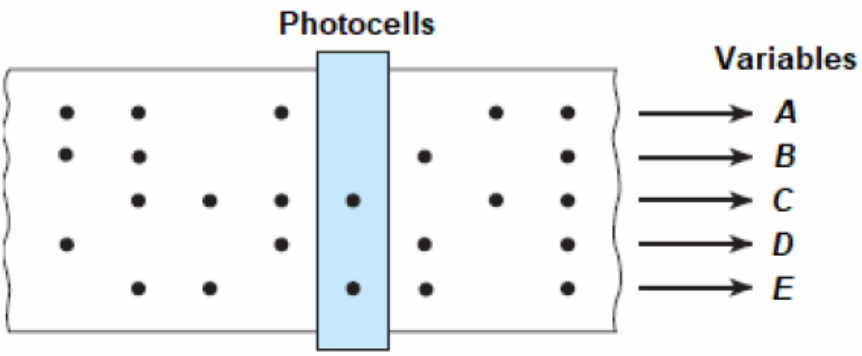
c)



d)



36. Q22. A paper tape reader used as a computer input device reads a tape with five rows of holes as shown below. A hole punched in the tape indicates logic 1, and no hole indicates logic 0. As each hole pattern passes under the photocells, the pattern is translated into logic signals as a variable: A, B, C, D, or E. A valid pattern on the tape has at least one hole, and an invalid pattern has no hole or all five holes punched. Which of the following is a logical expression that has logic 1 when a valid pattern is being read and logic 0 when an invalid pattern is being read? Here, + represents logical OR, · represents logical AND, and $\overline{A}$ represents the negation of A in the logic expression. In the figure, • represents a punched hole on the tape. d



a) $(\overline{A \cdot B \cdot C \cdot D \cdot E}) + (A \cdot B \cdot C \cdot D \cdot E)$

b) $(A + B + C + D + E) \cdot (\bar{A} + \bar{B} + \bar{C} + \bar{D} + E)$

c) $(\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E}) + (\overline{A + B + C + D + E})$

d) $\overline{(A \cdot B \cdot C \cdot D \cdot E) + (\bar{A} \cdot \bar{B} \cdot \bar{C} \cdot \bar{D} \cdot \bar{E})}$

Q2 2021

37. **Q1.** Which of the following is equivalent to the logic expression below? b

$(x + y) \cdot (x + z)$

Here, the letters are logic variables; $x + y$, $x \cdot y$, and $\bar{x}$ are OR, AND, and NOT operations on the corresponding variables, respectively.

a) $x \cdot (y + z)$ b) $x + y \cdot z$

c) $x \cdot y + y \cdot z$ d) $(\bar{x} + y) \cdot z$

38. Q2. Which of the following is a decimal that is represented as a finite digit octal fraction?
a) 0.3 b) 0.4 c) 0.5 d) 0.8

39. Q11. Which of the following is a special register that contains the address of the next instruction to be fetched?
a) Accumulator b) Program Counter (PC)
c) Stack Pointer d) Timer

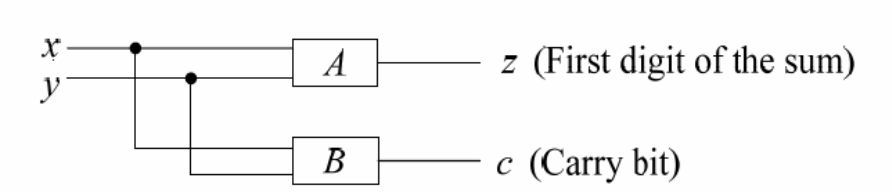
40. Q12. Which of the following is the performance of a CPU in MIPS when the instruction mix of the CPU is as listed in the table below? Here, the CPU does not use a pipeline architecture.

Instruction type	Instruction execution time in μs	Appearance ratio
Register to register operation	0.1	40%
Register from memory operation	0.3	50%
Unconditional branch operation	0.6	10%

a) 0.04 b) 0.25 c) 4 d) 25

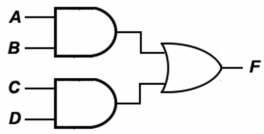
41. Q14. Which of the following is an appropriate description of USB 3.0?
a) It is a serial interface that adopts isochronous transmission that is suitable for audio or video, and has a broadcast transmission mode.
b) It is a serial interface that has a data transmission mode of 5 Gbit/s that is called super speed.
c) It is a serialized ATA specification that connects a PC to a peripheral device.
d) It is an interface that uses four (4) pairs of signal lines transmitting two (2) bits of information in one (1) clock and has a maximum throughput of 1 Gbit/s.

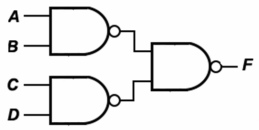
42. Q21. The half adder in the diagram below adds two (2) single-digit binary numbers, x and y, and produces z (the first digit of the sum) and c (the carry bit) as outputs. Which of the following is the appropriate combination of gate devices A and B? a

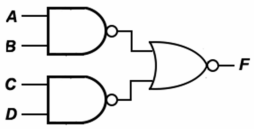


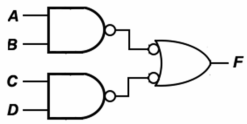
	A	B
a)	Exclusive logical sum (XOR)	Logical product (AND)
b)	Logical product (AND)	Logical sum (OR)
c)	Negative logical product (NAND)	Negative logical sum (NOR)
d)	Negative logical sum (NOR)	Exclusive logical sum (XOR)

43. Q22. Which of the following is not an implementation of the function F = A •B + C•D? Here, "•" represents the logic AND operation, and "+" represents the logic OR operation in the expression.

a) 

b) 

c) 

d) 

October / November 2021

44. Q1. What is the octal equivalent value of the hexadecimal number 7B5?
a) 735 b) 3665 c) 7551 d) 7561

45. Q2. For a non-negative integer x, which of the following gives the remainder after division of x by 8 as a result?
a) Performing a bitwise AND operation on x and 7
b) Performing a bitwise AND operation on x and 248
c) Performing a bitwise OR operation on x and 8
d) Performing a bitwise OR operation on x and 15

46. Q3. For three sets A, B and C, which of the following equalities holds? Here, U and ∩ are the union and intersection symbols, respectively.

a) (AUB) ∩ (A∩C) = B∩ (AUC)
b) (AUB) ∩ C = (AUC) ∩ (BUC)
c) (A ∩ C) U (B∩A) = (A∩B) U (B∩C)
d) (A∩C) U (B∩C) = (AUB) ∩C

47. Q11. Which of the following is an appropriate term for a special register that contains the address of the next instruction to be fetched?
a) Accumulator b) Instruction register

c) Program counter d) Status register

48. Q12. In memory systems, when data is detected in the cache, it is known as a hit. When data is not detected in the cache, it is read from the main memory and is known as a miss. Which of the following is the approximate hit ratio for the specifications in the table below? Here, effective access time is calculated as the weighted average of hit time and miss time, and other overhead is ignored.

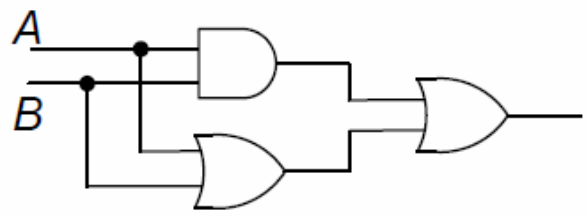
Specifications	Time (ns)
Access time of the cache	100
Access time of the main memory	900
Effective access time of the processor	250

a) 0.25 b) 0.35 c) 0.73 d) 0.81

49. **Q13.** Which of the following is a computer architecture where each instruction is divided into multiple stages (e.g., fetch, decode, and execute) in the processor and multiple functional units execute two or more instructions in parallel by slightly shifting execution stages of the instructions?
a) Multicore b) Pipeline c) RISC d) VLIW

50. Q14. Which of the following is a connection method that is referred to as a daisy chain?
a) A keyboard, a mouse, and a printer are connected to a USB hub, and the USB hub is connected to a PC.
b) A PC and a measuring device are connected with RS-232C, and the PC and a printer are connected by USB.
c) A PC is connected from its own Thunderbolt connection port with a cable to one of the two (2) 4K displays, each of which is equipped with two (2) Thunderbolt connection ports, and the display is connected to the other display with a cable.
d) Several network cameras and PCs are connected to a network hub.

51. **Q21.** Which of the following is a logical expression that is equivalent to the logic circuit shown below?



a) A AND B b) A AND (A OR B)
c) A OR B d) B AND (A OR B)

Q2 2020

52. **Q1.** For two 8-bit signed integers *A* and *B* in 2's complement format, which of the following will cause an overflow when the addition of *A* and *B* is executed? b

	A	*B*
a)	0111 1111	1111 1110
b)	0111 1111	0111 1110
c)	1000 0000	0111 0000
d)	1111 1111	1111 1111

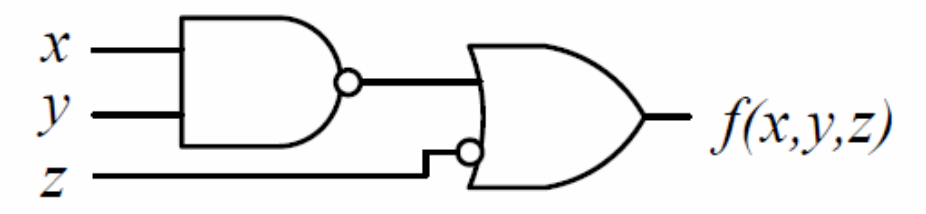
53. Q2. What is the probability of getting at least two heads when a fair coin is flipped five times?
a) 0.78125 b) 0.8125 c) 0.84375 d) 0.875
Q9.

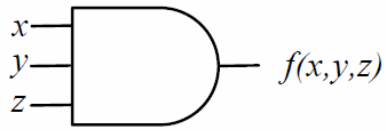
54. Q10. Which of the following is classified as an internal interrupt?
a) An interrupt due to an abnormal power condition, such as a momentary loss of the commercial power supply
b) An interrupt due to having performed division by zero
c) An interrupt due to the completion of input or output
d) An interrupt due to the occurrence of a memory parity error

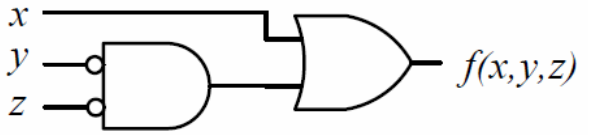
55. Q11. Which of the following is an appropriate characteristic of SRAM compared with DRAM?
a) Compared with DRAM, SRAM consumes more power while it is idle.
b) Compared with DRAM, SRAM needs a fewer number of transistors to store one bit of data.
c) SRAM does not need to be refreshed periodically as flips flops retain data, and DRAM needs to be refreshed at fixed intervals to retain data.
d) SRAM stores data in a combination of capacitors and transistors, and DRAM stores data in a set of transistors called flip-flops.

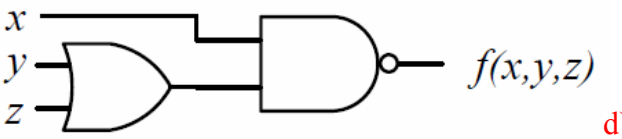
56. Q21. Which of the following is an appropriate description of flash memory?
a) Data must be rewritten periodically.
b) Flash memory can be rewritten at high speed and is used in the cache memory of the CPU.
c) The content can be erased electrically in units of blocks.
d) The entire content can be erased by ultraviolet rays.

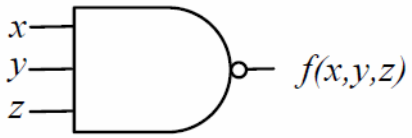
57. Q22. Which of the following is equivalent to the circuit below?



a)


b)


c)


d)


58. b

Q23. Which of the following is an appropriate equation of the XOR operator? Here, " • " represents the logical AND, "+" represents the logical OR, and $\overline{P}$ represents the inverse of P in the logical expression.

a) $X = (A \cdot B) \cdot \overline{(A \cdot B)}$
b) $X = (A + B) \cdot \overline{(A \cdot B)}$
c) $X = (A \cdot B) \cdot \overline{(A + B)}$
d) $X = (A + B) \cdot \overline{(A + B)}$

ch-3 59. Q25. Audio signals are recorded using 8-bit samples at a sampling rate of 11,000 times per second. When a flash memory of 512×10^6 bytes is used, what is the maximum recording time of such data in minutes?
a) 77 b) 96 c) 775 d) 969

October 2020

60. Q1. When the decimal arithmetic expression, 7 / 32, is evaluated, which of the following represents the result in binary?
a) 0.001011 b) 0.001101 c) 0.00111 d) 0.0111

61. Q2. A contradiction is a Boolean expression that always evaluates as FALSE for any assignment of truth values to its variables. Which of the following is a contradiction? Here, " · ", " + ", and " ¯ " represent the AND, OR, and NOT operators, respectively. a

a) $(p \cdot (\bar{p} + q)) \cdot \bar{q}$
b) $(p \cdot \bar{q}) \cdot (\bar{p} + \bar{q})$
c) $p + (p \cdot q)$
d) $\bar{p} + (p \cdot \bar{q}) + q$

62. Q3. A factory manufactures the same products on two production lines, A and B. Line A manufactures 60% of all products, and B manufactures the remaining 40%. Defect rates of products manufactured in A and in B are 2% and 1%, respectively. When a product was

randomly chosen for inspection among the products manufactured in this factory, it was found to be defective. What is the percentage of probability that the product was manufactured in Line A?
a) 40 b) 50 c) 60 d) 75

63. **Q4.** For an 8-bit code with the most significant bit as its parity bit, which of the following is used to obtain the lower seven (7) bits other than parity?
a) Perform a bitwise AND operation with 0F in hexadecimal
b) Perform a bitwise AND operation with 7F in hexadecimal
c) Perform a bitwise OR operation with 0F in hexadecimal
d) Perform a bitwise XOR (exclusive OR) operation with FF in hexadecimal

64. Q10. When the CPU needs data, it first accesses the cache memory. When the data is not available in the cache memory, the CPU accesses the main memory. If the miss ratio is 0.2 and the access times for cache memory and main memory are as shown below, what is the approximate average memory access time in ns for the CPU? Here, there are only cache memory and main memory for the CPU, the access time for main memory includes the time to confirm whether the data is available in cache memory, and the overhead time for the cache management can be ignored.

Access destination	Access time (ns)
Cache Memory	75
Main Memory	1500

a) 315 b) 360 c) 1,215 d) 1,260

65. **Q11.** Which of the following causes an external interrupt?
a) Notification of elapsed time by a timer
b) The execution of a division-by-zero instruction
c) The execution of a non-existent operation code
d) The occurrence of a page fault

66. Q12. Which of the following is an appropriate explanation of a device driver?
a) Software to control peripheral devices that are connected to a PC
b) Software to install an application on a PC
c) Software to invade another PC and cause damage
d) Software to register the operation procedures for a keyboard or other devices and to automate this operation

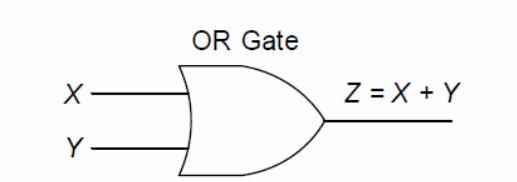
67. Q19. Which of the following represents appropriate handling for open source software according to OSI's definition?
a) For open- source software that is created for a specific industry, the scope of publishing of the source code can be limited to that industry.

b) If open- source software is to be modified for uses such as internal use by a company without being redistributed, the modified part of the source code does not have to be published.
c) When open- source software is modified and redistributed, the same license as the original software must be used for distribution so that the distribution conditions are remain the same as the original software.
d) When open- source software is redistributed by a third party as a product, the developer of the open- source software can charge a license fee to the third party.

68. Q20. Which of the following is an appropriate description of DRAM?
a) It is memory that requires a refresh operation, and it is used as the main memory of a PC.
b) It is non-volatile memory of a NAND type or a NOR type, and it is used as an SSD.
c) It is non-volatile memory that is capable of erasing and writing data in byte units, and it is used when data need to be retained even when the power supply is turned off.
d) Its memory cells consist of flip-flops, and it is used for cache memory.

69. Q21. Which of the following is a secondary (rechargeable) battery?
a) Alkaline–manganese dry-cell battery b) Fuel cell
c) Lithium-ion battery d) Silver-oxide battery

70. **Q22.** Which of the following is the correct gate that converts the 2-input OR gate shown below into a NAND gate if the output of the added gate is respectively connected to input X and input Y?



a) AND b) NOR c) NOT d) OR

April 2019

71. Q1. For an eight-bit integer x represented in two's complement format, which of the following yields the value of 5x? Here, the overflow or underflow can be ignored in this multiplication.
a) Shift x to the left by 1 bit, then add the initial value of x to it.
b) Shift x to the left by 2 bits, then add the initial value of x to it.
c) Shift x to the right arithmetically by 1 bit, then subtract the initial value of x from it.
d) Shift x to the right arithmetically by 2 bits, then subtract the initial value of x from it.

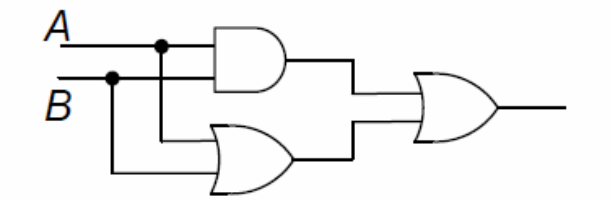
72. Q2. How many four-digit decimal numbers are made from four (4) different digits between 0 and 9? Here, a four-digit decimal number has a non-zero leading digit.
a) 4320 b) 4436 c) 4536 d) 5040

73. Q10. Which of the following is an appropriate characteristic of SRAM compared to DRAM?
Here, SRAM and DRAM are compared in products manufactured in the same or similar semiconductor geometric process.
a) SRAM consumes more power, particularly when idle, compared to DRAM.
b) SRAM is non-volatile, whereas DRAM is volatile.
c) SRAM needs to be refreshed, whereas DRAM does not.
d) SRAM uses more transistors in a memory cell compared to DRAM.

74. Q11. In a memory system that has a cache memory, which of the following causes an increase in the average memory access time?
a) A decrease in the access time to the cache memory
b) A decrease in the cache hit rate
c) A decrease in the cache miss penalty
d) A decrease in the cache miss rate

75. Q12. There exists a storage system in which one (1) block is composed of eight (8) sectors of 500 bytes each, and the storage area is block-wise allocated to the files. When a 2,000-byte file and 9,000-byte file are to be saved, what is the total number of sectors that is allocated to these two (2) files? Here, the sectors that are occupied by the directory information and other such management information can be ignored.
a) 22 b) 26 c) 28 d) 32

76. Q23. Which of the following is a logical expression that is equivalent to the logic circuit shown below?



a) A AND B b) A AND (A OR B) c) A OR B d) B AND (A OR B)

October 2019

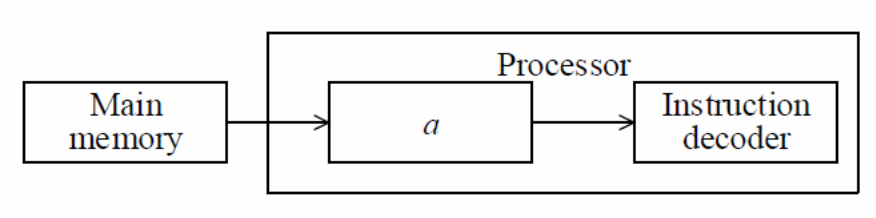
77. Q1. For logical variables p and q, which of the following is a logical expressions that evaluates to true for any values of p and q? b

a) $\bar{p} + (p \cdot q)$ b) $(p \cdot q) + (\bar{p} + (p \cdot \bar{q}))$
c) $(p \cdot \bar{q}) \cdot (\bar{p} + q)$ d) $((\bar{p} \cdot q) \cdot (p \cdot q)) \cdot \bar{q}$

78. Q2. What is the Hamming distance of bit strings 10101 and 11110?
a) 0 b) 2 c) 3 d) 5

79. Q3. A candy box contains four flavors of candies: 6 lemon-flavored, 12 strawberry-flavored, 8 orange-flavored and 4 grape-flavored. When a candy is randomly chosen from the box, what is the probability that it is either lemon- or orange-flavored?
a)4/9 b)7/15 c)6/11 d)7/8

80. Q12. The figure shows the storage sequence of instructions fetched by a processor. Which of the following corresponds to a?



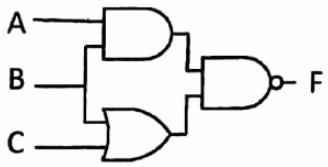
a) Accumulator b) Data cache
c) Instruction register d) Program register (program counter)

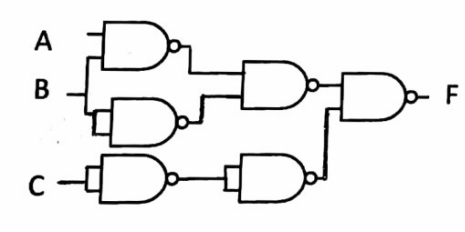
81. Q13. Which of the following is an appropriate description of cache memory?
a) Cache memory is used to fill a gap in memory capacity between the physical memory and the virtual memory.
b) Due to significant improvements in the access speed of semiconductor memory, the need for cache memory is decreasing.
c) If a cache miss occurs, an interrupt is generated, and data is transferred from the main memory to the cache memory by the program.
d) When the write instruction is executed, the cache memory is rewritten in two ways. In one, both the cache memory and the main memory are rewritten, and in the other, only the cache memory is rewritten, and the main memory is rewritten when the relevant data is removed from the cache memory.

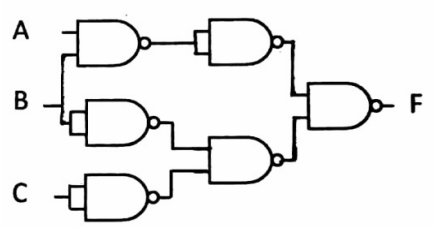
82. Q22. Which of the following is a sequential circuit that has two (2) stable states?
a) Adder circuit b) Capacitor c) Flip-flop d) NAND gate

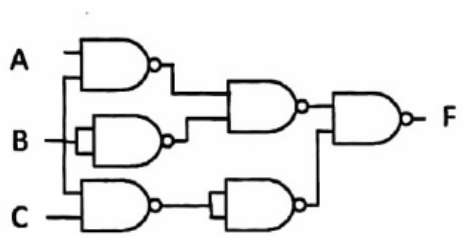
83. Q23. Which of the following is an appropriate description of flash memory?
a) All its contents can be erased at once with ultraviolet rays.
b) Data can be electronically erased in block units.
c) It can be rewritten at a high speed and is used for the cache memory of a CPU.
d) It needs to rewrite data periodically.

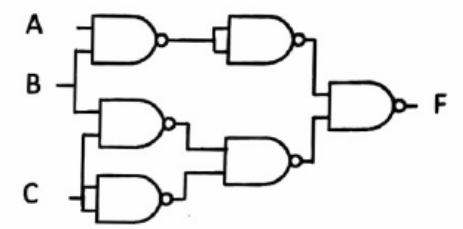
84. Q24. Which of the following is an equivalent representation of the circuit below where only NAND gates are used?



a) 

b) 

c) 

d) 

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85. Q1. There is a register where an integer value is stored in binary. Let x be a positive integer which is stored into the register, then perform the operations below.
(1) Shift the content of the register to the left by 2 bits
(2) Add x to the register.
How many times larger than the integer x is the content of the register?
a) 3 b) 4 c) 5 d) 6

86. Q2. When three sets A, B and C are given, which of the following equalities holds? Here, U and ∩ are union and intersection symbols, respectively. d

a) $(A \cup B) \cap (A \cap C) = B \cap (A \cup C)$
b) $(A \cup B) \cap C = (A \cup C) \cap (B \cup C)$
c) $(A \cap C) \cup (B \cap A) = (A \cap B) \cup (B \cap C)$
d) $(A \cap C) \cup (B \cap C) = (A \cup B) \cap C$

87. Q3. For two logical variables X and Y, a logical operation X NAND Y is defined as a composite operation NOT (X AND Y). Which of the following is equivalent to the logical operation X OR Y?
a) ((X NAND Y) NAND X) NAND Y
b) (X NAND X) NAND (Y NAND Y)
c) (X NAND Y) NAND (X NAND Y)
d) X NAND (Y NAND (X NAND Y))

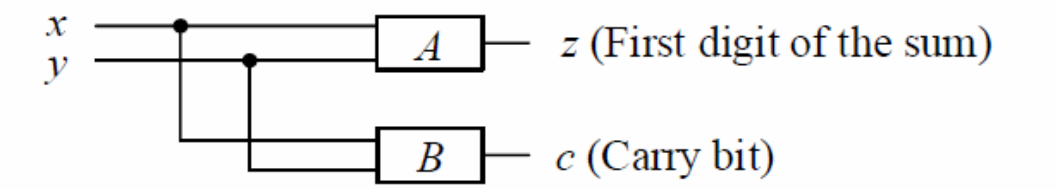
88. Q9. Which of the following addressing modes determines the effective address by adding the value of the instruction address register (program counter) to the value recorded in the address part of the instruction?
a) Absolute addressing b) Base addressing
c) Indexed addressing d) Relative addressing

89. Q10. A computer has two levels of memories, cache memory and main memory, with an access time of 0.01 μs and 0.1 μs respectively. If the hit ratio of the cache memory is 90%, which of the following is the appropriate average memory access time for this system? In this scenario, if the data is in the cache memory, the processor accesses the data directly with an access time of 0.01 μs. However, if a cache miss occurs, the data is required to be transferred from the main memory to the cache memory first, and then subsequently accessed from the cache memory. Thus, the access time becomes 0.11 μs.
a) 0.011 μs b) 0.019 μs c) 0.020 μs d) 0.091 μs

90. Q11. Which of the following is an output device for the computer?
a) Camera b) Mouse c) Printer d) Scanner
91. Q12. What is the average rotational latency of a hard disk drive in milliseconds when its rotation speed is 2000 rotations per minute?
a) 10 b) 15 c) 25 d) 30

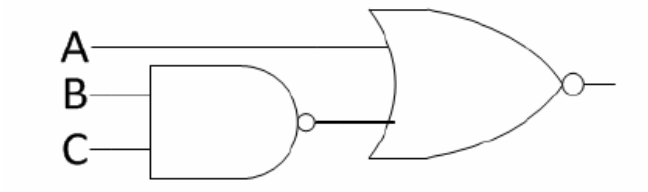
92. Q21. A D/A converter with a resolution of 8 bits generates an output voltage of 0 volts for a digital input value of 0, and an output voltage of 2.5 volts for a digital input value of 128. When the lowest 1 bit of the digital input value is changed, which of the following is the change (in volts) of the output voltage that is generated by the D/A converter?
a) 2.5/128 b) 2.5/255 c) 2.5/256 d) 2.5/512

93. Q22. The half adder in the diagram below adds two (2) single-digit binary numbers x and y, and produces z (the first digit of the sum) and c (the carry bit) as output. Which of the following is the appropriate combination of gate devices A and B? a

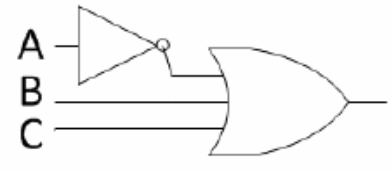


	A	*B*
a)	Exclusive logical sum (XOR)	Logical product (AND)
b)	Logical product (AND)	Logical sum (OR)
c)	Negative logical product (NAND)	Negative logical sum (NOR)
d)	Negative logical sum (NOR)	Exclusive logical sum (XOR)

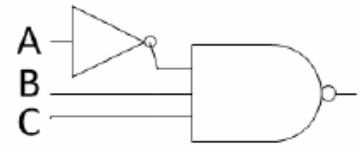
94. Q23. Which of the following is equivalent to the logic circuit shown below?



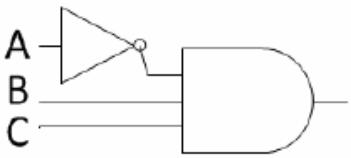
a)



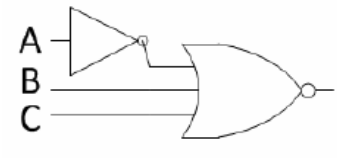
b)



c)



d)



95. Q25. Which of the following is a process in PCM to capture analog values from audio signals at a regular interval?

a) Encoding b) Reverse quantization c) Quantization d) Sampling

96. Q47. Which of the following is the appropriate combination of the basic concept of object orientation?

a) Abstraction, encapsulation, inheritance, class

b) Embodiment, structuring, continuation, class

c) Normalization, encapsulation, division, class

d) Virtualization, structuring, projection, class

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97. Q1. Which of the following is a logical expression equivalent to the exclusive-OR operation of logical variables p and q? Here, "V", "∩", and "¬" are OR, AND, and NOT operators, respectively. b

a) $\neg p \vee q$ b) $(p \vee q) \wedge \neg(p \wedge q)$

c) $\neg(p \vee q) \vee (p \wedge q)$ d) $(p \wedge \neg q) \vee \neg(q \wedge p)$

98. Q2. Among the bit strings of length 4, how many of them either start with 1 or end with 00?

a) 4 b) 8 c) 10 d) 12

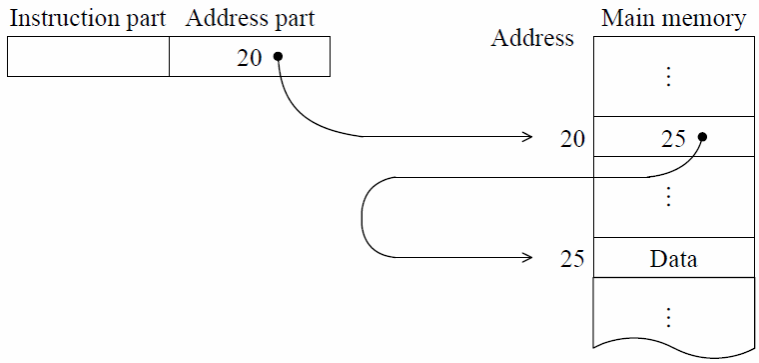
99. Q3. A factory manufactures the same products in two production lines A and B, where 60% of the products are manufactured in A, and the remaining in B. Defective rates of the products manufactured in A and B are 2% and 1%, respectively. When a product was randomly chosen for inspection, it was found to be defective. What is the percent probability that the product was manufactured in A?

a) 40 b) 50 c) 60 d) 75

100. Q10. Which of the following is a special purpose register that stores the result of a comparison or the sign of the result of an arithmetic operation?

a) Accumulator b) Flags register c) Instruction register d) Program counter

101. Q11. Which of the following is the addressing mode that references data in main memory as shown in the figure below?



a) Direct addressing b) Indexed addressing c) Indirect addressing d) Relative addressing

102. Q13. Which of the following is an appropriate explanation of USB 3.0?

a) It uses a serial interface that has a 5 Gbps data transfer mode called super speed.

b) It uses a serial interface that has both an isochronous transfer mode suitable for voice, video, and other data, and a broadcast transfer mode.

c) It uses an interface that transmits 2 bits of information in one (1) clock cycle with four (4) pairs of signal lines, and has a maximum throughput of 1 Gbps.

d) It uses the serial version of ATA interface that is standardized for the connection of a PC to peripheral devices.

103. Q14. Which of the following is an appropriate description of the effect of cache memory?

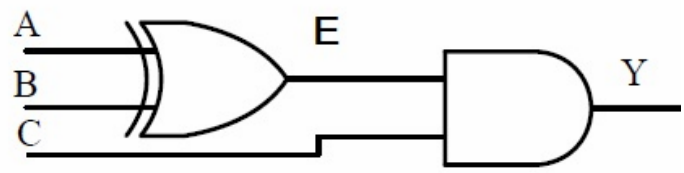
a) By reading data from main memory and storing it in cache memory, and then processing instructions in parallel in cache memory, operations are performed at high speed.

b) By reading data from main memory and storing it in cache memory, data transfer is performed at high speed when the CPU reads the same data later.

c) By reading instructions and data simultaneously from main memory to cache memory, data transfer is performed at high speed.

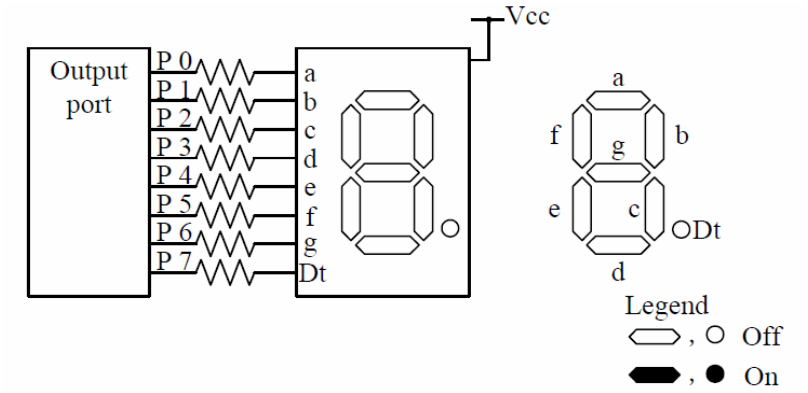
d) By reading instructions from main memory and storing them in cache memory, and then decoding and executing them in cache memory, operations are performed at high speed.

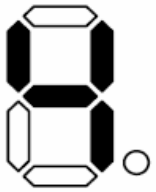
104. Q22. There is a logic circuit shown below. When the input values are A = 1, B = 0, and C = 1, which of the following is the combination of the values of E and Y?



a) E = 0, Y = 0 b) E = 0, Y = 1 c) E = 1, Y = 0 d) E = 1, Y = 1

105. Q24. In a lighting circuit for an anode-common type LED with seven (7) segments, when 92 in hexadecimal is written out to the output port, which of the following is displayed? Here, P7 is the most significant bit (MSB), P0 is the least significant bit (LSB), and the LED lights up when the port output is 0.



a)  b)  c)  d) 

106. Q26. An audio signal is sampled 11,000 times per second while each sample is recorded as an 8-bit data. When a 512×10^6-byte capacity flash memory is used, what is the maximum number of minutes to record such data?
a) 77 b) 96 c) 775 d) 969

107. Q48. Which of the following is the appropriate combination of Class and Object in Object Oriented Programming? a

	Class	Object
a)	A class can be termed as a group of objects with similar behavior and similar attributes.	An object is a particular instance of a class.
b)	A class can be termed as a group of objects with similar behavior and similar attributes.	An object is the blueprint of the class.
c)	A class contains the real values of its attributes.	An object has the definition and behavior of a class.
d)	A class is an instance of a particular object.	An object can be defined as a template that describes the behavior that the class of its type support.

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108. Q1. For an 8-bit binary number, which of the following sets the middle 4 bits to 1s while inverting the remaining bits?

a) Performing a bitwise AND operation with 00111100
b) Performing a bitwise NAND operation with 11000011
c) Performing a bitwise OR operation with 11000011
d) Performing a bitwise XOR operation with 00111100

109. Q2. Which of the following is logically equivalent to the expression below? Here A, B, C, and D are integers, '<' is a less-than operator, and '≤' is a less-than-or-equal-to operator.

not ((A ≤ B) or (C < D))

a) (A < B) and (C ≤ D) b) (A < B) or (C ≤ D)
c) (B < A) and (D ≤ C) d) (B < A) or (D ≤ C)

110. Q3. There are 16 cards numbered from 1 to 16. When four cards are randomly chosen at the same time, what is the probability that all of them are even?
a)1/26 b)1/24 c)1/20 d)1/16

111. Q4. For two sets A and B of cardinalities 3 and 2, how many maps from A to B exist?
a) 1 b) 5 c) 8 d) 9

112. Q10. Which of the following is the addressing mode where the instruction contains the address and the address is modified by a value from another register?
a) Direct addressing mode b) Indexed addressing mode
c) Memory indirect addressing mode d) Register indirect addressing mode

113. Q11. Which of the following is the computer architecture where processors execute multiple instruction streams on multiple data streams in parallel?
a) MIMD b) MISD c) SIMD d) SISD

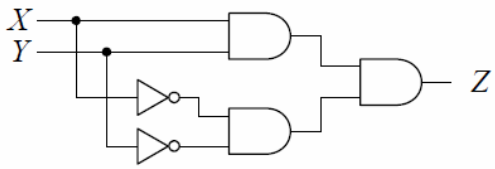
114. Q12. Which of the following is an appropriate explanation of memory interleaving?
a) It allows CPU to access different banks of the main memory simultaneously.
b) It improves CPU performance by connecting I/O interface directly to the main memory.
c) It makes use of a fast memory between the CPU and the main memory, which serves as a buffer for frequently accessed data.
d) It widens the data bus to read or write several bytes between the CPU and the main memory in a single process.

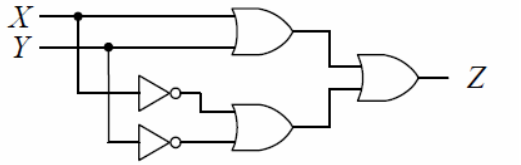
115. Q13. Which of the following is an appropriate role for a device driver?
a) It decides the next task to be executed from tasks waiting for execution.
b) It directly controls hardware according to requests from an application program.
c) It interprets command strings that are entered by the user, and starts the applicable program.
d) It manages the display status on the screen in multiple windows.

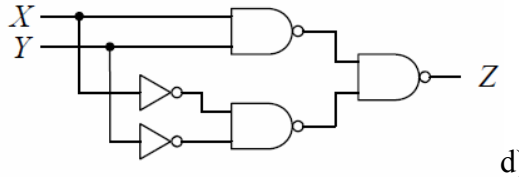
116. Q23. Which of the following is a characteristic of DRAM?
a) Even if the power supply is cut, it can retain stored data.

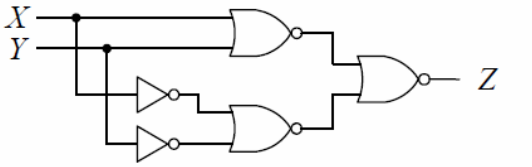
b) Memory refresh to retain stored data is not necessary.
c) The memory cell structure is simple, so high integration is possible and a low price per bit can be achieved.
d) Writing and erasing data are performed in blocks or in a whole chip.

117. Q24. Which of the following is the logical circuit that generates "1" as the output signal Z, only when the input signals X and Y have the same value?

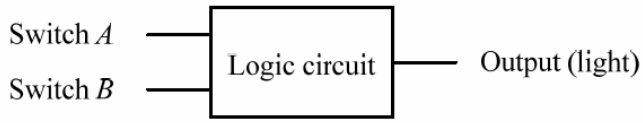
a) 

b) 

c) 

d) 

118. Q25. Which of the following logic circuits meets the condition described below?
[Condition]
A light is turned on and off by using switches A and B located at the top and bottom of the stairs. The light can be turned on and off by using one switch, regardless of the status of the other switch.



a) AND b) NAND c) NOR d) XOR

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119. Q1. What is the octal representation of a hexadecimal fraction F1B0.C?
a) 170660.6 b) 361540.14 c) 743300.6 d) 5213052.3

120. Q2. When two unbiased coins are tossed and an unbiased six-sided die is rolled at the same time, what is the probability that at least one coin shows heads and the die shows an even number?
a) 1/4 b) 3/8 c) 1/2 d)3/4

121. Q8. There are two boxes; the first box contains two green balls and three red balls; the second box contains three green balls and two red balls. A boy randomly selects a box from the two, and then randomly picks a ball from that box. If the ball is red, what is the probability that he selected the first box?
a) 3/20 b) 3/10 c) 1/2 d) 3/5

122. Q9. Which of the following is an appropriate explanation of symmetric multiprocessing (SMP)?

a) One CPU core serves as a master, while the other CPU cores act as slaves and perform the tasks assigned to them by the master.
b) One or more programs are loaded in the main memory, and only one program at a time is able to get the CPU for the execution while all the others are waiting their turns.
c) Several CPU cores have schedules for their own tasks, with priorities set by the operating system with equal access to the memory and system resources.
d) While one stage of an instruction is being processed, other instructions may be processed at a different stage so that multiple instructions can be processed at the same time.

123. Q10. To determine an effective address from the value recorded in the address part of instruction, various addressing modes are used. Which of the following modes uses the value of the address part as an effective address?
a) Absolute addressing b) Base plus index addressing
c) Indexed addressing d) PC relative addressing

124. **Q11.** Which of the following is a memory device that stores programs or data in factories, and only has the read operation for the stored programs or data?
a) DRAM b) Flash memory c) Mask ROM d) SRAM

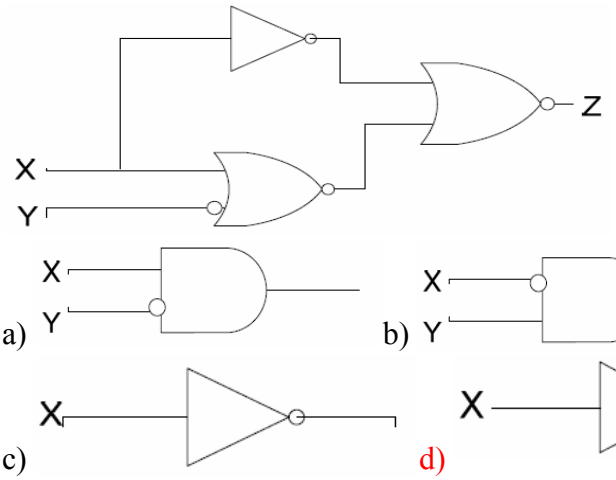
125. Q12. Which of the following is an appropriate role of a device driver?
a) It decides the next task to be executed from tasks queued up for execution.
b) It directly controls the hardware according to requests from an application program.
c) It interprets the command strings that are entered by the user, and starts the applicable program.
d) It manages the display status on the screen in multiple windows.

126. Q17. In input/output management, which of the following is an appropriate function of a buffer?
a) Enabling an input/output device to be handled in the same way as a file
b) Enabling the use of an input/output device without the need to consider its unique specifications by creating a data exchange layer between an input/output device and a processing device
c) Notifying a processing device when an input/output device becomes available for use
d) Reducing the difference in processing speed by establishing a special area of memory between an input/output device and a processing device

127. Q20. Which of the following is an appropriate explanation of optimization in a compiler?
a) Analyzing the source code and generating an object code with an improved run-time processing efficiency
b) Generating an intermediate code for an interpreter rather than generating an object code
c) Generating an object code that displays the called subprogram name or the content of a variable at a particular point in time during the execution of the program

d) Generating an object code that operates in a computer with a different architecture from the computer in which the compiler is implemented

128. **Q21.** Which of the following is equivalent to the logic circuit below?



129. **Q22.** Which of the following is a logic gate combination that provides an output 1 when both inputs are 0?

a) AND or XOR b) NAND or XOR c) NOR or XNOR d) OR or XNOR

130. **Q23.** Which of the following uses a flip-flop circuit in a memory cell?

a) DRAM b) EEPROM c) SDRAM d) SRAM

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130. Q1. Which of the following decimal values is equivalent to a hexadecimal fraction 0.B1? d

a) $2^0 + 2^{-2} + 2^{-3} + 2^{-7}$ b) $2^0 + 2^{-3} + 2^{-4} + 2^{-8}$

c) $2^{-1} + 2^{-3} + 2^{-4} + 2^{-7}$ d) $2^{-1} + 2^{-3} + 2^{-4} + 2^{-8}$

131. Q2. Which of the following is a solution for the logical equation on variable X below? Here, A,B, and C are logical constants; the operators "+", "·", and "¯" denote logical OR, logical AND, and NEGATION, respectively. d

$$A \cdot B + X + B \cdot C = A \cdot B + \bar{A} \cdot C$$

a) $A \cdot C$ b) $\bar{B} \cdot \bar{C}$ c) $\bar{B} + C$ d) $\bar{A} \cdot C$

132. Q3. Alice and Mary take a math exam. The probability of passing this exam for Alice and Mary is 2/3 and 3/5, respectively. What is the probability that at least one of them will pass the exam?

a) 1/5 b) 7/15 c) 3/5 d) 13/15

133. Q11. In a CPU with a four (4)-stage pipeline composed of fetch, decode, execute, and write back, each stage takes 10, 6, 8, and 8 ns, respectively. Which of the following is an approximate average instruction execution time in nanoseconds (ns) in the CPU? Here, the number of instructions to be executed is sufficiently large. In addition, the overhead for the pipelining process is negligible, and the latency impact from all hazards is ignored.
a) 6 b) 8 c) 10 d) 32
134. Q12. Which of the following is the computer architecture where a processor executes the same instruction on multiple data?
a) MIMD b) MISD c) SIMD d) SISD

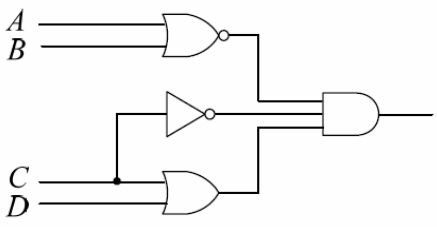
135. Q13. Which of the following is an addressing mode that provides an offset to the program counter (PC) content to determine the address of the operand?
a) Immediate addressing mode b) Indirect addressing mode
c) Register indirect addressing mode d) Relative addressing mode

136. Q14. Which of the following is used to translate a logical address generated by a CPU into a physical address?
a) Direct Memory Access Controller (DMAC) b) Memory Address Register (MAR)
c) Memory Management Unit (MMU) d) Translation Lookaside Buffer (TLB)

137. Q15. Which of the following is an appropriate description concerning cache memory?
a) In a multi-tasking environment, a cache memory maintains data from each task to improve performance.
b) Multiprocessors where each has a cache memory need to synchronize values within the cache to maintain coherency.
c) The operating system manages the data transfer between registers and a cache memory.
d) The speed and size of a cache memory are the only consideration when improving performance.

138. Q17. Which of the following is an appropriate description of throughput?
a) Even if some idle time resulting from operator intervention between the end of a job and the start of the next job occurs in a system, throughput is not affected.
b) Multi-programming contributes to reducing turnaround time, but is not useful in improving throughput.
c) Spooling, which involves temporarily saving the output to a printer in a hard disk, is useful in improving throughput.
d) Throughput is an index of CPU performance and is not affected by the I/O speed, overhead time, and other such factors.

139. Q24. Which of the following is a logical (or Boolean) expression that is equivalent to the logic circuit shown below? Here, "+" is the logical sum, " . " is the logical product, and "$\overline{X}$" is the negation of X. d



a) $\overline{A \cdot B \cdot \overline{C}} \cdot C \cdot D$ b) $(\overline{A} + \overline{B}) \cdot \overline{C} \cdot (C + D)$

c) $\overline{A \cdot B} + \overline{C} + D$ d) $\overline{A} \cdot \overline{B} \cdot \overline{C} \cdot D$

140. Q25. Which of the following is a sequential circuit that has two (2) stable states?
a) Adder circuit b) Flip-flop c) NAND gate d) NOR gate
141. Q26. Which of the following is an appropriate input for a common anode seven-segment display to display a character shown as output? Here, A represents the most significant bit (MSB) and G represent the least significant bit (LSB).

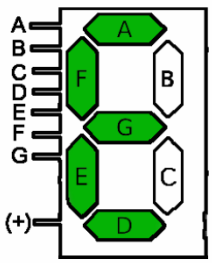


Figure: Display of character "E" in a seven-segment display

a) 0110000 b) 0000110 c) 1001111 d) 1111001

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142. Q1. If a given bit string contains at least one 1-bit, the algorithm below leaves the rightmost 1-bit unchanged but makes all the others 0. For example, if the given bit string is 00101000, the result will be 00001000. Which of the following is the appropriate logical operation to be filled in D?
Step 1: By regarding the given bit string A as an unsigned binary number, let B be the result of subtracting 1 from A.
Step 2: Calculate the XOR (exclusive logical sum) of A and B, and let C be the result.
Step 3: Calculate the D of A and C, then set the result back to A.
a) AND (logical product) b) NAND (negative logical product)
c) OR (logical sum) d) XOR (exclusive logical sum)

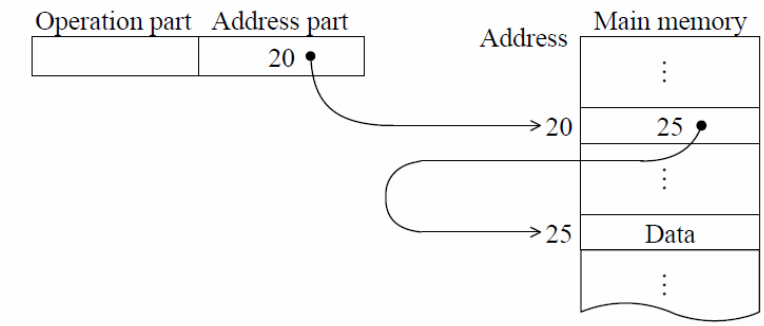
143. Q2. When 4-bit signed numbers in 2's complement are used, which of the following operations will cause either an overflow or an underflow?
a) Add B to A when A is 0110 and B is 1111.
b) Add B to A when A is 1110 and B is 0110.
c) Subtract B from A when A is 0111 and B is 1010.
d) Subtract B from A when A is 1111 and B is 1111.

144. Q3. When two unbiased dice are rolled one by one, what is the probability that either the first one is 2 or the sum of the two is less than 5?
a) 1/6 b) 2/9 c) 5/18 d) 1/3

145. Q4. A leap year is either a multiple of 4 but not a multiple of 100, or a multiple of 400. How many leap years are there from 1998 to 2110?
a) 26 b) 27 c) 28 d) 29

146. Q10. Which of the following is classified as an internal interrupt?
a) An interrupt because of the occurrence of a memory parity error
b) An interrupt because of the operation of division by zero (0)
c) An interrupt caused by a power failure, such as an instantaneous failure of the commercial power supply
d) An interrupt caused by the completion of I/O

147. Q9. Which of the following is the addressing method that references data in the main memory as shown in the figure below?



a) Direct addressing b) Indexed addressing c) Indirect addressing d) Relative addressing

148. Q12. Which of the following lists contain A through D in the order of shorter effective memory access time of the main memory?

	Cache memory			Main memory
	Existence	Access time (nanoseconds)	Hit rate (%)	Access time (nanoseconds)
A	No	-	-	15
B	No	-	-	30
C	Yes	20	60	70
D	Yes	10	90	80

a) A, B, C, D b) A, D, B, C c) C, D, A, B d) D, C, A, B

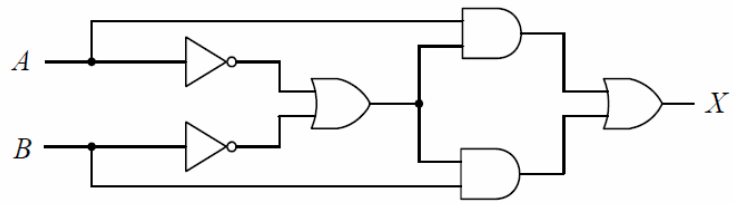
149. Q19. There is a system in which the print requests waiting for output are assigned to an available printer in an order of A, B, and C, and then the printer available first among the three (3) printers A through C of the same model. If the print time of each print request is 5, 12, 4, 3, 10, and 4 (minutes) in the order of the requests waiting for output, which of the

following lists of printers is arranged in an order starting from the longest time assigned for printing? Here, all printers are available in the initial state.
a) A, B, C b) B, A, C c) B, C, A d) C, B, A

150. Q20. Which of the following is an open source integrated development environment that includes software and support tools for application development?
a) Eclipse b) Perl c) PHP d) Ruby

151. Q21. Which of the following is a characteristic of DRAM and not of SRAM?
a) It does not require refresh nor access operations in order to retain data.
b) It has a simple memory cell structure, and thus the price per bit is low.
c) It is mainly used for cache memory
d) It uses flip-flops for the memory cells to save data.

152. Q22. Which of the following is a logical expression that is equivalent to the digital circuit shown in the figure below? Here, "•" is the logical product, "+" the logical sum, and "$\overline{X}$" the negation of X. c



a) $X = A \cdot B + \overline{A \cdot B}$ b) $X = A \cdot B + \overline{A} \cdot \overline{B}$
c) $X = A \cdot \overline{B} + \overline{A} \cdot B$ d) $X = (\overline{A} + B) \cdot (A + \overline{B})$

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153. Q1. Which of the following is the appropriate combination that represents the decimal number "–19" in 8-bit one's complement binary and 8-bit two's complement binary? d

	One's complement binary	Two's complement binary
a)	00010011	11101100
b)	00010011	11101101
c)	11101100	11101100
d)	11101100	11101101

154. Q2. Which of the following is the appropriate binary fraction that is equivalent to the decimal value 5.525? Here, the binary string enclosed in parentheses is repeated infinitely.
a) 101.11 b) 101.1000011 c) 101.10(0011) d) 101.100(0011)

155. Q3. When three apples are removed at random from a box that contains four green apples and eight red apples, what is the probability that the first two apples are green and the third (or last) apple is red? Here, once an apple is removed, it is not put back into the box.
a) 1/18 b) 8/121 c) 4/55 d) 2/27

156. Q10. As shown in the table below, there are a total of 86 coins that are composed of five types of coins. Of those 86 coins, 60 coins are picked up so that the total value can be maximized. What is the total value in dollars? Here, 100 cents are equivalent to 1 dollar.

Type of coin	Number of coins
5-cent	20
10-cent	30
20-cent	25
50-cent	10
1-dollar	1

a) 6 b) 9 c) 10.5 d) 13.4

157. Q11. As shown the figure and table below, there are two types of CPUs X and Y that have the same configuration except that the access times of cache memory and main memory are different from each other. All other conditions of the two CPUs are the same.
When a certain program is executed on both CPU X and CPU Y, the processing time of each CPU is the same. Under these conditions, what is the hit ratio of the cache memory? Here, there are no effects from other than CPU processing.

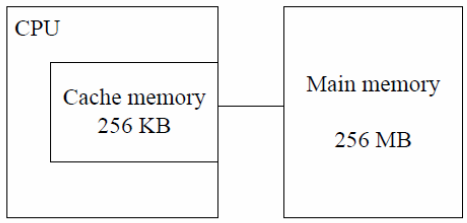


Figure Configuration

Table Access time

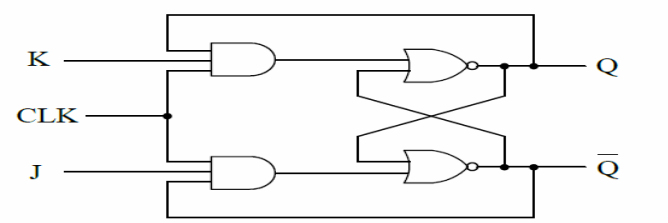
Unit: Nanosecond

	CPU *X*	CPU *Y*
Cache memory	40	20
Main memory	400	580

a) 0.75 b) 0.90 c) 0.95 d) 0.96

158. Q14. Which of the following is an appropriate explanation of a capacitive touch panel?
a) An electric field is formed on the surface, and the touched position is detected on the basis of the change in the surface electric charge.
b) Electrode switches are aligned in a matrix shape, and the touched position is detected by the electronically conducted electrode.
c) The touched position is detected on the basis of the change in the reflection of the infrared ray that is blocked by touching the panel.
d) Voltage is applied to an electrically resistant film, and the touched position is detected on the basis of the change in resistance.

159. Q23. The logic circuit below shows a JK flip-flop. Which of the following is the appropriate truth table for the JK flip-flop. Here, the state of each output signal is affected only when the clock signal CLK changes from 0 to 1. “No Change” means that each output signal maintains its previous state, and “Toggle” means that each output signal switches (or toggles) its state “from 0 to 1” or “from 1 to 0.”



a)

Input signals		Output signals	
J	K	Q	$\overline{Q}$
0	0	No change	
0	1	0	1
1	0	1	0
1	1	Toggle	

b)

Input signals		Output signals	
J	K	Q	$\overline{Q}$
0	0	Toggle	
0	1	0	1
1	0	1	0
1	1	No change	

c)

Input signals		Output signals	
J	K	Q	$\overline{Q}$
0	0	No change	
0	1	1	0
1	0	0	1
1	1	Toggle	

d)

Input signals		Output signals	
J	K	Q	$\overline{Q}$
0	0	Toggle	
0	1	1	0
1	0	0	1
1	1	No change	

160. Q25. Which of the following is a memory module that uses a flip-flop circuit in a memory cell?

a) DRAM b) EEPROM c) SDRAM d) SRAM

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161. Q1. What is the sum of two binary fractions 1.0101 and 1.0111 expressed in decimal?

a) 2.5 b) 2.75 c) 2.875 d) 2.9375

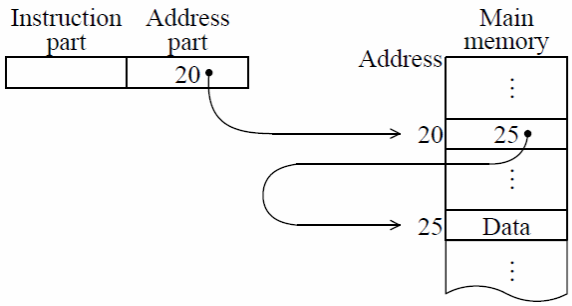
162. Q2. b

Which of the following is the logical expression equivalent to $\overline{A} + B \cdot \overline{C} + \overline{B}$?

a) $\overline{A}$ b) $\overline{A \cdot B \cdot C}$

c) $A \cdot (\overline{B} + C) \cdot B$ d) $\overline{A} + \overline{C}$

163. Q10. Which of the following is the addressing method that references data in main memory as shown in the figure below?



a) Direct addressing b) Index addressing c) Indirect addressing d) Relative addressing

164. Q11. When data is read into a processor and there are no hits in the cache memory, which of the following is the action that the cache memory control unit performs?
a) The required data is read from disk cache to main memory by using the block transfer mechanism.
b) The required data is read from main memory to cache memory by using the block transfer mechanism.
c) The required data is read from the hard disk to cache memory by using the block transfer mechanism.
d) The required data is written from cache memory to the hard disk by using the block transfer mechanism.

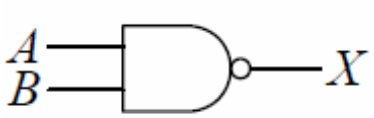
165. Q12. Which of the following statement is true for DMA Controller?
a) DMA controller enables data transfer directly between input/output devices and the memory while the CPU can perform some other operations.
b) DMA controller enables data transfer directly between the cash memory and the main memory while the processor is at the waiting state.
c) DMA controller enables input/output devices to read from and write to the main memory through CPU and system bus.
d) DMA controller enables the CPU to access the main memory directly while input/output devices communicate among themselves at the same time.

166. Q13. Consider a disk drive that has a capacity of 8 GB. The drive has 5 platters with two surfaces, 10,000 tracks per surface and 200 sectors per track. How many bytes are in each sector? Here, 1GB is 1,000,000,000 bytes.
a) 100 b) 200 c) 400 d) 800

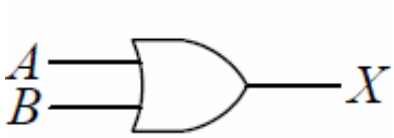
167. Q21. Which of the following is an appropriate explanation of DRAM?
a) It is memory that needs to be refreshed, and is used for main memory in a PC.
b) It is non-volatile memory that can erase and write data in units of one byte, and it is used when data preservation is required even if the power supply is interrupted.
c) It is non-volatile memory that has NAND types and NOR types, and is used for SSD.
d) Its memory cells are composed of flip-flops, and it is used for cache memory.

168. Q22.
Which of the following is the logic circuit that generates the same result as the logical expression $X = \overline{A} \cdot B + A \cdot \overline{B} + \overline{A} \cdot \overline{B}$? Here, "•" is the logical product, "+" is the logical sum, and $\overline{A}$ is the negation of A.

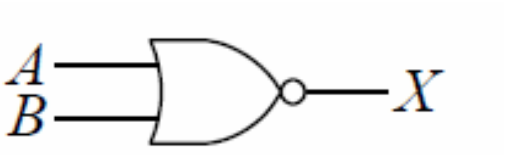
a)



b)



c)



d)

**********End**********