Parameter Name	Description	Read or write	Default Value	**L2:user =** user can modify/adjust **L1:aps/spx =** only change if you know what you're doing **L0:LLRF4/usrp =** defined at board level infrastructure (do NOT touch)
in_amp_set	sets amplitude of LO used for input down-conversion	rw	73785	L2
in_phase_set	sets phase of the LO used for input down-conversion	rw		L2
out_amp_set	sets amplitude of LO used for output up-conversion	rw	73785	L2
out_phase_set	sets phase of LO used for output up-conversion	rw	0	L2
ddsa_phstep_h	ddsa tuning	rw	245411	L1
ddsa_phstep_l	ddsa tuning	rw	1653	L1
ddsa_modulo	dds modulo readback	rw	7	L1
resync	Resynchronizes ddsa and ddsb. There are 2 dds' in the code, ddsa generates the LO used for digital up/down convert for all channels. ddsb is another dds which allows a separate ,LO frequency to be used for detecting harmonics	rw	0	NA
show_test_cnt	a simple adder that counts the number of data pages. It is used to check for continuous data in the waveform. It should be a sawtooth waveform if no pages are lost, a jump or discontinuity signals that a page has been lost.	rw	0	L0
wave_samp_per	a horizontal axis zoom feature for waveform data. It controls the period of the CIC decimation filter used for waveform capture.	rw	2	L2
wave_shift	this is a vertical scaling for the waveforms. It is meant to take out the scaling of the CIC filter determined by wave_samp_per	rw	4	L2
xsel	A 2 bit number which selects which ADC input goes to the ddsb multiplier/downconverter. It can be found in sel_dsp.v	rw	0	L1
close_loop	N/A. Doesn't do anything, left over from other project	rw	0	L2
ch_keep	controls which channels are kept for waveform display/capture. Chooses 8 channels out of 12. It's a 12 bit number, each bit representing one of the 12 channels, a 1 denotes that channel is kept. The 12 channels are: I and Q data of each ADC (total of 8), I/Q of signal downconverted by ddsb (xsel), rest ??	rw	4080	L1
int_ena	Integral Control 1=enable	rw	1	L2
chirp_sel	Chirp Output Control, 1=enable	rw	0	L2
chirp_density	Chirp Pulse Density, nominally set to 3, what are units?	rw	0	L2
cw_sel	Continuous Wave Mode Select, 1=CW (used for outputting constant frequency)	rw	0	L2
gdr_sel	Generator Driven Resonator Select, 1=GDR	rw	1	L2
no_mag	Disables magnitude/phase calculation (mag_phase.v) for SEL operation. Needs to be turned off for GDR mode	rw	1	L2
notch_en	Notch Filter Enable Control, 1=enable, used for cavity emulator	rw	1	L2
chirp_power	Chirp Magnitude Control	rw	0	L2
ref_phase_lock	Reference Phase ,Lock Control, 1=ON	rw	0	L2
ref_phase_reset	Reference Phase Reset, 1=reset reference phase lock process, ??	rw	0	L2
amp_set	Cavity in-phase (I) setpoint	rw	1000000	L2
pha_set	Cavity quadrature (Q) setpoint	rw	0	L2
amp_prop	Proportional Gain for I loop	rw	0	L2
pha_prop	Proportional Gain for Q loop	rw	50000	L2
amp_freq	Integral zero location for I loop	rw	0	L2
pha_freq	Integral zero location for Q loop	rw	0	L2
pha_kick	1=Apply small step input for measuring step response	rw	0	L2
reset_rx	resets the USB interface receiver	rw	0	L0
reset_tx	reset the USB interface transmit	rw	0	L0
enable_rx	enable the USB interface receive	rw	1	L0
enable_tx	enable the USB interface transmit	rw	1	L0
ad95xx	Pre-determined AD9512 parameter setting	rw	0	L0
tpat_speed	"test pattern" generator speed control, found in llrf4_dsp.vh, used for testing USB correctness and speed, also used for pacing of production data flow	rw	2730	L1
src_sel	selects what data is streamed to USB, src_sel=2 chooses production waveform data stream	rw	2	L0
dbg_sel	?? Is it used ?? no, not used	rw	0	L0
en_adc0	power on ADC0	rw	1	L1
en_adc1	power on ADC1	rw	1	L1
en_adc2	power on ADC2	rw	1	L1

en_adc3	power on ADC3	rw	1	L1
en_dac	power on DAC	rw	1	L1
en_slowadc	power on slow add(MCP3208)	rw	1	L1
en_pin	set GEEK_PIN not used	rw	0	na
max1820_sync_enable	asynchronous multiplexer on output	rw	0	L0
max1820_mux_ctl	asynchronous multiplexer on output	rw	0	L0
dac_reconfig	single cycle trigger for reconfigure operation	rw	0	L0
max1820_div_ctl	max1820 core power supply synchronization	rw	0	L0
mcp_3208_divset	configuration of clock divider	rw	42	L0
mcp3208_trigset	mcp3208 trig (every 1920 * usbclk)	rw	1920	L0
mcp3208_lochan	not used	rw	1	L0
mcp3208_lothresh	not used	rw	300	L0
vhf_tuner	not used	rw	0	L0
frequency	FPGA clock frequency(counted by USB clock)	r		
circle_count	Circular Buffer index	r		
circle_fault	Circular Buffer detected fault happened	r	0	
circle_wrap	Circular Buffer wrapped when stopped	r		
adc1_min	minimum value of IF adc1 input	r		
adc1_max	maximum value of IF adc1 input	r		
adc2_min	minimum value of IF adc2 input	r		
adc2_max	maximum value of IF adc2 input	r		
adc3_min	minimum value of IF adc3 input	r		
adc3_max	maximum value of IF adc3 input	r		
adc4_min	minimum value of IF adc4 input	r		
adc4_max	maximum value of IF adc4 input	r		
sel_freq	measured SEL loop frequency (relative to DDS since it tracks down-converted I/Q quadrant mapping history)	r		
sel_freq_errs	SEL loop frequency error counter - counts if there was a quadrant skipped in the I/Q quadrant mapping history tracking)	r		
laser_freq	not used, we don't have laser here	r	0	
rf_zeros	place holder for rf status interlock interface	r	0	
rf_permit	place holder for rf status interlock interface	r	0	
rf_master	place holder for rf status interlock interface	r	0	
rf_on	place holder for rf status interlock interface	r	0	
phase_ref	not used	r		
time1	time stamp bits 0-15	r		
time2	time stamp bits 16-47	r		
time3	time stamp bits 48-63	r		
freq_Hz	DSP Clock Frequency as measured by on board USB crystal (same as frequency, except convert unit to Hz assuming the USB clock is 48MHz)	r		
yscale	full scale value for current wave_shift and wave_samp_per	r		
timestamp1	time stamp bit 0-31	r		
timestamp2	time stamp bit 32-63	r		
mcp_1	mcp 3208 channel index	r	1	
core_current	measured FPGA power current	r		
mcp_2	mcp 3208 channel index	r	2	
lo_power	LLRF4 Local Oscillator power measured with detector chip on LLRF4 board with one of eight slow ADC channels	r		
mcp_3	mcp 3208 channel index	r	3	
ai_1	Slow ADC input? Which channel J7-28	r		
mcp_4	mcp 3208 channel index	r	4	
ai_2	Slow ADC input? Which channel J7-29	r		
mcp_5	mcp 3208 channel index	r	5	
ac_loopback	DAC loopbackJ9-3	r		
mcp_6	mcp 3208 channel index	r	6	
n_a		r		
mcp_7	mcp 3208 channel index	r	7	
5V	5V power monitor from one of the slow adc channels	r		
mcp_8	mcp 3208 channel index	r	8	
J20	J20 connector value	r		
page_id_0	page id at the beginning of the page	r		
page_id_f	page id at the end of the page	r		
na	not used, space holder	r		
checksum	check sum for the page to valid the usb transmission	r		