Computer Organization #3

FIT - HUI

May, 2013

Digital Logic Level

1 ALU 1 bit

Considering a 1-bit ALU at Fig. 1

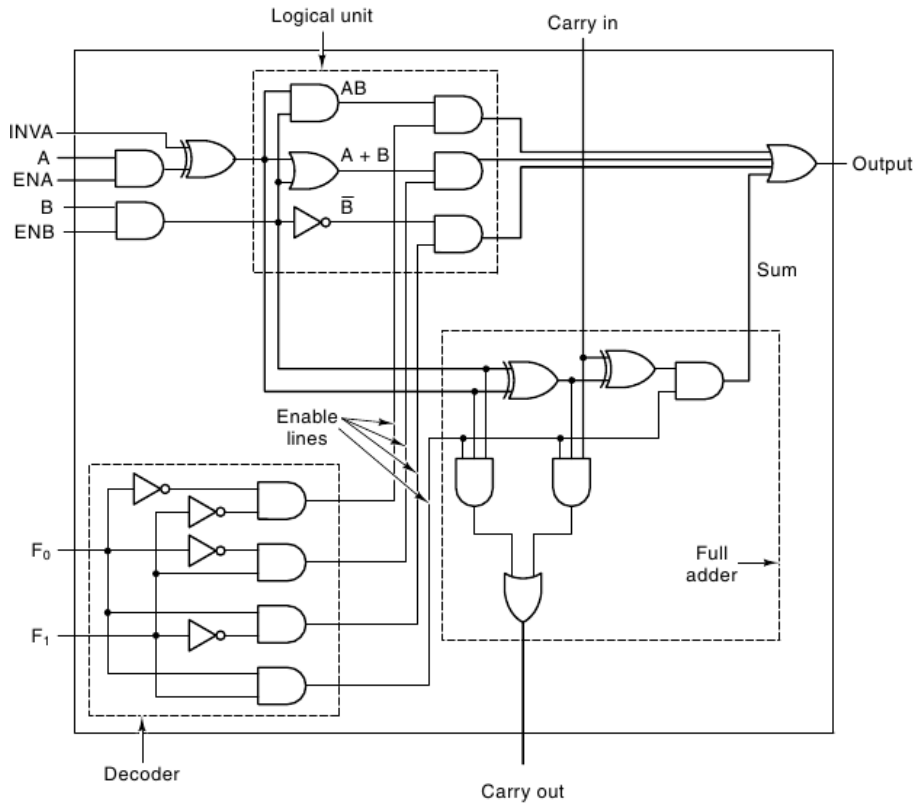

Figure 1: A 1-bit ALU

1. Explain why this ALU called 1-bit ALU?
2. Figure out the role of F0, F1. How many function does this ALU support?
3. Sometimes it is useful for an 8-bit ALU such as Fig. 2 to generate the constant 1 as output. Give two different ways this can be done. For each way, specify the values of the six control signals.

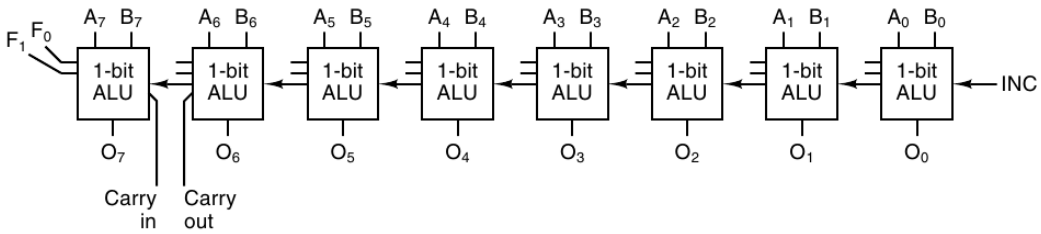

Figure 2: Eight 1-bit ALU slices connected to make an 8-bit ALU. The enables and invert signals are not shown for simplicity

4. A 16-bit ALU is built up of 16 1-bit ALUs, each one having an add time of 10 nsec. If there is an additional 1 nsec delay for propagation from one ALU to the next, how long does it take for the result of a 16-bit add to appear?

2 Memory

The 4 × 3 memory of Fig. 3 uses 22 AND gates and three OR gates.

1. Explain the roles of A0, A1, CS, RD, OE.

2. If the circuit were to be expanded to 256 × 8, how many of each AND, OR gates would be needed?

3 Bus

1. A 32-bit CPU with address lines A2-A31 requires all memory references to be aligned. That is, words have to be addressed at multiples of 4 bytes, and half-words have to be addressed at even bytes. Bytes can be anywhere. How many legal combinations are there for memory reads, and how many pins are needed to express them? Give two answers and make a case for each one.

2. Calculate the bus bandwidth needed to display a VGA (640 × 480) true-color movie at 30 frames/sec. Assume that the data must pass over the bus twice, once from the CD-ROM to the memory and once from the memory to the screen.

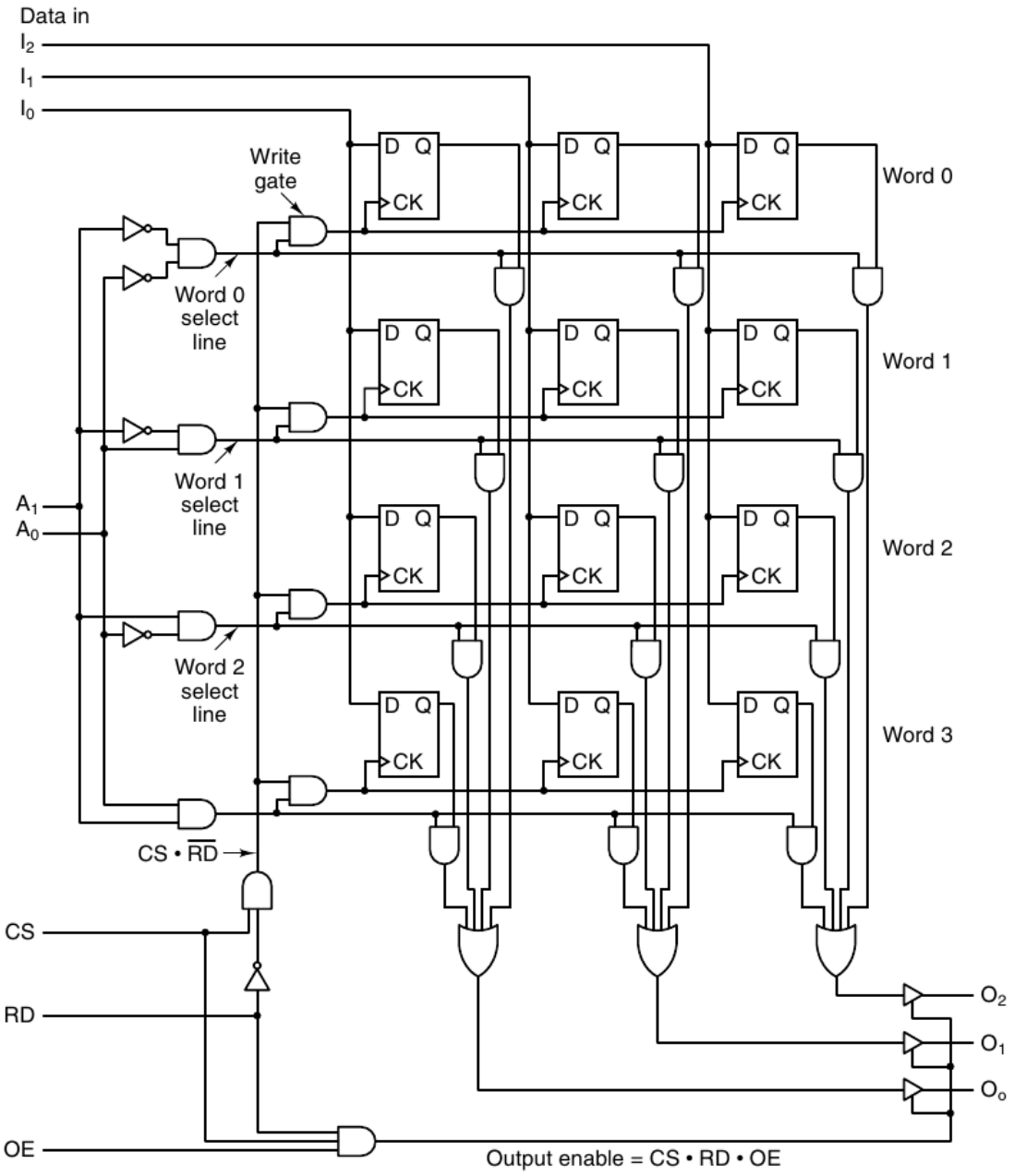

Figure 3: Logic diagram for a 4 × 3 memory. Each row is one of the four 3-bit words. A read or write operation always reads or writes a complete word.