RMIT University

School of Science and Technology (SST)

EEET2602 – Engineering Design 2

Project Report

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1 Introduction

In this project, we are required to build a Voltage Regulated Power Supply mounted on a Printed Circuit Board (PCB) which is designed in Eagle. The circuit is powered by a 18V AC input signal and has ability to transform a 3.3V DC output signal at 1A maximum load. To achieve the final output, there are some aims that we need to manage.

- Reducing output voltage ripple until it smaller 2%.
- When the circuit is overloaded (current > 2V), the switching stops.
- Optimize the size of capacitor as well as the size of PCB.
- Using snubber circuit and non-polarized film capacitor to smooth the output voltage and mitigate high frequency noise.
- Understanding how AC signal is transformed to wished DC signal, and how the output signal is change with various load (66Ω, 10Ω, 3.3Ω).
- Understanding how to control buck converter by the IC chip, how the PWM IC chip produce signal, then provide signal to buck converter.

2 Block Diagram

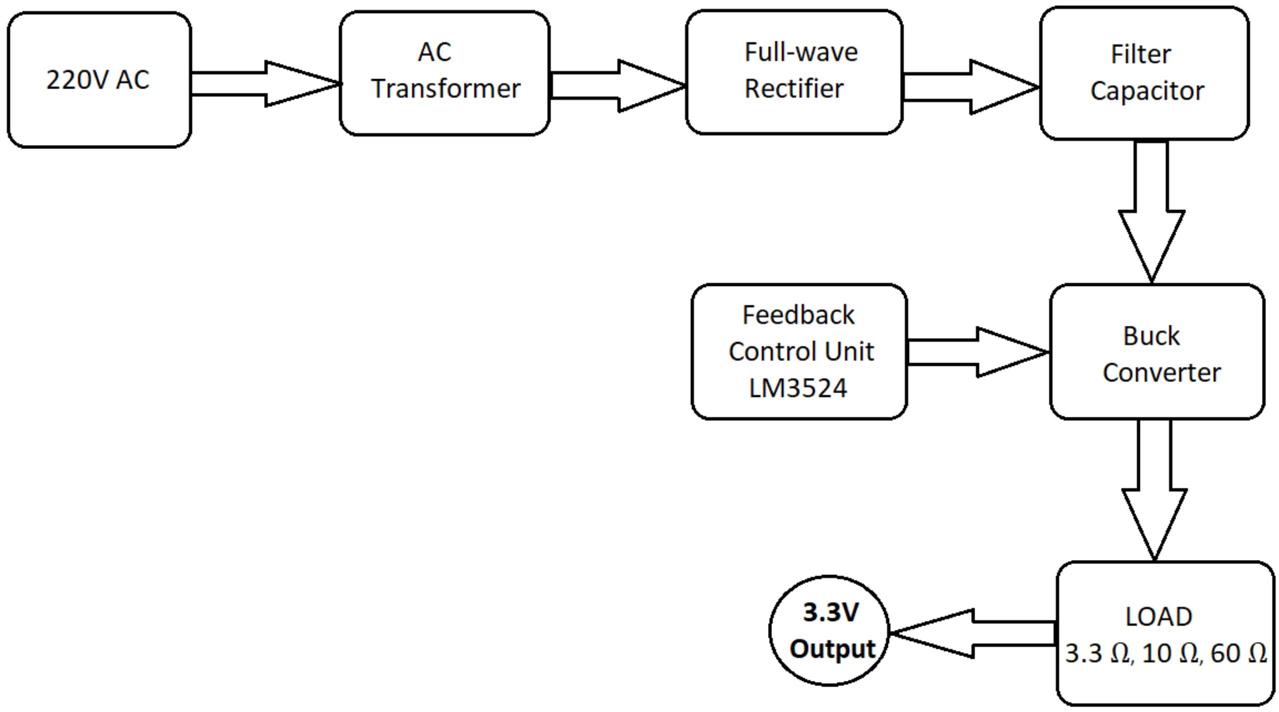

Figure 1: Block diagram of the whole circuit.

3 Circuit Analysis

The Pulse Width Modulated Switching Voltage Regulator uses to step down the voltage when signal went through the regulator which control by Feedback Control Unit. There are 3 main parts in this circuit:

- Before buck converter: Take the 220V signal and by the transformer, the voltage stepdown to 18V. After that, the full-wave rectifier which constructed by 4 diodes, which allow current flow in one way, to convert the 18V AC signal into DC signal. This signal is filter by 2 capacitor C1 and C2 to reduce the noise and ripple voltage.
- The IC control unit: the important part which run the IRF9Z34 FET. The PWM collects the power from the previous part and creates the frequency to control the switch on and off fluently. The sawtooth signals are created at pin 3, there frequency is defined by R10 and C7. Then they are compared and modified with the

signal at pin 9, pin 11 to 14, and provide the final signal connected to Gate. When the final signal of PWM is transmitted to Buck converter, there are 2 resistor which help to drive down the current go into the main circuit by voltage divider.

- At buck converter: the signal is sent to the buck converter when the MOSFET is on. At first, the initial signal is kept stable by the snubber circuit. The inductor limits the current runt through it. It is charging when the MOSFET on, and discharge when the switch off that construct the loop. At the output, there are 2 capacitors which filter out the output signal to less ripple. Especially, R7 is the protection when the circuit overcurrent by turning off the switch immediately.

4 Circuit Calculation

4.1 Upper circuit

a. Input Voltage (V_{rect})

- We got V_{AC} after transformer about $12\sqrt{2}$ V, then this signal went through the full-bridge rectifier which converts the AC signal into DC signal. Therefore, we get the V_{rect}:

$$V_{rect} = V_{p\,(AC)} - 2 \times V_D = 12\sqrt{2} - 1.4 = 15.57\ (V)$$

b. Input capacitor and Bypass capacitor (C_1 & C_2 & C_4)

- The input capacitor helps the V_{rect} signal almost DC with a little bit with ripple. There is the equation of the ripple voltage at input which relates with the input voltage:[1]

$$\Delta V_{IN} = \frac{(1 - \frac{V_{out}}{V_{in}}) \times I_{o\,MAX} \times V_o}{C_{in} \times f_{switch} \times V_{in}} + \left(1 - \frac{V_{out}}{V_{in}}\right) \times I_{o\,MAX} \times ESR_{MAX}$$

$$= \frac{(1 - \frac{3.3}{15.57}) \times 1 \times 3.3}{C_{in} \times 100 \times 10^3 \times 15.75} + \left(1 - \frac{V_{out}}{15.75}\right) \times 1 \times ESR_{MAX}$$

(ESR is the constant value)

If we want to minimize the ripple voltage, we should increase the value of the input capacitor, because they inverse proportion. Base one Lab 4, which DC input voltage equals to 15V, is chosen 2200 uF filter capacitor; hence, in this project, we use the same value with the capacitor in Lab4 (C1 = 2200 uF).

- The bypass capacitors are added at input and output to reduce the AC noise. Because our circuit has 50k Hz, the noise not that much, so we chose the small value for all bypass capacitor to filter it. ($C_2 = C_4 =$ 0.01 uF). [4] [6]

c. Resistors at Gate (R_1 & R_5)

- There are 2 resistors which connect between the Source pin and Gate pin of the MOSFET. These effect on the signal of the MOSFET that can be more stable by reduce the voltage from the PWM into the MOSFET with divide the voltage go through 2 resistors. Depend on the datasheet of IRF9Z34 MOSFET [2], we got the range of voltage at Gate (-20 V < V_{Gate} < 20 V) which represent for the output of these 2 resistor, and the input equal to the VDC (15.57 V).

Voltage divider: $$V_{Gate} = \frac{R_5}{R_5 + R_1} \times V_{DC}$$

$$10\ V = \frac{R_5}{R_5 + R_1} \times 15.75\ V \text{ (choose } V_{Gate} = 10 \text{ V)}$$

We choose $R_5 = 6800\ \Omega$; therefore, $R_1 = 3900\ \Omega$. The higher resistors we select, the lower current run through the Gate.

d. Snubber circuit (C_5 & R_2)

- Snubber circuit is used to eliminate the high-frequency noises and spike of voltage [5]. In figure.... We can see that the waveform contains noise and spike. When we add a Cs (C5) = 10nF (small capacitor is usually used to handle high frequency [5]), the spike nearly disappears. Then we used some equations to calculate the remain value of the snubber circuit: [5]

$$C = \frac{Cs}{3} = 3.3 \times 10^{-9}(F)$$

$$Z = Rs\,(R2) = \sqrt{\frac{L}{Cs}} = \sqrt{\frac{\frac{1}{(2\pi fr)^2 \times C}}{Cs}}$$

$$\Rightarrow Cs = 56\,(\Omega).$$

Then we choose Rs = 56Ω.

e. Output capacitor (C_4)

- The output capacitor acts like the filter to filter out any ripple voltage of the output signal. By some research, we found out the formular to collect the value of the output capacitor: [3]

$$C_o = \frac{(V_{in} - V_{out}) \times V_{out} \times T^2}{8 \times \Delta V_o \times V_{in} \times L}$$

$$= \frac{(15.75 - 3.3) \times 3.3 \times \left(\frac{1}{100 \times 10^3}\right)^2}{8 \times \Delta V_o \times 15.75 \times 100 \times 10^{-6}}$$

Therefore: $$\Delta V_o = \frac{(15.75 - 3.3) \times 3.3 \times \left(\frac{1}{100 \times 10^3}\right)^2}{8 \times C_o \times 15.75 \times 100 \times 10^{-6}}$$

The requirement asks us to minimize the ripple output voltage below 2%:

$$\Rightarrow \frac{(15.75 - 3.3) \times 3.3 \times \left(\frac{1}{100 \times 10^3}\right)^2}{8 \times C_o \times 15.75 \times 100 \times 10^{-6}} < 2\%$$

⇨ $C_o > 0.1625$ uF.

To lessen the ripple output voltage, we choose 2200uF which is higher than 0.1625 uF.

f. Feedback resistors (R3 & R6)

- Because the pin 1 (INV) and pin 2 (NI) of the IC chip is the input of an error amplifier in the chip which is used to adjust the signal (increase or decrease) to give a stable signal. If the difference or error in voltage occurs. V_{INV} (V_{IN-}) equals to V_{NI} (V_{IN+}) = 2.5V and the expectation voltage at output is 3.3V. so we can apply voltage divider to find the value of R3 and R6.

$$V_{IN-} = \frac{R6}{R3 + 6} \times V_{OUT}$$

$$\Leftrightarrow 2.5 \times R3 + 2.5 \times R6 = 3.3 \times R6$$

$$\Rightarrow R3 = 0.32 \times R6.$$

If we choose the value R3 is 1.5kΩ, the value of R6 is 4.687kΩ. Then we choose the value of R6 is 4.7kΩ.

4.2 Feedback control unit (PWM chip – LM3542)

a. The oscillator frequency (R10 & C7)

- Since the required switching frequency is approximately 100 kHz. And it is set by the components R10 and C7. Then we have an equation: [3]

$$f_{OSC} = \frac{1}{R_T C_T} \Leftrightarrow f_{OSC} = \frac{1}{R_{10} C_7}$$

$$\Rightarrow 100 \times 10^3 \approx \frac{1}{R_{10} C_7}$$

We choose the value of R_{10} is 1kΩ, then the value of C_7:

$$100 \times 10^3 \approx \frac{1}{1k\Omega \times C_7} \Rightarrow C_7 \approx 0.01\mu\text{F}.$$

So C_7 = 0.01µF is chosen.

b. The resistors at pin 2 (R8 & R9)

- From the project description, the reference voltage (pin 16) is 5V and at Pin 2 of LM3524DN which, is Non-inverting (IN+), is normally set to achieve a 2.5V. So, we can apply voltage divider to find resistors R8 & R9:

$$V_{IN+} = \frac{R9}{R9 + R8} \times V_{REF}$$

$$\Leftrightarrow 2.5 = \frac{R9}{R9 + R8} \times 5$$

$$\Leftrightarrow 2.5 \times R9 + 2.5 \times R8 = 5 \times R9$$

$$\Rightarrow R8 = R9.$$

We choose the value of R8 and R9 is 5000Ω like datasheet of LM3524. However, there is no 5000Ω resistor in our school, 4700Ω resistor is chosen.

c. Protection circuit (R11 & C6)

Based on the datasheet of the LM3524DN chip, at pin 9 – compensation. The value of capacitor (C6) is 0.001µF and resistor (R11) is 50kΩ. In our circuit we chose according to datasheet C6 is 0.001µF and R11 is 47kΩ (because 50kΩ is not available in our school and the nearest value is 47kΩ). The reason we choose value from datasheet is it's reliable and it has been tested many times by professionals. [3]

d. Bypass capacitor (C8)

- In order to mitigate the effect of a localized fluctuation of the voltage rails supplying the chip, we use a small capacitor to guarantee the stability of the chip's supply voltage. The value of it is 0.01µF. [4] [6]

RESISTOR (Ω)

R1	3900
R5	6800
R2	56
R7	0.1
R3	1500
R6	4700
R8	5000
R9	5000
R10	1000
R11	50000

CAPACITOR (F)

C1	2200 u
C2	0.01 u
C5	3.3 p
C3	2200 u
C4	0.01 u
C6	0.001 u
C7	0.01 u
C8	0.01 u

5 Measurement and Results

5.1 Oscillator output at pin 3, switching frequency at pin 12, protection circuit at pin 9 and snubber circuit.

- Figure 9 show the frequency, that the IC chip created, is nearly 100kHz. And it meets the requirement which require to create 100kHz frequency.
- Figure 10 show the saw-tooth waveform with the frequency is about 86kHz. And the switching frequency is fixed.
- The result of protection circuit is shown in figure 8. We can see the switch stopped when it is overloaded.
- As we can see in figure 11 and 12, it shows that the spike in the waveform is smaller and almost disappeared by applying C5 and R2

5.2 Output voltage and output voltage ripple

According to figure 3, 5, 7 which show output signal of light load (66Ω - 50mA), medium load (10Ω - 330mA) and rated load (3.3Ω - 1000mA).

- We can see that as light load is applied, the output voltage is approximately 3.3V. When the medium load is applied, the voltage decreases to 2.5V. The output voltage is 0.9V as the rated load is applied. According to Watt's Law:

$$I = \frac{P}{V}$$

  The power P is constant because we use one 18V AC for all load, current I and voltage V is inverse proportion. So, as the current load increases, the voltage decrease. For 66Ω load, the current run through circuit is small, the effect of voltage drop does not happen. For 10Ω and 3.3Ω load, the current become bigger, then the output voltage drops.

- When the load resistor decreases, the voltage ripple decrease. Overall, the voltage ripple is successfully minimized (ripple voltage of all load below 150mA) by appropriate selection of the compensation values and the filter capacitors.

6 Conclusion

In conclusion, we can state that our Pulse Width Modulated Switching Voltage Regulator circuit worked as expected. It produces 3.3VDC output at the maximum load 1A. The circuit produce a very small ripple voltage (all load below 150mA). The snubber circuit has eliminated the spike in the waveform. Over current protection circuit keep the circuit safe from overloaded which is shown in the demonstration section. However, in case of medium load and full load, the output voltage does not reach 3.3V. Due to the Watt's Law, the higher load, the smaller voltage.

There are things that interesting and useful that we found in this course.

- The process to transform AC to desired DC signal.
- How to reduce ripple voltage by bypass capacitor.
- How to control the IRF9Z34 MOSFET by using a PWM IC LM3524.
- Understanding the behaviour of IC, snubber circuit, over current protection circuit.

7 References

[1] "Capacitor Calculation for Buck converter IC", *Rohmfs.rohm.com*, 2021. [Online]. Available: http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/capacitor_calculation_appli-e.pdf. [Accessed: 26- Jan- 2021]

[2] "IRF9Z34 datasheet", *Vishay.com*, 2021. [Online]. Available: https://www.vishay.com/docs/91092/sihf9z34.pdf. [Accessed: 26- Jan- 2021]

[3] "LM3524D datasheet", *Datasheetspdf.com*, 2021. [Online]. Available: https://datasheetspdf.com/pdf-file/49876/NationalSemiconductor/LM3524D/1?fbclid=IwAR2twc1hBC2dAoq51RF4k_AnbdnsWCo_KboeiqkeUp9uDfVQ-Sc2_HzK3kE. [Accessed: 26- Jan- 2021]

[4] "What is a Bypass Capacitor?", *Learningaboutelectronics.com*, 2021. [Online]. Available: http://www.learningaboutelectronics.com/Articles/What-is-a-bypass-capacitor.html. [Accessed: 26- Jan- 2021]

[5] 2016. "Snubber Circuit For Buck Converter IC". [pdf] ROHM.com, p.5. Available at: http://rohmfs.rohm.com/en/products/databook/applinote/ic/power/switching_regulator/buck_snubber_app-e.pdf [Accessed 26 January 2021].

[6] "Decoupling Techniques", Analog.com. [Online]. Available: https://www.analog.com/media/en/training-seminars/tutorials/MT-101.pdf. [Accessed: 26- Jan- 2021].

8 Appendix

8.1 66Ω load resistor (50mA)

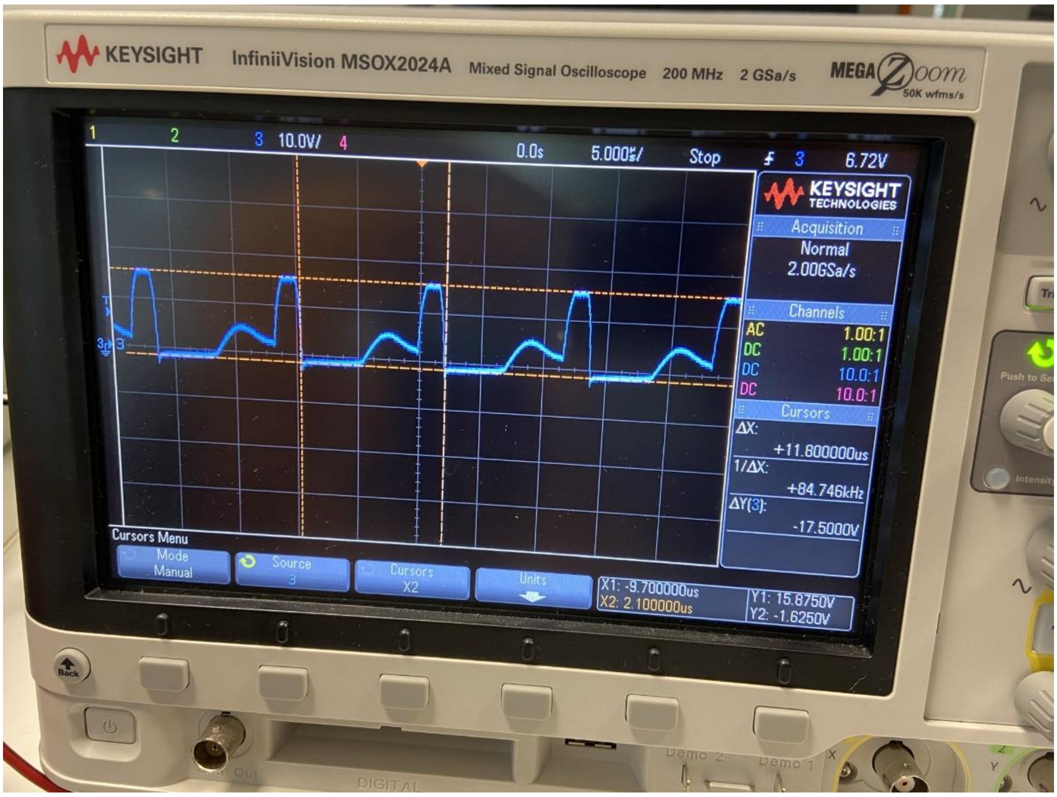

Figure 2: Voltage on the node where Q1, D3, and L1 meet.

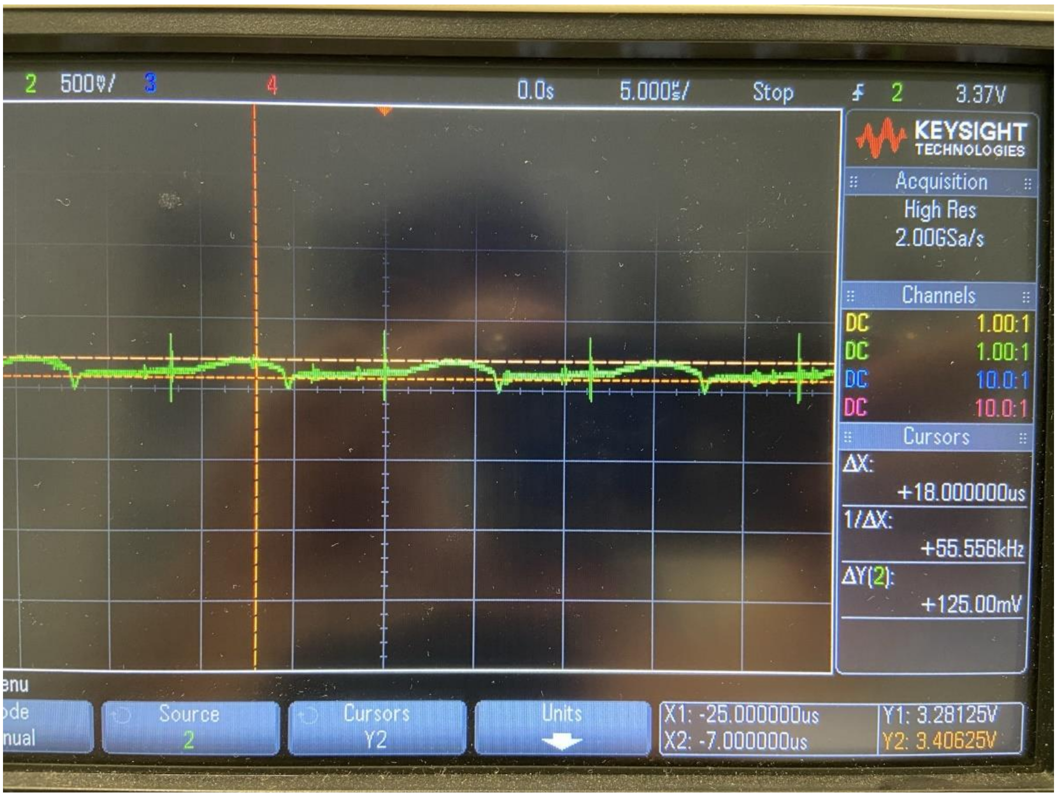

Figure 3: Voltage at 66 ohms load resistor.

8.2 10Ω load resistor (330mA)

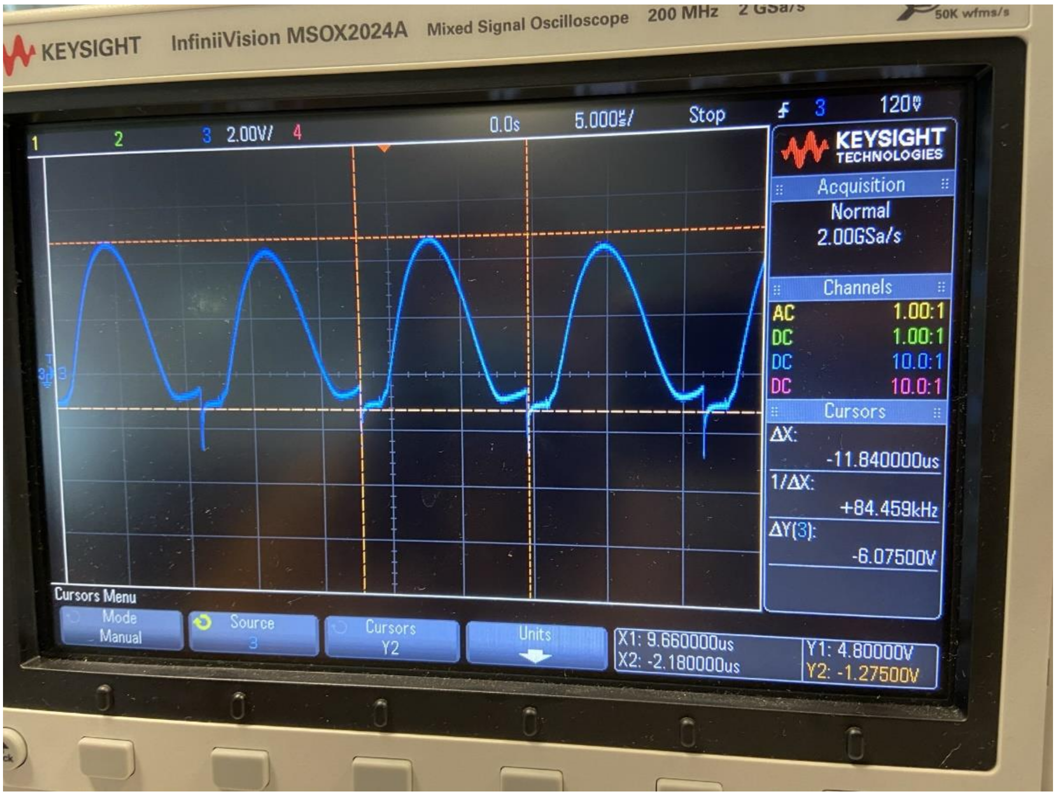

Figure 4: Voltage on the node where Q1, D3, and L1 meet.

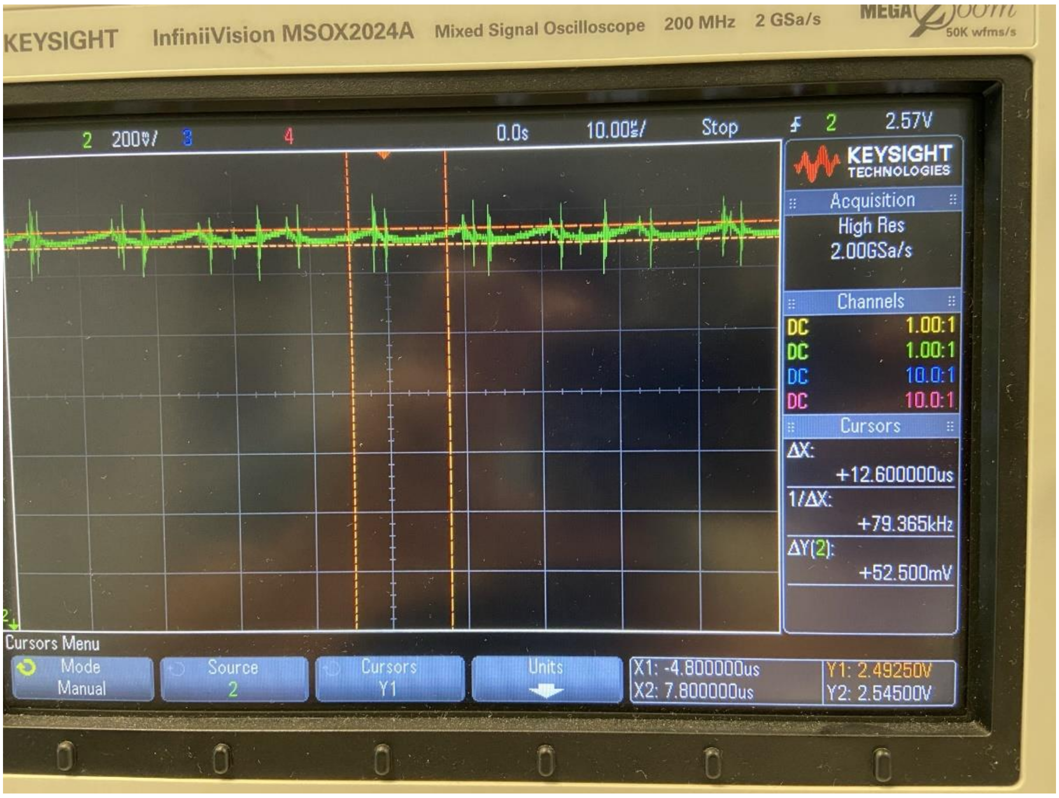

Figure 5: Voltage at 10 ohms load resistor.

8.3 3.3Ω load resistor (1000mA)

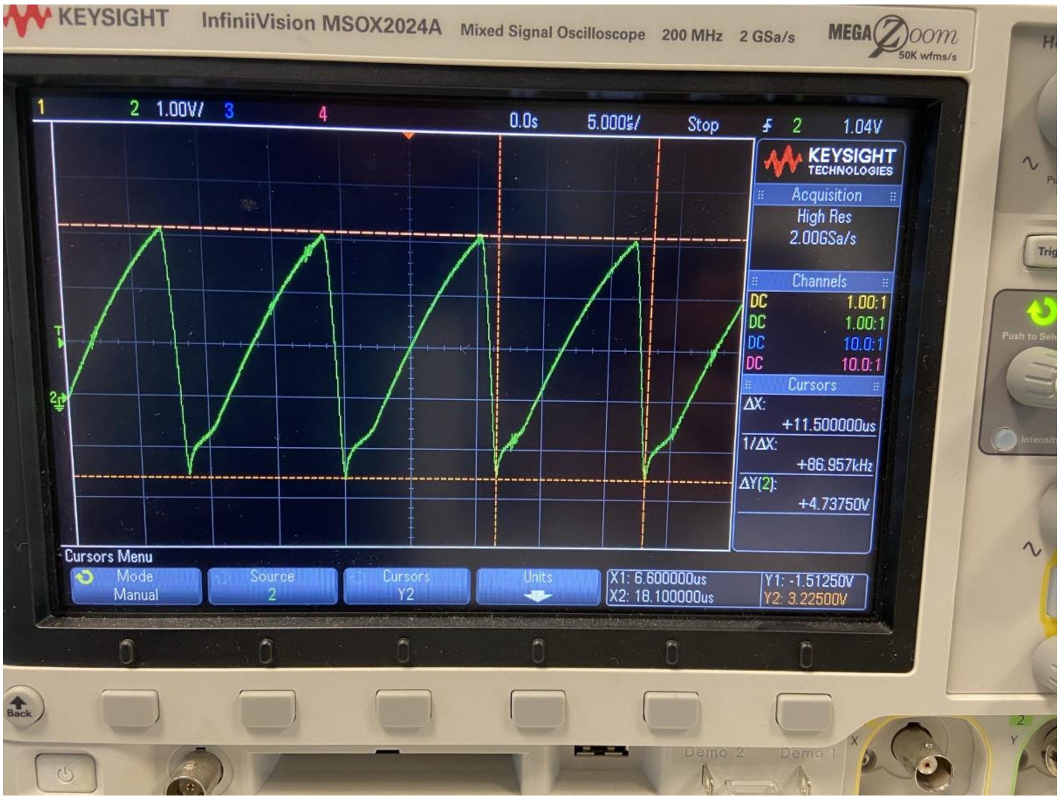

Figure 6: Voltage on the node where Q1, D3, and L1 meet.

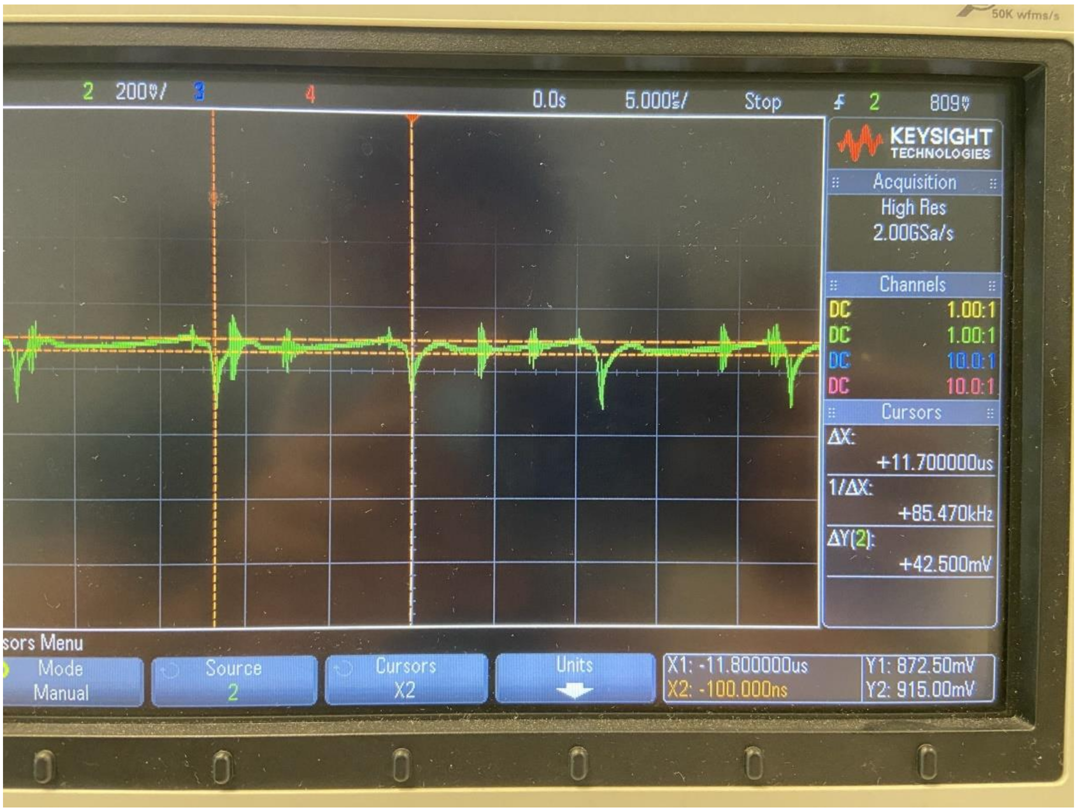

Figure 7: Voltage at 3.3 ohms load resistor.

8.4 0.1Ω load resistor (>2A) to test overloaded case

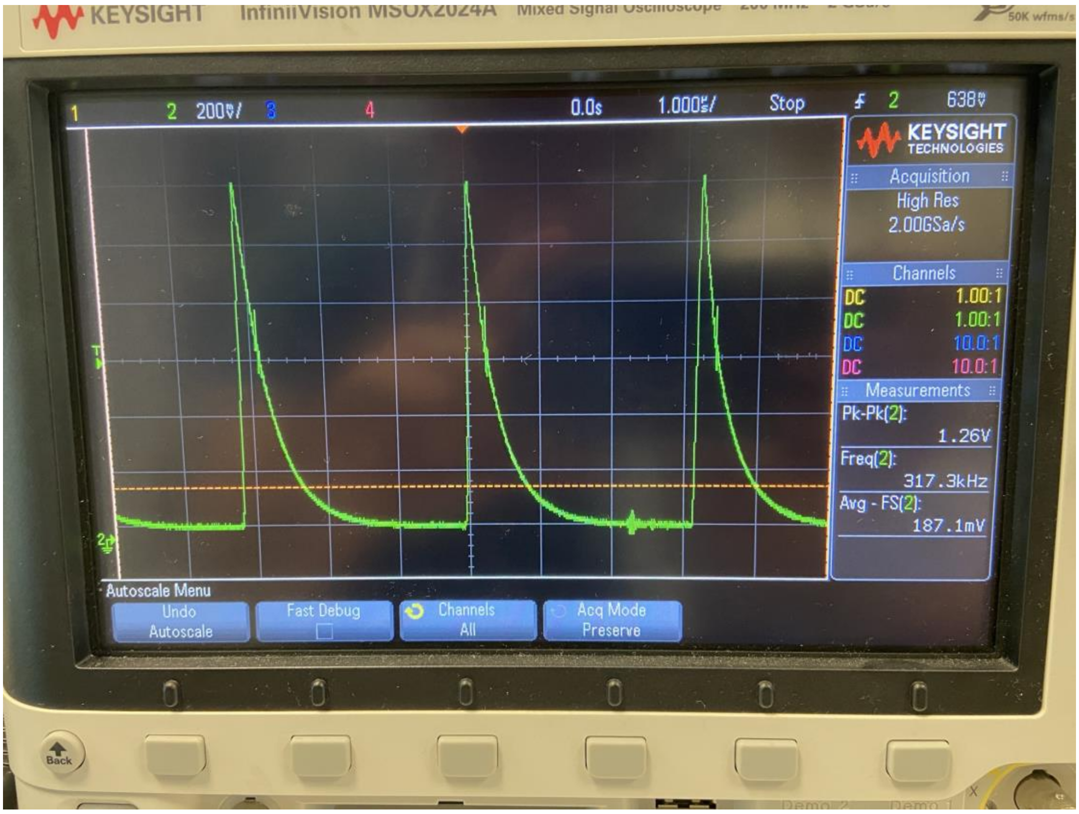

Figure 8: switching frequency of 0.1ohm load.

8.5 Oscillator output (pin 3) and switching frequency (pin 12) of IC

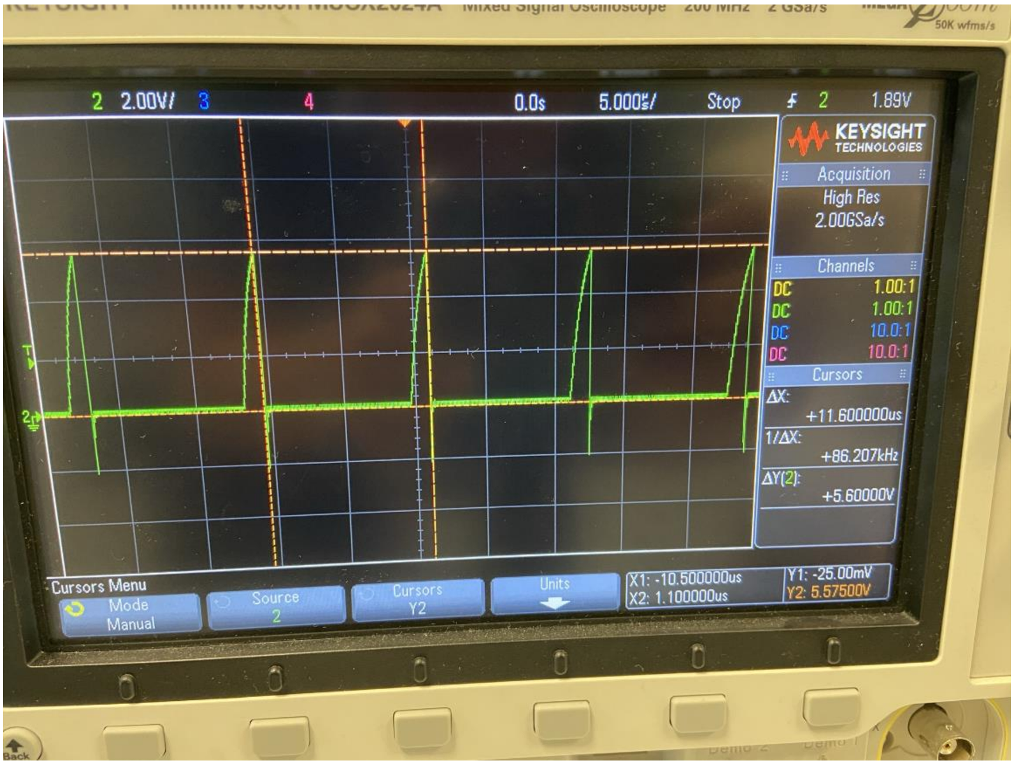

Figure 9: Oscillator output at pin 3 of LM3524 chip.

Figure 10: Switching frequency at pin 12.

8.6 Snubber circuit

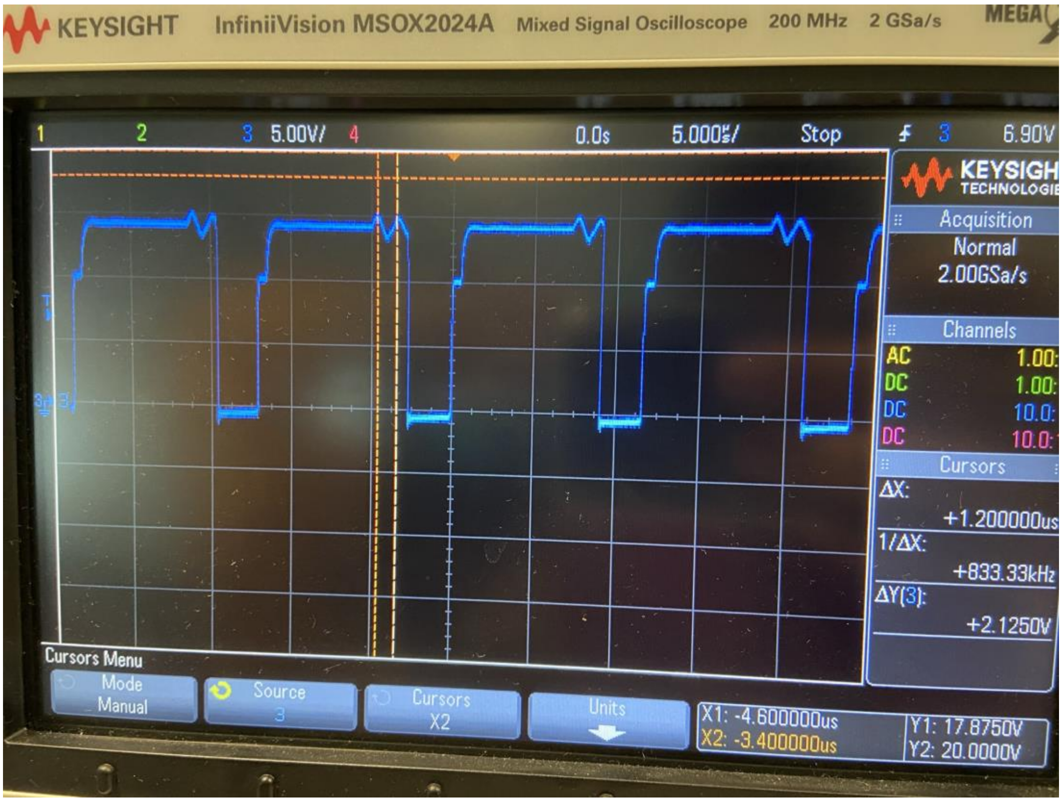

Figure 11: The waveform before adding snubber circuit.

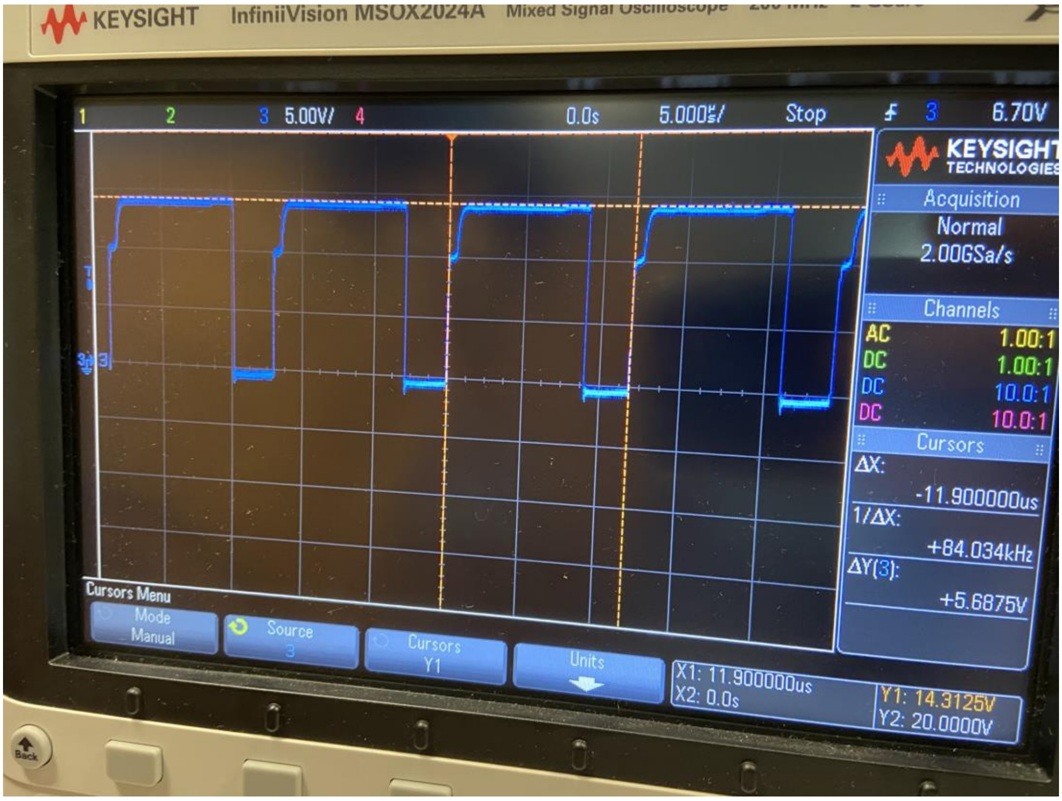

Figure 12: The waveform after adding snubber circuit.