數位電路設計 課號-1173, Spring 2021

Digital Circuit Design – Midterm II

1. (20%) Finish the uncompleted logic diagram of 4-bit carry lookahead adder (CLA) design as shown in Fig. 1, where the PFA denotes partial full adder. Please answer the following items:

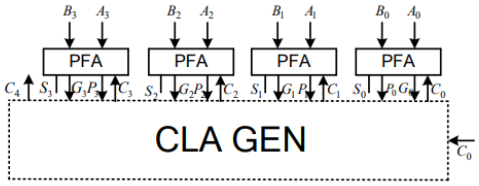



Fig. 1. Uncompleted 4-bit carry lookahead adder.

(a) (4%) Show Boolean functions of carry propagate $P_0$, $P_1$, $P_2$, $P_3$ and carry generate $G_0$, $G_1$, $G_2$, $G_3$.

(b) (4%) Show Boolean functions of the carry-out bits $C_1$, $C_2$, $C_3$, $C_4$ and sum $S_0$, $S_1$, $S_2$, $S_3$ in terms of carry propagate and carry generate functions of (a).

(c) (6%) Complete the block diagram of 4-bit carry lookahead adder (CLA) using AND, OR, XOR gates only.

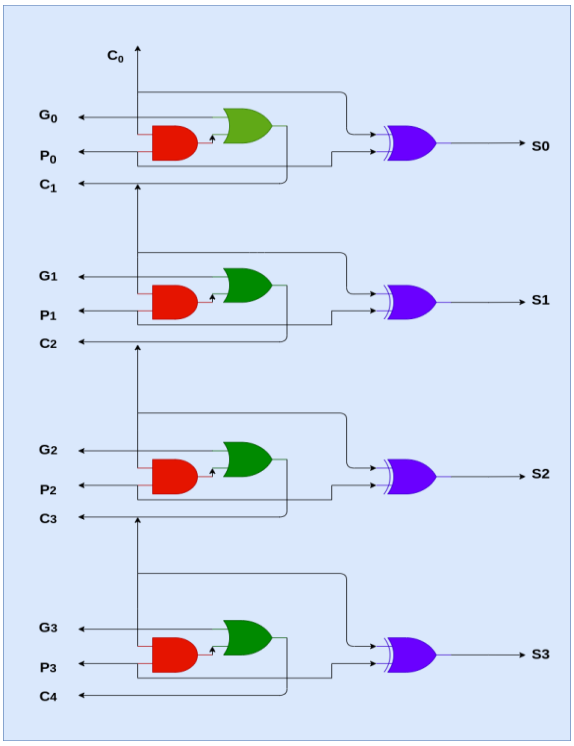
(d) (6%) Given delays of AND, OR, XOR gates with 2ut, 3ut, and 6ut, respectively, please calculate the propagation delay of 4-bit CLA.

1.

a) $P_i = A_i \oplus B_i$ and $G_i = A_i * B_i$

b) $S_i = P_i \oplus C_i$ and $C_{i+1} = G_i + P_i C_i$

**C) Block diagram of 4-bit carry look ahead adder (CLA)**




**d) 21 ut or 17 ut**

2. (16%) A BCD-to-seven-segment decoder is a combinational circuits that converts a decimal digit in BCD to an appropriate code for the selection in an indicator used to display the decimal digit in a familiar form. The seven outputs of the decoder (a, b, c, d, e, f, g) select the corresponding segments in the display, as shown in Fig. 2(a). The numeric display chosen to represent the decimal digit is shown in Fig. 2(b). Please answer the following questions.
(a) (5%) Show the truth table for input {A, B, C, D} and output {a, b, c, d, e, f, g}.
(b) (5%) Using a truth table and K's maps, show Boolean equations of the BCD-to-seven-segment decoder.
(b) (6%) Using a truth table and K's maps, depict the logic diagrams of the corresponding Boolean equations of the BCD-to-seven-segment decoder using NAND-NAND two-level stages with a minimum number of gates.


Fig. 2. (a) segment designation and (b) numerical designation for display.

(a)

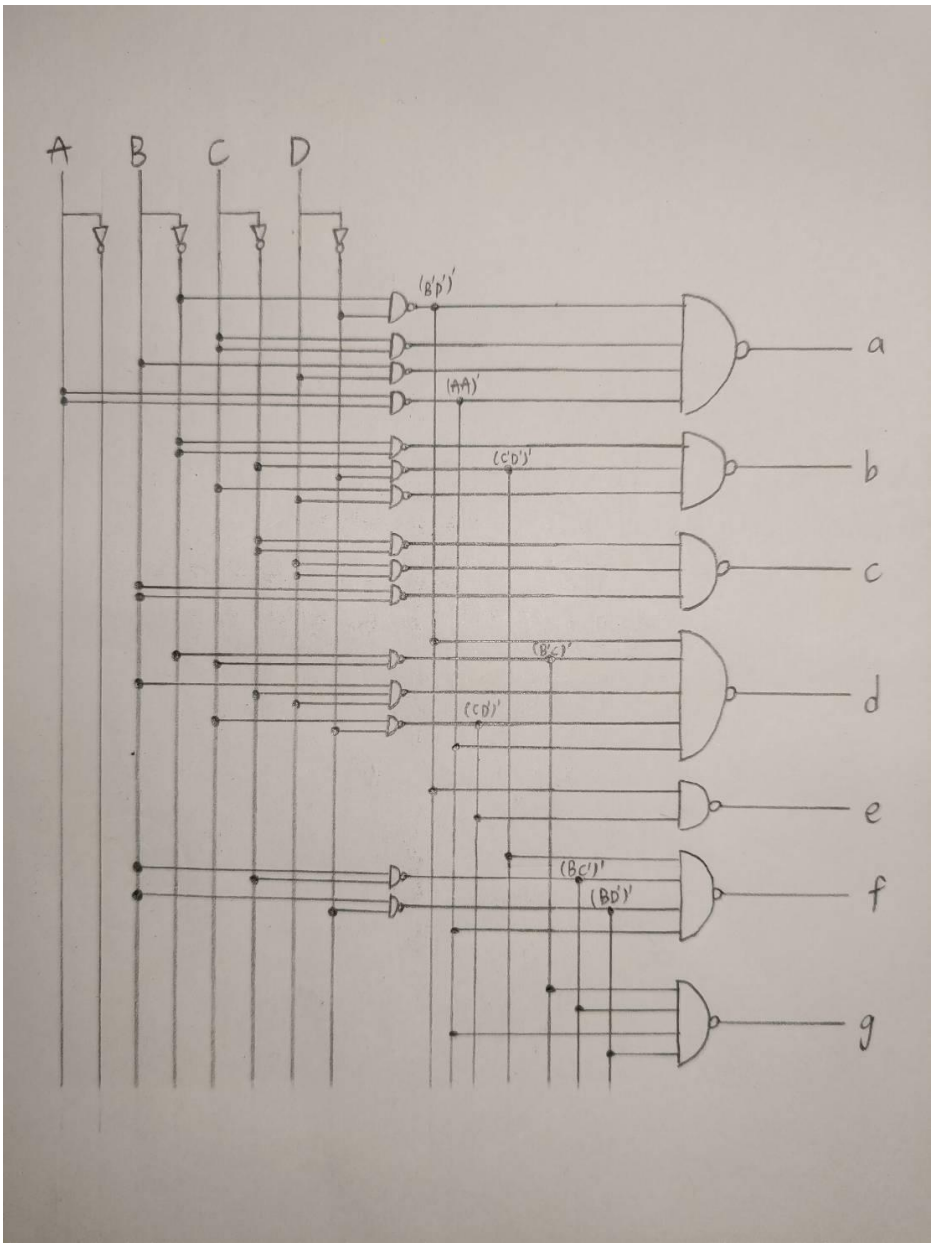
| Inputs | | | | Outputs | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| A | B | C | D | a | b | c | d | e | f | g |
| 0 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 |
| 0 | 0 | 0 | 1 | 0 | 1 | 1 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 |
| 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 1 |
| 0 | 1 | 0 | 0 | 0 | 1 | 1 | 0 | 0 | 1 | 1 |
| 0 | 1 | 0 | 1 | 1 | 0 | 1 | 1 | 0 | 1 | 1 |
| 0 | 1 | 1 | 0 | 1 | 0 | 1 | 1 | 1 | 1 | 1 |
| 0 | 1 | 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 |
| 1 | 0 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 1 | 1 |
| 1 | 0 | 0 | 1 | 1 | 1 | 1 | 1 | 0 | 1 | 1 |
| 1 | 0 | 1 | 0 | X | X | X | X | X | X | X |
| 1 | 0 | 1 | 1 | X | X | X | X | X | X | X |
| 1 | 1 | 0 | 0 | X | X | X | X | X | X | X |
| 1 | 1 | 0 | 1 | X | X | X | X | X | X | X |
| 1 | 1 | 1 | 0 | X | X | X | X | X | X | X |
| 1 | 1 | 1 | 1 | X | X | X | X | X | X | X |

(b)

a. B'D' + C + BD + A
b. B' + C'D' + CD

c. C' + D + B
d. B'D' + B'C + BC'D + CD' + A
e. B'D' + CD'
f. C'D' + BC' + BD' + A
g. B'C + BC' + A + BD'

(c)



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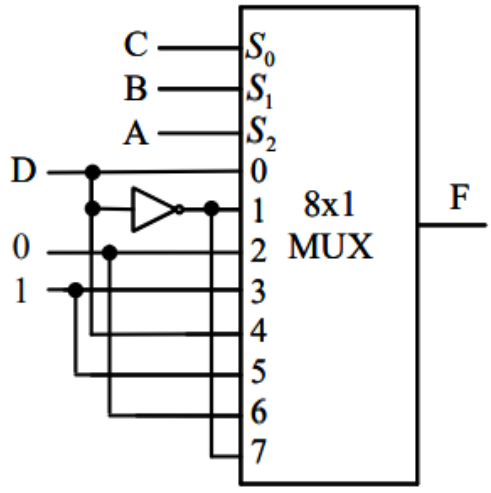
3. According the following truth table, use MUX based scheme to implement the Boolean function: F(A, B, C, D) =Σ(1, 2, 6, 7, 9, 10, 11, 14). For example, the block diagram of function F is revealed in Fig. 3 while an 8x1 MUX is applied to implement the truth table. (Per gate incorrect -2)

Multiplexer 8x1

| No | Inputs | | | | Outputs | AB Condition |
|---|---|---|---|---|---|---|
| | A | B | C | D | F | |
| 0 | 0 | 0 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | F=D |
| 2 | 0 | 0 | 1 | 0 | 1 | |
| 3 | 0 | 0 | 1 | 1 | 0 | F=D' |
| 4 | 0 | 1 | 0 | 0 | 0 | |
| 5 | 0 | 1 | 0 | 1 | 0 | F=0 |
| 6 | 0 | 1 | 1 | 0 | 1 | |
| 7 | 0 | 1 | 1 | 1 | 1 | F=1 |
| 8 | 1 | 0 | 0 | 0 | 0 | |
| 9 | 1 | 0 | 0 | 1 | 1 | F=D |
| 10 | 1 | 0 | 1 | 0 | 1 | |
| 11 | 1 | 0 | 1 | 1 | 1 | F=1 |
| 12 | 1 | 1 | 0 | 0 | 0 | |
| 13 | 1 | 1 | 0 | 1 | 0 | F=0 |
| 14 | 1 | 1 | 1 | 0 | 1 | |
| 15 | 1 | 1 | 1 | 1 | 0 | F=D' |



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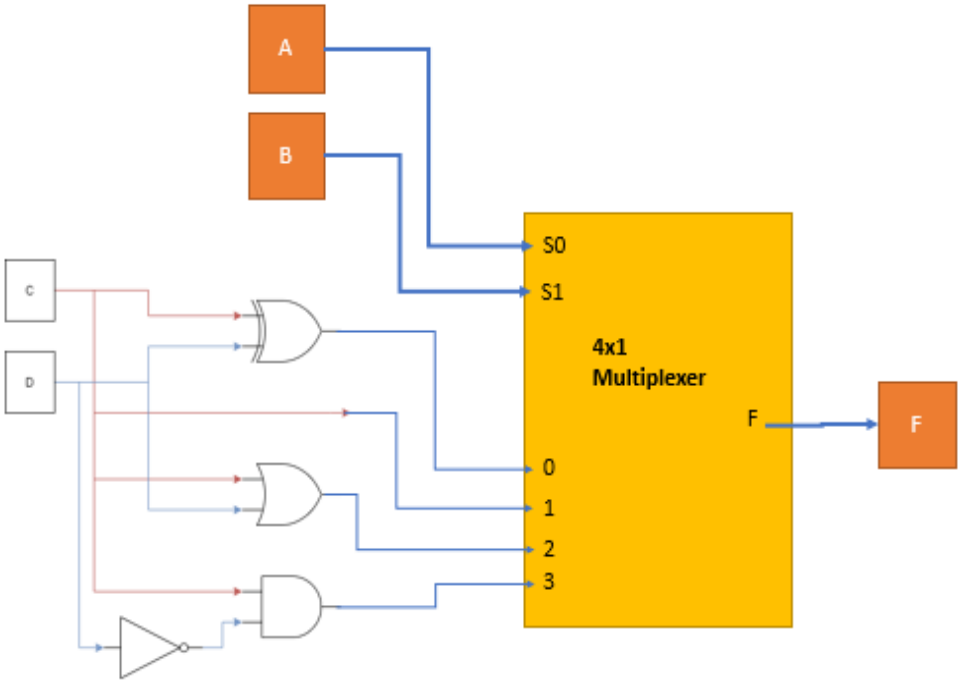
| No | Inputs | | | | Outputs | AB Condition |
|---|---|---|---|---|---|---|
| | A | B | C | D | F | |
| 0 | 0 | 0 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | |
| 2 | 0 | 0 | 1 | 0 | 1 | |
| 3 | 0 | 0 | 1 | 1 | 0 | F=C'D+CD' |
| 4 | 0 | 1 | 0 | 0 | 0 | |
| 5 | 0 | 1 | 0 | 1 | 0 | |
| 6 | 0 | 1 | 1 | 0 | 1 | |
| 7 | 0 | 1 | 1 | 1 | 1 | F=C |
| 8 | 1 | 0 | 0 | 0 | 0 | |
| 9 | 1 | 0 | 0 | 1 | 1 | |
| 10 | 1 | 0 | 1 | 0 | 1 | |
| 11 | 1 | 0 | 1 | 1 | 1 | F=D+C |
| 12 | 1 | 1 | 0 | 0 | 0 | |
| 13 | 1 | 1 | 0 | 1 | 0 | |
| 14 | 1 | 1 | 1 | 0 | 1 | |
| 15 | 1 | 1 | 1 | 1 | 0 | F=CD' |



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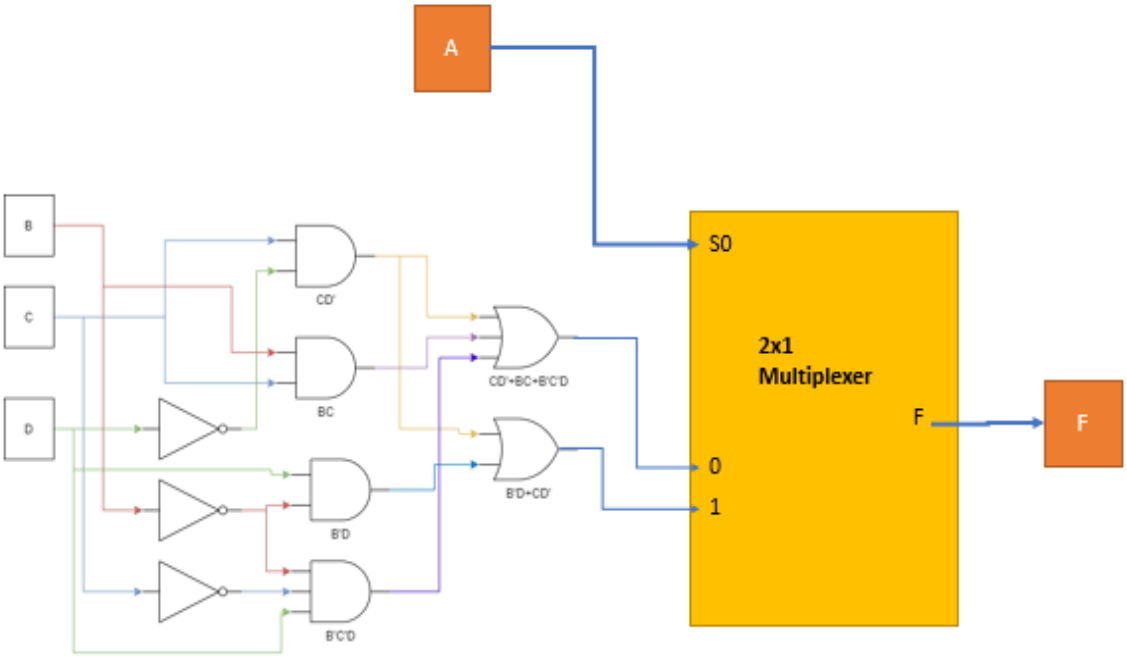
| No | Inputs | | | | Outputs | AB Condition |
|---|---|---|---|---|---|---|
| | A | B | C | D | F | |
| 0 | 0 | 0 | 0 | 0 | 0 | |
| 1 | 0 | 0 | 0 | 1 | 1 | |
| 2 | 0 | 0 | 1 | 0 | 1 | |
| 3 | 0 | 0 | 1 | 1 | 0 | |
| 4 | 0 | 1 | 0 | 0 | 0 | |
| 5 | 0 | 1 | 0 | 1 | 0 | |
| 6 | 0 | 1 | 1 | 0 | 1 | |
| 7 | 0 | 1 | 1 | 1 | 1 | F=CD'+BC+B'C'D |
| 8 | 1 | 0 | 0 | 0 | 0 | |
| 9 | 1 | 0 | 0 | 1 | 1 | |
| 10 | 1 | 0 | 1 | 0 | 1 | |
| 11 | 1 | 0 | 1 | 1 | 1 | |
| 12 | 1 | 1 | 0 | 0 | 0 | |
| 13 | 1 | 1 | 0 | 1 | 0 | |
| 14 | 1 | 1 | 1 | 0 | 1 | |
| 15 | 1 | 1 | 1 | 1 | 0 | F=B'D+CD' |



4. Considering the block diagram of Fig. 4, please answer the following questions:

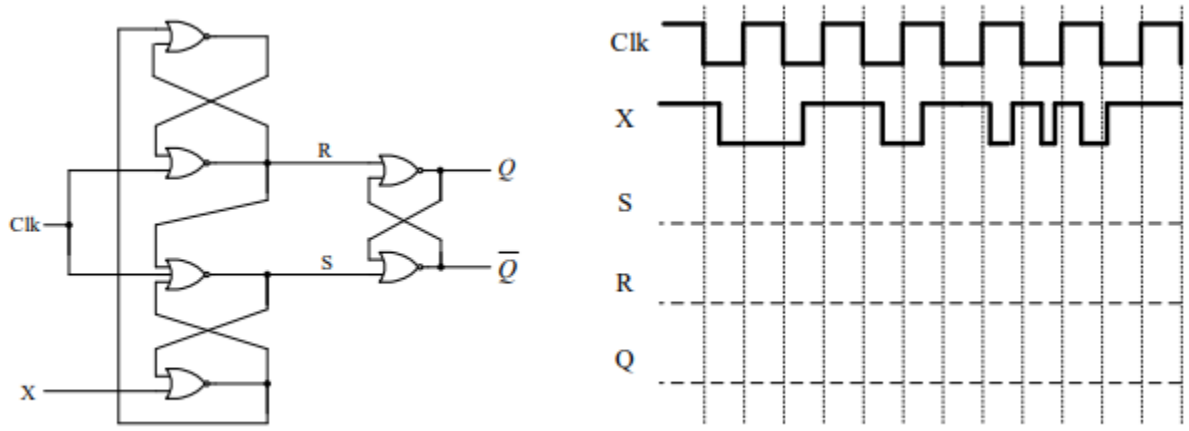
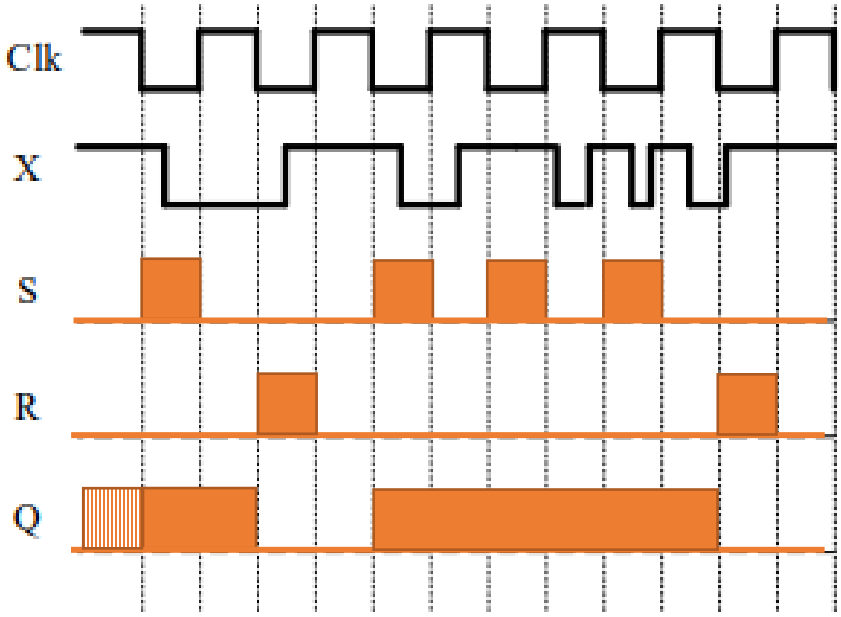



Fig. 4. (a) Block diagram and (b) timing diagram.

(a) (18%) According the block diagram of Fig. 4(a), finish the timing diagram in Fig. 4 *(18/8=2.25)*
*If too many minus but still have correct +2*




(b) (2%) Is it a latch or flip-flop? Must give some reasons.

**Flip flop because it need clock to operate, latch do not use clock to operate.**

(c) (2%) Is it positive level sensitive, negative level sensitive, positive edge trigger, or negative edge trigger?
**It is negative edge trigger**

# 5.

5. (28%) Design a sequence detector that can **detect a sequence of three or more consecutive 1s in a string of bits** coming through an input line. In this case, the detector output will be 1. Otherwise, the sequence detector output will be zero. Please answer the following questions.
   (a) (5%) Please show the state diagram and state table in Table 1, where the branch denotes input and the circle denotes state(**S**)/output(**Y**). Given the state assignment as follow: **$S_0$= AB=00, $S_1$= AB=01, $S_2$=AB=10, $S_3$=AB=11**.
   (b) (5%) Considering D flip-flop and applying the K-maps method to optimize the Boolean state functions and output equation **Y** in terms of input **X** and present state bits **A, B**, please write down the state equations (**$D_A$** and **$D_B$**) and output equation (**Y**) in terms of input and present states.
   (c) (5%) Depict the logic diagram for this sequential sequence recognizer using positive edge-trigger D flip-flops with "Positive Asynchronous Reset" and "CLK" signals, and combinational gates.
   (d) (5%) Considering JK flip-flop and applying the K-maps method to optimize the Boolean state functions and output equation **Y** in terms of input **X** and present state bits **A, B**, please write down the state equations (**$J_A$**, **$K_A$**, **$J_B$**, and **$K_B$**) and output equation (**Y**) in terms of input and present states.
   (e) (5%) Depict the logic diagram for this sequential sequence recognizer using positive edge-trigger JK flip-flops with "Positive Asynchronous Reset" and "CLK" signals, and combinational gates.
   (f) (3%) Does the circuit belong to Mealy machine or Moore machine? Please must give reasons.

Table 1 of Problem 5

| Present State | | Input | Next State | | Output |
|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | *y* |
| 0 | 0 | 0 | | | |
| 0 | 0 | 1 | | | |
| 0 | 1 | 0 | | | |
| 0 | 1 | 1 | | | |
| 1 | 0 | 0 | | | |
| 1 | 0 | 1 | | | |
| 1 | 1 | 0 | 0 | 0 | |
| 1 | 1 | 1 | 1 | 1 | |

(a)

答案有兩種， y 最後三個是 011 or 101。

State diagram 自己畫

5%) Depict the logic diagram for this sequential sequence recognizer using positive edge-trigger JK flip-flops with "Positive Asynchronous Reset" and "CLK" signals, and combinational gates.

(3%) Does the circuit belong to Mealy machine or Moore machine? Please must give reasons.

Table 1 of Problem 5

| Present State | | Input | Next State | | Output |
|---|---|---|---|---|---|
| *A* | *B* | *x* | *A* | *B* | *y* |
| 0 | 0 | 0 | 0 | 0 | 0 |
| 0 | 0 | 1 | 0 | 1 | 0 |
| 0 | 1 | 0 | 0 | 0 | 0 |
| 0 | 1 | 1 | 1 | 0 | 0 |
| 1 | 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 1 | 0 or 1 |
| 1 | 1 | 0 | 0 | 0 | 1 or 0 |
| 1 | 1 | 1 | 1 | 1 | 1 |

The END

(b)

$D_A$ = Ax + Bx

$D_B$ = Ax + B'x

If 011, y = AB

If 101, y = Ax

(c)

自己畫

(d)

$J_A$ = Bx

$J_B$ = x

$K_A$ = x’

$K_B$ = A’+ x’

If 011, y = AB

If 101, y = Ax

(e)

自己畫

(f)

If 011 , y = AB , 輸出只看 state 不看 input , moore machine

If 101 , y = Ax , 輸出看 state 還看 input , mealy machine

**Iikm**