Midterm (II)

1. (20%) Finish the uncompleted logic diagram of 4-bit carry lookahead adder (CLA) design as shown in Fig. 1, where the PFA denotes partial full adder. Please answer the following items:

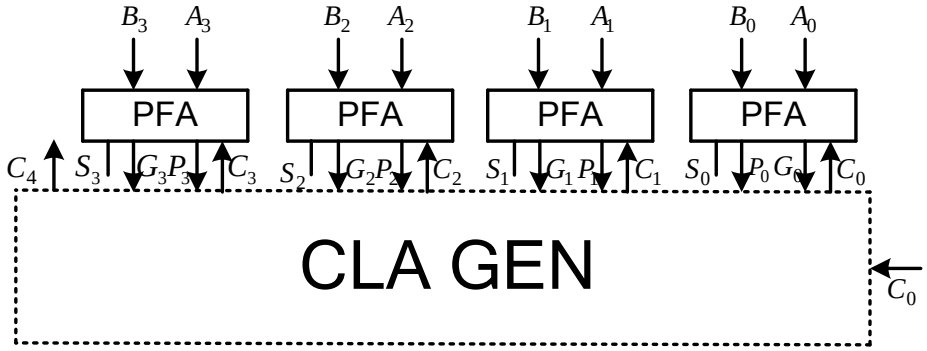

Fig. 1. Uncompleted 4-bit carry lookahead adder.

   (a) (4%) Show Boolean functions of carry propagate P_0, P_1, P_2, P_3 and carry generate G_0, G_1, G_2, G_3.

   (b) (4%) Show Boolean functions of the carry-out bits C_1, C_2, C_3, C_4 and sum S_0, S_1, S_2, S_3 in terms of carry propagate and carry generate functions of (a).

   (c) (6%) Complete the block diagram of 4-bit carry lookahead adder (CLA) using AND, OR, XOR gates only.

   (d) (6%) Given delays of AND, OR, XOR gates with 2ut, 3ut, and 6ut, respectively, please calculate the propagation delay of 4-bit CLA.

2. (10%) Design a full-subtractor circuit (i.e., logic diagram) with three inputs, *x*, *y*, B_{in}, and two outputs *Diff* and B_{out}. The circuit subtracts $x - y - B_{in}$, where B_{in} is the input borrow, B_{out} is the output borrow, and *Diff* is the difference.

   (a) (5%) show the truth table of a full-subtractor.

   (b) (5%) show the logic diagram of a full-subtractor.

3. (5%) According to the Verilog code in Fig. 2, please write down the state equation.

```
module X1X2_FF (input X1, X2, CLK, output reg Q, output Q_b);
assign Q_b = ~Q;
       always @ (posedge CLK)
       case ({X1, X2})
       2'b00: Q <= !Q;
       2'b01: Q <= 1'b1;
       2'b10: Q <= 1'b0;
       2'b11: Q <= Q;
       endcase
endmodule
```

Fig. 2. Verilog Code.

4. (15%) According to the truth table in Table 1, please use a MUX-based approach to implement the Boolean function: $F(A, B, C, D) = \Sigma(0, 4, 6, 7, 8, 9, 11, 14)$. For example, the block diagram of function ***F*** is revealed in Fig. 3 while an 8x1 MUX is applied to implement the Table 1.

Table 1: Truth Table

Inputs				Output
A	B	C	D	F
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	1
0	1	0	1	0
0	1	1	0	1
0	1	1	1	1
1	0	0	0	1
1	0	0	1	1
1	0	1	0	0
1	0	1	1	1
1	1	0	0	0
1	1	0	1	0
1	1	1	0	1
1	1	1	1	0

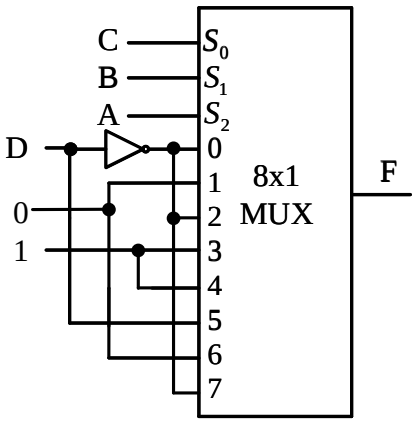

Fig. 3. Block diagram using 8x1 MUX.

(a) (7%) Using one 4x1 MUX and combinational gates to implement Table 1, please show the block diagram of function ***F***.

(b) (8%) Using one 2x1 MUX and combinational gates to implement Table 1, please show the block diagram of function ***F***.

5. (22%) Considering the block diagram of Fig. 4, please answer the following questions:

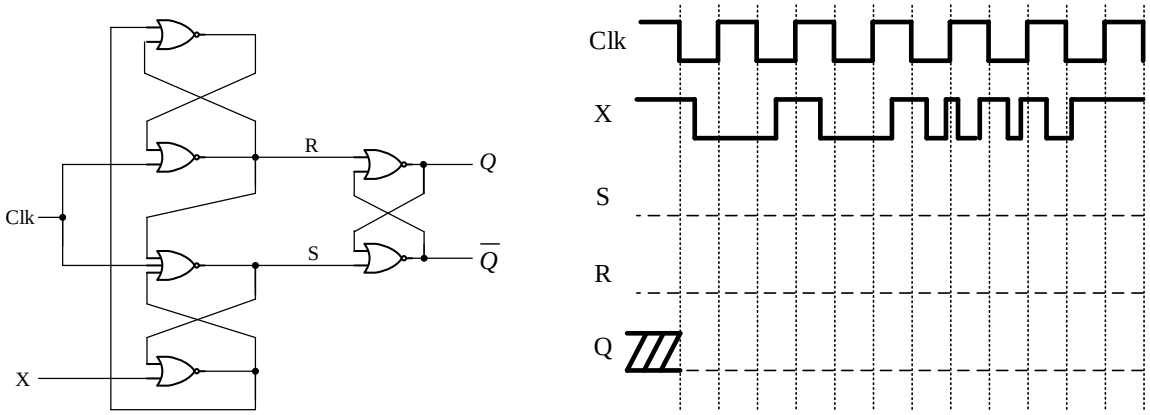

Fig. 4. (a) Block diagram and (b) timing diagram.

(a) (18%) According the block diagram of Fig. 4(a), finish the timing diagram in Fig. 4(b).

(b) (2%) Is it a latch or flip-flop? Please provide the reasons.

(c) (2%) Is the circuit positive level sensitive, negative level sensitive, positive edge trigger, or negative edge trigger?

6. (28%) Design a sequence detector that can **detect a sequence of three or more consecutive 1s in a string of bits** coming through an input line. In this case, the detector output will be 1. Otherwise, the sequence detector output will be zero. Please answer the following questions.
   (a) (5%) Please show the state diagram and state table in Table 2, where the branch denotes input and the circle denotes state(**S**)/output(**Y**). Given the state assignment as follow: **S_0= AB=00, S_1= AB=01, S_2=AB=10, S_3=AB=11**.
   (b) (5%) Considering D flip-flop and applying the K-maps method to optimize the Boolean state functions and output equation **Y** in terms of input **X** and present state bits **A, B**, please write down the state equations (**D_A** and **D_B**) and output equation (**Y**) in terms of input and present states.
   (c) (5%) Depict the logic diagram for this sequential sequence recognizer using positive edge-trigger D flip-flops with "Positive Asynchronous Reset" and "CLK" signals, and combinational gates.
   (d) (5%) Considering JK flip-flop and applying the K-maps method to optimize the Boolean state functions and output equation **Y** in terms of input **X** and present state bits **A, B**, please write down the state equations (**J_A**, **K_A**, **J_B**, and **K_B**) and output equation (**Y**) in terms of input and present states.
   (e) (5%) Depict the logic diagram for this sequential sequence recognizer using positive edge-trigger JK flip-flops with "Positive Asynchronous Reset" and "CLK" signals, and combinational gates.
   (f) (3%) Does the circuit belong to Mealy machine or Moore machine? Please must give reasons.

Table 2 of Problem 5

Present State		Input	Next State		Output
A	*B*	*x*	*A*	*B*	*y*
0	0	0			
0	0	1			
0	1	0			
0	1	1			
1	0	0			
1	0	1			
1	1	0	0	0	
1	1	1	1	1	

The END

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