ABSTRACT

This project report presents a refined design of a feature-rich digital clock system. The system integrates a conventional clock (with user-selectable 12-hour or 24-hour modes) alongside auxiliary functions: a programmable countdown timer (which activates an alarm at zero) and a stop-watch (count-up) mode. Timekeeping is implemented with cascaded JK flip-flop counters, and all outputs drive a multiplexed multi-digit seven-segment display. Input buttons for mode and time-setting are decoded via a demultiplexing scheme. The design was fully simulated to verify correct operation of all modes.

INTRODUCTION

Problem Statement

Timekeeping devices are an integral part of daily life, enabling individuals to manage schedules, track elapsed time, and coordinate activities. While basic digital clocks are readily available, their functionality is often limited to simple time display, and they lack multi-purpose features such as integrated alarms, timers, and stopwatches.

The absence of multifunctionality requires users to rely on multiple devices or applications, leading to inefficiencies in time management. In engineering terms, this presents a design gap: creating a single, compact, and energy-efficient system capable of handling multiple time-related tasks with a user-friendly interface.

Proposed Solution:
Design and implement a Multi-Functional Digital Clock using Logisim that integrates:

- Real-time clock display (hours, minutes, seconds)
- Multiple alarms
- Countdown timer
- Stopwatch
- 12-hour/24-hour display modes
- User interface for intuitive configuration through buttons and switches

The system should be modular, allowing incremental feature addition, and designed using synchronous digital logic principles for accuracy and reliability

DESIGN METHODOLOGY

Timekeeping Module

The timekeeping module serves as the core functional block of the digital clock, responsible for accurately tracking and updating the current time. Its design ensures precise counting of seconds, minutes, and hours while providing the necessary signals for display and mode control.

The main role of the timekeeping module is to:

- Receive a stable clock signal from the system's oscillator or clock divider.
- Increment time units in a cascading fashion (seconds → minutes → hours).
- Interface with the display control logic to present the current time.
- Support both normal clock mode and additional functionalities such as stopwatch or countdown timer (as per the system design).

The timekeeping module is implemented using **counters, multiplexers, and BCD-to-7 segment converters**, with cascading logic to ensure correct time progression.

a) Clock Division

- The incoming high-frequency clock signal (e.g., 50 MHz in FPGA systems) is divided down to a **1 Hz pulse** using a **clock divider circuit**.
- This 1 Hz signal represents **one second intervals** and serves as the timing reference for the entire module.

b) Seconds and Minutes counter schematic

- Once seconds reach 60, a carry pulses the **Minutes counter**, which has an identical structure (mod-10 followed by mod-6) to count 0–59. When minutes overflow at 60, the **Hours counter** increments. The hours logic uses a programmable modulus: in 24-hour mode it counts 0–23 (resetting at 24),. Each stage is a JK flip-flop configured as a divide-by-n counter: for instance, tying J=K=1 makes a toggle flip-flop (T-flip-flop). This modular JK-flip-flop design makes it easy to reuse circuits: additional gating and reset inputs implement the roll-over conditions.

d) Hour Counter

- The hour counter counts from 00 to 23 in **24-hour mode** (or from 01 to 12 in 12-hour mode with an AM/PM flag).

In 24-hour mode, once the counter reaches 24, it resets to 00

e) Zero Detection Logic

- The zero-detection logic is a combinational circuit that outputs a high signal when all counter outputs are zero.
- This is especially important in countdown mode, where the system must signal completion when time reaches 00:00:00.

Alarm Module

The alarm module alerts the user when a pre-set time is reached by comparing the current time with stored alarm values. The user sets the hours and minutes via push buttons or switches, which are stored in counters. An Alarm Enable control allows the alarm to be turned on or off without erasing the set time.

A comparator continuously checks the current and stored times; when they match, it sends a high logic signal through an AND gate with the Alarm Enable signal to trigger the alert. The output can drive a buzzer, LED, or both. Some designs include a timer to limit the alarm's duration, and the alarm can be silenced using the reset control or disabling the Alarm Enable.

Debouncing prevents false triggers, while memory retention preserves settings during power loss. Multiple alarms can be supported by adding more registers and comparators. Practical and reliable, the alarm module enhances the clock with precise time alerts and user-friendly controls

Countdown Timer Module

The countdown timer module measures a set duration in reverse, starting from a user-defined value and ending at zero—ideal for cooking, experiments, event reminders, and other timed tasks. The user enters the desired hours, minutes, or seconds via input controls, which are stored in preset registers. Once started, cascaded down-counters decrement in sync with one-second pulses from the system oscillator, borrowing from higher units when needed.

When all counters reach zero, the module triggers an alert—such as a buzzer or LED—to signal completion. Start, Pause, and Reset controls, along with debouncing circuitry, ensure smooth and accurate operation. Compact, precise, and easy to use, the countdown timer adds practical versatility to the digital clock system.

Stopwatch Module

The stopwatch module is a key feature of the digital clock system, measuring elapsed time from zero with high precision. Unlike a countdown timer, which runs from a preset value to zero, the stopwatch counts upward, making it ideal for sports, lab experiments, and other duration-tracking applications.

When the Start control is activated, the module resets its registers to zero and begins counting clock pulses from the system oscillator. These pulses pass through a frequency divider to produce a one-second signal, which drives cascaded up-counters for seconds, minutes, and hours. Each counter overflows into the next unit (e.g., 59 seconds → 1 minute), ensuring accurate long-term measurement.

The module supports Start, Stop, and Reset functions, with debouncing circuitry to prevent switch-bounce errors. A stable clock source, such as a crystal oscillator, maintains accuracy despite temperature or power variations. Advanced designs may include memory for lap or split times.

Overall, the stopwatch enhances the digital clock's versatility with precise, reliable, and user-friendly elapsed-time measurement

Display Multiplexing

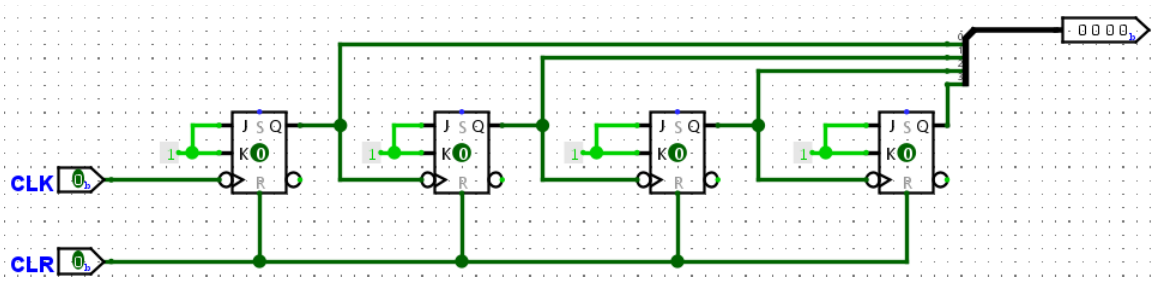
All digit outputs (hours, minutes, seconds, and stopwatch digits) share a **multiplexed display driver**. Instead of separate decoders for each digit, we use a multiplexer (or digital switch) to feed one BCD-to-7-seg decoder at a time. On each refresh cycle, the multiplexer selects the BCD outputs of a different digit block, and the decoder drives the seven segments. In practice, the circuit sequentially activates each digit's common pin (anode or cathode) in turn. As demonstrated in similar designs, "a multiplexer was used to take all the outputs from the counters and provide only one input to the seven-segment decoder… eliminating the need to use a separate seven-segment decoder for each output". This time-division multiplexing reduces hardware cost and power.

Button Input and Demultiplexing

To handle multiple user buttons (mode select, set, start/stop, etc.) with limited input lines, we employ a demultiplexer scheme. A demultiplexer takes one input line and routes it to one of many outputs based on select signals. In our design, each button is connected to an output of an n-to-1 decoder. The controller drives the decoder's address lines, which sequentially enable each output. When an output is enabled, pressing the corresponding button toggles the shared input line, allowing the microcontroller logic to poll each button in turn. This is analogous to how displays are scanned: for example, a 3-to-8 decoder can activate one digit of a 4-digit display at a time, except here it activates one button's circuit at a time. Using a demultiplexer lets us share a single input pin for multiple switches.

MODULAR JK FLIP-FLOP ARCHITECTURE

All of the above counters and timing circuits are constructed from modular JK flip-flop blocks. Each JK flip-flop can toggle or hold its output; by fixing J=K=1, the flip-flop toggles state on each clock pulse (functioning as a T-flip-flop). Cascading these in series yields a ripple binary counter: for instance, the $\overline{Q}$ output of the least significant bit is used as the clock input for the next bit. This ripple arrangement is simple to implement and demonstrated in many tutorials. For synchronous behavior, we can simultaneously clock all JK stages. We also include synchronous preset/clear lines so that on reaching terminal count (e.g. 60 seconds or 24 hours), all flip-flops reset together. This "modular design" approach simplifies debugging and reuse: each digit counter is a self-contained JK-flip-flop module with its own reset logic.



SIMULATION RESULTS

The design was implemented and tested in a digital logic simulator.. The 12/24-hour switch was verified by changing the counting modulus of the hour counter. In countdown mode, setting a preset time (e.g. 01:30) caused the display to decrement each second, and the alarm output asserted precisely when the count reached 00:00. In stopwatch mode, the counters incremented from 00:00 when “start” was pressed, and paused or reset as expected on button events. The multiplexed display correctly showed each digit (segmented at high speed), and no flicker was observed. Overall, the simulation confirmed that each subsystem (counters, multiplexer demultiplexer input scanning, and alarm trigger) functions as intended.

REAL-WORLD IMPLEMENTATION CONSIDERATIONS

4.1 Cost

- Using discrete ICs (counters, decoders, etc.) would be cost-effective for low-scale production but could be replaced by a microcontroller (e.g., ATmega328P) for integration and cost reduction at scale.

4.2 Power Consumption

- A CMOS-based design ensures minimal static power draw. Battery-powered implementation would require optimizing oscillator and display drivers.

4.3 Size

- FPGA or microcontroller-based designs would significantly reduce PCB footprint compared to discrete logic circuits.

4.4 Reliability

- In hardware, switch debouncing circuits and crystal oscillators ensure accuracy and long-term stability.

4.5 Interfacing

- Real-world versions could integrate USB for firmware updates or Bluetooth for mobile app synchronization.

CONCLUSION

We have presented a coherent digital clock design that integrates multiple timing functions in a single system. The clock supports both 12-hour and 24-hour formats and includes a countdown timer (with alarm) and a user-controlled stopwatch. Key design techniques include using cascaded JK flip-flop counters for timekeeping, a multiplexer to scan the shared seven-segment display, and a demultiplexer for efficient button handling. The modular JK flip-flop approach simplified the counter logic. Simulation results verified all features, showing accurate time-keeping and correct mode behavior. Future work could involve hardware implementation on an FPGA or discrete ICs, and adding more advanced features such as date display or multiple alarms.

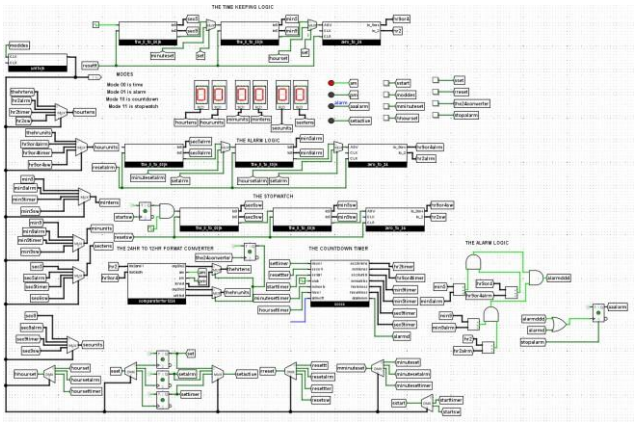
REFERENCES

1. Lessons in Electric Circuits, Vol. 3: Digital. AllAboutCircuits.com.
2. BCD to 7 Segment Decoder. GeeksforGeeks, 2024.
3. Mano, M. Morris. *Digital Design*. Pearson, 6th Edition, 2017.
4. Logisim Documentation, Carl Burch.
5. Floyd, Thomas L. *Digital Fundamentals*. Pearson, 11th Edition, 2015.

APPENDICES

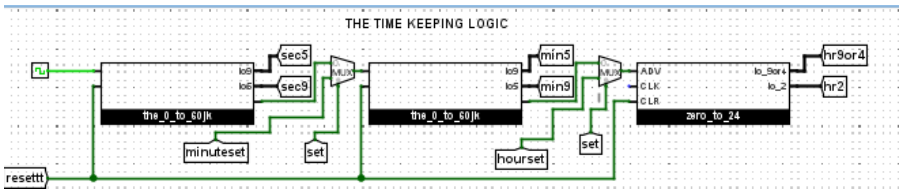
Appendix A – Full System Schematic

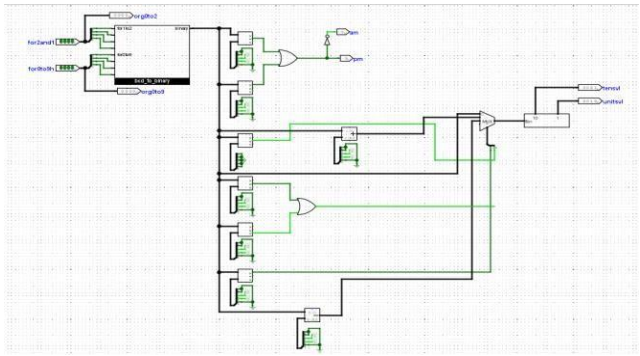
- Complete Logisim Evolution schematic of the integrated digital clock system, including timekeeping, stopwatch, countdown timer, alarm circuit, display multiplexing, and button demultiplexing.



Appendix B – Timekeeping Module Circuit Diagram

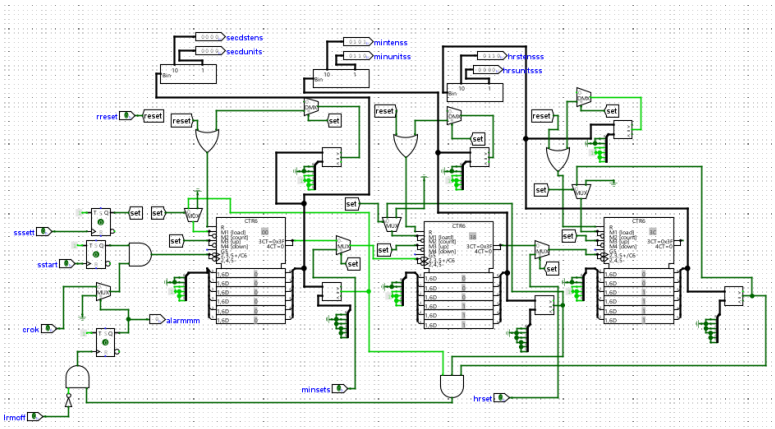
- Detailed schematic showing cascaded JK flip-flop counters for seconds, minutes, and hours, with 12-hour/24-hour format switching logic.





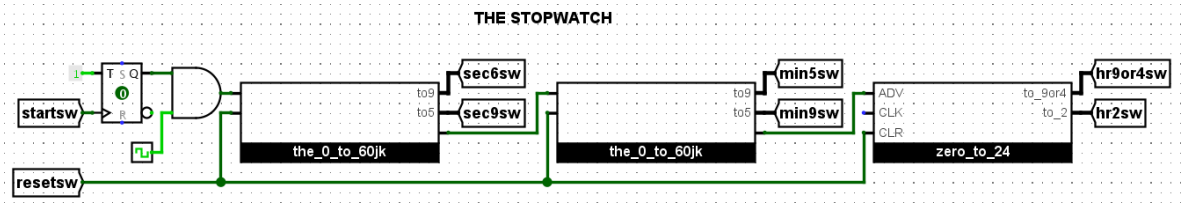
Appendix C – Countdown Timer Circuit Diagram

- Schematic of CTR6-based countdown counter chain with zero detection logic and alarm trigger.



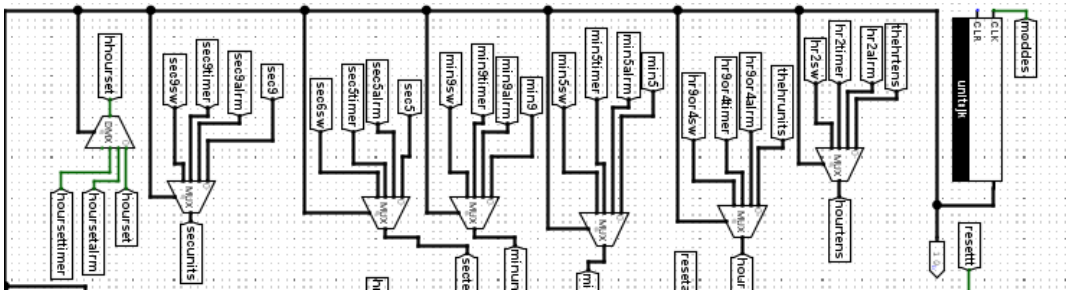
Appendix D – Stopwatch Module Circuit Diagram

- Schematic showing T flip-flop and AND gate–based control logic for counting pulses into the stopwatch counters.



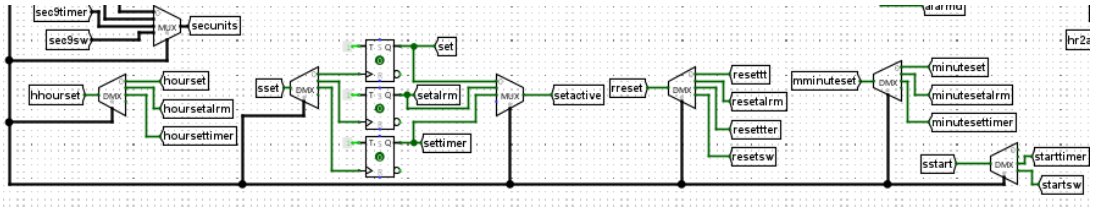
Appendix E – Display Multiplexing Circuit

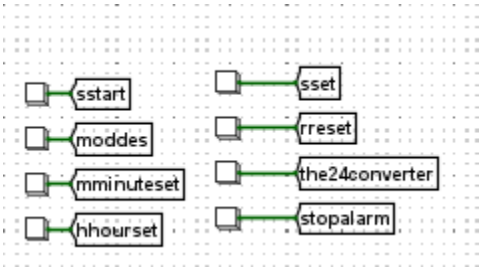
- Diagram showing the multiplexer-based digit scanning arrangement for the seven-segment display.



Appendix F – Button Input and Demultiplexing Circuit

- Schematic showing the demultiplexer arrangement for scanning multiple control buttons using shared input lines.





Appendix G – Component Datasheets

1. 74LS90 – Decade Counter (BCD)

- **Function:** Divides input clock frequency and provides BCD outputs for 0–9 counting.
- **Use in Project:** Implemented seconds, minutes, and hours counting.
- **Key Specs:**
  - Supply Voltage: 4.75V to 5.25V
  - Maximum Clock Frequency: ~42 MHz
  - Typical Propagation Delay: 23 ns
  - Package: DIP-14
- **Datasheet Source:** Texas Instruments 74LS90 Datasheet

2. 74LS47 – BCD to 7-Segment Decoder/Driver

- **Function:** Converts BCD input into the corresponding 7-segment display pattern.

- **Use in Project:** Displaying hours, minutes, and seconds.
- **Key Specs:**
    - Input Logic: TTL-compatible
    - Output Drive: Suitable for common anode displays
    - Propagation Delay: 25 ns typical
    - Package: DIP-16
- **Datasheet Source:** Texas Instruments 74LS47 Datasheet

3. 74LS85 – 4-bit Magnitude Comparator

- **Function:** Compares two 4-bit binary values and outputs equality, greater than, or less than signals.
- **Use in Project:** Alarm time comparison with current time.
- **Key Specs:**
    - Supply Voltage: 4.75V to 5.25V
    - Max Frequency: 35 MHz
    - Typical Delay: 18 ns
    - Package: DIP-16
- **Datasheet Source:** Texas Instruments 74LS85 Datasheet

4. 555 Timer IC (for Real-World Clock Pulse)

- **Function:** Generates a stable 1 Hz clock signal for the counters.
- **Use in Project:** In simulation, replaced by Logisim's built-in clock generator; in hardware, the 555 would be used.
- **Key Specs:**
    - Operating Voltage: 4.5V to 15V
    - Max Output Current: 200 mA
    - Frequency Stability: ±1%
    - Package: DIP-8
- **Datasheet Source:** NE555 Datasheet

5. 7-Segment Display – Common Anode

- **Function:** Displays decimal digits 0–9 based on input signals.
- **Use in Project:** Visual time output.
- **Key Specs:**
    - Forward Voltage per Segment: ~2V
    - Max Current per Segment: 20 mA
    - Viewing Angle: ~60°
- **Datasheet Source:** Example – Kingbright SC56 Datasheet