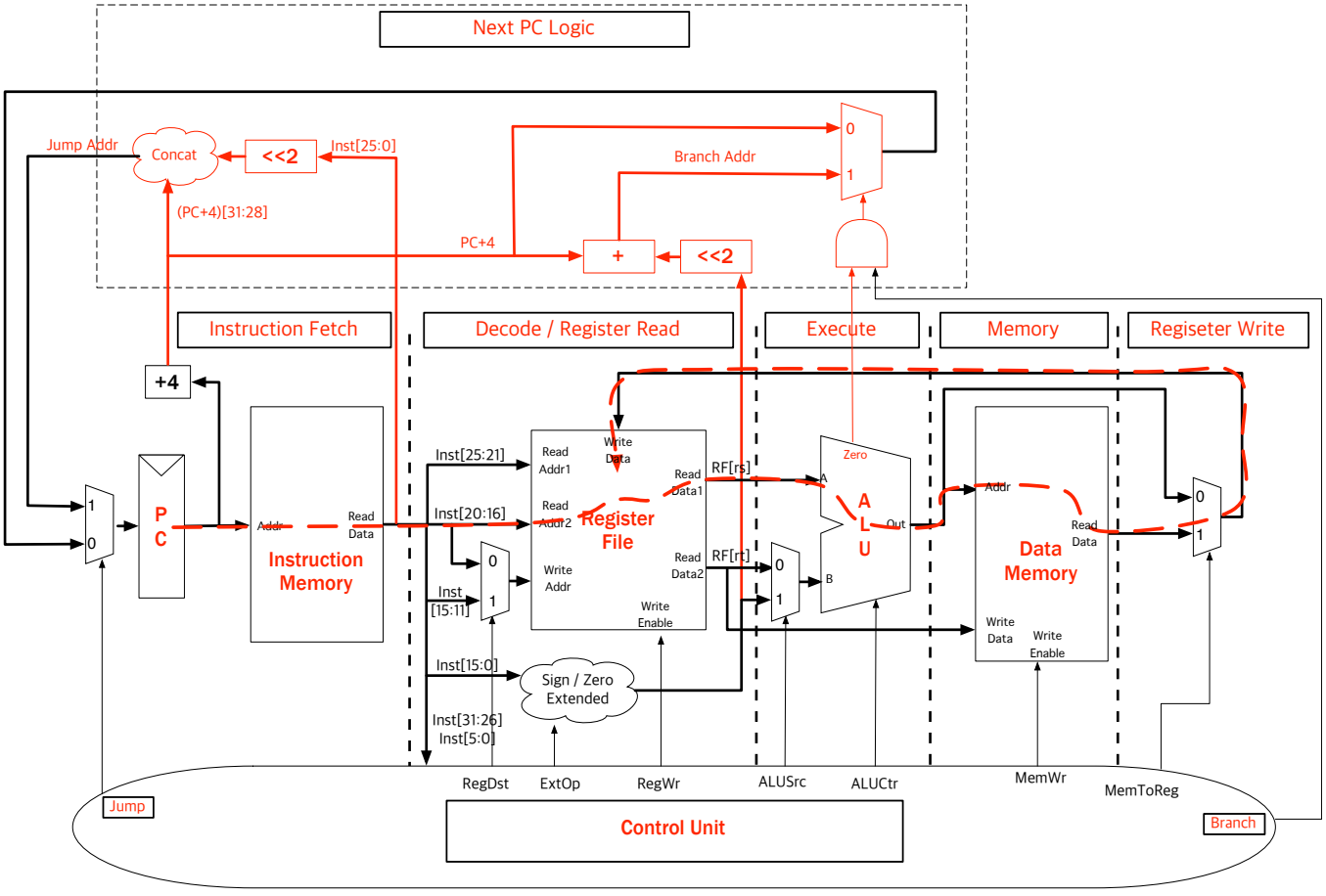
Single Cycle CPU Design

Here we have a single cycle CPU diagram. Answer the following questions:

1. Name each component.
2. Name each datapath stage and explain its functionality.

Stage	Functionality
Instruction Fetch	Send an address to the instruction memory Read the instruction (MEM[PC])
Decode / Register Read	Generate the control signal values using the opcode & funct fields Read the register values with the rs & rt fields Sign / zero extend the immediate
Execute	Perform arithmetic / logical operations
Memory	Read from / write to the data memory
Register Write	Write back the ALU result / the memory load to the register file

3. Provide data inputs and control signals to the next PC logic.
4. Implement the next PC logic.



Single Cycle CPU Control Logic

Clocking Methodology

- The input signal to each state element must stabilize before each rising edge.
- Critical path: Longest delay path between state elements in the circuit.
- $t_{clk} \geq t_{clk\text{-}to\text{-}q} + t_{CL} + t_{setup}$, where t_{CL} is the critical path in the combinational logic.
- If we place registers in the critical path, we can shorten the period by reducing the amount of logic between registers.
- $t_{hold} \leq t_{clk\text{-}to\text{-}q} + t_{min}$ where t_{min} is the shortest path through the combinational logic.

Single Cycle CPU Performance Analysis

The delays of circuit elements are given as follows:

Element	Register clk-to-q	Register Setup	MUX	ALU	Mem Read	Mem Write	RegFile Read	RegFile Setup
Parameter	$t_{clk\text{-}to\text{-}q}$	t_{setup}	t_{mux}	t_{ALU}	$t_{MEMread}$	$t_{MEMwrite}$	t_{RFread}	$T_{RFsetup}$
Delay(ps)	30	20	25	200	250	200	150	20

1. Give an instruction that exercises the critical path.

Load Word (lw)

2. What is the critical path in the single cycle CPU?

Red dashed line in the diagram

3. What are the minimum clock cycle, t_{clk}, and the maximum clock frequency, f_{clk}? Assume the $t_{clk\text{-}to\text{-}q}$ > hold time.

$t_{clk} >= t_{clk\text{-}to\text{-}q\ (PC)} + t_{IMEMread} + t_{RFread} + t_{ALU} + t_{DMEMread} + t_{mux} + t_{RFsetup}$

$= 30 + 250 + 150 + 200 + 250 + 25 + 20 = 925$ ps

(this is for the simplified diagram above; your actual CPU would have more muxes!)

$f_{clk} = 1/t_{clk} <= 1/ (925\text{ ps}) = 1.08$ GHz

4. What is the maximum hold time? Assume the time for an adder is $t_{ADD} = 100$ ps.

The shortest path between one register and the next is from PC to PC for instructions that increment PC by 4 (all instructions but branches and jumps).

$t_{hold} \leq t_{clk\text{-}to\text{-}q} + t_{ADD} + 2*t_{mux} = 30 + 100 + 2*25 = 180$ ps

Synchronous Logic

1. Fill out the timing diagrams for the circuits below: