Computer Organization and Architecture

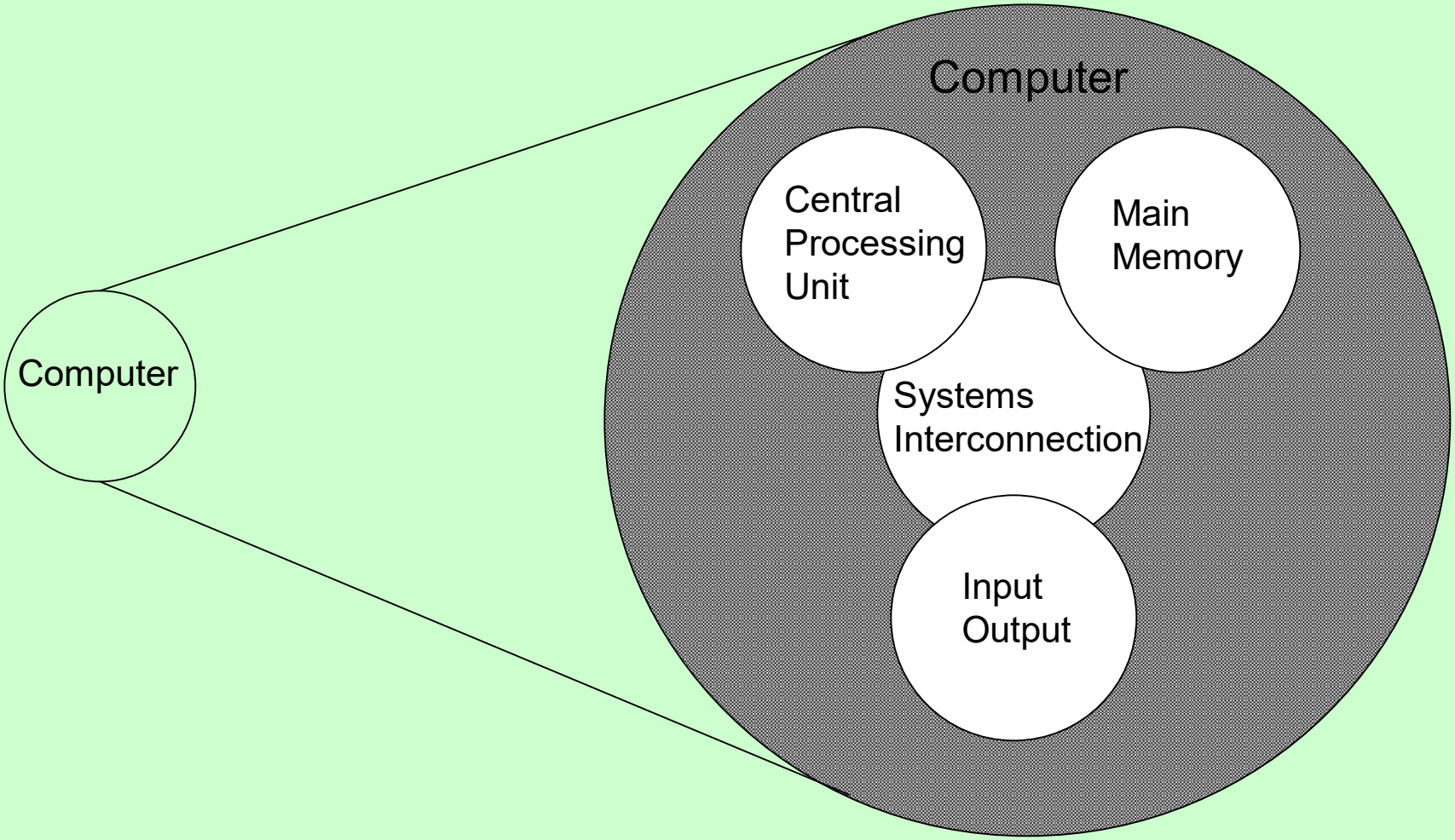
1. Structure & Function

- Structure is the way in which components relate to each other
- Function is the operation of individual components as part of the structure

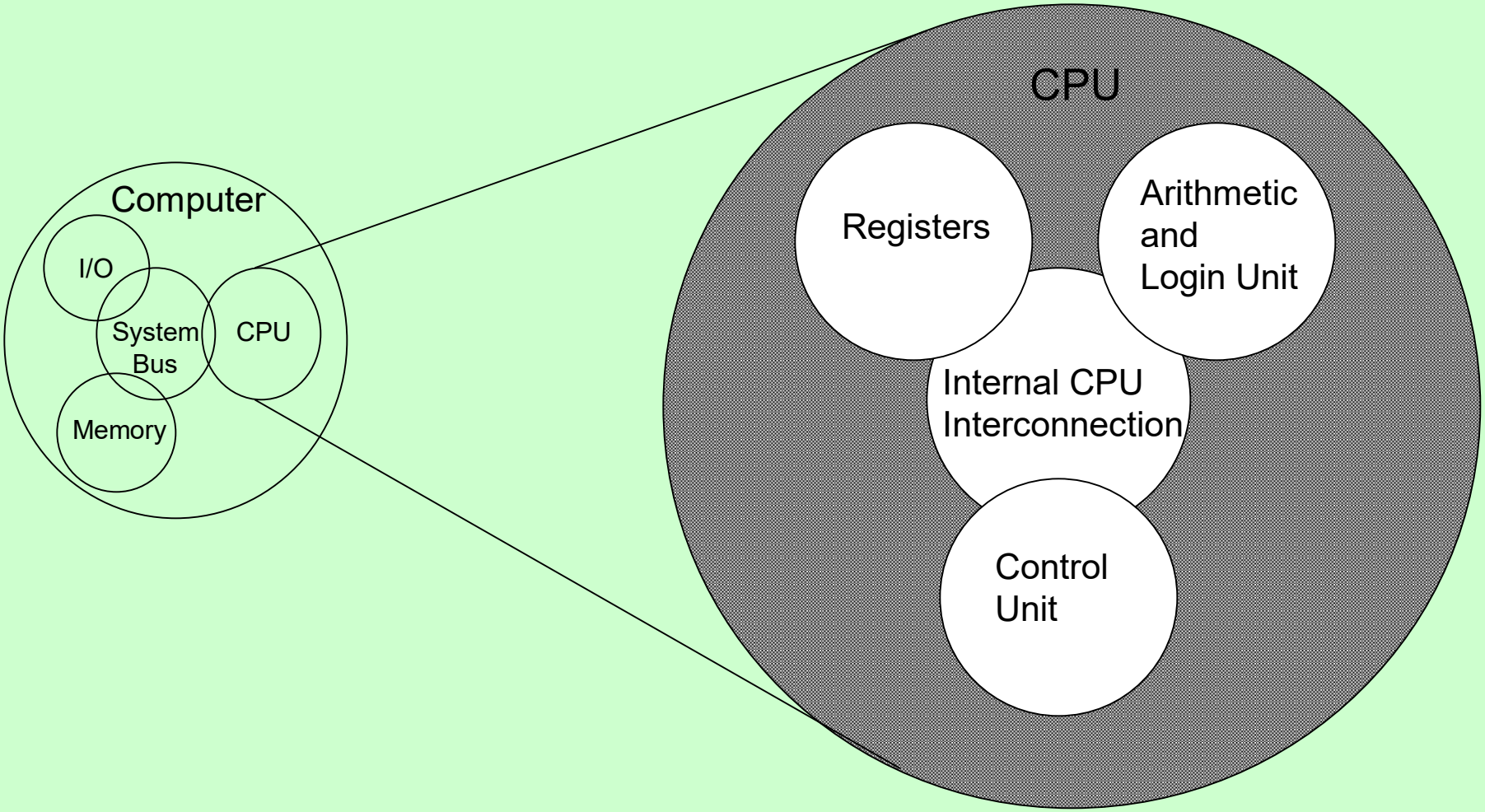
Function

- All computer functions are:
  - Data processing
  - Data storage
  - Data movement
  - Control

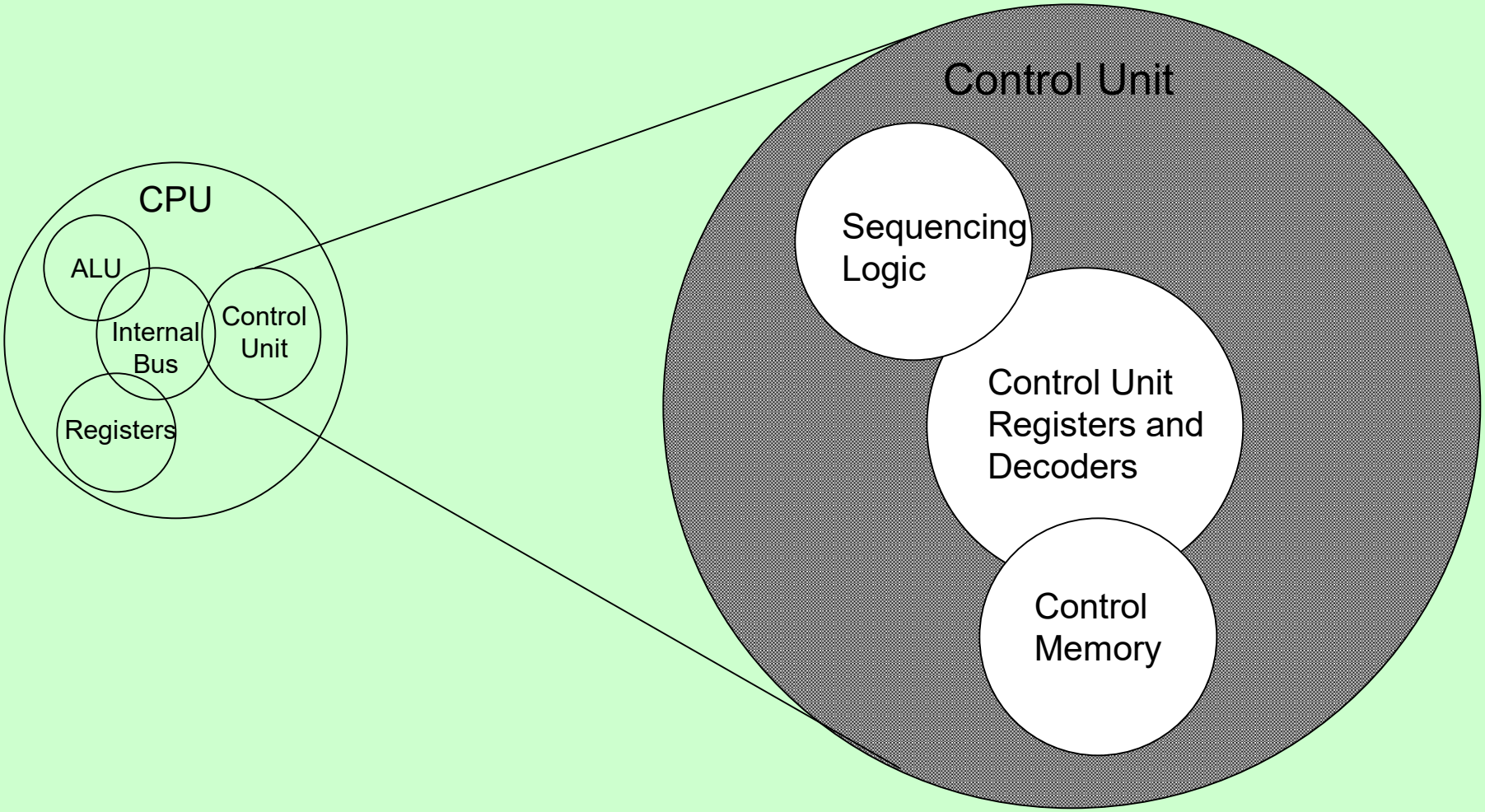
Structure - Top Level



Structure - The CPU



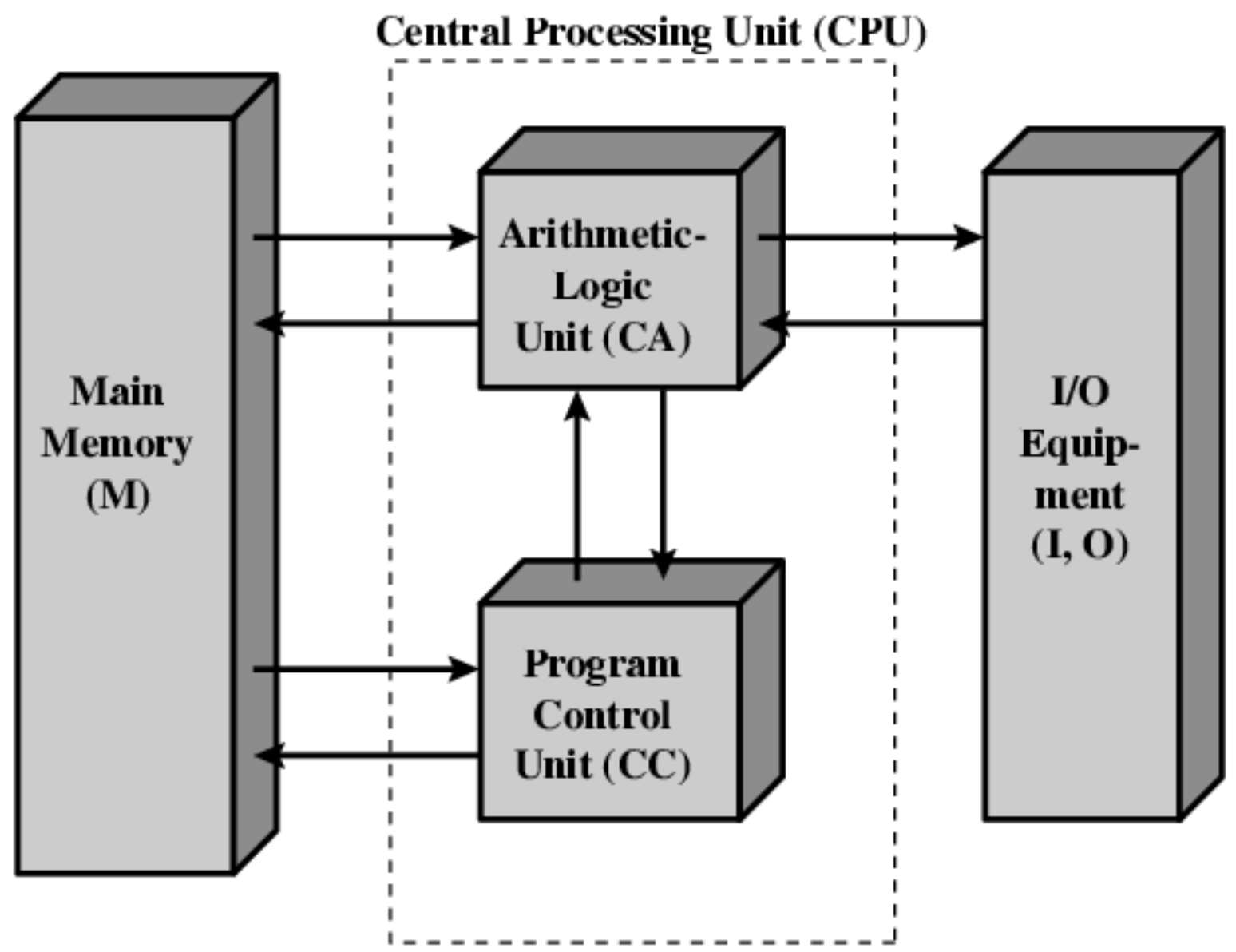
Structure - The Control Unit



2. Von Neumann Architecture

- Stored Program concept
- Main memory storing programs and data
- ALU operating on binary data
- Control unit interpreting instructions from memory and executing
- Input and output equipment operated by control unit
- Completed 1952

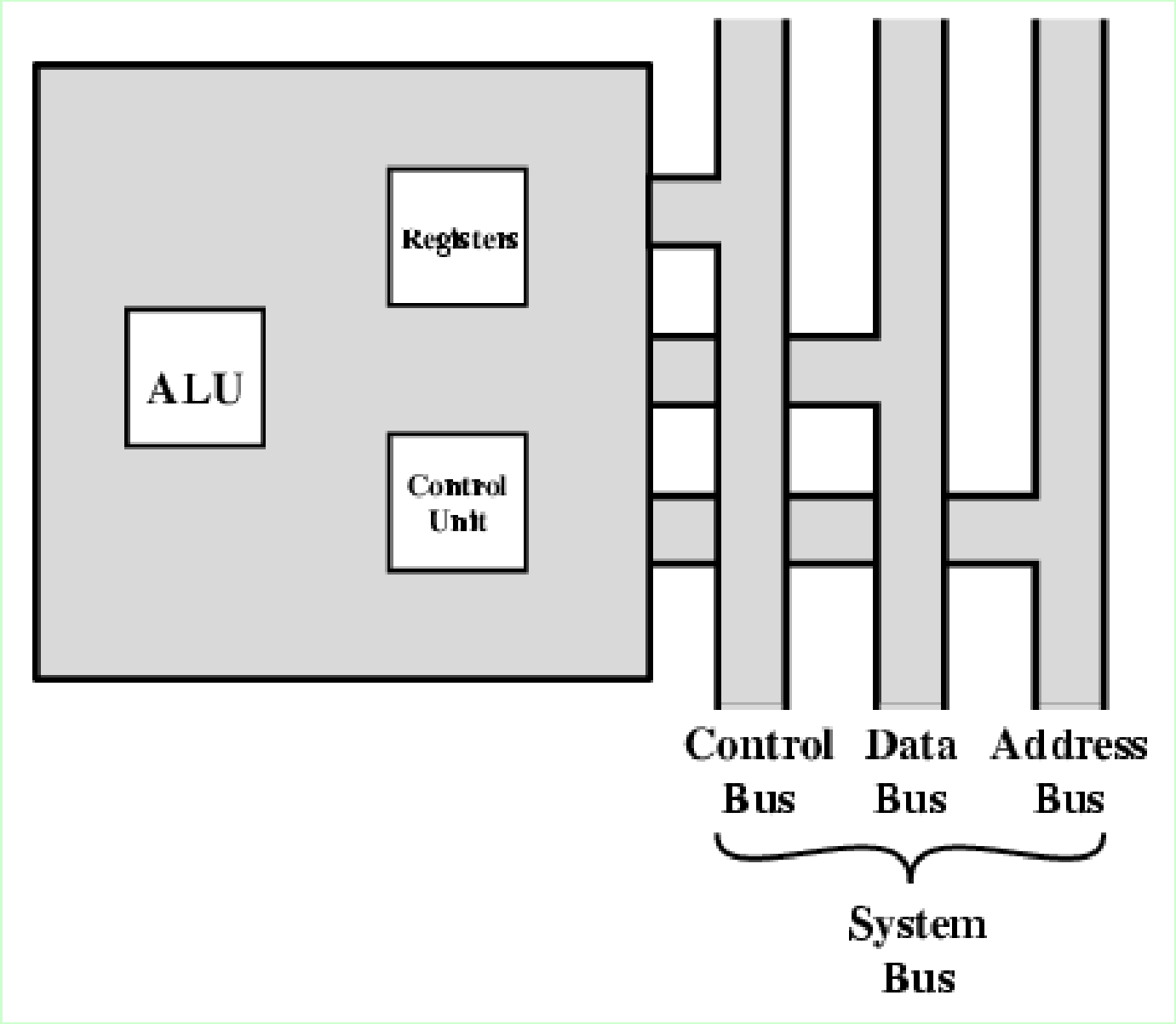
Structure of von Neumann machine



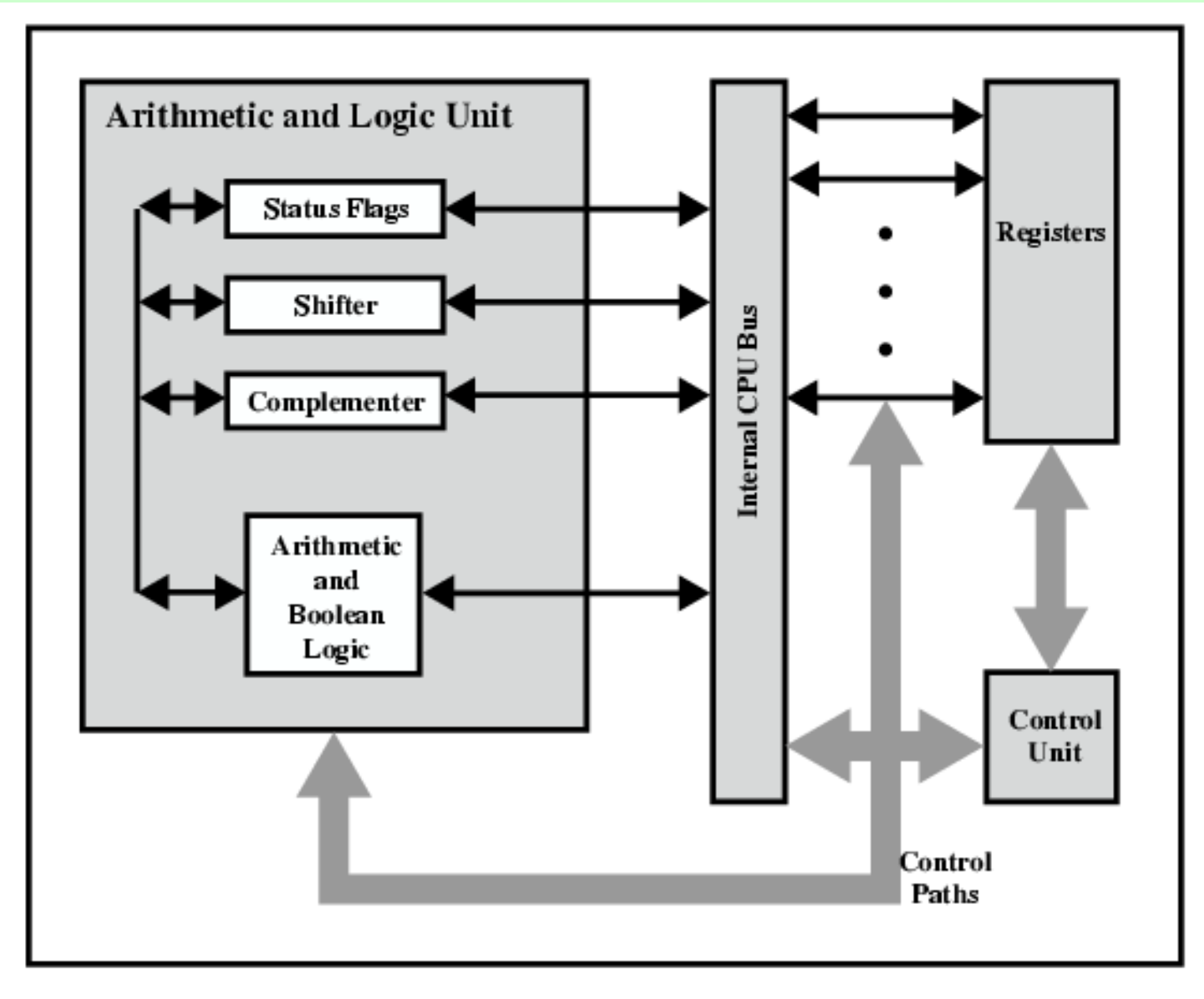
Computer Architecture

- CPU:The Control Unit and the Arithmetic and Logic Unit constitute -Central Processing Unit
- I/O: Data and instructions need to get into the system and results out
  - —Input/output
- Temporary storage of code and results is needed
  - —Main memory

CPU With Systems Bus



CPU Internal Structure



3. CPU Working Cycles

- Fetch instructions and data
- Interpret instructions
- Execute or Process data
- Store or Write data

What is a program?

- A sequence of steps
- For each step, an arithmetic or logical operation is done
- For each operation, a different set of control signals is needed

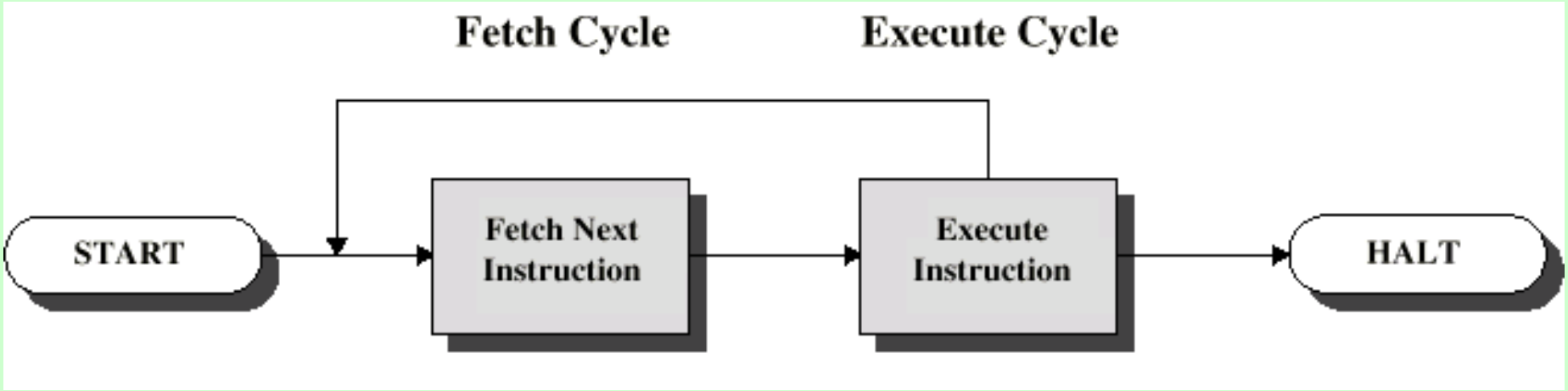
Function of Control Unit

- For each operation a unique opcode is provided
  - e.g. ADD, MOVE
- CU accepts the code and issues the control signals

- We have a computer!

Instruction Cycle

- Two steps:
  - Fetch
  - Execute



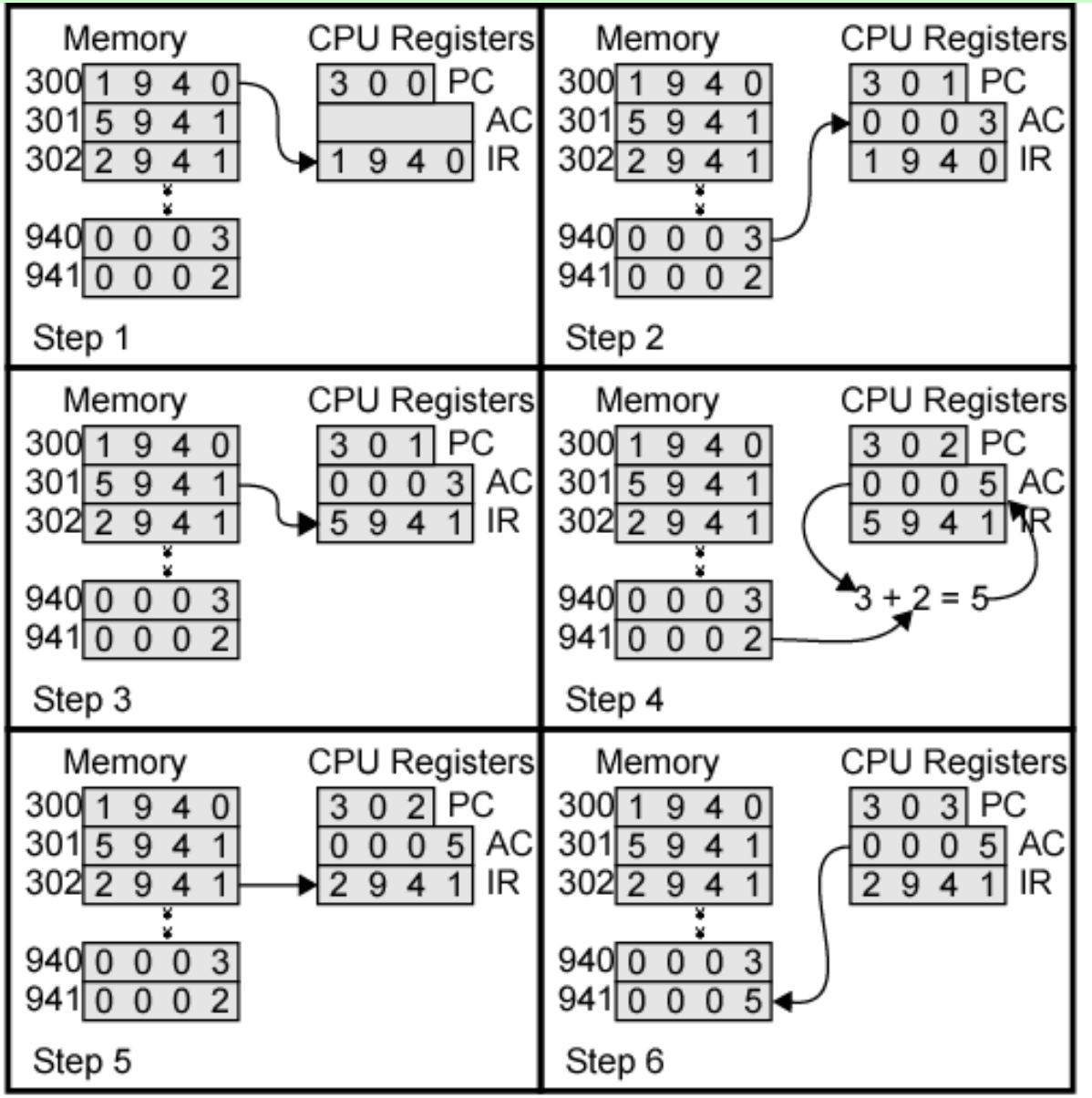
Fetch Cycle

- Program Counter (PC) holds address of next instruction to fetch
- Processor fetches instruction from memory location pointed to by PC
- Increment PC
  - —Unless told otherwise
- Instruction loaded into Instruction Register (IR)
- Processor interprets instruction and performs required actions

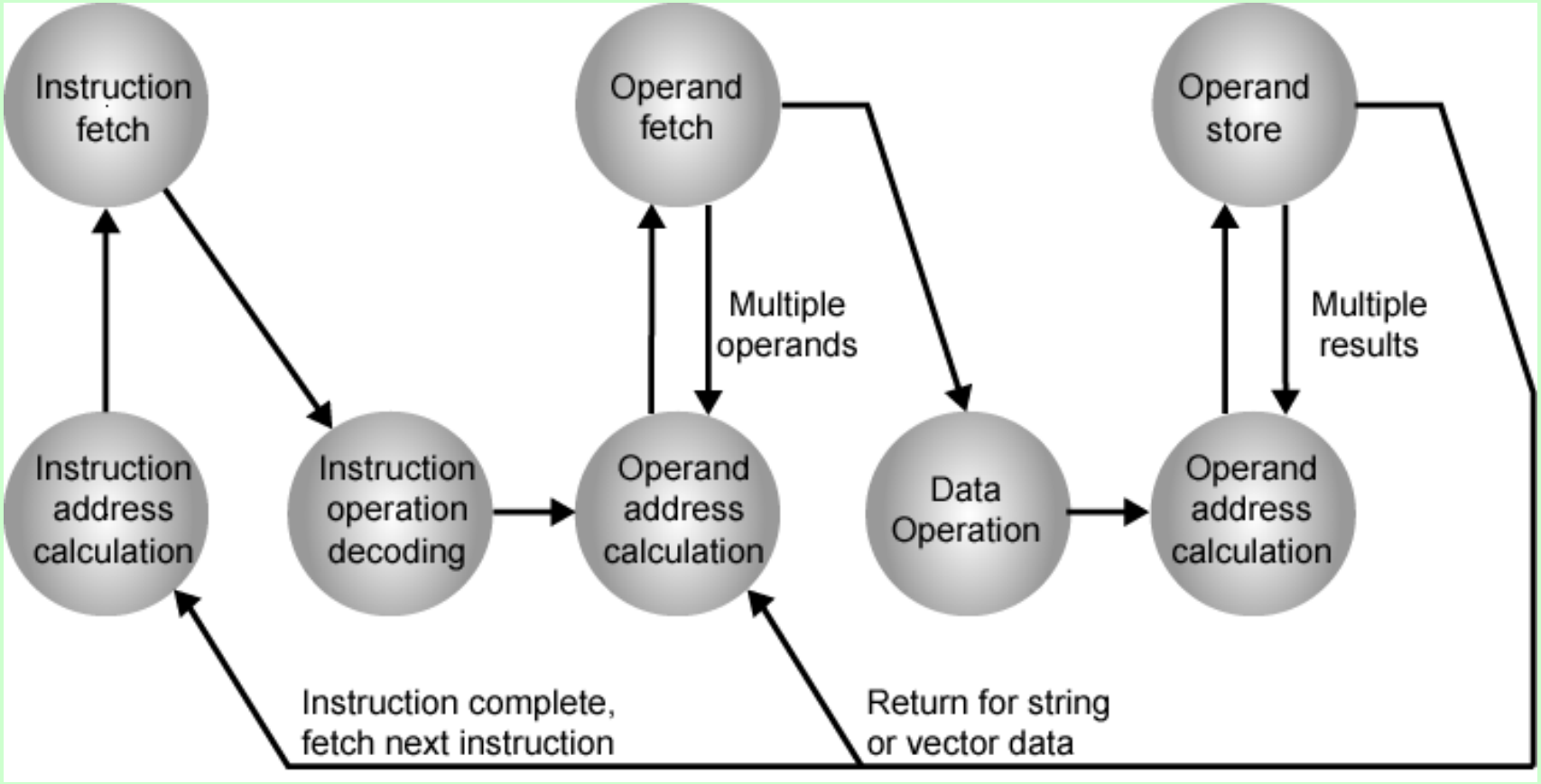
Execute Cycle

- Processor-memory
  - —data transfer between CPU and main memory
- Processor I/O
  - —Data transfer between CPU and I/O module
- Data processing
  - —Some arithmetic or logical operation on data
- Control
  - —Alteration of sequence of operations
  - —e.g. jump
- Combination of above

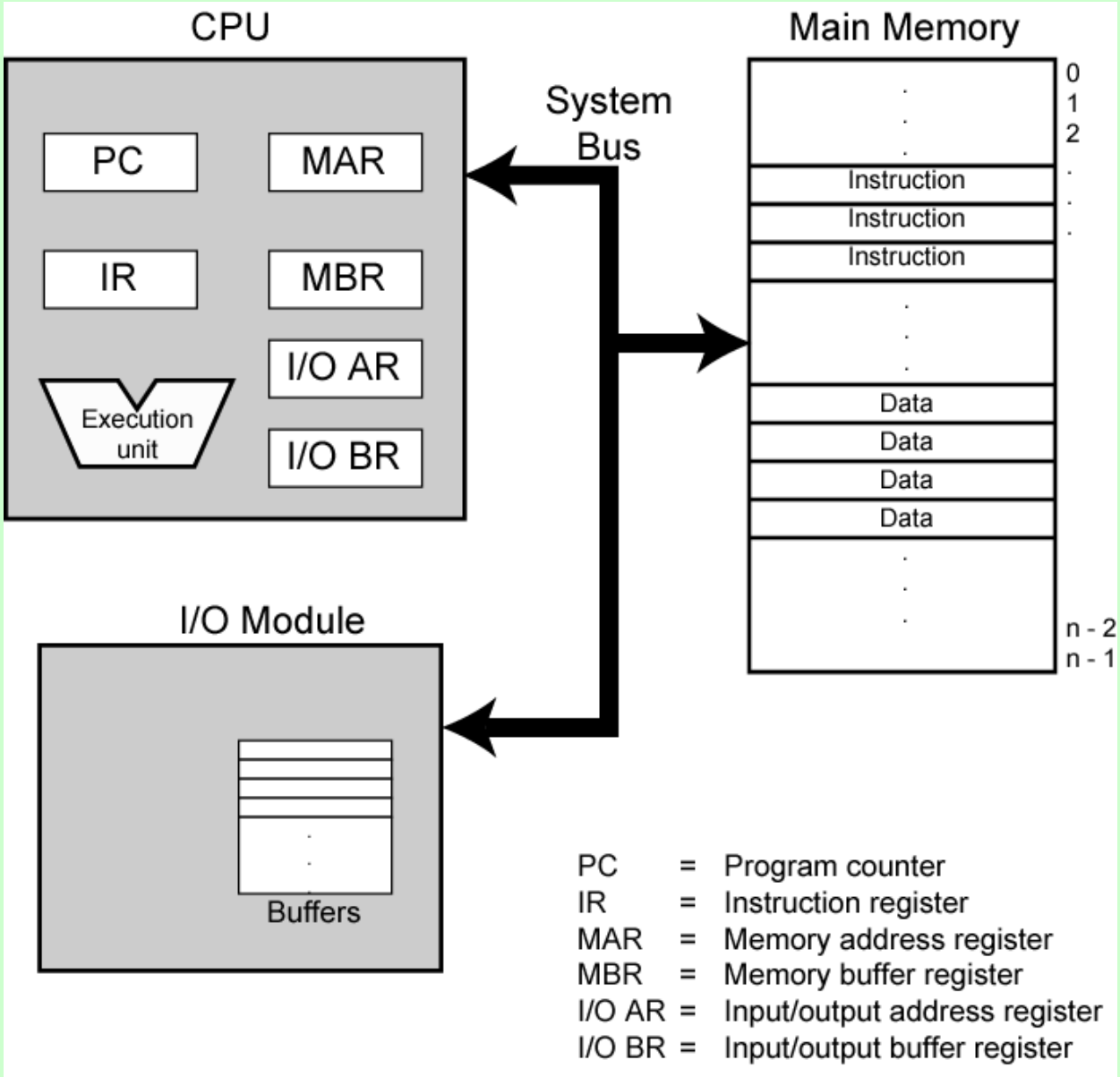
Example of Program Execution

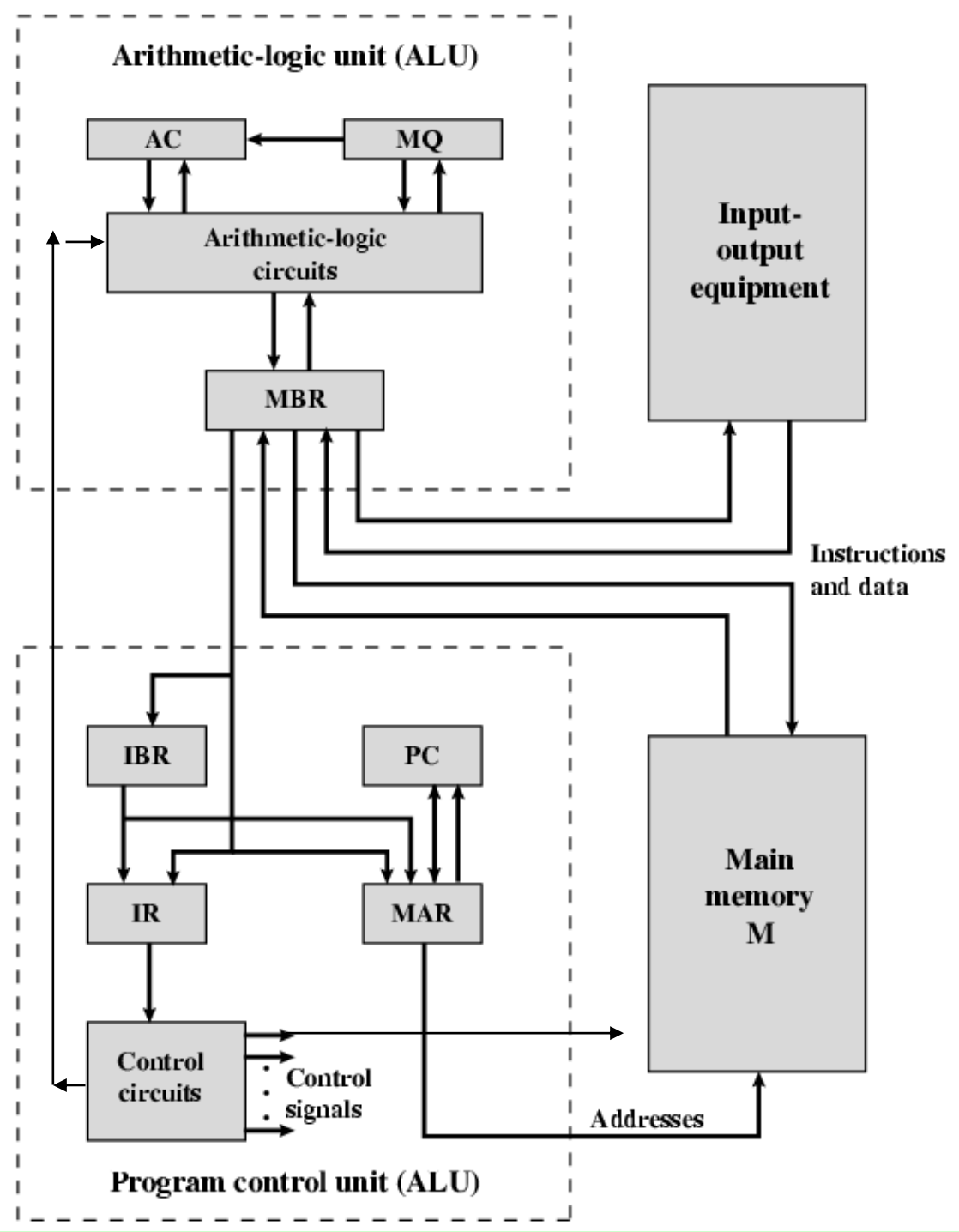


Instruction Cycle State Diagram



Computer Components: Top Level View

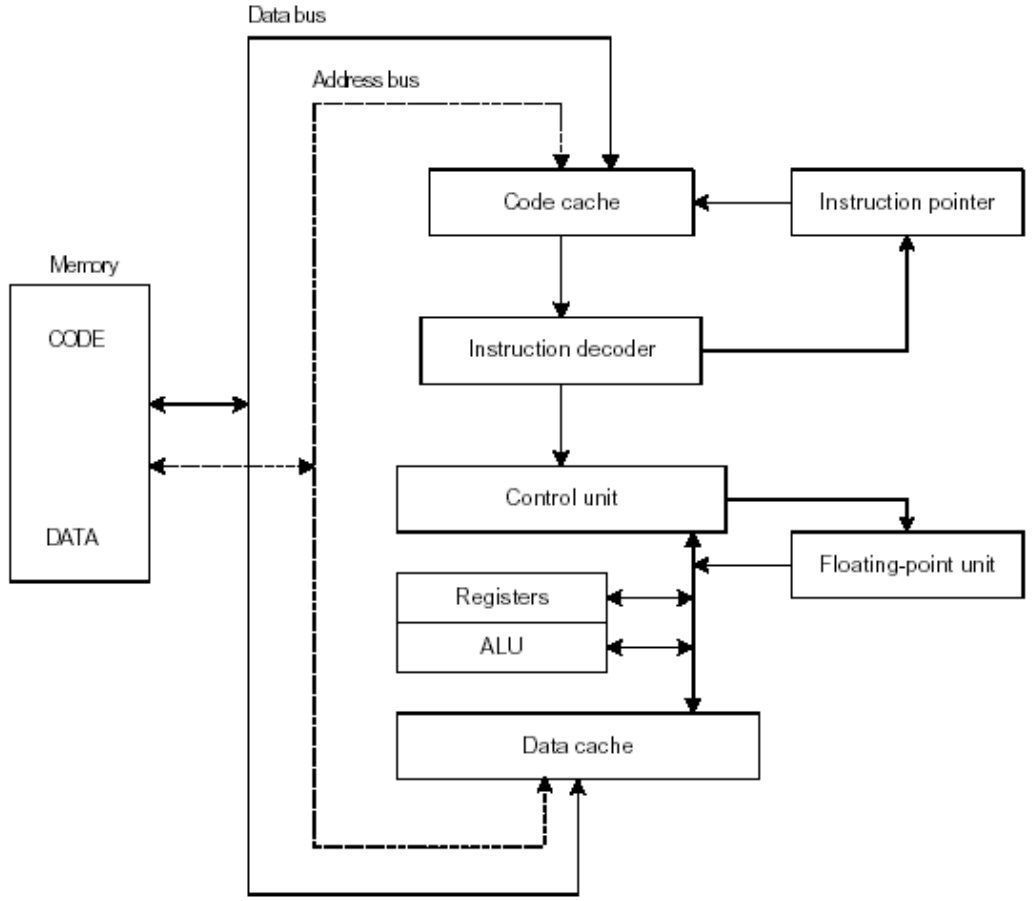



Arithmetic-logic unit (ALU)
AC
MQ
Arithmetic-logic circuits
MBR
Input-output equipment
Instructions and data
IBR
PC
IR
MAR
Main memory M
Control circuits
Control signals
Addresses
Program control unit (ALU)

Instruction Execution Cycle

- Fetch
- Decode
- Fetch operands
- Execute
- Store output

Figure 2–2 Simplified Pentium CPU Block Diagram.



4. Connecting-Bus

- All the units must be connected
- Different type of connection for different type of unit
  - Memory
  - Input/Output
  - CPU

CPU Connection

- Reads instruction and data
- Writes out data (after processing)
- Sends control signals to other units
- Receives (& acts on) interrupts

Buses

- There are a number of possible interconnection systems
- Single and multiple BUS structures are most common
- e.g. Control/Address/Data bus (PC)

What is a Bus?

- A communication pathway connecting two or more devices
- Usually broadcast
- Often grouped
  - A number of channels in one bus
  - e.g. 32 bit data bus is 32 separate single bit channels

Data Bus

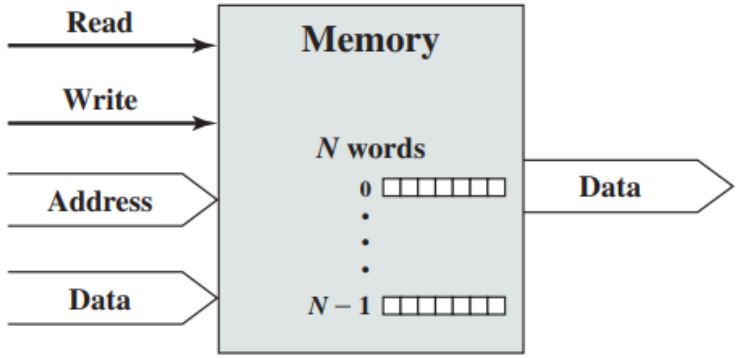
- Carries data
  - —Remember that there is no difference between “data” and “instruction” at this level
- Width is a key determinant of performance
  - —8, 16, 32, 64 bit

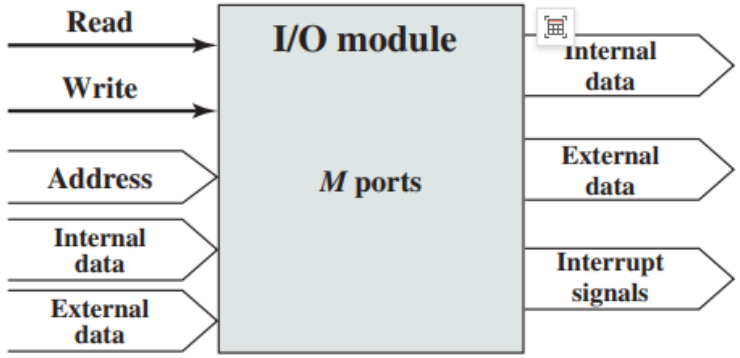
Address bus

- Identify the source or destination of data
- e.g. CPU needs to read an instruction (data) from a given location in memory
- Bus width determines maximum memory capacity of system
  - e.g. 8080 has 16 bit address bus giving 64k address space

Control Bus

- Control and timing information
  - —Memory read/write signal
  - —ALU/Register
  - —Interrupt request
  - —Clock signals





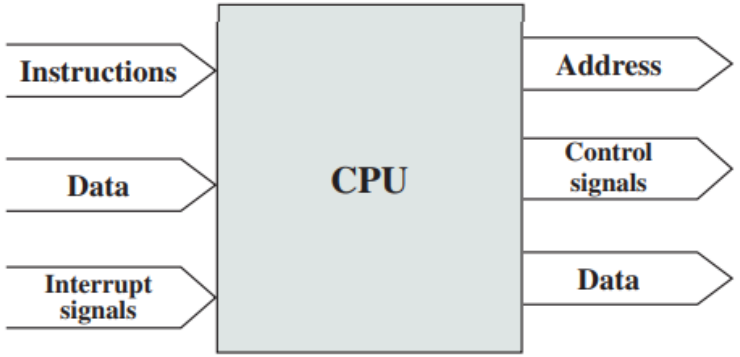
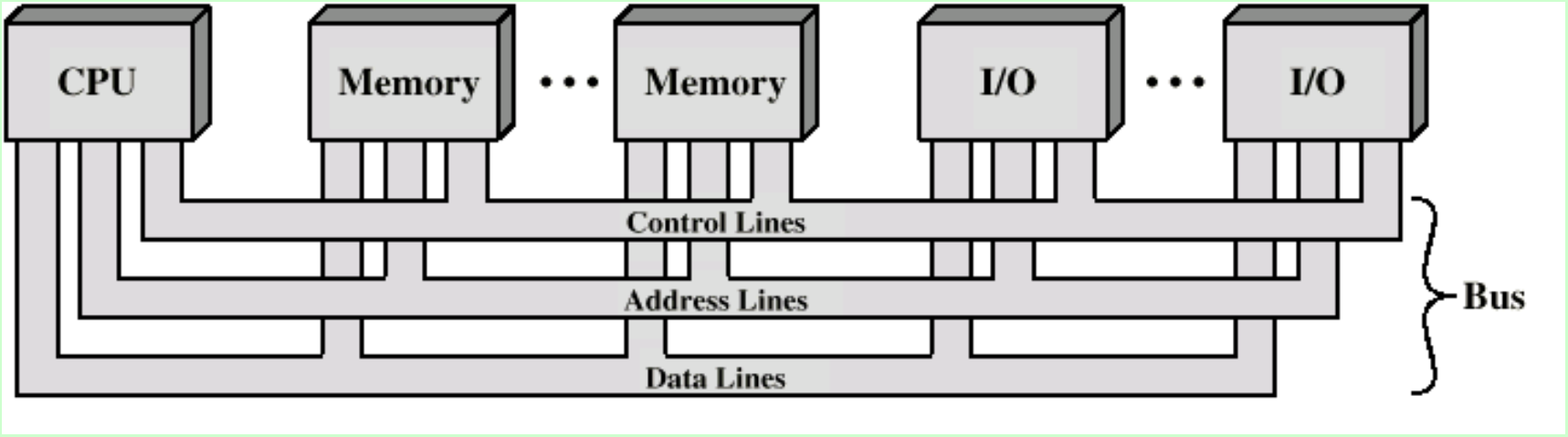


Figure 3.15 Computer Modules

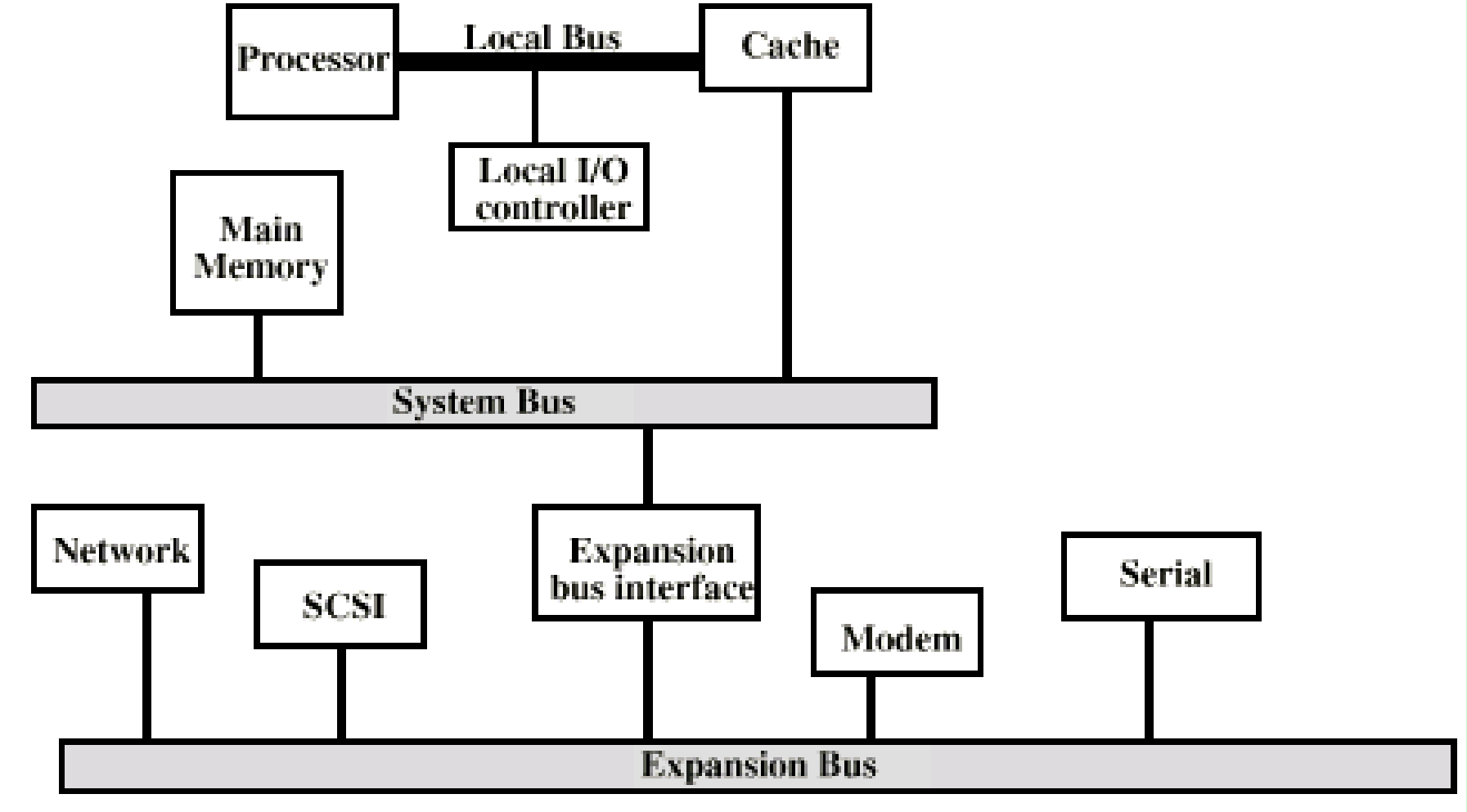
Bus Interconnection Scheme



Single Bus Problems

- Lots of devices on one bus leads to:
  - Propagation delays
    - Long data paths mean that co-ordination of bus use can adversely affect performance
    - If aggregate data transfer approaches bus capacity
- Most systems use multiple buses to overcome these problems

Traditional (ISA) (with cache)



Bus Types

- Dedicated
  - Separate data & address lines
- Multiplexed
  - Shared lines
  - Address valid or data valid control line
  - Advantage - fewer lines
  - Disadvantages
    - More complex control
    - Ultimate performance

Bus Arbitration(仲裁)

- More than one module controlling the bus
- e.g. CPU and DMA controller
- Only one module may control bus at one time
- Arbitration may be centralised or distributed

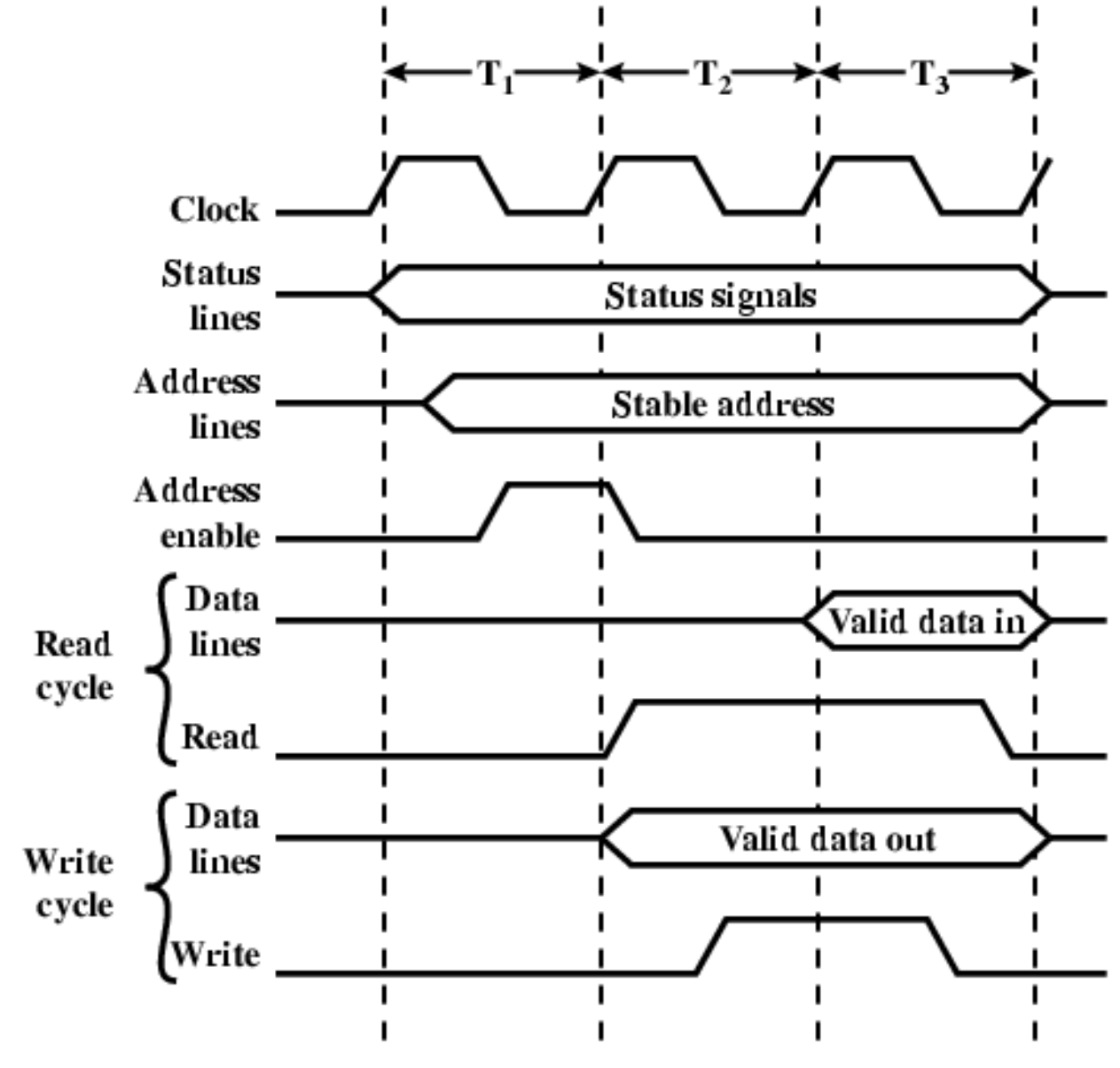
Centralised or Distributed Arbitration

- Centralised
  - —Single hardware device controlling bus access
    - – Bus Controller
    - – Arbiter
  - —May be part of CPU or separate
- Distributed
  - —Each module may claim the bus
  - —Control logic on all modules

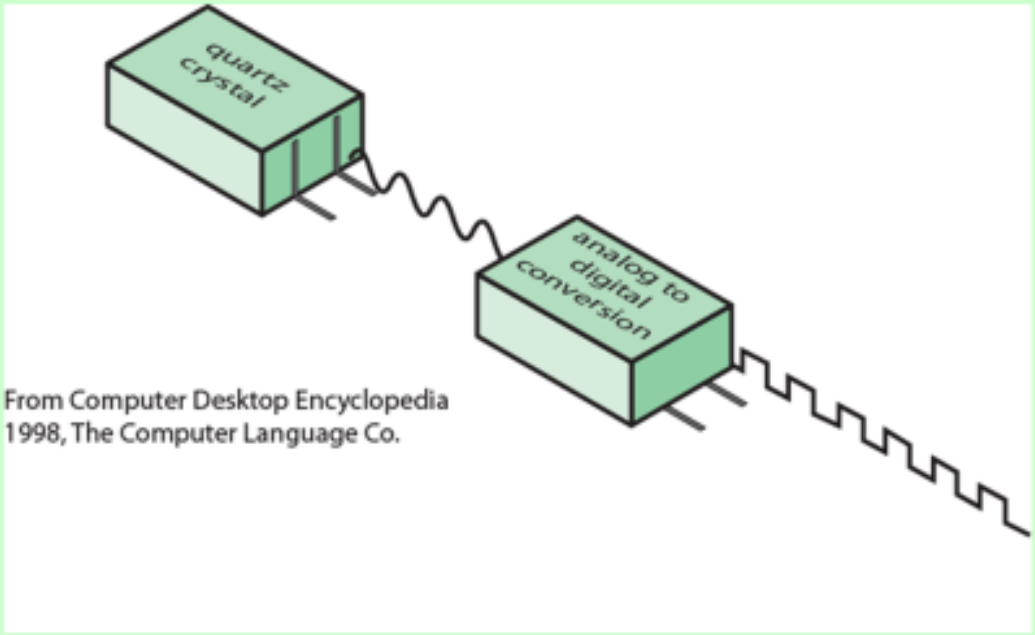
5. Timing

- Co-ordination of events on bus
- Synchronous
  - —Events determined by clock signals
  - —Control Bus includes clock line
  - —A single 1-0 is a bus cycle
  - —All devices can read clock line
  - —Usually sync on leading edge
  - —Usually a single cycle for an event

Synchronous Timing Diagram

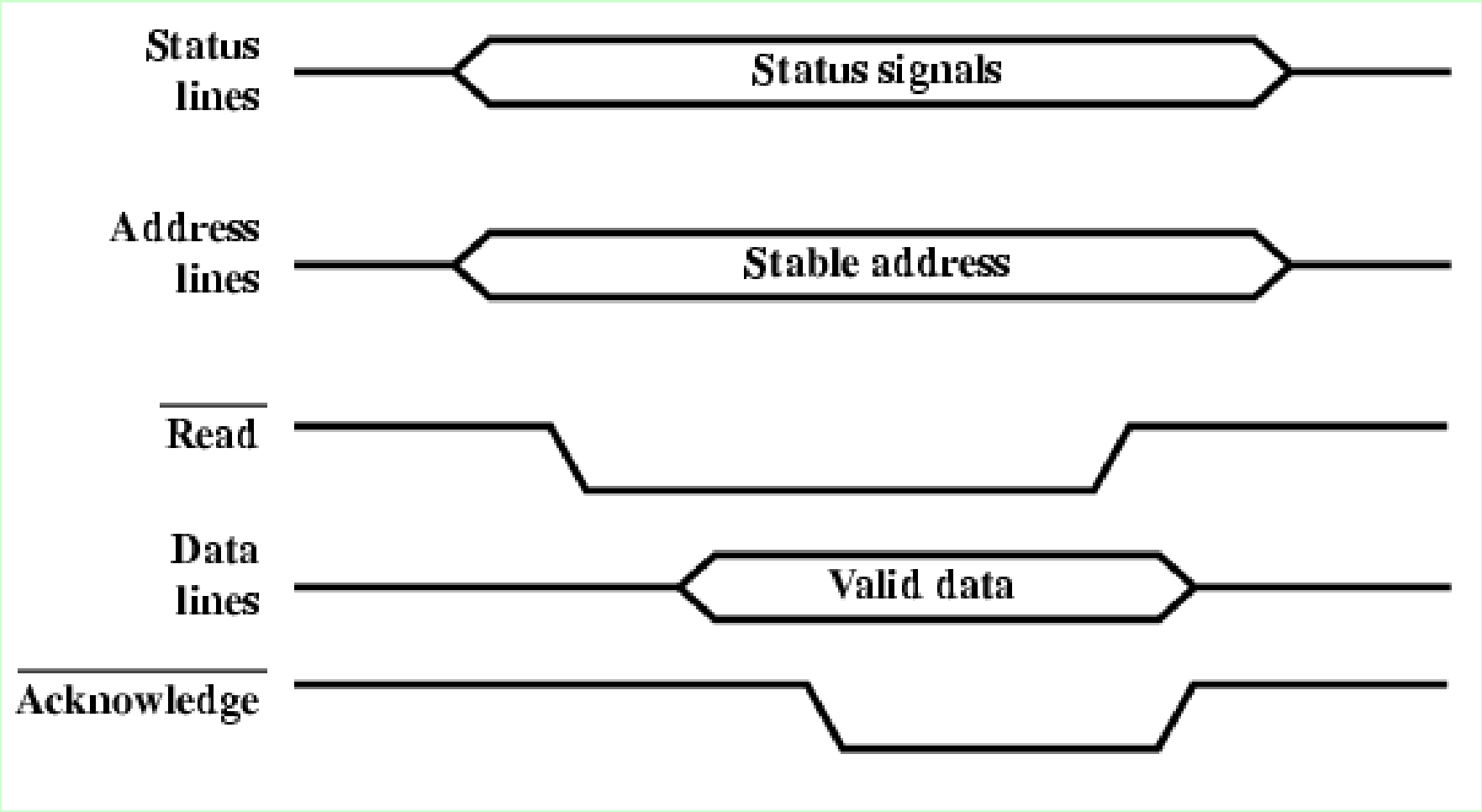


System Clock

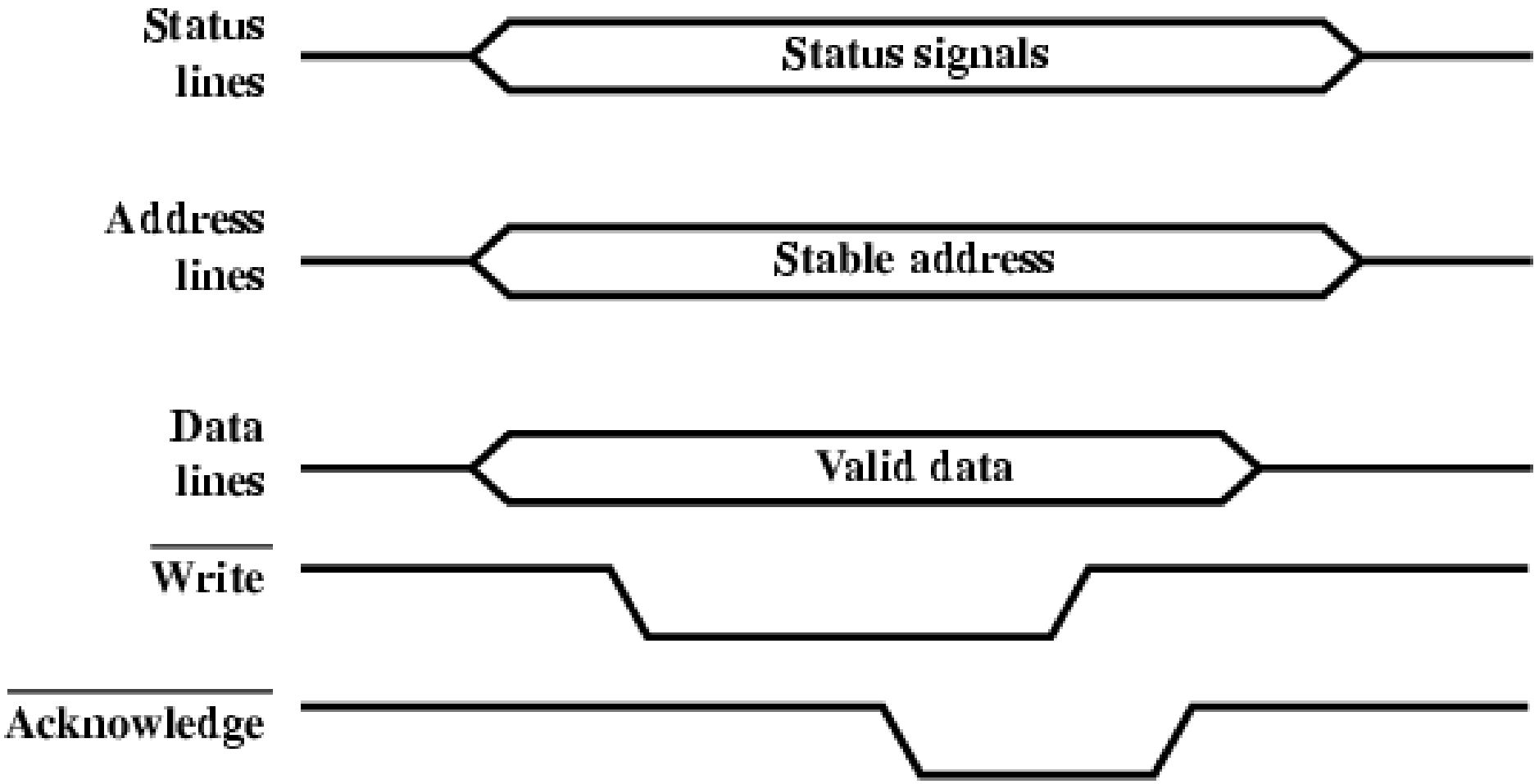


From Computer Desktop Encyclopedia
1998, The Computer Language Co.

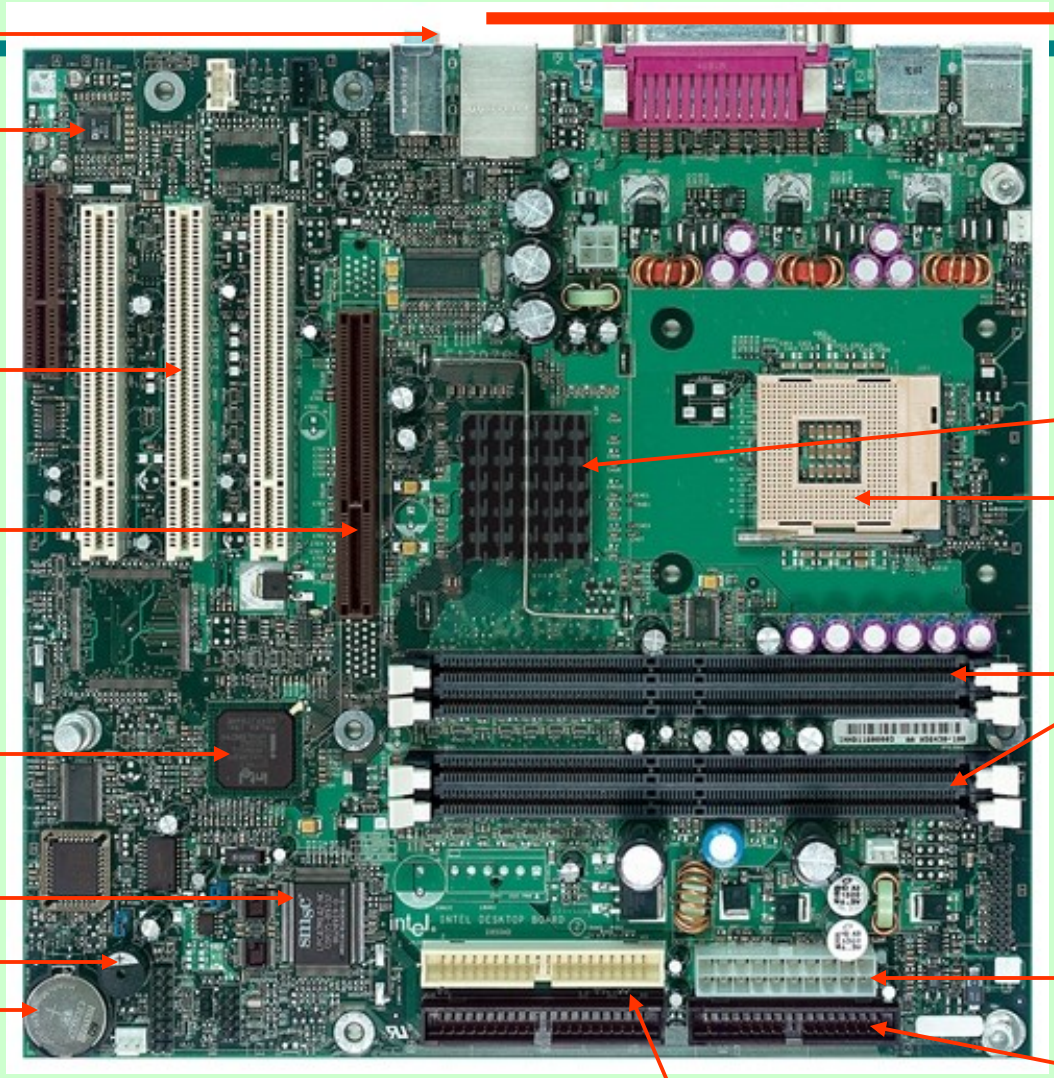
Asynchronous Timing – Read Diagram



Asynchronous Timing – Write Diagram

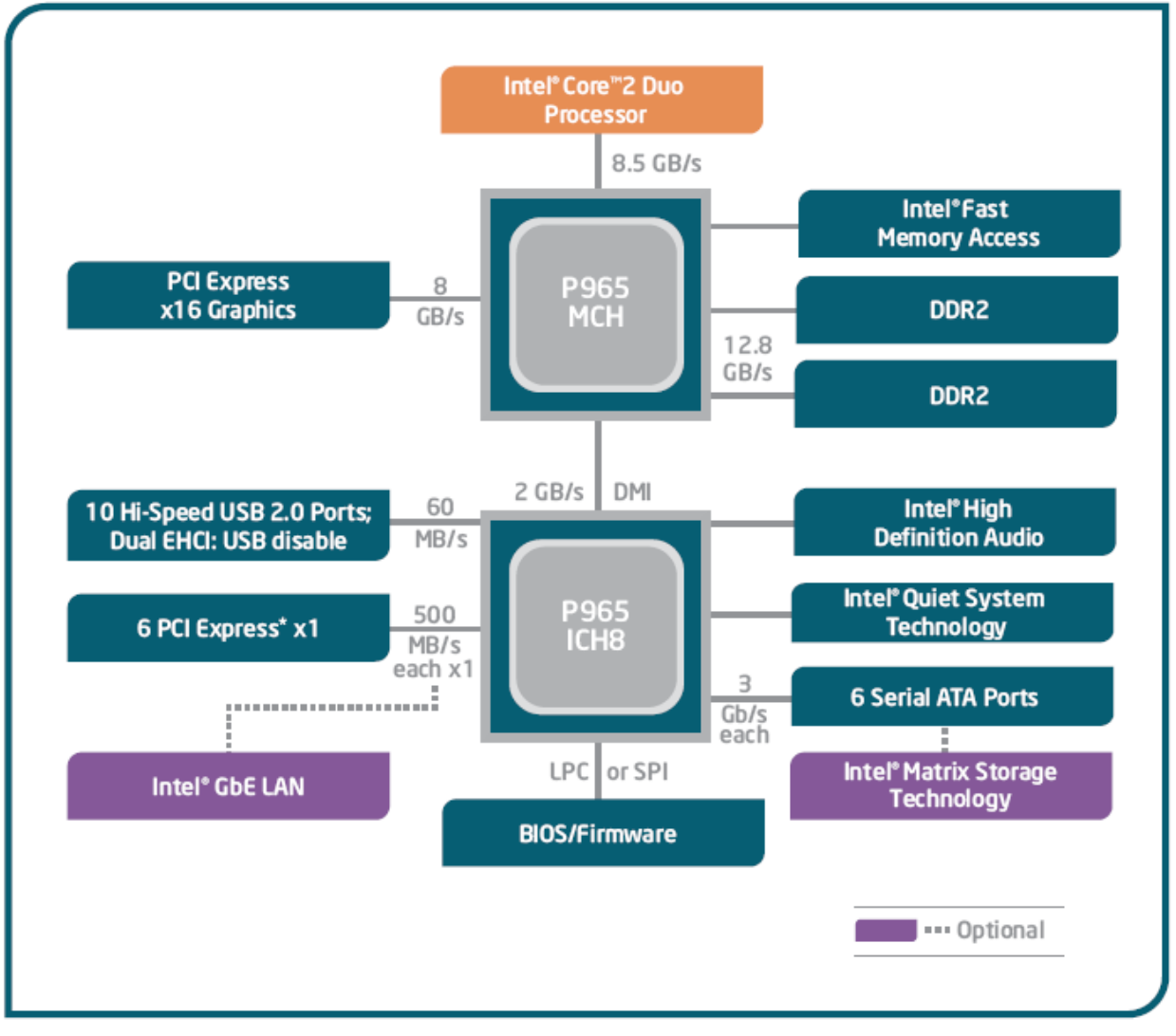


Intel D850MD Motherboard



Source: Intel® Desktop Board D850MD/D850MV Technical Product Specification

Intel 965 Express Chipset



Input-Output Ports

- USB (universal serial bus)
  - intelligent high-speed connection to devices
  - up to 12 megabits/second
  - USB hub connects multiple devices
  - *enumeration*: computer queries devices
  - supports *hot* connections
- Parallel
  - short cable, high speed
  - common for printers
  - bidirectional, parallel data transfer
  - Intel 8255 controller chip

Input-Output Ports (cont)

- Serial
  - —RS-232 serial port
  - —one bit at a time
  - —uses long cables and modems
  - —16550 UART (universal asynchronous receiver transmitter)
  - —programmable in assembly language

Device Interfaces

- ATA host adapters
  - intelligent drive electronics (hard drive, CDROM)
- SATA (Serial ATA)
  - inexpensive, fast, bidirectional
- FireWire
  - high speed (800 MB/sec), many devices at once
- Bluetooth
  - small amounts of data, short distances, low power usage
- Wi-Fi (wireless Ethernet)
  - IEEE 802.11 standard, faster than Bluetooth

PCI Bus

- Peripheral Component Interconnection
- Intel released to public domain
- 32 or 64 bit
- 50 lines

PCI Bus Lines (required)

- Systems lines
  - —Including clock and reset
- Address & Data
  - —32 time mux lines for address/data
  - —Interrupt & validate lines
- Interface Control
- Arbitration
  - —Not shared
  - —Direct connection to PCI bus arbiter
- Error lines

PCI Bus Lines (Optional)

- Interrupt lines
  - —Not shared
- Cache support
- 64-bit Bus Extension
  - —Additional 32 lines
  - —Time multiplexed
  - —2 lines to enable devices to agree to use 64-bit transfer
- JTAG/Boundary Scan
  - —For testing procedures

Video Output

- Video controller
  - —on motherboard, or on expansion card
  - —AGP (accelerated graphics port technology)*
- Video memory (VRAM)
- Video CRT Display
  - —uses raster scanning
  - —horizontal retrace
  - —vertical retrace
- Direct digital LCD monitors
  - —no raster scanning required

Sample Video Controller (ATI Corp.)

- 128-bit 3D graphics performance powered by RAGE™ 128 PRO
- 3D graphics performance
- Intelligent TV-Tuner with Digital VCR
- TV-ON-DEMAND™
- Interactive Program Guide
- Still image and MPEG-2 motion video capture
- Video editing
- Hardware DVD video playback
- Video output to TV or VCR