

intel64_page_entry_base

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graph BT; A[intel64_pdpt_entry] --> C[intel64_page_entry_base]; B[intel64_pml4_entry] --> C;
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The diagram illustrates a hierarchical relationship between three Intel 64 architecture structures. At the top is a box labeled 'intel64_page_entry_base'. Below it are two boxes: 'intel64_pdpt_entry' on the left and 'intel64_pml4_entry' on the right. A horizontal line connects the top of these two boxes, and a vertical arrow points from the center of this line up to the bottom of the 'intel64_page_entry_base' box, indicating that both 'intel64_pdpt_entry' and 'intel64_pml4_entry' inherit from or are derived from 'intel64_page_entry_base'.

intel64_pd_entry

intel64_pdpt_entry

intel64_pml4_entry