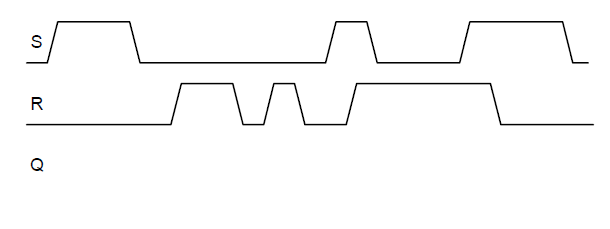
**Computer Architecture and Organization**

Winter 2024

Assignment 2

**Question\_1**

Given the input waveforms shown below sketch the output, Q, of a RS flip-flop.



A diagram of a block diagram

Description automatically generated

**Figure 1 – RS Flip Flop diagram because I forgot what it was. Remembering what it was it becomes clear that a flip flop maintains its state when set until reset. It gets awkward when both set and reset are equal to one as the flip flop enters a forbidden state.**

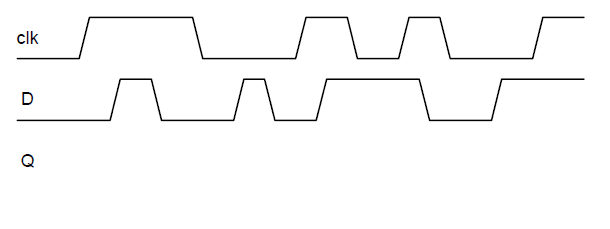
A line drawing of a graph

Description automatically generated

**Figure 2 – Q waveform output of the RS flipflop.**

**Question\_2**

Given the input waveforms shown below, sketch the output, Q, of a D flip-flop.



A diagram of a block diagram

Description automatically generated

Figure 3 – D Flip Flop diagram so I can remember what the heck I am working with. When the clock signal rises, that clock signal is the output Q.

A black and yellow line

Description automatically generated

Figure 4 -Waveform output for a D Flip Flop.

**Question\_3**

The toggle (T) flip-flop has one input, CLK, and one output, Q. On each rising edge of CLK, Q toggles to the complement of its previous value.

Draw a schematic for a T flip-flop using a D flip-flop and an inverter, also derive the truth table

I need to draw a machine that flip its output to its previous output on every rising edge of the clock.

A cartoon of a shirt

Description automatically generated

Figure 3A – A T flip flop made using a D flip flop, because the inversion of Q is fed into itself on every clock edge, the circuit toggles to the complement of its previous value of every clock edge.

|  |  |  |
| --- | --- | --- |
| CLK | Q | Q(t+1) |
| 0 | 0 | 1 |
| 1 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 1 | 0 |

**Question\_4**

A JK flip-flop receives a clock and two inputs, J and K. On the rising edge of the clock, it updates the output, Q. If J and K are both 0, Q retains its old value. If only J is 1, Q becomes 1. If only K is 1, Q becomes 0. If both J and K are 1, Q becomes the opposite of its present state.

(a) Construct a JK flip-flop using a D flip-flop and some combinational logic.

(b) Construct a D flip-flop using a JK flip-flop and some combinational logic.  
  
Step 1 – Construct a Truth Table because I don’t know what to do.

|  |  |  |  |
| --- | --- | --- | --- |
| J | K | D | Q |
| 0 | 0 | Q | Q |
| 1 | 0 | 1 | 1 |
| 0 | 1 | 0 | 0 |
| 1 | 1 | NOT Q | OPPOSITE Q |

A diagram of a circuit

Description automatically generated

Figure 4 -A Circuit using AND circuits and MUX to make sure the values of Q are appropriate. Please note that the combination of J =0, k=1 does not have a connection to the D latch, this ensures that the value for D is 0. The rest makes sure that the value of Q is passed back to itself through a multiplexer. This is probably not the most efficient design – but it does work! Yup, just googled it, my design is worse – but I came up with it on my own!

A drawing of a diagram

Description automatically generated

Figure 4B – the D flip flop made out of the JK flip flop. All that we needed for it to be the D flip flop was elimination of the possibility that J and K were the same. This can be accomplished using an inverter from a single input ensuring that they are always different.

**Question\_5**

Using binary state encodings, complete a state transition table and output table for the

FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

I am sorry professor, I do not understand how to accomplish these problems, it appears that they need a table that lists the current state, the inputs, and next state. However I am not sure what it means to calculate the value of the next state when multiple values are passed to a single circle? I genuinely do not understand how to build these tables. I have watched multiple youtube videos describing how to make them and I am not grasping the idea.

Diagram, venn diagram

Description automatically generated

A table with numbers and letters

Description automatically generated

**A reminder of what the heck binary is for numbers. I will literally never remember.**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **S2** | **S1** | **S0** | **A** | **B** | **S2** | **S1** | **S0** |
| **0** | **0** | **1** |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| **0** | **1** | **0** |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| **0** | **1** | **1** |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| **1** | **0** | **0** |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| **1** | **0** | **1** |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| **1** | **1** | **0** |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
|  |  |  |  |  |  |  |  |
| **1** | **1** | **1** |  |  |  |  |  |
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|  |  |  |  |  |  |  |  |

**Question\_6**

Using binary state encodings, complete a state transition table and output table for the

FSM. Write Boolean equations for the next state and output and sketch a schematic of the FSM.

Diagram

Description automatically generated