**CSC 3100 Exam 2**

**Questions:**

A diagram of a state

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**A diagram of a number of circles and arrows

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**Figure 1-1 – State Diagram For Question 1**

A diagram of a function

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**Figure 1-2 Deduction that Z = NOT(X) based on the inputs and outputs.**

A diagram of a circuit

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**Let’s take a look at this Question 2, looks like there are 2 flip flops, A and B. Looks like A is a JK flip flop with inputs NOT B and X – which has an annoying state table , whereas B is a Toggle flip flop – which inverts states when T is 1. For sake of laziness we are going to assume the default state is 0. The transition table does not require us to calculate Z anyway, so don’t worry about it.**

**I literally cannot do intermediate states in my head, so they are included on the state transition diagram**

**Table 2 – State Transition Table For Question 2**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| **A** | **B** | **X = J** | **A’** | **B’ = K** | **T = X OR (A’)** | **‘A** | **‘B** |
| **0** | **0** | **0** | **1** | **1** | **1** | **0** | **1** |
| **0** | **0** | **1** | **1** | **1** | **1** | **1** | **1** |
| **0** | **1** | **0** | **1** | **0** | **1** | **0** | **0** |
| **0** | **1** | **1** | **1** | **0** | **1** | **1** | **0** |
| **1** | **0** | **0** | **0** | **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **1** | **1** | **0** | **1** |
| **1** | **1** | **0** | **0** | **0** | **0** | **1** | **1** |
| **1** | **1** | **1** | **0** | **0** | **1** | **1** | **0** |

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**Figure 2-1 Karnaugh Map For States to get state equations**

**S0 = A XOR B**

**S1 =**

**S3 = ABX’ + A’B’X**

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**Figure 2 – State Diagram For Question 2 – At this point I have noted that I did not notice the little circles for question 4, meaning all my work is invalid and I am running out of time.**

A diagram of a circuit

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**These are flip flops, which means if they achieve a value on the clock edge they are set to that new state. I am assuming they are edge triggered that are triggered on the rising edge of the clock – WAIT FUDGE THE LITTLE CIRCLE MEANS THAT IT IS FALLING CLOCK EDGE TRIGGERED THIS MEANS ALL MY PREVIOUS WORK IS INCORRECT CURSE YOU LITTLE CIRCLES I HATE YOU SO MUCH, which means that the current value of X is passed to the flip flop IF AND ONLY IF the clock FALLS It was not specified if these are synchronously or asynchronously resettable flip flops, I assumed they were asynchronous.**

**Let’s write down what we should expect:**

**Outputs should be z**

**Input is X and Clear, let’s represent these X1 and X0 so we can make the diagram look cleaner.**

**00**

**01**

**10**

**11**

**For A, there are clearly only 2 states: One where Q remains outputting 1, and one where Q remains outputting 0.**

**For B, it is similar to A, except there is a XOR gate between the output and input. Which means the output and input must NOT be equal. Ug. That’s too complicated to draw a diagram for, let’s make a truth table. It should be noted that this truth table does not take into account clock edge – as it is assumed the output is only on clock edge. There are briefly moments on the clock edge where the input x is opposite of the output y and z is equal to 1 as a result. This only occurs when X = 1, the clock has not risen, and Y = 0, or X = 0, the clock has not risen, and Y = 1.**

**Table 4-B-1- Truth table for 4(B) For clock edge FALLING only**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **X** | **CLEAR SIGNAL** | **CLEAR = NOT CLEAR** | **Y** | **Z = X XOR Y** |
| **0** | **0** | **1** | **0** | **0** |
| **0** | **1** | **0** | **0** | **0** |
| **1** | **0** | **1** | **0** | **1** |
| **1** | **1** | **0** | **1** | **0** |

**A drawing of a couple of circles

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**Figure 4-A-1- State Diagram for The Moore Machine.**

A diagram of a molecule

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**Figure 4 -B-1 -State Diagram for Problem 4 part B – Mealy Machine**

**A graph with red lines

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**Figure 4-2- Waveform diagram for Question 4. It**

A diagram of a circuit

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**This is made up of two parts, a DG latch, when G is up, the latch is transparent, meaning outputs change based on current inputs, when G is down, it means that the previous input is retained regardless of change in A. and a JK flip flop (which is an abomination). The CLK is a falling edge clock because of the little circle.**

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**Figure 3 – Timing diagram for question 3**

A diagram of a circuit

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**Professor, did you create your truth table correctly? Please note that the equation for Y0 is NAND(NOT X, NOT Y, NOT E), but for entry (0,0,0) which should be be (1,1,1) which would be NAND = 0. However this is not the case on your truth table.**

A diagram of a circuit

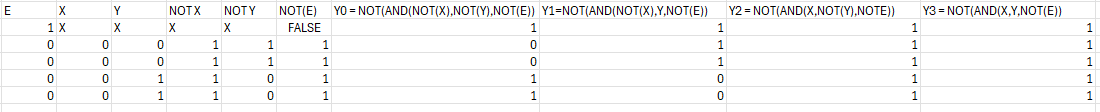
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**Figure 6-1 – Looking at the equations, and the results DO NOT match your truth table. However, I am one hundred percent certain on these equations**

A diagram of a circuit

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**Your truth table marks Y3 as 0 for this, however following the entries through the circuit, it is very clearly 1.**



**Table 6 – Truth Table For The Pictured Circuit.**