COSE321 Computer Systems Design

Assignment #1

No late turn-in accepted

Follow the "Lab setup instructions" on the class page, and finish until the page #22.

What and How to submit:
Open the generated elf "csd_lab.elf" as shown in the lab, take a screenshot and upload it to Blackboard before the class.

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class_experiments_v21 - csd_lab/Debug/csd_lab.elf - Vitis IDE

File Edit Search Xilinx Project Window Help

Design Debug

Explorer

- csd_lab.elf - [arm/le]
  - csd_lab_Debug.build.ui.log
  - csd_lab.elf.size
  - makefile
  - objects.mk
  - sources.mk
  - Xilinx.spec
- src
  - csd_asm.S
  - csd_main.c
  - platform.config.h

csd_asm.S   csd_main.c   csd_lab.elf

```
100578:   f3af 8000    nop.w
10057c:   e8bd 4008    ldmia.w sp!, {r3, lr}
100580:   e7be         b.n 100500 <register_tm_clones>
100582:   bf00         nop

00100584 <main>:
.extern csd_main

.global main

main:
    mov r0, #10
100584:   e3a0000a     mov r0, #10
    mov r1, #3
100588:   e3a01003     mov r1, #3
    add r0, r0, r1
10058c:   e0800001     add r0, r0, r1
    ldr r0, =src
100590:   e59f002c     ldr r0, [pc, #44]    ; 1005c4 <forever+0x8>
    ldr r1, =dst
100594:   e59f102c     ldr r1, [pc, #44]    ; 1005c8 <forever+0xc>
    mov r2, #16
100598:   e3a02010     mov r2, #16

0010059c <loop>:
```

Outline

There is no active editor that provides an outline.

Assistant

- csd_lab_system [System]
  - csd_lab [Application]
    - **Debug**
    - Release
  - csd_platform [Platform]

Console   Problems   Vitis Log   Guidance

Build Console [csd_lab, Debug]

14:05:08 Build Finished (took 1s.500ms)