CEG 3136 – Computer Architecture II
Tutorial 3 – The Parallel Ports
Fall 2019

Consider loading the values in to the following registers as shown below:
DDRA: Binary value 11110000
PORTA: Binary value 00000000

1) If PUPAE in the PUCR register is set to 0, what can be said about the voltage levels that will appear at PA0 to PA3?

***If no key is pressed*, the voltage levels on pins PAx (x=0,1,2,3) <u>will float</u> as there is no active element connected to the pins that drive the voltages to any level.**

***If a key linked between* Col_x (x = 0,1,2,3) *and* Row_y (y = 0,1,2,3) *is pressed*, a connection will be made from pin PAx (a PORTA input) to the corresponding Row_y line (y = 0,1,2,3) linked to a PORTA output. Since PORTA=%0000**0000** (PA(y+4)=0), Row_y line is connected to ground, and the voltage at pin PAx will be subsequently 0. If Row_y lines would be connected to +5V (PORTA = %1111**0000**, i.e., PA(y+4) = 1), then the voltage at PAx would be +5V.**

What if PUPA is set to 1?

***If no key is pressed*, the voltage levels at the pins PAx <u>will be 5V</u> since pullup resistors have been activated (**PUPAE = 1**) and will drive the pins to this level.**

***When a key is pressed*, the voltage level at the (column) pin connected to that key is brought down to 0V since the corresponding Row_y line is connected to ground, i.e., PA(y+4) = 0 (PORTA=%0000**0000**). The pin PAx would stay at +5V if Row_y would be connected to +5V, i.e., PA(y+4) = 1 (identical behaviour like in the previous case, when** PUPAE=0**).**

2) What bit patterns would you find in PORTA (data register) when pressing the following keys (assume that PUPAE is set to 1):
   a. 1: 0000 1110
   b. 4: 0000 1110
   c. 0: 0000 1101
   d. C: 0000 0111
   e. 3: 0000 1011
   f. #: 0000 1011
3) Note that some bits patterns are the same for different keys in question 2. Any idea how you could change the register contents of PORT A to be able to differentiate keys? **To differentiate keys only one output bit should be cleared to zero. Consider the keys 1 and 4. Clearing bit 4 to zero in PORTA (and setting bits 5 to 7 to 1) would mean that bit 0 becomes zero when key 1 is pressed but remains 1 when key 4 is pressed. Similarly setting bit 5 in PORTA (and setting bits 4, 6, 7 to 1) would mean that bit 0 becomes 0 when key 4 is pressed and remains 1 when key 1 is pressed. Now the bit patterns that appears in PORTA for keys 1 and 4 becomes:**
   a. **1: 1110 1110**
   b. **4: 1101 1110**

   Keep in mind that the bits 4 to 7 must be set by the CPU, while bits 0 to 3 are set by the hardware.

4) Given the logic from question 3, complete the table on the next page to show what differentiating bit patterns would appear in PORTA when each key is pressed.

Key	PA7	PA6	PA5	PA4	PA3	PA2	PA1	PA0
1	1	1	1	0	1	1	1	0
2	1	1	1	0	1	1	0	1
3	1	1	1	0	1	0	1	1
A	1	1	1	0	0	1	1	1
4	1	1	0	1	1	1	1	0
5	1	1	0	1	1	1	0	1
6	1	1	0	1	1	0	1	1
B	1	1	0	1	0	1	1	1
7	1	0	1	1	1	1	1	0
8	1	0	1	1	1	1	0	1
9	1	0	1	1	1	0	1	1
C	1	0	1	1	0	1	1	1
*	0	1	1	1	1	1	1	0
0	0	1	1	1	1	1	0	1
#	0	1	1	1	1	0	1	1
D	0	1	1	1	0	1	1	1