CEG 3136 – Computer Architecture II
Tutorial 6 – Interrupts
Fall 2019

Part A – The circuit for invoking an IRQ

Design and draw a circuit to attach a push button switch to the IRQ line of the HCS12. You must provide hardware debouncing. Define all details in your circuit – pin numbers, connections to Vcc (5 volts) and ground.

Available parts:

74VHCT14 Schmidt Inverter (see attached data sheet)
Resistors: 1 kΩ, 10kΩ, 100kΩ, 1MΩ,
Capacitors: 1 μF, 2 μF, 5 μF, 10 μF
One push button switch

Important facts –

1) The equation for voltage change when charging a capacitor: $V_{cap} = V_{cc}(1 - e^{-t/\tau})$, where τ = RC (R in ohms and C in farads).
2) The voltage across the capacitor must not reach 2V within 1 ms.

Part B - Developing the software

Each time the switch is pressed, an IRQ is generated. Develop the software to meet the following requirements:

1) When the button switch has been pressed 10 times, display on the terminal the message "WOW, this interrupt stuff really works".

The main routine should be the code that displays the message. Use the IRQ ISR to decrement a counter that the main routine monitors and resets.

Option: Modify your code so that an asterisk "*" is displayed each time the button switch is pressed. Again, do not use the ISR to display the asterisk. You will need to set up communication between the ISR and the main code.

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74VHCT14A
Hex Schmitt Inverter

General Description

The VHCT14A is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. The VHCT14A contains six independent inverters which are capable of transforming slowly changing input signals into sharply defined, jitter-free output signals.

Protection circuits ensure that 0V to 7V can be applied to the input pins without regard to the supply voltage and to the output pins with V_{CC} = 0V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3V to 5V systems and two supply systems such as battery backup.

Features

- High speed: t_{PD} = 5.0 ns (typ) at T_A = 25°C
- High noise immunity: V_{IH} = 2.0V, V_{IL} = 0.8V
- Power down protection is provided on all inputs and outputs
- Low noise: V_{OLP} = 1.0V (max)
- Low power dissipation:
  I_{CC} = 2 μA (max) @ T_A = 25°C
- Pin and function compatible with 74HCT14

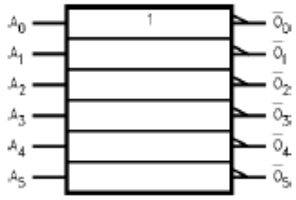
Ordering Code:

Order Number	Package Number	Package Description
74VHCT14AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
74VHCT14ASJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHCT14AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT14AMTCX_NL (Note 1)	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHCT14AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

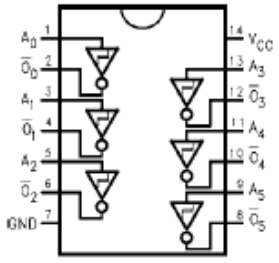
Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Note 1: "_NL" indicates Pb-Free package (per JEDEC J-STD-020B). Device available in Tape and Reel only.

Logic Symbol



Connection Diagram



Pin Descriptions

Pin Names	Description
A_n	Inputs
$\overline{O}_n$	Outputs

Truth Table

A	$\overline{O}$
L	H
H	L