Lab1_Team6_Report

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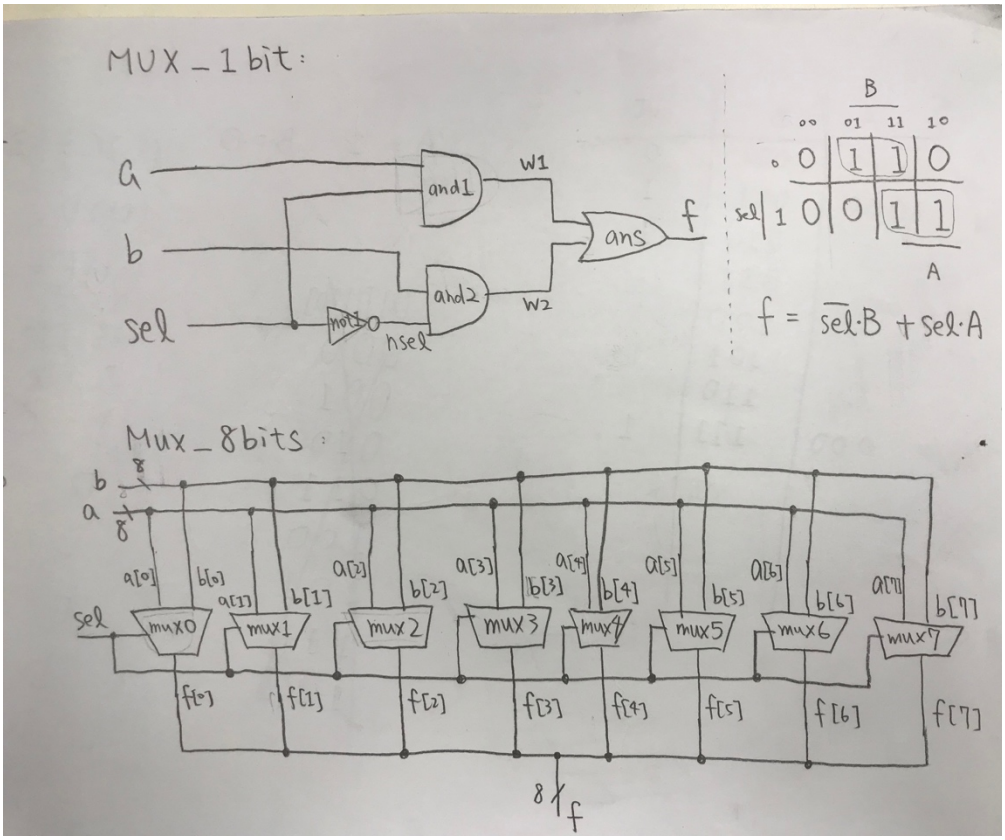
Question 1:

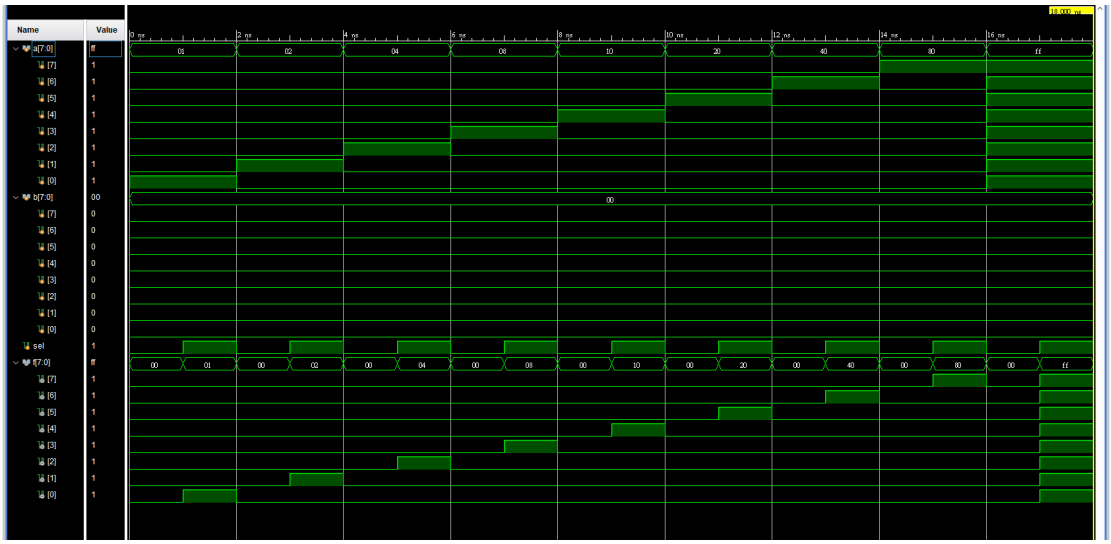
1. Gate-level schematics:



2. Design Explanation:
   - By truth table and K-map, we can derive the Boolean expression for a 1-bit multiplexor.
   - Using 8 1-bit multiplexors, we can select the right bit from the two 8-bit inputs for the output.

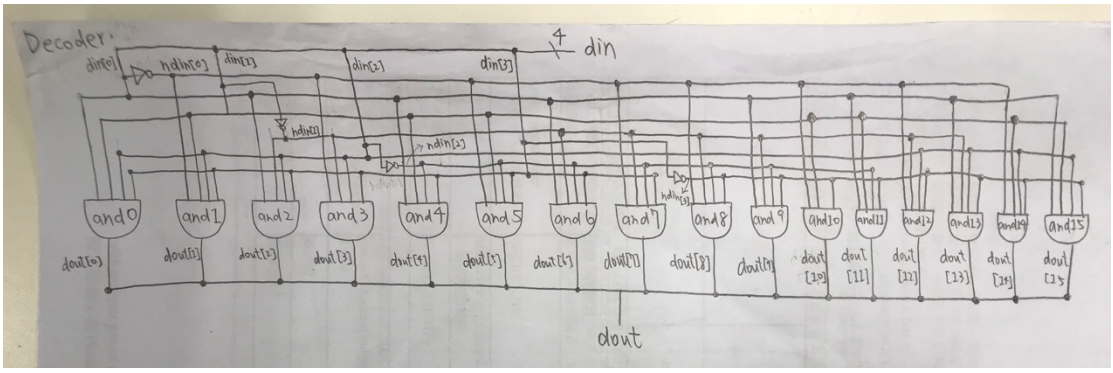
3. Testing:

- I generated 8 patterns, each tested with two selections (1 and 0) to check if every bit is working properly.



Question 2:

1. Gate-level schematics:

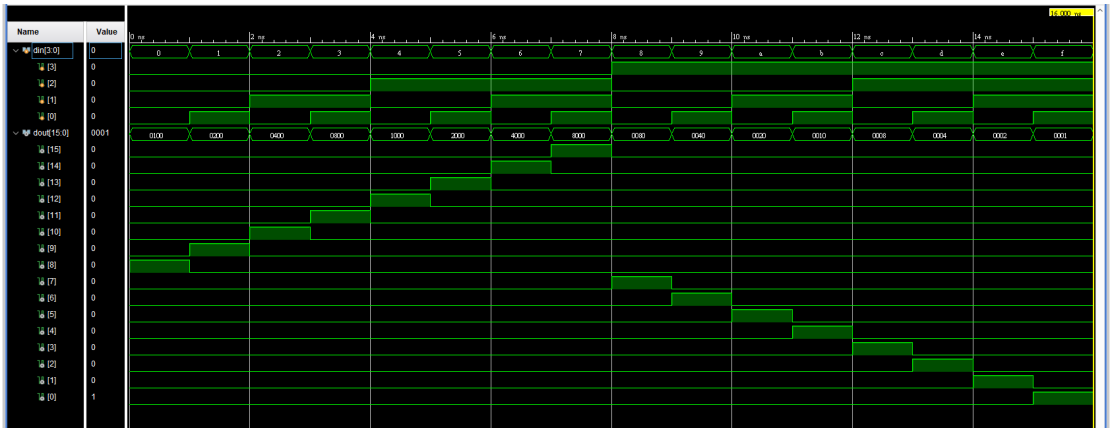


2. Design Explanation:

- I tried to make a 4 to 16 with 2 to 1 decoders, but in vain. Therefore, we decided to generate the Boolean expression for every bit and convert the expressions into logic gates.

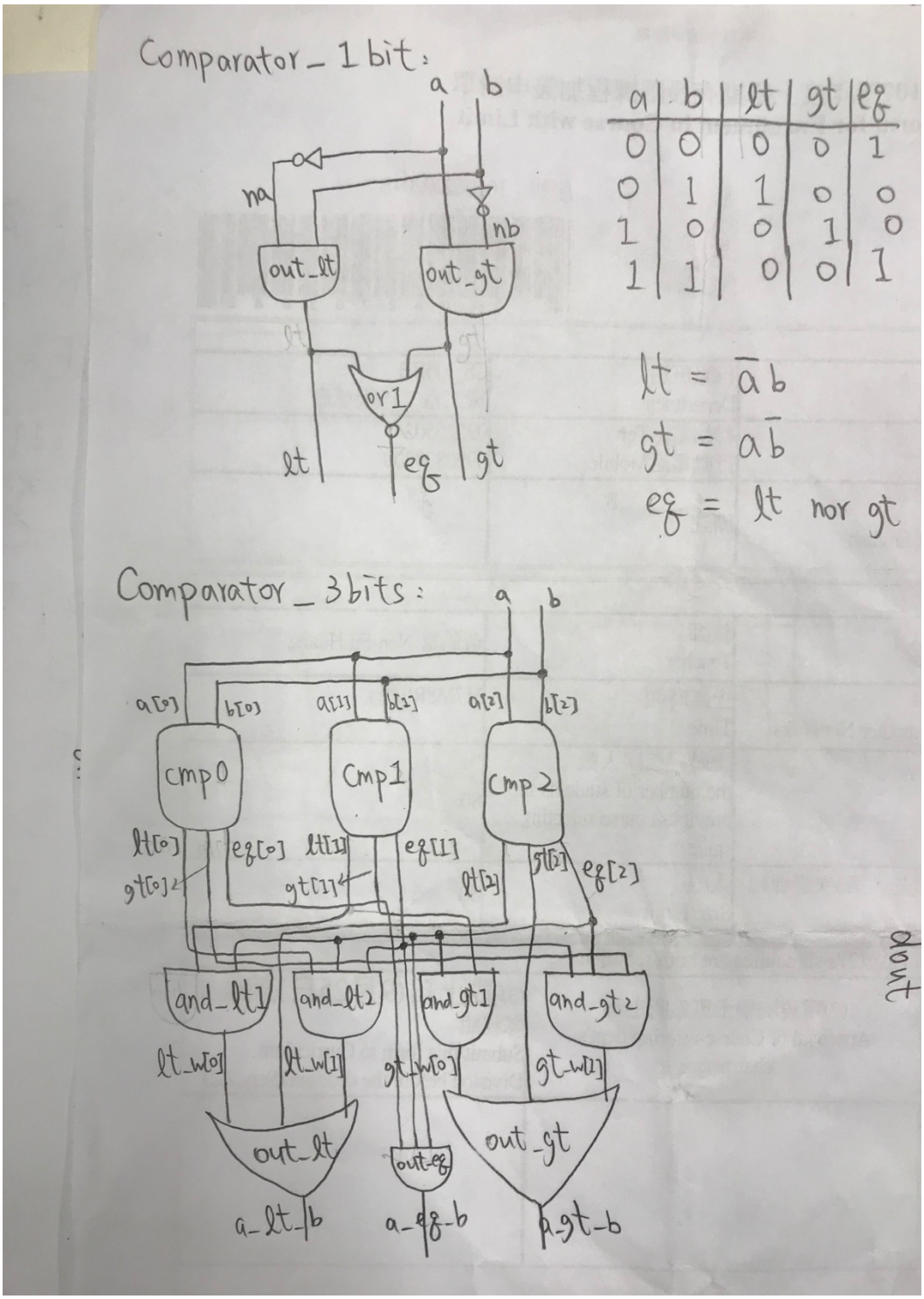
3. Testing:

- I generated all the possibilities and checked if every test pattern yields the correct result.



Question 3:

1. Gate-level schematics:

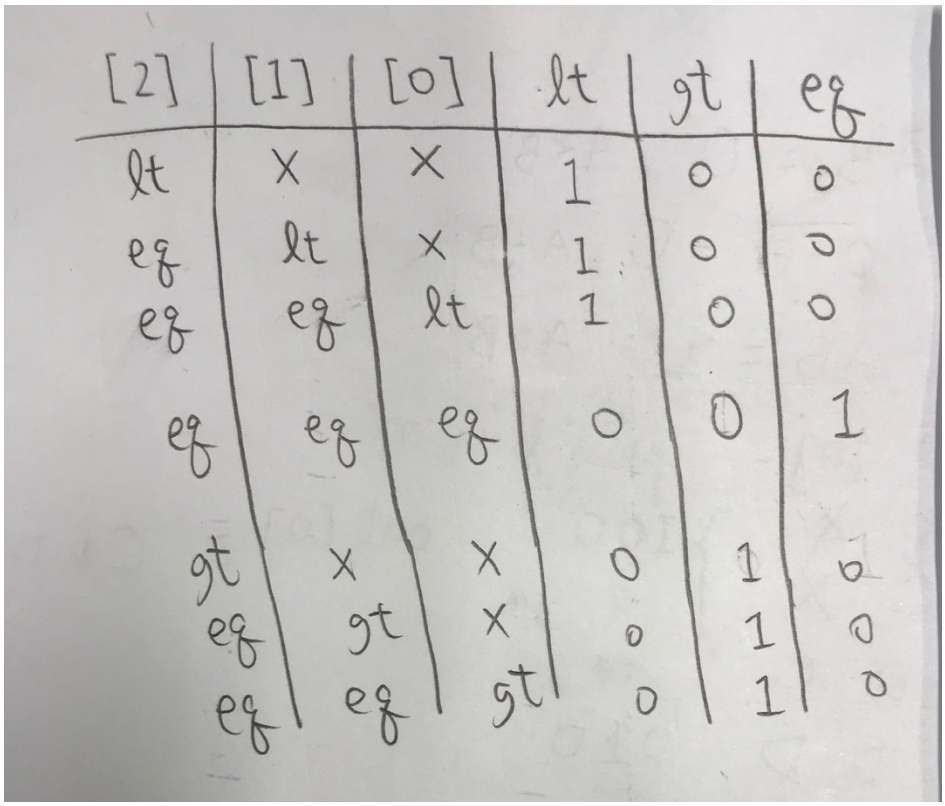


2. Design explanation:

- Derived a 1-bit comparator by truth table. Took some time to

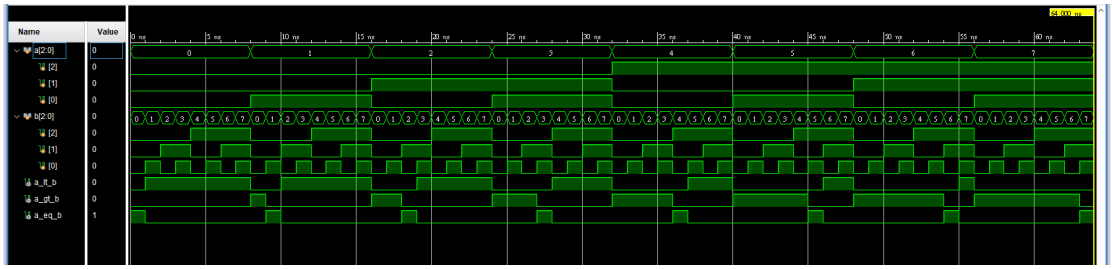
figure out the simplicity of using nor gate.

- Tried to make a 3-bit comparator using 3 1-bit comparators. Drew a truth table to derive the Boolean expression for the three outputs.



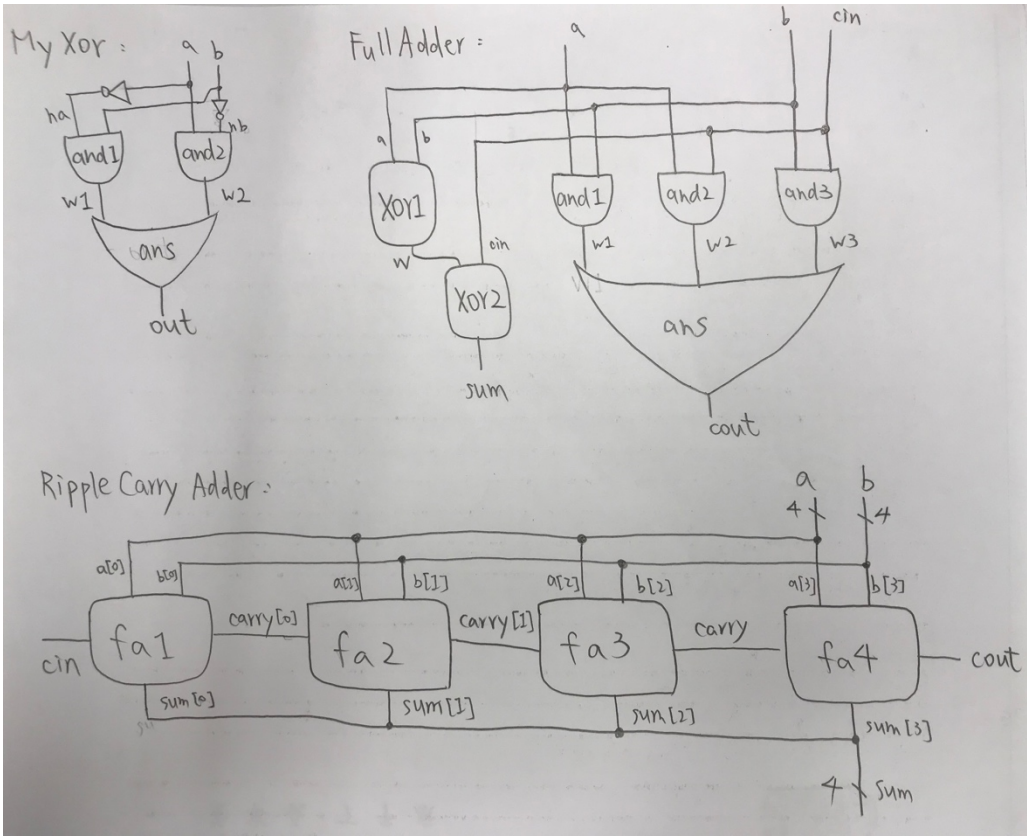
[2]	[1]	[0]	lt	gt	eq
lt	X	X	1	0	0
eq	lt	X	1	0	0
eq	eq	lt	1	0	0
eq	eq	eq	0	0	1
gt	X	X	0	1	0
eq	gt	X	0	1	0
eq	eq	gt	0	1	0

3. Testing:
   - I generated all the possibilities and checked the results with the wave form.



Question 4:

1. Gate-level schematic:

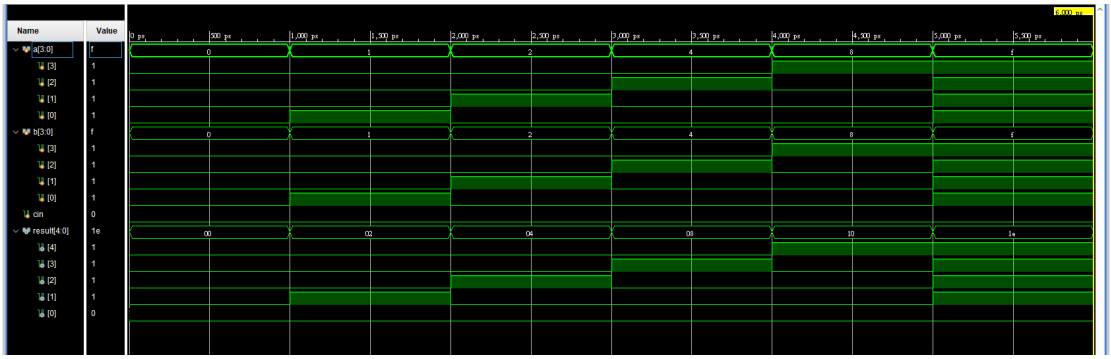


2. Design explanation:

- Derived from truth table, MyXor is an alternative to the xor gate.
- With the help of professor Lee's keynotes, a full adder is made effortlessly.
- Again, with the hints in professor's keynotes, the ripple carry adder is made without breaking a sweat.

3. Testing:

- I generated 8 test patterns to test if each bit adds properly. The last test pattern with two maximum numbers tests if all works together smoothly and the last carry is valid.



What I've learned:

- Always check the number of bits of every signal. I spent a lot of time debugging the ripple carry adder, only to find out the problem is the signal in the test bench, not the design.
- A basic review of last semester's logic design.
- Some Verilog coding techniques that my teammate taught me.
- Realized the power of truth table.
- Had a better sense of what is actually going on in the wave forms (nWave is Greek to me).
- 王駿：除了複習了上學期所教有關 mux,decoder,carry, comparator 等等東西, 也更了解這學期才開始使用的 Vivado 的操作.加上之前並不會要求由我們自己打 Testbench,所以這也算是一大挑戰. 此外,Lab1 要求我們全部都只能用 gate level 來進行 coding, 這對於已經習慣用 behavior 的我來說也算是一大難關。

Contributions:

- 王駿 wrote the first three questions, and 陳騰鴻 did the last one.
- 陳騰鴻 then read his code and revised a little bit of each design.
- Finally, 陳騰鴻 wrote all the test benches and did the report.