Homework 07: AntVengers!

Due on Jun 04 23:59

Objective

In this assignment, you are going to design a simple finite-state machine to explore and escape the maze with limited inputs from outside environment. In addition, you can also learn some Verilog coding and shell script tricks which may help you not only in HDL coding but also software programming, including

1. The way to import data from an ASCII file to a memory in Verilog;
2. The ability to pass a string or number to the Verilog simulator at runtime;
3. The style of using a header file with `define in Verilog;
4. The usage of the compiler directives, `ifdef/`endif in Verilog;
5. The usage of the task in Verilog;
6. The usage of simple shell scripts to help simplify the simulation.

Problem Description and Design Specification

You woke up and found yourself becoming an Ant-Man (or Wasp?!), being trapped in a dark Maze Universe!! You also lost the eyesight! But instead, you got two antennae, left and right. In the first place, you know that you need to escape the Maze Universe (and save the world, of course. With Great Power Comes Great Responsibility, you know)!

Using the two antennae as the inputs you can sense the Maze walls. Design the finite-state machine to explore and escape the maze universe.

1. Please read hw07-2_AntVengers.pdf for the detailed problem description.
   a. Read the hw07-3_00_README.txt for the description about each source file and the simulation details too.
   b. Look into the source file. Remember that the source code is the best documentation to a programmer.
2. Your mission is to replace the ant_suit.v. Note that the sample module is just a Zombie who walks in a fixed order of moves.
3. Test your Ant Suit with the different mazes. Design your own ones with the size bigger than 15x15.
4. We also list two challenges for you:
   a. Challenge of narrow corridors and/or narrow corners
   b. Challenge of wall islands
5. You have to discuss the possible solution to either one of the challenges in details. Pick

the one you like.

6. To gain extra points, you can propose possible solutions to both the challenges. You can also provide the solutions to either one challenge or both, in Verilog.
7. Write a report to summarize all the discussions.

   NOTE:

   No score if you simply cut-and-paste waveforms or draw some diagram without proper discussion.

Note

1. **Raise the discussion for any questions when in doubt.**
2. **Submit the source code and the electrical report based on TA's instructions.**