CS2102 02 Digital Logic Design June 01, 2018

Final Assignment: Convolution Engine for Image Processing

Due on Jun 25 23:59

Objective

In this final assignment, you are going to design a simple convolution engine for the edge detection of image processing applications. Please refer to Wikipedia for more details. In addition, you can also learn some more Verilog coding and also software programming skills:

- Verilog coding skill with file IO and array;
- 2. Verilog design style and hand-shaking with timing consideration;
- 3. Verilog design style with SRAM block;
- 4. The usage of Makefile.

Note:

- a. For Makfile, you may refer to online resources such as 鳥哥的 Linux 私房菜 http://linux.vbird.org/linux_basic/1010index.php
- b. Source code is the best document!

Problem Description and Design Specification

We are going to design a 5x5 convolution filter (kernel) of edge detection. The input is a gray-scale 256x256 image.

- 1. Please read final-2.pdf for the further details.
- 2. The design template can be found in conv_engine2018_vX.tgz, where vX denotes the version (which can be v1, v2, etc.). Always check for the latest version. Under Linux/Unix, use the follow command to extract the tar-gzipped file:
 - \$ tar zxvf conv_engine2018_vX.tgz
- 3. Look into load_bmp.v, which is the main testbench. Learn what the testbench does to load the image, convert the pixels into the gray-scale ones, and store into the SRAM.
- 4. Stuey the IO signals, block diagram and timing. Your mission is to design filter.v.
- 5. Learn how to use Makefile to integrate the simulation.
- 6. Complete and verify your design with the golden responses. The testbench will also convert your outputs in the SRAM to a BMP file. You may look into the details.
- 7. Write a report to summarize all the discussions.

Note

- 1. Raise the discussion for any questions when in doubt.
- 2. Submit the source code and the electrical report based on TA's instructions.
- 3. No score if you simply cut-and-paste waveforms or draw some diagram without proper discussion.

Most importantly, enjoy your final project!!