Homework 02: Verilog Practice

Due on March 22 23:59pm

1. Design a game box of Rock-Paper-Scissors game (you know the game well). Rock beats scissors; paper beats rock; and scissors beat paper. There are two players, R and S, which are represented by two 2-bit vectors. That is, $R = \{r1, r0\}$, and $S = \{s1, s0\}$, respectively. Each player enters a two-bit vector to indicate rock, paper, or scissors. So there are four input bits, $\{r1, r0, s1, s0\}$. The two-bit output $\{y1, y0\} = 01$ indicates that the player R wins; $\{y1, y0\} = 10$ indicates that the player S wins. The output is 11 when there is a tie (that is, when the two players enter the same input and no one wins). If anyone enters an invalid input 00, the output will be invalid (i.e., 00). The coding of input and output is defined as follows:

	Inputs $\{r1, r0\}$ or $\{s1, s0\}$
Rock	01
Paper	10
Scissors	11
Invalid	00

	Outputs $\{y1, y0\}$
R wins	01
S wins	10
Tie	11
Invalid	00

For example, if $\{r1, r0, s1, s0\} = 1001$, it means R is paper and S is rock; R wins. Therefore, the output $\{y1, y0\}$ will be 01.

a. List the truth table of the game box.
b. Design a Verilog module to realize the game box. Write a testbench to verify the design.
c. Write a short report of a paragraph or two to summarize whether you encounter problems, and how you solve them. Also attach the simulation result and a screenshot of the waveform.

Hint: You may start with the majority circuit as a reference, modify and extend its Verilog code.

Note: Submit the source code and the electrical report based on TA's instructions.