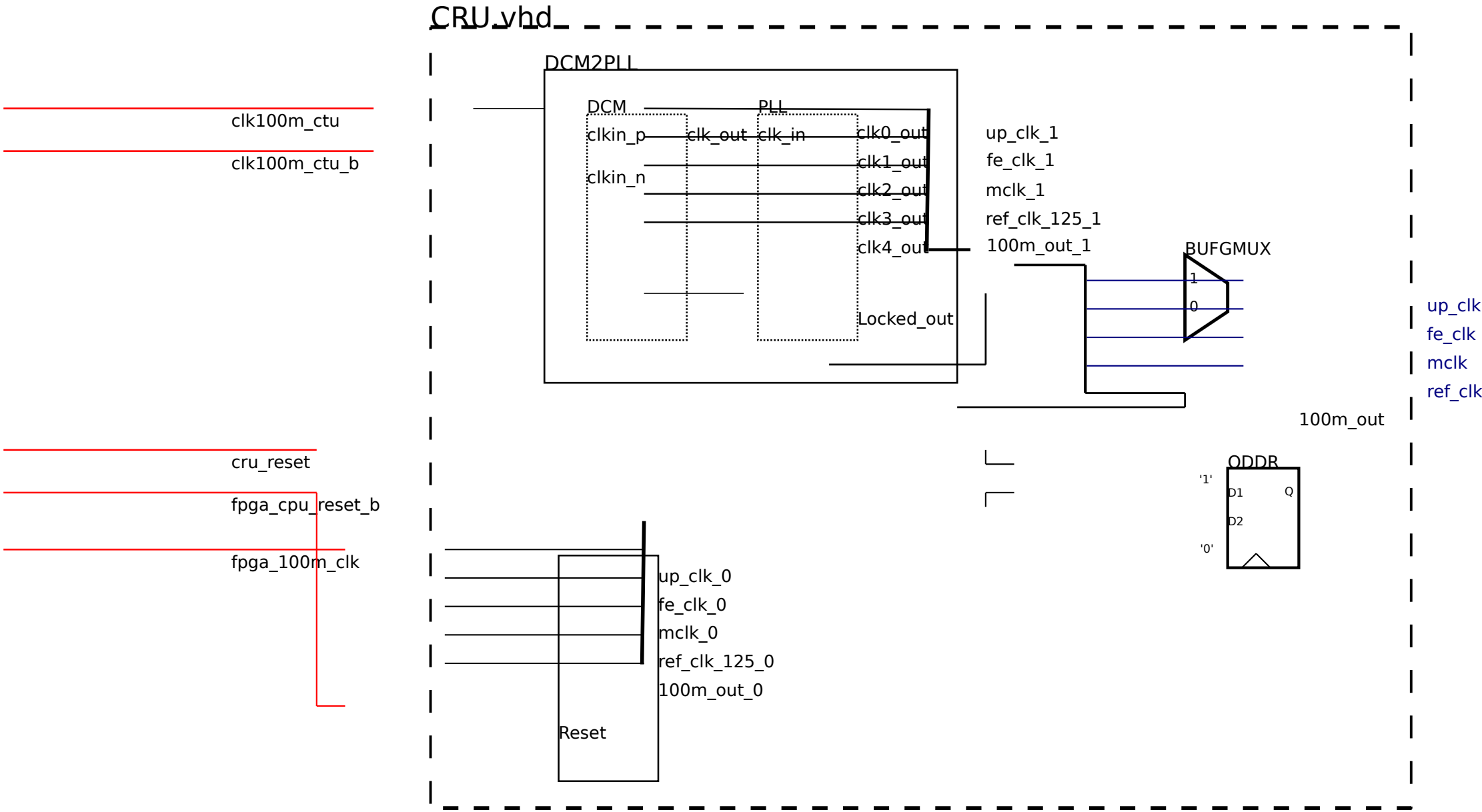
CRU.vhd
DCM2PLL
DCM
PLL
clkin_p
clkin_n
clk_out
clk_in
clk0_out
clk1_out
clk2_out
clk3_out
clk4_out
Locked_out
up_clk_1
fe_clk_1
mclk_1
ref_clk_125_1
100m_out_1
BUFGMUX
1
0
up_clk
fe_clk
mclk
ref_clk
100m_out
ODDR
'1'
D1
D2
'0'
Q
clk100m_ctu
clk100m_ctu_b
cru_reset
fpga_cpu_reset_b
fpga_100m_clk
up_clk_0
fe_clk_0
mclk_0
ref_clk_125_0
100m_out_0
Reset