//	
	//
// 선행처리 지시	// 시스템에서 사용할 전역 변수 선언
//	
	//
#include "DSP28x_Project.h" // Device Headerfile and Examples Include File	Uint16 Loop_cnt;
	Uint16 SW1_cnt, SW2_cnt, SW3_cnt, SW4_cnt, SW1;
#define SYSTEM_CLOCK 150E6 /* 150MHz */	Uint16 ADC_value01;
#define TBCLK 150E6 /* 150MHz */	Uint16 BackTicker;
//	Uint16 EPwm5IsrTicker;
	float32 PWM_DUTY_RATIO_A = 0.2;
	float32 PWM_CARRIER = 20E3;
//	float32 PwmDutyRatioA;
// 함수 선언	float32 FallingEdgeDelay:
//	float32 RisingEdgeDelay;
void InitEPwm5Module(void);	//
interrupt void EPwm5Isr(void);	
//isr함수 선언	
<pre>interrupt void Xint3_isr(void);</pre>	//
interrupt void Xint4_isr(void);	
interrupt void Xint5_isr(void);	// 메인 함수 - 시작
<pre>interrupt void Xint6_isr(void);</pre>	//
//	void main(void)
	{
	//

	====	150MHz/(1*2) = 75MHz
// Step 1. Disable Global Interrupt		
//		
DINT:		//
IER = 0x0000;		
IFR = $0x0000$;		
//		//
	====	
		// Step 3. 인터럽트 초기화:
		//
//		InitPieCtrl():
// Step 2. 시스템 컨트롤 초기화:		IER = 0x0000;
//		IFR = $0x0000$;
InitSysCtrl();		/*
		Step 4
EALLOW:		4.1 Pie Vector Table Re-allocation
SysCtrlRegs.HISPCP.bit.HSPCLK = 1; HSPCLK = SYSCLKOUT/(HISPCP*2)	//	*/
GpioCtrlRegs.GPAPUD.bit.GPIO8 = 0; pull-up on GPIO6 (EPWM5A) */	/* Enable	InitPieVectTable();
GpioCtrlRegs.GPAPUD.bit.GPIO9 = 0; pull-up on GPIO7 (EPWM5B) */	/* Enable	
GpioCtrlRegs.GPAMUX1.bit.GPIO8 = 1; GPIO6 as EPWM5A */	/* Configure	
GpioCtrlRegs.GPAMUX1.bit.GPIO9 = 1; GPIO7 as EPWM5B */	/* Configure	/*
EDIS;	// HSPCLK =	Step 5

5.1 Interrupt Service routine re-mapping and Interrupt vector enable	Step 6 6.1 Initialize Periphrals for User Application
*/	*/
/* Interrupt Service Routine Re-mapping */	/* Initialize EPWM4 Module */
EALLOW:	InitEPwm5Module():
PieVectTable.EPWM5_INT = &EPwm5Isr	
EDIS;	//
// Vector Remapping	// Step 3. ADC 초기화
EALLOW;	//
PieVectTable.XINT3 = &Xint3_isr;	
PieVectTable.XINT4 = &Xint4_isr;	InitAdc();
PieVectTable.XINT5 = &Xint5_isr;	
PieVectTable.XINT6 = &Xint6_isr;	// ADC 설정
EDIS;	AdcRegs.ADCTRL3.bit.ADCCLKPS = 3; // ADCCLK = HSPCLK/(ADCCLKPS*2)/(CPS+1)
//	AdcRegs.ADCTRL1.bit.CPS = 1; // ADCCLK = 75MHz/(3*2)/(1+1) = 6.25MHz
/* Enable PIE group 3 interrupt 4 for EPWM4_INT */	AdcRegs.ADCTRL1.bit.ACQ_PS = 3; // 샘플 /홀드 사이클 = ACQ_PS + 1 = 4 (ADCCLK기준)
PieCtrlRegs.PIEIER3.bit.INTx5 = 1;	AdcRegs.ADCTRL1.bit.SEQ_CASC = 1; // 시퀀 스 모드 설정: 직렬 시퀀스 모드 (0:병렬 모드, 1:직렬 모드)
(Englis CDU INTO for EDWINA INT . /	AdcRegs.ADCMAXCONV.bit.MAX_CONV1 = 1; // ADC 채널수 설정: 2개(=MAX_CONV+1)채널을 ADC
/* Enable CPU INT3 for EPWM4_INT */ IER = M_INT3;	AdcRegs.ADCCHSELSEQ1.bit.CONV00 = 0; // ADC 순서 설정: 1번째로 ADCINAO 채널을 ADC
	AdcRegs.ADCCHSELSEQ1.bit.CONV01 = 8; // ADC 순서 설정: 2번째로 ADCINBO 채널을 ADC
/*	//

	//
//	==
	EALLOW;
// GPIO 초기화	GpioCtrlRegs.GPBCTRL.bit.QUALPRD1 = 0xFF; // (GPIO40~GPIO47) Qual period 설정
//	GpioCtrlRegs.GPBQSEL1.bit.GPIO44 = 2; // Qualification using 6 samples
EALLOW;	GpioCtrlRegs.GPBQSEL1.bit.GPIO45 = 2; // Qualification using 6 samples
GpioCtrlRegs.GPBMUX1.bit.GPIO44 = 0; // 핀 기 선택: GPIO44	GpioCtrlRegs.GPBQSEL1.bit.GPIO46 = 2; // Qualification using 6 samples
GpioCtrlRegs.GPBMUX1.bit.GPIO45 = 0; // 핀 기 선택: GPIO45	GpioCtrlRegs.GPBQSEL1.bit.GPIO47 = 2; //
GpioCtrlRegs.GPBMUX1.bit.GPIO46 = 0; // 핀 기 선택: GPIO46	Qualification using 6 samples EDIS:
GpioCtrlRegs.GPBMUX1.bit.GPIO47 = 0; // 핀 기 선택: GPIO47	//
GpioCtrlRegs.GPBDIR.bit.GPIO44 = 0; GPIO44 입출력 선택: Input	//
GpioCtrlRegs.GPBDIR.bit.GPIO45 = 0; GPIO45 입출력 선택: Input	
GpioCtrlRegs.GPBDIR.bit.GPIO46 = 0; GPIO46 입출력 선택: Input	// //
GpioCtrlRegs.GPBDIR.bit.GPIO47 = 0; GPIO47 입출력 선택: Input	// Step 6. XINT 초기화
EDIS;	//
//	== EALLOW;
	GpioIntRegs.GPIOXINT3SEL.bit.GPIOSEL = 47; // 외 부 인터럽트 XINT3로 사용할 핀 선택: GPIO47
	GpioIntRegs.GPIOXINT4SEL.bit.GPIOSEL = 46; // 외 부 인터럽트 XINT4로 사용할 핀 선택: GPIO46
//	== GpioIntRegs.GPIOXINT5SEL.bit.GPIOSEL = 45; // 외 부 인터럽트 XINT5로 사용할 핀 선택: GPIO45
// Step 5. Qualification 초기화	GpioIntRegs.GPIOXINT6SEL.bit.GPIOSEL = 44; // 외

무 인터럽트 XIN16로 사용할 핀 선택: GP1044	
EDIS;	// Step 7. Initialize Application Variables
XIntruptRegs.XINT3CR.bit.POLARITY = 0; // XINT3 인터럽트 발생 조건 설정: 입력 신호의 하강 엣지 XIntruptRegs.XINT4CR.bit.POLARITY = 0; // XINT4 인터럽트 발생 조건 설정: 입력 신호의 상승 엣지 XIntruptRegs.XINT5CR.bit.POLARITY = 0; // XINT5 인터럽트 발생 조건 설정: 입력 신호의 하강 엣지 XIntruptRegs.XINT6CR.bit.POLARITY = 0; // XINT6 인터럽트 발생 조건 설정: 입력 신호의 하강 & 상승 엣지	//
XIntruptRegs.XINT3CR.bit.ENABLE = 1; // XINT3 인터럽트 : Enable XIntruptRegs.XINT4CR.bit.ENABLE = 1; //	ADC_value01 = 0; BackTicker = 0; EPwm5IsrTicker = 0;
XINT4 인터럽트: Enable XIntruptRegs.XINT5CR.bit.ENABLE = 1: // XINT5 인터럽트: Enable XIntruptRegs.XINT6CR.bit.ENABLE = 1: // XINT6 인터럽트: Enable	PwmDutyRatioA = PWM_DUTY_RATIO_A; FallingEdgeDelay = (1.0 / TBCLK) > EPwm5Regs.DBFED;
AINTO 한타입으 · Ellable	RisingEdgeDelay = (1.0 / TBCLK) > EPwm5Regs.DBRED;
시/ 외부 인터터트 포합된 생각 기타를 받아 기타를 보고 기타를 가는 기타를 받아 기타를	//=====================================
PieCtrlRegs.PIEIER12.bit.INTx3 = 1: // PIE 인 터럽트(XINT5) : Enable	//
PieCtrlRegs.PIEIER12.bit.INTx4 = 1; // PIE 인 터럽트(XINT6): Enable	// Enable global Interrupts and higher priority real-time debug events:
IER = M_INT12: // CPU 인터럽 트(INT12) : Enable	//

```
EINT;
        // Enable Global interrupt INTM
                                                 EPwm5Regs.DBRED;
  ERTM;
         // Enable Global realtime interrupt DBGM
                                                        PWM_CARRIER = 20E3;
//-----
_____
                                                        PwmDutyRatioA =
                                                                          ((float32)ADC_value01
                                                 (float32)65535 )*(float32)0.475;
                                                        EPwm5Regs.TBPRD = (TBCLK / PWM_CARRIER)
                                                 / 2;
//----
                                                        EPwm5Regs.CMPA.half.CMPA
_____
                                                 (EPwm5Regs.TBPRD + 1) * PwmDutyRatioA;
  // IDLE loop. Just sit and loop forever :
                                                        EPwm5Regs.CMPB = (EPwm5Regs.TBPRD + 1) *
                                                 (1 - PwmDutyRatioA);
  for (;;)
                                                        Loop_cnt++;
    AdcRegs.ADCTRL2.bit.SOC_SEQ1
// ADC 시퀀스 시작
                                                        BackTicker++;
    DELAY_US(0.64L);
                                   // ADC 시퀀
스 변환시간(약0.64usec)만큼지연
                                                        SW1_cnt = 0;
    ADC_value01
                           AdcRegs.ADCRESULT0;
                                                     }
 // ADC 결과 저장
                                                      else if (SW1 == 1 && SW3_cnt % 2 == 1 &&
                                                 SW4_cnt \% 2 == 0)
    if (SW1 == 1 \&\& SW3\_cnt \% 2 == 0 \&\& SW4\_cnt
% 2 == 0)
    {
                                                        EPwm5Regs.DBFED = 0;
                                                        EPwm5Regs.DBRED = 0;
      EPwm5Regs.DBFED = 0;
                                     /* 1usec,
Falling Edge Delay */
                                                        FallingEdgeDelay
                                                                           (1.0)
                                                                                     TBCLK)
                                                 EPwm5Regs.DBFED;
      EPwm5Regs.DBRED = 0;
                                     /* lusec,
Rising Edge Delay */
                                                        RisingEdgeDelay
                                                                           (1.0)
                                                                                     TBCLK)
                                                 EPwm5Regs.DBRED;
      FallingEdgeDelay
                                   TBCLK)
                          (1.0)
EPwm5Regs.DBFED;
                                                        PWM_CARRIER = 20E3;
                                                        PwmDutyRatioA
                                                                     = ((float32)ADC_value01
      RisingEdgeDelay
                          (1.0)
                                   TBCLK)
```

```
(float32)65535) * (float32)0.475;
       EPwm5Regs.TBPRD = (TBCLK / PWM_CARRIER)
                                                              BackTicker++;
/ 2;
                                                              SW1_cnt = 0;
       EPwm5Regs.CMPB = (EPwm5Regs.TBPRD + 1) *
(1 - PwmDutyRatioA);
                                                           }
                                                           else if (SW3_cnt % 2 == 1 && SW4_cnt % 2 == 1)
       Loop_cnt++;
                                                           {
                                                              EPwm5Regs.CMPA.half.CMPA = 0;
       BackTicker++;
                                                              EPwm5Regs.CMPB = 5000;
       SW1_cnt = 0;
                                                              Loop_cnt++;
     }
                                                              BackTicker++:
     else if (SW1 == 1 && SW3_cnt % 2 == 0 &&
                                                           }
SW4_cnt \% 2 == 1)
                                                           //----프로젝트2
     {
                                                           else if (SW1 == 2)
       EPwm5Regs.DBFED = 0;
                                         /* lusec.
Falling Edge Delay */
                                                           {
       EPwm5Regs.DBRED = 0;
                                         /* lusec,
                                                              PWM_CARRIER = 100E3
                                                                                               200E3
Rising Edge Delay */
                                                      (float32)ADC_value01 / (float32)65535;
       FallingEdgeDelay = (1.0)
                                       TBCLK)
                                                              EPwm5Regs.TBPRD = (TBCLK / PWM_CARRIER)
EPwm5Regs.DBFED;
                                                      / 4;
       RisingEdgeDelay
                        = (1.0
                                       TBCLK)
                                                              EPwm5Regs.CMPA.half.CMPA
EPwm5Regs.DBRED;
                                                      (EPwm5Regs.TBPRD + 1) * PwmDutyRatioA;
       PWM_CARRIER = 20E3;
                                                              EPwm5Regs.CMPB = (EPwm5Regs.TBPRD + 1) *
                                                      (1 - PwmDutyRatioA);
       PwmDutyRatioA = ((float32)ADC_value01
(float32)65535 )* (float32)0.475;
                                                              Loop_cnt++;
       EPwm5Regs.TBPRD = (TBCLK / PWM_CARRIER)
                                                              BackTicker++;
/ 2;
                                                              SW1_cnt = 0;
       EPwm5Regs.CMPA.half.CMPA
(EPwm5Regs.TBPRD + 1) * PwmDutyRatioA;
                                                           // -----프로젝트3
                                                           else if (SW1 >= 3)
       Loop_cnt++;
```

```
{
       EPwm5Regs.DBFED = 75 * (float32)ADC_value01
/ (float32)65535;
       EPwm5Regs.DBRED = 75 * (float32)ADC_value01
/ (float32)65535;
       FallingEdgeDelay
                                        TBCLK)
                            (1.0 /
EPwm5Regs.DBFED;
       RisingEdgeDelay
                         = (1.0
                                        TBCLK)
EPwm5Regs.DBRED;
       EPwm5Regs.CMPA.half.CMPA
(EPwm5Regs.TBPRD + 1) * 0.5;
       EPwm5Regs.CMPB = (EPwm5Regs.TBPRD + 1) *
(1 - 0.5);
       Loop_cnt++;
       BackTicker++;
       SW1_cnt = 0;
     }
     if (SW3_cnt % 2 == 1)
       EPwm5Regs.CMPA.half.CMPA = 0;
     }
     if (SW4_cnt % 2 == 1)
     {
       EPwm5Regs.CMPB = 5000;
     }
  }
   메인 함수 - 끝
   ISR 함수 정의
```

```
interrupt void Xint3_isr(void)
   DINT;
   DELAY_US(500000);
   SW1_cnt++;
   SW1 = SW1_cnt;
   EINT:
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP12;
interrupt void Xint4_isr(void)
   SW2_cnt++;
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP12;
}
interrupt void Xint5_isr(void)
   SW3_cnt++;
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP12;
}
interrupt void Xint6_isr(void)
   SW4_cnt++;
   PieCtrlRegs.PIEACK.all = PIEACK_GROUP12;
interrupt void EPwm5Isr(void)
   EPwm5IsrTicker++;
   /* Clear INT flag for this timer */
   EPwm5Regs.ETCLR.bit.INT = 1;
   /* Acknowledge this interrupt to receive more
interrupts from group 3 */
```

```
PieCtrlRegs.PIEACK.bit.ACK3 = 1;
                                                          EPwm5Regs.AQCTLB.bit.CBU = 1;
                                                                                            /* Set EPWM5A
}
                                                        on CNTR=Zero */
void InitEPwm5Module(void)
                                                          EPwm5Regs.AQCTLB.bit.CBD = 2;
                                                                                                   /* Clear
                                                        EPWM5A on CNTR=CMPA, Up-Count */
{
  /* Setup Counter Mode and Clock */
                                                        /* Set Dead-time */
  EPwm5Regs.TBCTL.bit.CTRMODE = 2;
                                           /* Count
                                                          EPwm5Regs.DBCTL.bit.IN_MODE = 2;
                                                                                                /* EPWMxA
Up (Asymmetric) */
                                                        is the source for both falling-edge & rising-edge delay
  EPwm5Regs.TBCTL.bit.HSPCLKDIV = 0;
                                          /* TBCLK
= SYSCLKOUT / (HSPCLKDIV * CLKDIV) = 150MHz */
                                                          EPwm5Regs.DBCTL.bit.OUT_MODE = 3;
                                                        Dead-band is fully enabled for both rising-edge delay
  EPwm5Regs.TBCTL.bit.CLKDIV = 0;
                                                        on EPWMxA and falling-edge delay on EPWMxB */
  /* Setup Phase */
                                                          EPwm5Regs.DBCTL.bit.POLSEL = 2;
                                                                                                  /* Active
                                                        High Complementary (AHC). EPWMxB is inverted */
  EPwm5Regs.TBPHS.half.TBPHS = 0;
                                           /* Phase
is 0 */
                                                          EPwm5Regs.DBFED = 450;
                                                                                                  /* 3usec.
                                                        Falling Edge Delay */
  EPwm5Regs.TBCTL.bit.PHSEN = 0;
                                          /* Disable
phase loading */
                                                          EPwm5Regs.DBRED = 450;
                                                                                                  /* 3usec.
                                                        Rising Edge Delay */
                                    Setup
                                             Period
(Carrier Frequency) */
                                                                                   /* Set Interrupts */
                                                          EPwm5Regs.ETSEL.bit.INTSEL = 1;
  EPwm5Regs.TBPRD = (TBCLK / PWM_CARRIER) / 4;
                                                                                               /* Select INT
/* Set Timer Period, (150MHz/20KHz)/4 = 1,875 () */
                                                       on CNTR=Zero */
                                           /* Clear
                                                          EPwm5Regs.ETPS.bit.INTPRD = 1;
  EPwm5Regs.TBCTR = 0;
                                                                                                /* Generate
Counter */
                                                        INT on 1st event */
                            /* Set Compare Value
                                                          EPwm5Regs.ETSEL.bit.INTEN = 1;
                                                                                              /* Enable INT
                                                        */
  EPwm5Regs.CMPA.half.CMPA
(Uint16)((EPwm5Regs.TBPRD
PWM_DUTY_RATIO_A);
                       /* Set Compare A Value to
50% */
  EPwm5Regs.CMPB = (Uint16)((EPwm5Regs.TBPRD + 1)
*(1 - PWM_DUTY_RATIO_A));
  /* Set actions */
  EPwm5Regs.AQCTLA.bit.CAU = 1;
                                            /* Set
EPWM5A on CNTR=Zero */
  EPwm5Regs.AQCTLA.bit.CAD = 2;
                                           /* Clear
EPWM5A on CNTR=CMPA, Up-Count */
```