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**T.C.**

**FENERBAHÇE UNIVERSITY**

**FACULTY OF ENGINEERING AND ARCHITECTURE**

**COMP2007 – LOGICAL SYSTEM DESIGN PROJECT**

**FB-CPU RTL DESING**

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**Summary:**

The project is an educational venture into the world of digital design, employing the Verilog language to replicate the function of CPUs using FPGA technology. It serves as a practical learning tool, circumventing the high costs and complexity of actual FPGAs with the use of simulators. The project's essence is the creation of a CPU model, the cpu, supported by a memory module and a testbench for rigorous functionality testing. This approach offers a comprehensive understanding of CPU operations and Verilog language application, ensuring that students can experiment with and learn from implementing and executing core CPU operations without the need for expensive hardware.

**Introduction:**

In this project, we immerse ourselves in the world of CPUs, constructing a rudimentary one using an FPGA simulator crafted by our lecturer, Mr. Levent. Through Verilog, we delve into the intricacies of CPU components and functions, aiming to comprehend the underpinnings of CPU operations. The endeavor to create a processor using FPGA technology not only enriches our understanding of digital design but also equips us with practical skills in executing core instructions within a programmable logic framework. This initiative bridges theory with application, providing a profound insight into the architecture and construction of CPUs.

**System Architecture**

We have used an FPGA simulator FPGAs are classified into two types: behavioral, which focus on functionality, and temporal, which considers timing characteristics and supports languages like as VHDL, Verilog, and SystemVerilog. ModelSim, XSIM, and VCS are popular tools. Waveform visualization, interactive debugging, code coverage, and performance profiling are all important aspects. Co-simulation is frequently supported by simulators, as is virtual prototyping for system-level testing. The design language, necessary functionality, and FPGA vendor all influence the decision.

**Software Used**

<https://avionchip.com/virtualfpga/>

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Von Neumann architecture was used in the FB-CPU RTL design.

**Results**

we used the FB-CPU Instruction Set Architecture to define what operations our processor can do. This included basic arithmetic like addition, subtraction, and multiplication, all handled by the Arithmetic Logic Unit. We thoroughly tested these functions with the AvionChipSimulator, which has helped us learn how a CPU works AND understand the parts of a CPU, like the PC, IR, and more, as well as getting to know the Verilog language and how to use FPGA simulators.

**Project Team**

* **KIMIA\_GHORBANI**

**(https://github.com/kimiaghorbani/logic-system-design1/blob/main/kimiaghorbaniCV.docx)**

* **MENA\_GHAZOWAN\_HAMOOD (https://github.com/itsmeminaa/logical\_design/blob/main/menahamoodCV.docx)**
* **JIBRAN AKBER(https://github.com/jibran-akber/CV.git)**

**Project's Link** : https://github.com/kimiaghorbani/logic-system-design1/blob/main/fbucpu.v

**Project's Slides Link** https://github.com/kimiaghorbani/logic-system-design1/blob/main/FBU\_CPU\_RTL\_GP.pptx

**Project's Youtube Video** https://youtu.be/EjeOHa63cro

**Refrence**

<http://www.levent.tc/>