parallel_matrix_multiplier Project Status			
Project File:	Matrix_multiplier.xise	**Parser Errors:**	No Errors
Module Name:	parallel_matrix_multiplier	**Implementation State:**	Synthesized
Target Device:	xc6slx150-3fgg484	• **Errors:**	No Errors
Product Version:	ISE 14.7	• **Warnings:**	122 Warnings (0 new)
Design Goal:	Balanced	• **Routing Results:**	
Design Strategy:	Xilinx Default (unlocked)	• **Timing Constraints:**	
Environment:	System Settings	• **Final Timing Score:**	

Device Utilization Summary (estimated values)			[-]
Logic Utilization	**Used**	**Available**	**Utilization**
Number of Slice Registers	2932	184304	1%
Number of Slice LUTs	4508	92152	4%
Number of fully used LUT-FF pairs	2261	5179	43%
Number of bonded IOBs	40	338	11%
Number of BUFG/BUFGCTRLs	1	16	6%
Number of DSP48A1s	16	180	8%

Detailed Reports					[-]
Report Name	**Status**	**Generated**	**Errors**	**Warnings**	**Infos**
Synthesis Report	Current	Sat Feb 6 17:29:47 2021	0	122 Warnings (0 new)	423 Infos (0 new)
Translation Report					
Map Report					
Place and Route Report					
Power Report					
Post-PAR Static Timing Report					
Bitgen Report					

Secondary Reports		[-]
Report Name	**Status**	**Generated**
Post-Synthesis Simulation Model Report	Current	Sat Feb 6 17:45:44 2021

Date Generated: 02/06/2021 - 17:50:30