```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company: CECS 201
4   // Engineer: KIM MARZO
5   //
6   // Create Date:    03:34:57 03/25/2019
7   // Design Name: Binary to Seven Segment Display
8   // Module Name:    LAB5_VM
9   // Target Devices: Spartan 6
10  // Description: A behavioral verilog module for a hex to seven segment decoder
11  //////////////////////////////////////////////////////////////////////////////////
12  module LAB5_VM(hex, a, b, c, d, e, f, g, anodes
13      );
14
15     input [3:0] hex;
16     output a, b, c, d, e, f, g;
17     output [3:0] anodes;
18     reg a, b, c, d, e, f, g;
19     wire [3:0] anodes;
20
21        always @ (hex) begin
22           case (hex)
23              4'b0000: {a,b,c,d,e,f,g} = 7'b0000001;
24              4'b0001: {a,b,c,d,e,f,g} = 7'b1001111;
25              4'b0010: {a,b,c,d,e,f,g} = 7'b0010010;
26              4'b0011: {a,b,c,d,e,f,g} = 7'b0000110;
27              4'b0100: {a,b,c,d,e,f,g} = 7'b1001100;
28              4'b0101: {a,b,c,d,e,f,g} = 7'b0100100;
29              4'b0110: {a,b,c,d,e,f,g} = 7'b1100000;
30              4'b0111: {a,b,c,d,e,f,g} = 7'b0001111;
31              4'b1000: {a,b,c,d,e,f,g} = 7'b0000000;
32              4'b1001: {a,b,c,d,e,f,g} = 7'b0001100;
33              4'b1010: {a,b,c,d,e,f,g} = 7'b0001000;
34              4'b1011: {a,b,c,d,e,f,g} = 7'b1100000;
35              4'b1100: {a,b,c,d,e,f,g} = 7'b0000111;
36              4'b1101: {a,b,c,d,e,f,g} = 7'b1000010;
37              4'b1110: {a,b,c,d,e,f,g} = 7'b0110000;
38              4'b1111: {a,b,c,d,e,f,g} = 7'b0111000;
39              default: {a,b,c,d,e,f,g} = 7'b1111111;
40           endcase
41        end
42
43        assign anodes = 4'b1110;
44
45
46  endmodule
47
```