```
1   `timescale 1ns / 1ps
2   //////////////////////////////////////////////////////////////////////////////////
3   // Company: CECS 201
4   // Engineer: Kim Marzo
5   //
6   // Create Date:    11:46:31 03/18/2019
7   // Design Name: 4-bit priority encoder
8   // Target Devices: Spartan 6
9   //
10  // Description: A verilog module that makes use of "structural modelling"
11  // for a 4 bit priority encoder with D[3:0] as inputs and D[3] as the MSB
12  // and outputs Y[1:0] and V where Y[0] and Y[1] are the binary code for the
13  // highest priority input and V is true whenever any of any input from D[3:0]
14  // is asserted.
15  //////////////////////////////////////////////////////////////////////////////////
16
17  module priority_encoder(
18      input [3:0] D,
19      output [1:0] Y,
20      output V
21      );
22      wire W0;
23
24        and a1 (W0, D[1], ~D[2]);
25
26        or o1 (Y[1], D[2], D[3]),
27           o2 (Y[0], W0, D[3]),
28           o3 (V, D[0], D[1], D[2], D[3]);
29
30  endmodule
31
```