63 62 61 60 59 58 57 56 55 54 53 52 51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33 32 31 30 29 28 27 26 25 24 23 22 21 20 19 18 17 16 15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 (					
Channel Header	0 1 Channel Tag [15:0	)] Waveform Gap [	Waveform Gap [21:0]		DDR3 Start Address [25:14]
Channel Header	DDR3 Start Address [13:0]	Waveform Length [22:0]	FT	Trigger Number [23:0]	
Waveform 1 Header	Waveform Count [11:0]	DDR3 Start Address [25:0]	FT	Waveform Length [22:0]	
Waveform 1 Header	0 1 0	Channel Tag [15:0]	Wavefor	m Gap [21:0] Waveform Index [11:0]	
	Waveform 1 ADC Data				
Waveform 2 Header	Waveform Count [11:0]	DDR3 Start Address [25:0]	FT	Waveform	Length [22:0]
Waveform 2 Header	0 1 0	Channel Tag [15:0]	Wavefor	m Gap [21:0]	Waveform Index [11:0]
	Waveform 2 ADC Data				
	•••				
Waveform N Header	Waveform Count [11:0]	DDR3 Start Address [25:0]	FT	Waveform	Length [22:0]
Waveform N Header	0 1 0	Channel Tag [15:0]	Wavefor	m Gap [21:0]	Waveform Index [11:0]
	Waveform N ADC Data				
Channel Trailer	Channel Checksum				
Channel Trailer	Channel Checksum				
Channel Trailer	Data Integrity Check Data Transfer Time				