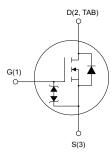


N-channel 400 V, 0.85 Ω typ., 5.4 A SuperMESH Power MOSFET in a DPAK package

Features







Order code	V _{DS}	R _{DS(on)} max.	I _D
STD7NK40ZT4	400 V	1 Ω	5.4 A

- 100% avalanche tested
- Gate charge minimized
- Very low intrinsic capacitance
- Zener-protected

Applications

Switching applications

Description

This high-voltage device is a Zener-protected N-channel Power MOSFET developed using the SuperMESH technology by STMicroelectronics, an optimization of the wellestablished PowerMESH. In addition to a significant reduction in on-resistance, this device is designed to ensure a high level of dv/dt capability for the most demanding applications.



AM01476v1 tab



Product status link STD7NK40ZT4

Product summary			
ode	STD7NK40ZT4		
	D=1.114.40=		

Froduct Summary			
Order code	STD7NK40ZT4		
Marking	D7NK40Z		
Package	DPAK		
Packing	Tape and reel		



1 Electrical ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V _{DS}	Drain-source voltage	400	V
V _{DGR}	Drain-gate voltage (R_{GS} = 20 k Ω)	400	V
V _{GS}	Gate-source voltage	±30	V
I-	Drain current (continuous) at T _C = 25 °C	5.4	
I _D	Drain current (continuous) at T _C = 100 °C	3.4	_ A
I _{DM} ⁽¹⁾	Drain current (pulsed)	21.6	Α
P _{TOT}	Total power dissipation at T _C = 25 °C	70	W
ESD	Gate-source, human body model (R = 1.5 kΩ, C = 100 pF)	3	kV
dv/dt ⁽²⁾	Peak diode recovery voltage slope	4.5	V/ns
T _{stg}	Storage temperature range	-55 to 150	°C
T _J	Operating junction temperature range	-55 to 150	°C

^{1.} Pulse width limited by safe operating area.

Table 2. Thermal data

Symbol	Parameter	Value	Unit
R _{thJC}	Thermal resistance, junction-to-case	1.78	°C/W
R _{thJA} ⁽¹⁾	Thermal resistance, junction-to-ambient	50	°C/W

^{1.} When mounted on an 1-inch² FR-4, 2 Oz copper board.

Table 3. Avalanche characteristics

Symbol	Parameter	Value	Unit
I _{AR}	Avalanche current, repetitive or not repetitive (pulse width is limited by T _J max.)	5.4	Α
E _{AS}	Single pulse avalanche energy (starting T _J = 25 °C, I _D = I _{AR} , V _{DD} = 50 V)	130	mJ

DS2855 - Rev 5 page 2/19

^{2.} $I_{SD} \le 5.4$ A, $di/dt \le 200$ A/ μ s, $V_{DD} < V_{(BR)DSS}$.



2 Electrical characteristics

 T_C = 25 °C unless otherwise specified.

Table 4. On/off states

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
V _{(BR)DSS}	Drain-source breakdown voltage	$I_D = 1 \text{ mA}, V_{GS} = 0 \text{ V}$	400			V
I	Zono moto vielto no due in oviment	V _{GS} = 0 V, V _{DS} = 400 V			1	
I _{DSS}	Zero gate voltage drain current	V _{GS} = 0 V, V _{DS} = 400 V, T _C = 125 °C ⁽¹⁾			50	μA
I _{GSS}	Gate body leakage current	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
V _{GS(th)}	Gate threshold voltage	$V_{DS} = V_{GS}$, $I_D = 50 \mu A$	3.00	3.75	4.50	V
R _{DS(on)}	Static drain-source on-resistance	V _{GS} = 10 V, I _D = 2.7 A		0.85	1	Ω

^{1.} Specified by design, not tested in production.

Table 5. Dynamic

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
C _{iss}	Input capacitance		-	535		pF
C _{oss}	Output capacitance	$V_{DS} = 25 \text{ V, f} = 1 \text{ MHz, } V_{GS} = 0 \text{ V}$	-	82		pF
C _{rss}	Reverse transfer capacitance	1		18		pF
Coss eq. (1)	Equivalent output capacitance	V _{GS} = 0 V, V _{DS} = 0 to 320 V		53		pF
Qg	Total gate charge	V _{DD} = 320 V, I _D = 5.4 A, V _{GS} = 0 to 10 V (see Figure 14. Test circuit for gate charge behavior)		19	26	nC
Q _{gs}	Gate-source charge			4		nC
Q _{gd}	Gate-drain charge			10		nC

^{1.} $C_{\text{oss eq.}}$ is defined as the constant equivalent capacitance giving the same charging time as C_{oss} when V_{DS} increases from 0 to 80% V_{DSS} .

Table 6. Switching times

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
t _{d(on)}	Turn-on delay time	$V_{DD} = 200 \text{ V}, I_D = 2.7 \text{ A},$	-	15	-	ns
t _r	Rise time	R _G = 4.7 Ω, V _{GS} = 10 V	-	15	-	ns
t _{d(off)}	Turn-off delay time	(see Figure 13. Test circuit for resistive load switching times and	-	30	-	ns
t _f	Fall time	Figure 18. Switching time waveform)	-	12	-	ns
$t_{r(Voff)}$	Off-voltage rise time	V _{DD} = 320 V, I _D = 5.4 A,	-	12	-	ns
t _f	Fall time	$R_G = 4.7 \Omega, V_{GS} = 10 V$	-	10	-	ns
t _c	Crossover time	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	20	-	ns

DS2855 - Rev 5 page 3/19



Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Тур.	Max.	Unit
I _{SD}	Source-drain current		-		5.4	Α
I _{SDM} ⁽¹⁾	Source-drain current (pulsed)		-		21.6	Α
V _{SD} ⁽²⁾	Forward on voltage	I _{SD} = 5.4 A, V _{GS} = 0 V	-		1.6	V
t _{rr}	Reverse recovery time	I _{SD} = 5.4 A, di/dt = 100 A/µs,	-	220		ns
Q _{rr}	Reverse recovery charge	V _{DD} = 50 V, T _J = 150 °C	-	990		nC
I _{RRM}	Reverse recovery current	(see Figure 15. Test circuit for inductive load switching and diode recovery times)	-	9		Α

- 1. Pulsed: pulse duration = 300 μ s, duty cycle 1.5%.
- 2. Pulse width is limited by safe operating area.

DS2855 - Rev 5 page 4/19



2.1 Electrical characteristics (curves)

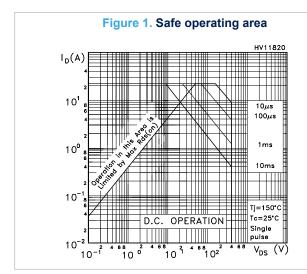


Figure 2. Thermal impedance $\delta = 0.5$ 10^{-1} 0.05 $Z_{th} = k * R_{thJC}$ $\delta = t_p / T$ 0.01 SINGLE PULSE t_p Τ 10^{-2} 10⁻⁵ 10⁻³ 10⁻² 10-4 10⁻¹

Figure 3. Output characteristics

HV11840

VGS=10V

9

9

9

7V

6

3

0

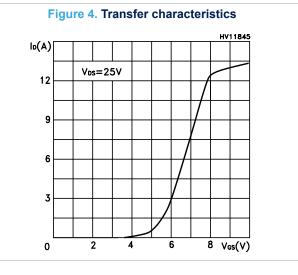
5

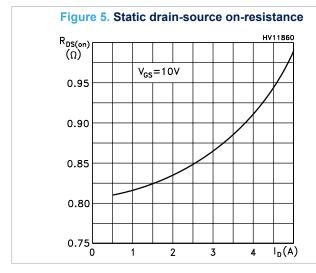
10

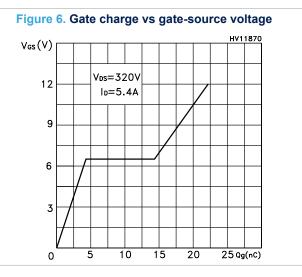
15

20

Vos(V)







DS2855 - Rev 5 page 5/19



Figure 7. Capacitance variations

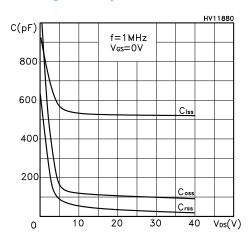


Figure 8. Normalized gate threshold voltage vs temperature

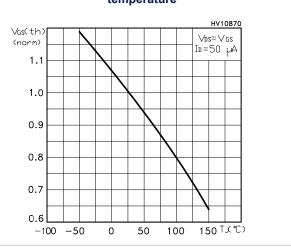


Figure 9. Normalized on-resistance vs temperature

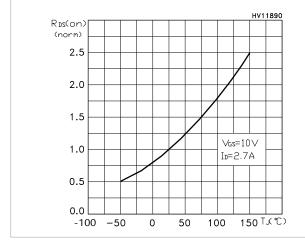


Figure 10. Source-drain diode forward characteristics

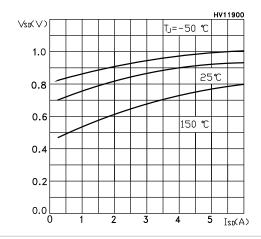


Figure 11. Normalized $V_{(BR)DSS}$ vs temperature

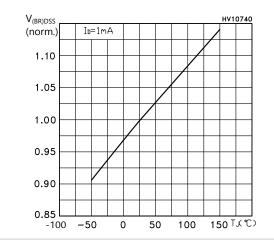
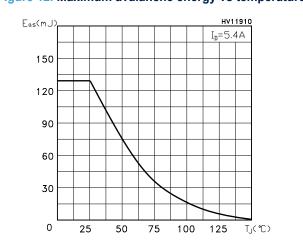


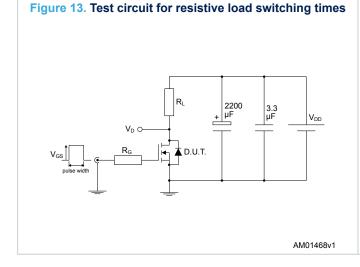
Figure 12. Maximum avalanche energy vs temperature



DS2855 - Rev 5 page 6/19



3 Test circuits



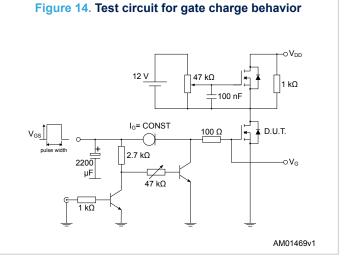
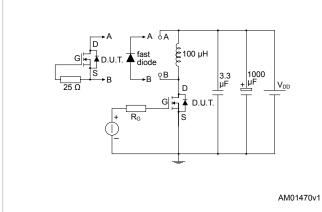


Figure 15. Test circuit for inductive load switching and diode recovery times



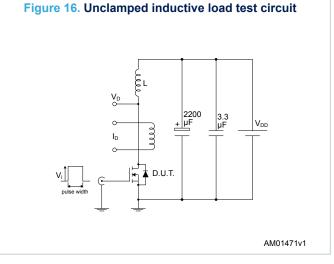


Figure 17. Unclamped inductive waveform

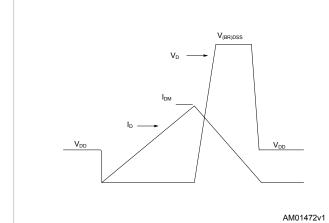
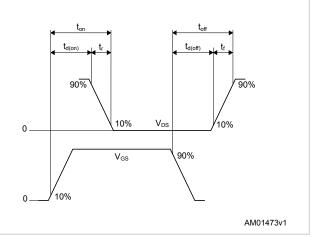


Figure 18. Switching time waveform



DS2855 - Rev 5 page 7/19

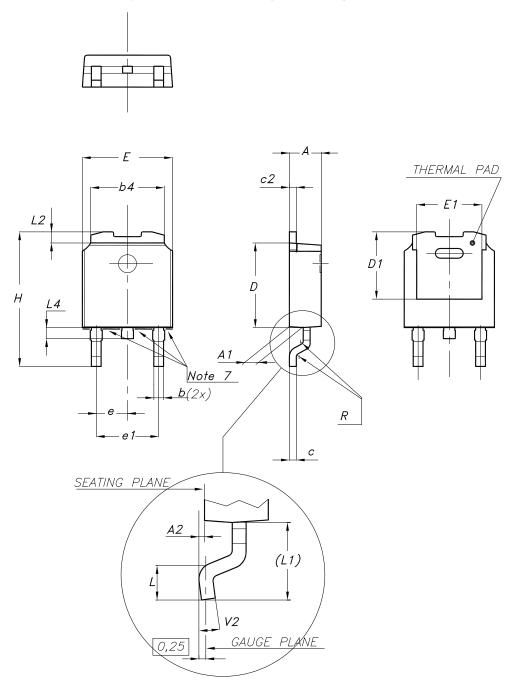


4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

4.1 DPAK (TO-252) type A package information

Figure 19. DPAK (TO-252) type A package outline



0068772_A_34

DS2855 - Rev 5 page 8/19



Table 8. DPAK (TO-252) type A mechanical data

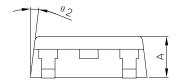
Dim.		mm	
Dim.	Min.	Тур.	Max.
Α	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
С	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
Е	6.40		6.60
E1	4.60	4.70	4.80
е	2.159	2.286	2.413
e1	4.445	4.572	4.699
Н	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

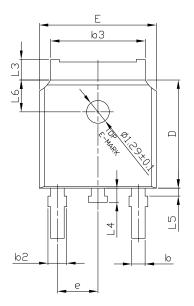
DS2855 - Rev 5 page 9/19

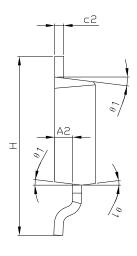


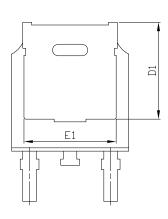
4.2 DPAK (TO-252) type C3 package information

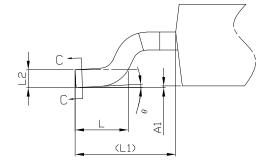
Figure 20. DPAK (TO-252) type C3 package outline











0068772_type-C3_rev34

DS2855 - Rev 5 page 10/19



Table 9. DPAK (TO-252) type C3 mechanical data

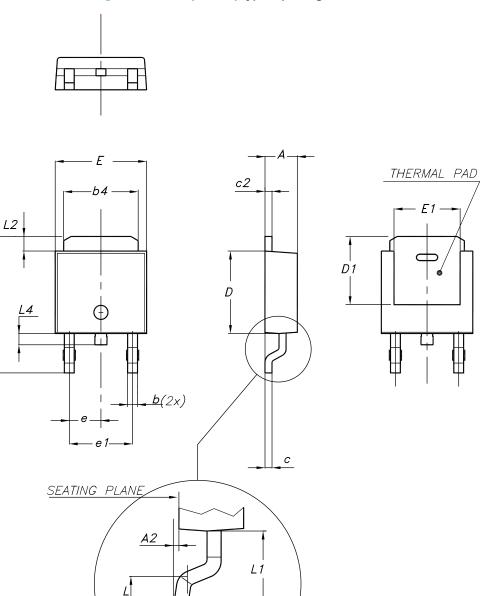
Dim.		mm				
Dilli.	Min.	Тур.	Max.			
А	2.20	2.30	2.38			
A1	0.00		0.10			
A2	0.90	1.01	1.10			
b	0.72		0.85			
b2	0.72		1.10			
b3	5.13	5.33	5.46			
С	0.47		0.60			
c2	0.47		0.60			
D	6.00	6.10	6.20			
D1	5.20	5.45	5.70			
Е	6.50	6.60	6.70			
E1	5.00	5.20	5.40			
е	2.186	2.286	2.386			
Н	9.80	10.10	10.40			
L	1.40	1.50	1.70			
L1		2.90 REF				
L2		0.51 BSC				
L3	0.90		1.25			
L4	0.60	0.80	1.00			
L5	0.15		0.75			
L6		1.80 REF				
θ	0°		8°			
θ1	5°	7°	9°			
θ2	5°	7°	9°			

DS2855 - Rev 5 page 11/19



4.3 DPAK (TO-252) type E package information

Figure 21. DPAK (TO-252) type E package outline



0068772_typeE_rev.34

DS2855 - Rev 5 page 12/19

GAUGE PLANE

0.508



Table 10. DPAK (TO-252) type E mechanical data

Dim.	mm			
	Min.	Тур.	Max.	
A	2.18		2.39	
A2			0.13	
b	0.65		0.884	
b4	4.95		5.46	
С	0.46		0.61	
c2	0.46		0.60	
D	5.97		6.22	
D1	5.21			
Е	6.35		6.73	
E1	4.32			
е		2.286		
e1		4.572		
Н	9.94		10.34	
L	1.50		1.78	
L1		2.74		
L2	0.89		1.27	
L4			1.02	

DS2855 - Rev 5 page 13/19



6.3 | Solution | Color | Colo

Figure 22. DPAK (TO-252) recommended footprint (dimensions are in mm)

Notes:

- 1) This footprint is able to ensure insulation up to 630 Vrms (according to CEI IEC 664-1)
- 2) The device must be positioned within \bigcirc 0.05 A B

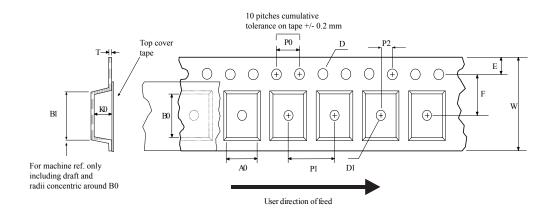
FP_0068772_34

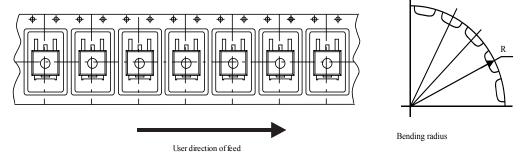
DS2855 - Rev 5 page 14/19



4.4 DPAK (TO-252) packing information

Figure 23. DPAK (TO-252) tape outline



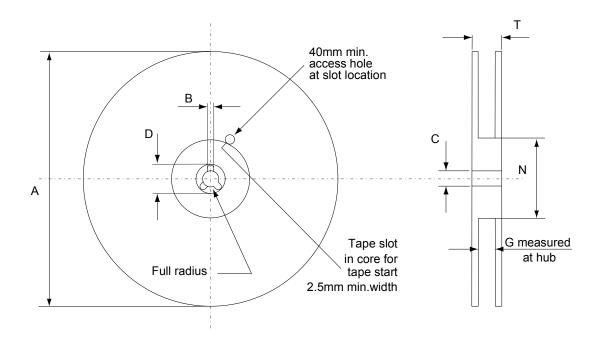


AM08852v1

DS2855 - Rev 5 page 15/19



Figure 24. DPAK (TO-252) reel outline



AM06038v1

Table 11. DPAK (TO-252) tape and reel mechanical data

Таре		Reel			
Dim	mm		Dive	mm	
Dim.	Min.	Max.	Dim.	Min.	Max.
A0	6.8	7	А		330
В0	10.4	10.6	В	1.5	
B1		12.1	С	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	Т		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base	qty.	2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
Т	0.25	0.35			
W	15.7	16.3			

DS2855 - Rev 5 page 16/19



Revision history

Table 12. Document revision history

Date	Revision	Changes
02-Sep-2002	2	Document updated.
11-Jul-2018	3	Part number STD7NK40Z-1 was moved to a separate datasheet, and the document was updated accordingly.
		Updated title, features, applications and description on cover page.
		Updated Section 1 Electrical ratings, Section 2 Electrical characteristics, Section 3 Test circuits and Section 4 Package information.
		Minor text changes
23-May-2023	4	The part numbers STP7NK40Z and STP7NK40ZFP have been moved to a separate datasheet and the document has been updated accordingly.
		Removed "Table 8. Gate-source Zener diode".
		Updated Section 4.1 DPAK (TO-252) type A package information, Section 4.3 DPAK (TO-252) type E package information and added Section 4.2 DPAK (TO-252) type C3 package information.
		Minor text changes.
24-May-2023	5	Updated Features on cover page.

DS2855 - Rev 5 page 17/19





Contents

1	Elec	trical ratings	2
2		etrical characteristics	
		Electrical characteristics (curves)	
3	Test	circuits	7
4	Pac	kage information	8
		DPAK (TO-252) type A package information	
	4.2	DPAK (TO-252) type C3 package information	10
	4.3	DPAK (TO-252) type E package information	12
	4.4	DPAK (TO-252) packing information	15
Revi	ision	history	17



IMPORTANT NOTICE - READ CAREFULLY

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgment.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. For additional information about ST trademarks, refer to www.st.com/trademarks. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2023 STMicroelectronics – All rights reserved

DS2855 - Rev 5 page 19/19