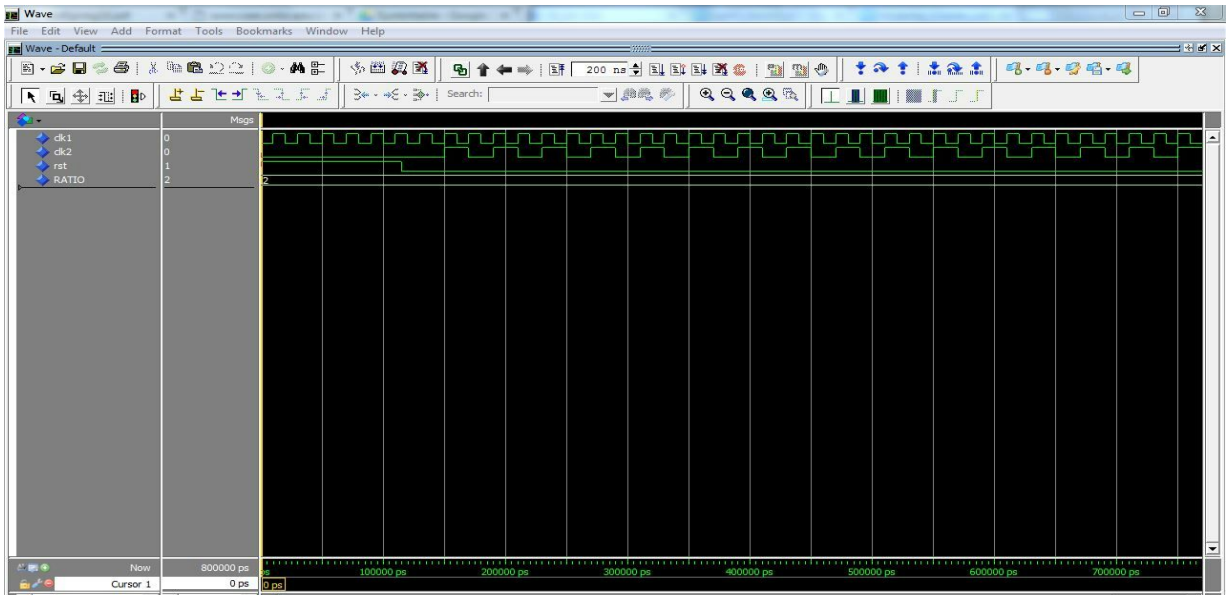
Name: Kinderley Charles
TA: Brandon Pollack
Section: 11F9
Assignment: Lab 04

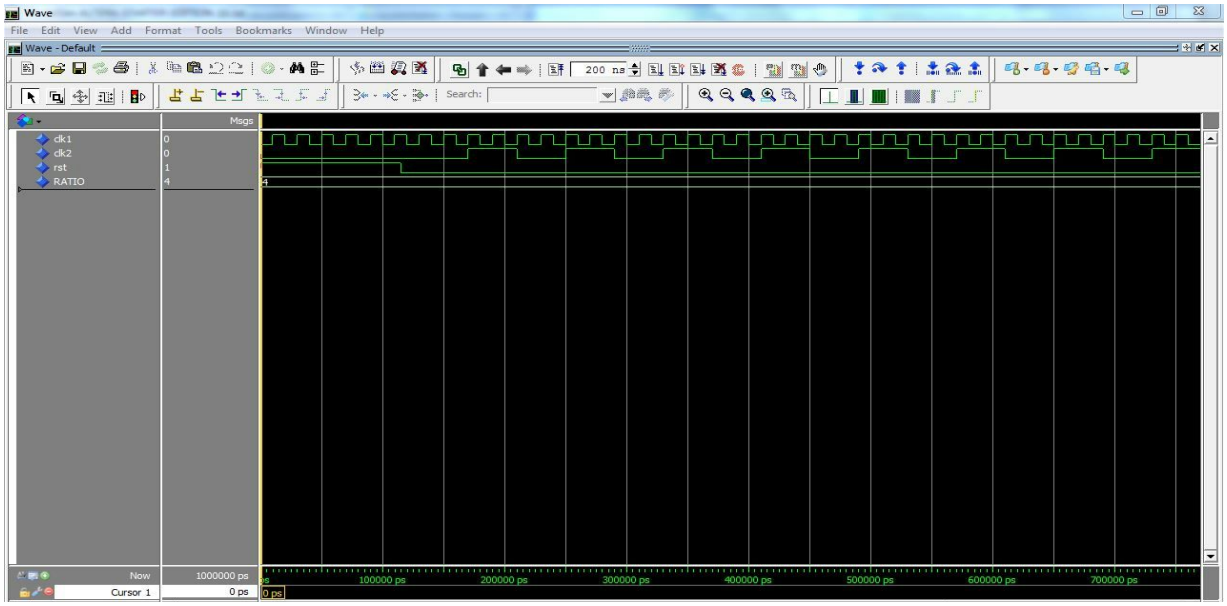
Lab 4: Sequential Logic and Finite State Machine

Part 1: Clock Divider and Clock Generator

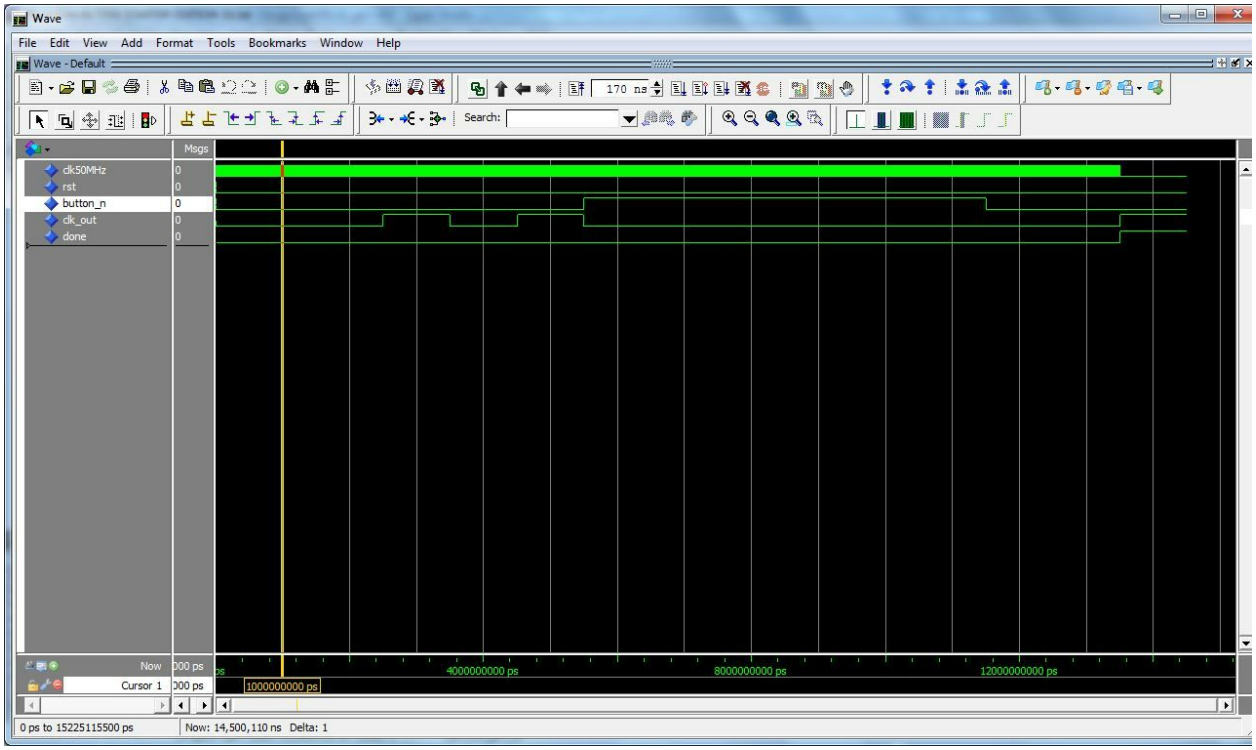
Clock Divider: ratio = 2



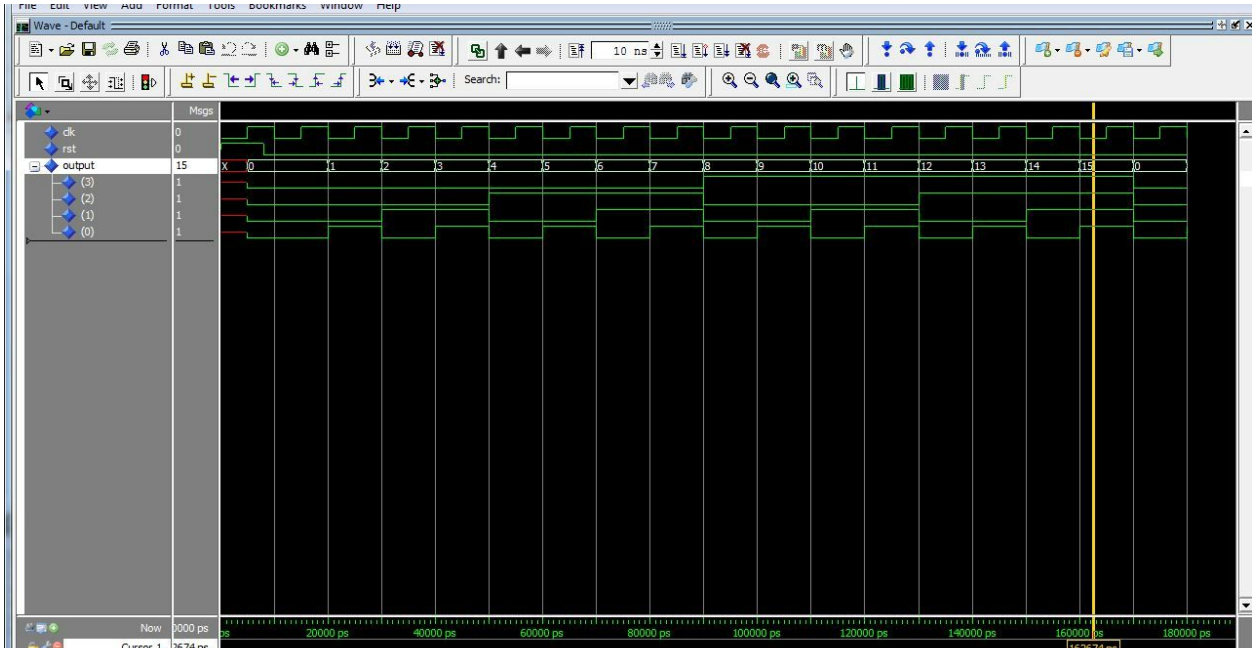
Clock Divider: ratio = 4



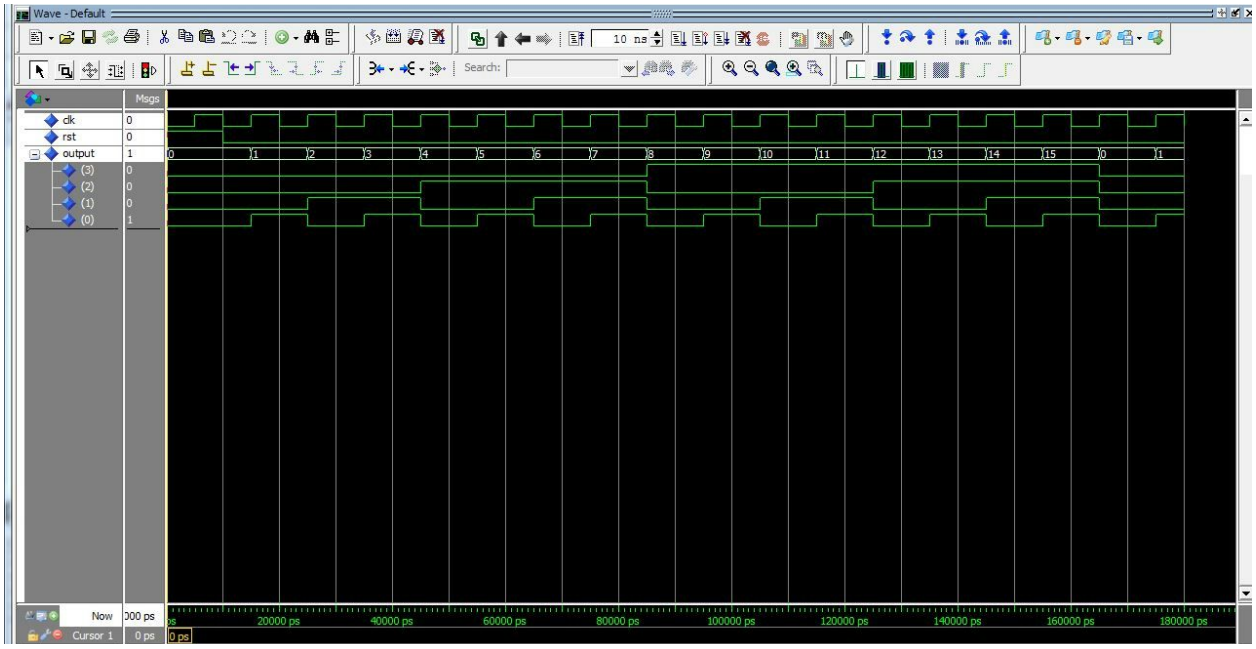
Clock Generator diagram



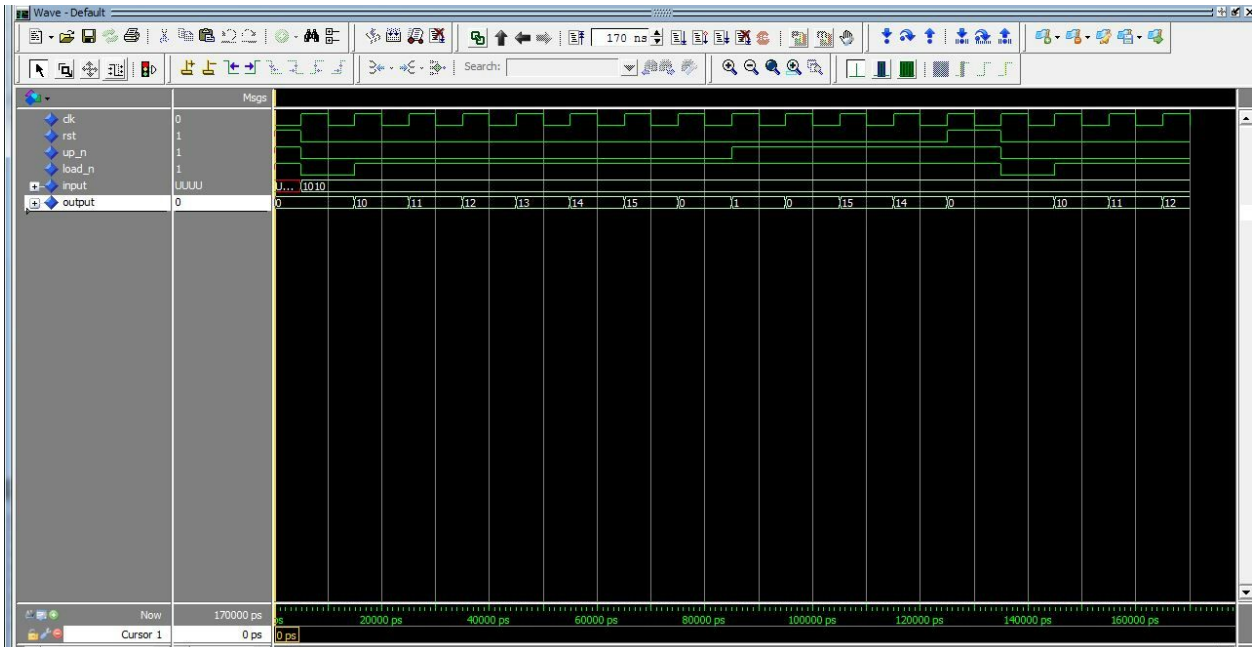
Part 2: 4 bit gray code counter using 1 process implementation



Part 3: 4 bit gray code counter using 2 processes implementation



Part 4: 4 Bit Up/Down counter with Load



Part 5: Top level file description

The top level entity fils map outs all the different components of the design to the FPGA board. It also connect all the different parts of the design among each other. To be specific, it connects the following components - counter, clock generator, and 4-bit gray counter.

The clock generator supplies the clock value to both the 4-bit gray counter and the regular counter. The gray counter sends its output to LED #3 while counter sends it output to LED #2.