WRIGHT STATE UNIVERSITY

EE4620L/EE6620L/CEG4324L/CEG6324L

DIGITAL INTEGRATED CIRCUIT DESIGN LAB

Lab 2

By

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Submission date: 03/14/2024

"I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code"

Signature : 

Date : 03/14/2024

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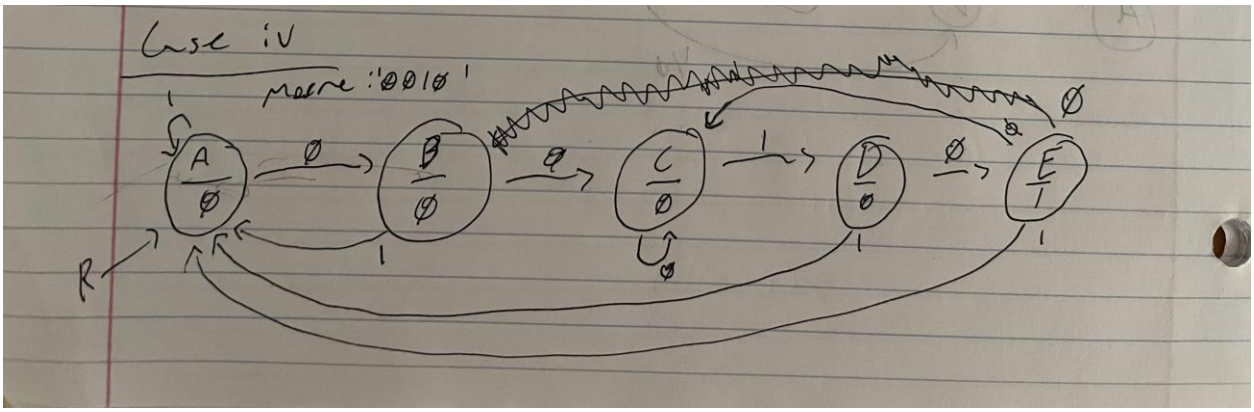
1. AIM / OBJECTIVE:

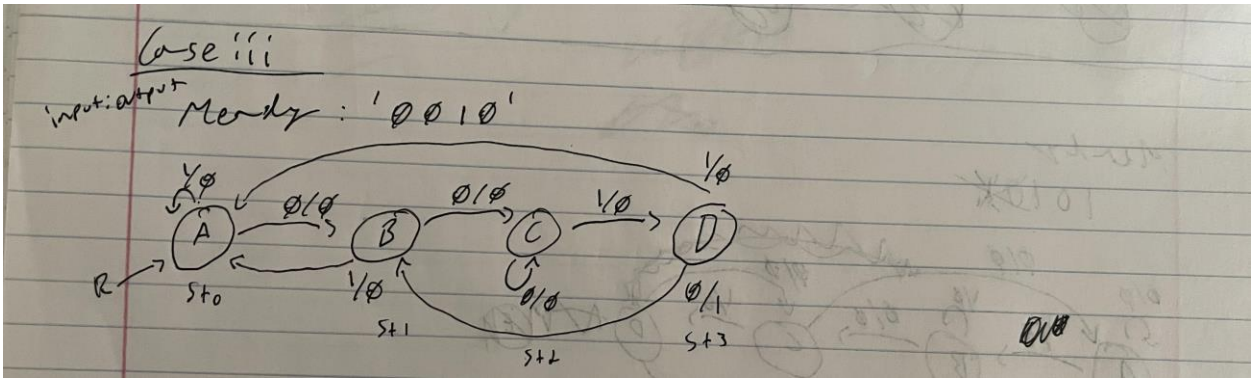
   The aim / objective of this lab was to explore the design space for sequential circuit designs and to become familiar with the Vivado simulation environment.

2. STG for Cases 3,4 (0010 for Mealy & Moore):

   Case 3:



   Case 4:



3. Design Code for all 4 cases:

Case 1:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity moore is
Port (  clk : in STD_LOGIC;
        din : in STD_LOGIC;
        rst : in STD_LOGIC;
        dout : out STD_LOGIC);
end moore;

architecture Behavioral of moore is
type state is (st0, st1, st2, st3);
signal present_state, next_state : state;
begin

synchronous_process: process (clk)
    begin
        if rising_edge(clk) then
            if (rst = '1') then
                present_state <= st0;
            else
                present_state <= next_state;
            end if;
        end if;
end process;

output_decoder : process(present_state, din)
begin
    case (present_state) is
        when st0 =>
            if (din = '1') then
                next_state <= st1;
            else
```

```
                next_state <= st0;
            end if;
        when st1 =>
            if (din = '1') then
                next_state <= st1;
            else
                next_state <= st2;
            end if;
        when st2 =>
            if (din = '1') then
                next_state <= st3;
            else
                next_state <= st0;
            end if;
        when st3 =>
            if (din = '1') then
                next_state <= st1;
            else
                next_state <= st2;
            end if;
        when others =>
                next_state <= st0;
    end case;
end process;
    dout <= '1' WHEN (present_state = st3) ELSE '0';
end Behavioral;
```

Case 2:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mealy is
Port ( clk : in STD_LOGIC;
din : in STD_LOGIC;
rst : in STD_LOGIC;
dout : out STD_LOGIC);
```

```
end mealy;

architecture Behavioral of mealy is
type state is (st0, st1, st2, st3);
signal present_state, next_state : state;
begin

syncronous_process : process (clk)
    begin
        if rising_edge(clk) then
            if (rst = '1') then
                present_state <= st0;
            else
                present_state <= next_state;
            end if;
        end if;
end process;

next_state_and_output_decoder : process(present_state, din)
    begin
        dout <= '0';
            case (present_state) is
                when st0 =>
                    if (din = '0') then
                        next_state <= st0;
                        dout <= '0';
                    else
                        next_state <= st1;
                        dout <= '0';
                    end if;
                when st1 =>
                    if (din = '1') then
                        next_state <= st1;
                        dout <= '0';
                    else
                        next_state <= st2;
                        dout <= '0';
                    end if;
                when st2 =>
```

```
                    if (din = '0')
                        next_state <= st0;
                        dout <= '0';
                    else
                        next_state <= st1;
                        dout <= '1';
                when others
                        next_state <= st0;
                        dout <= '0';
            end case;
end process;

end Behavioral;
```

Case 3:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity moore is
Port (  clk : in STD_LOGIC;
        din : in STD_LOGIC;
        rst : in STD_LOGIC;
        dout : out STD_LOGIC);
end moore;

architecture Behavioral of moore is
type state is (st0, st1, st2, st3, st4);
signal present_state, next_state : state;
begin

synchronous_process: process (clk)
    begin
        if rising_edge(clk) then
            if (rst = '1') then
                present_state <= st0;
            else
                present_state <= next_state;
```

```
            end if;
        end if;
end process;

next_state_and_output_decoder : process(present_state, din)
begin
    case (present_state) is
        when st0 =>
            if (din = '0') then
                next_state <= st1;
            else
                next_state <= st0;
            end if;
        when st1 =>
            if (din = '0') then
                next_state <= st2;
            else
                next_state <=st0;
            end if;
        when st2 =>
            if (din = '1') then
                next_state <= st3;
            else
                next_state <= st2;
        when st3 =>
            if (din = '0') then
                next_state <= st4;
            else
                next_state <= st0;
            end if;
        when st4 =>
            if (din = '0') then
                next_state <= st2;
            else
                next_state <= st0;
            end if;
    end case;
end process;
    dout <= '1' WHEN (present_state = st4) ELSE '0';
```

```
end Behavioral;
```

Case 4:

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity mealy is
Port ( clk : in STD_LOGIC;
din : in STD_LOGIC;
rst : in STD_LOGIC;
dout : out STD_LOGIC);
end mealy;

architecture Behavioral of mealy is
type state is (st0, st1, st2, st3);
signal present_state, next_state : state;
begin

syncronous_process : process (clk)
    begin
        if rising_edge(clk) then
            if (rst = '1') then
                present_state <= st0;
            else
                present_state <= next_state;
            end if;
        end if;
end process;

next_state_and_output_decoder : process(present_state, din)
    begin
        dout <= '0';
            case (present_state) is
                when st0 =>
                    if (din = '1') then
                        next_state <= st0;
                        dout <= '0';
```

```
                    else
                        next_state <= st1;
                        dout <= '0';
                    end if;
                when st1 =>
                    if (din = '1') then
                        next_state <= st0;
                        dout <='0';
                    else
                        next_state <= st2;
                        dout <= '0';
                when st2 =>
                    if (din = '0') then
                        next_state <= st2;
                        dout <= '0';
                    else
                        next_state <= st3;
                        dout <= '0';
                    end if;
                when st3 =>
                    if (din = '1') then
                        next_state <= st0;
                        dout <= '0';
                    else
                        next_state <= st1;
                        dout <= '1';
                    end if;
        end case;
end process;

end Behavioral;
```

4. TB Code:

Moore:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY tb_moore IS
END tb_moore;

ARCHITECTURE behavior OF tb_moore IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT moore
PORT(
clk : IN std_logic;
din : IN std_logic;
rst : IN std_logic;
dout : OUT std_logic
);
END COMPONENT;

--Inputs
signal clk : std_logic := '0';
signal din : std_logic := '0';
signal rst : std_logic := '0';

--Outputs
signal dout : std_logic;

-- Clock period definitions
constant clk_period : time := 20 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
```

```
uut: moore PORT MAP (
clk => clk,
din => din,
rst => rst,
dout => dout
);

-- Clock process definitions
clk_process :process
begin
clk <= '0';
wait for clk_period/2;
clk <= '1';
wait for clk_period/2;
end process;

-- Stimulus process
stim_proc: process
begin

rst <= '1';

wait for 100 ns;

rst <= '0';

din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '1';
```

```
wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;
```

```
din <= '0';

wait for 20 ns;

end process;

END;
```

Mealy:

```
LIBRARY ieee;
USE ieee.std_logic_1164.ALL;

ENTITY tb_moore IS
END tb_moore;

ARCHITECTURE behavior OF tb_moore IS

-- Component Declaration for the Unit Under Test (UUT)

COMPONENT mealy
PORT(
clk : IN std_logic;
din : IN std_logic;
rst : IN std_logic;
dout : OUT std_logic
);
END COMPONENT;

--Inputs
signal clk : std_logic := '0';
signal din : std_logic := '0';
signal rst : std_logic := '0';

--Outputs
signal dout : std_logic;

-- Clock period definitions
```

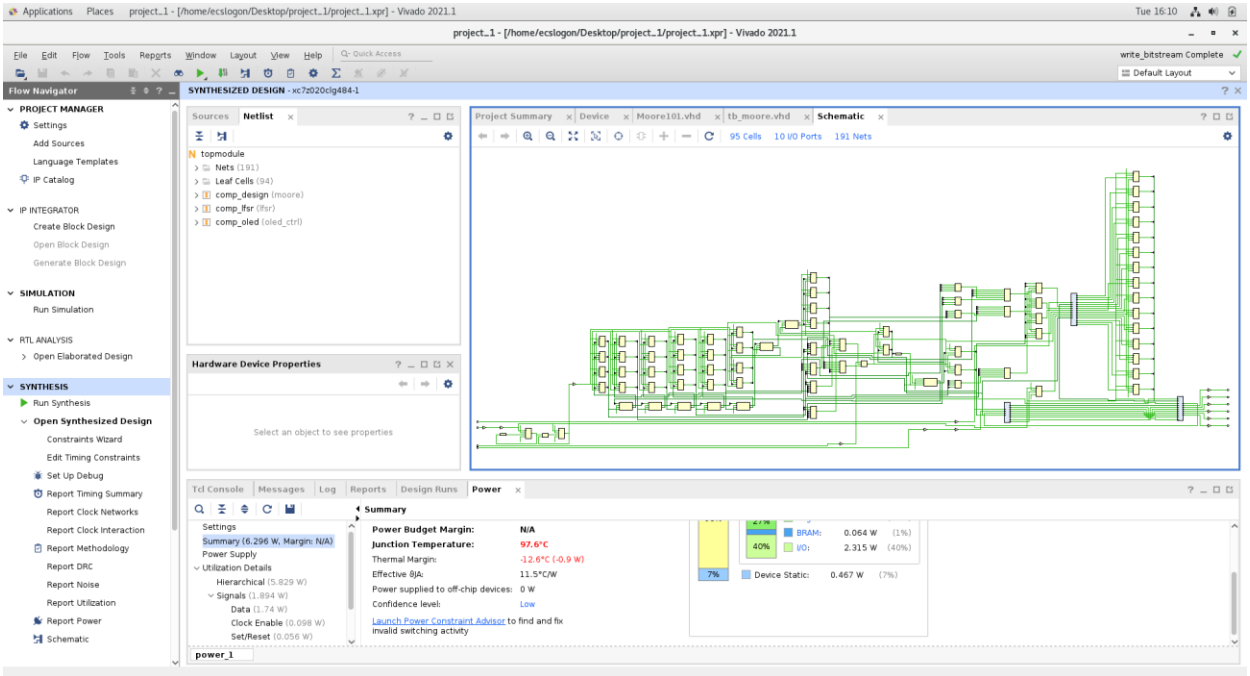
```
constant clk_period : time := 20 ns;

BEGIN

-- Instantiate the Unit Under Test (UUT)
uut: mealy PORT MAP (
clk => clk,
din => din,
rst => rst,
dout => dout
);

-- Clock process definitions
clk_process :process
begin
clk <= '0';
wait for clk_period/2;
clk <= '1';
wait for clk_period/2;
end process;

-- Stimulus process
stim_proc: process
begin

rst <= '1';

wait for 100 ns;

rst <= '0';

din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;
```

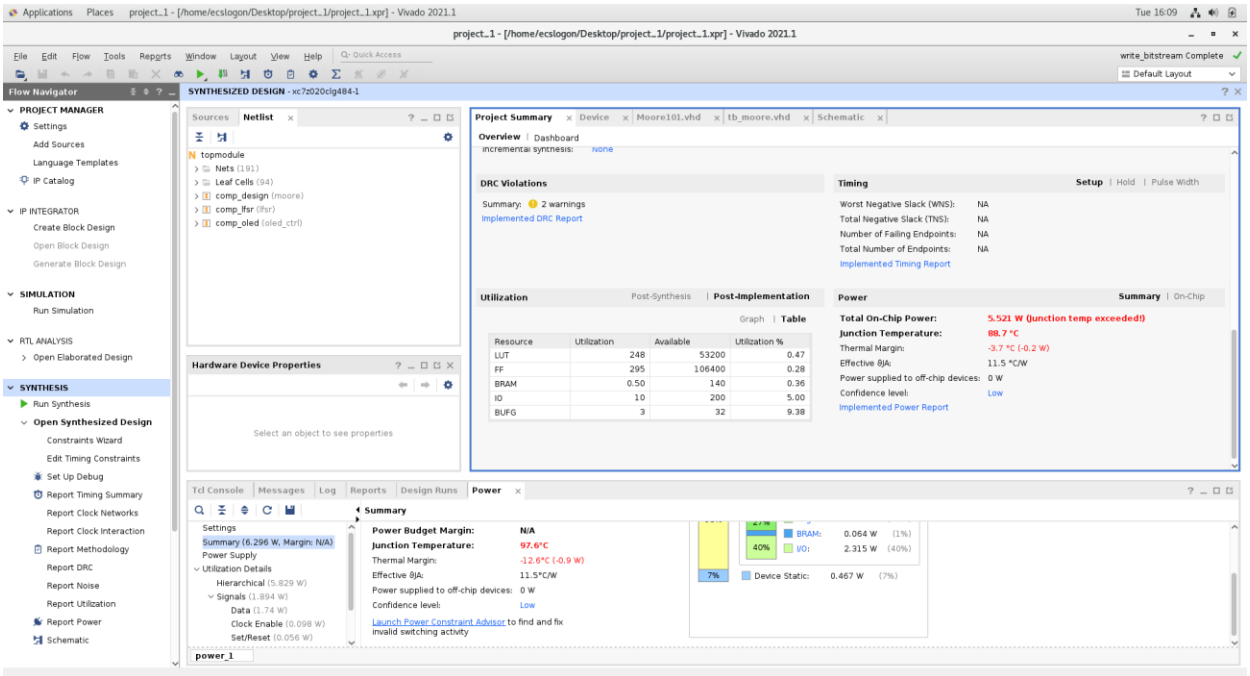
```
din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '1';

wait for 20 ns;

din <= '0';

wait for 20 ns;

din <= '0';

wait for 20 ns;
```

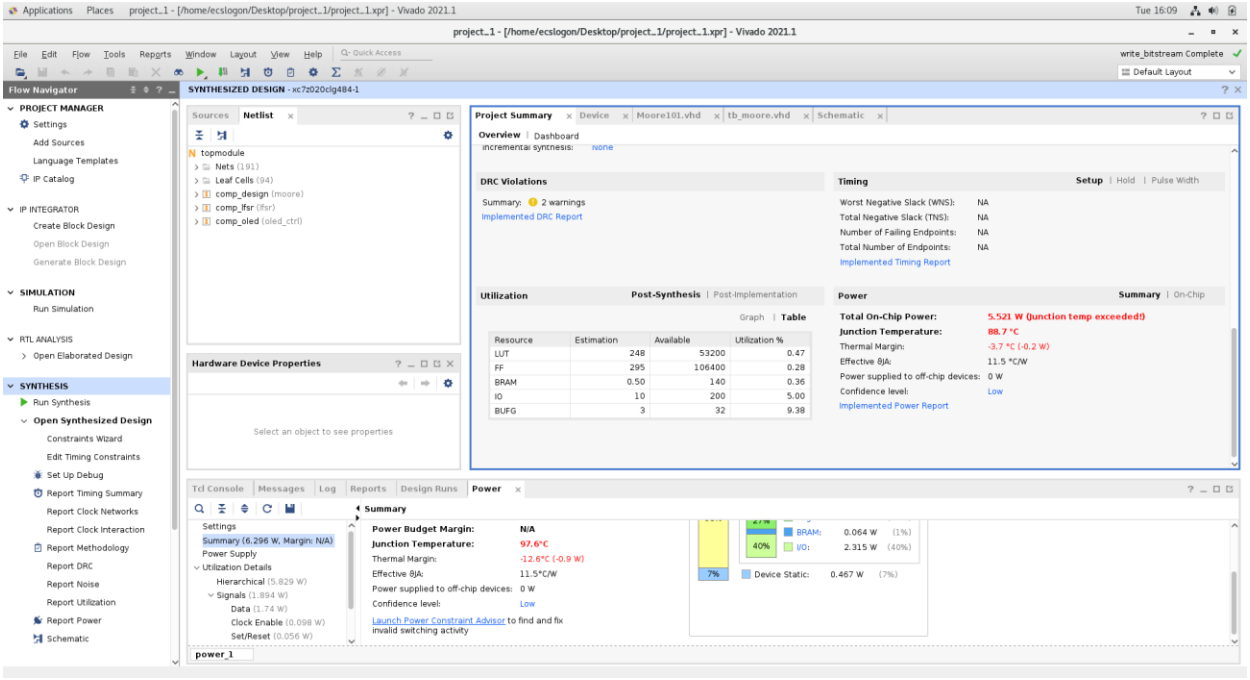
```
din <= '1';

wait for 20 ns;

din <= '0';

wait for 20 ns;

end process;

END;
```

5. Hardware Report:

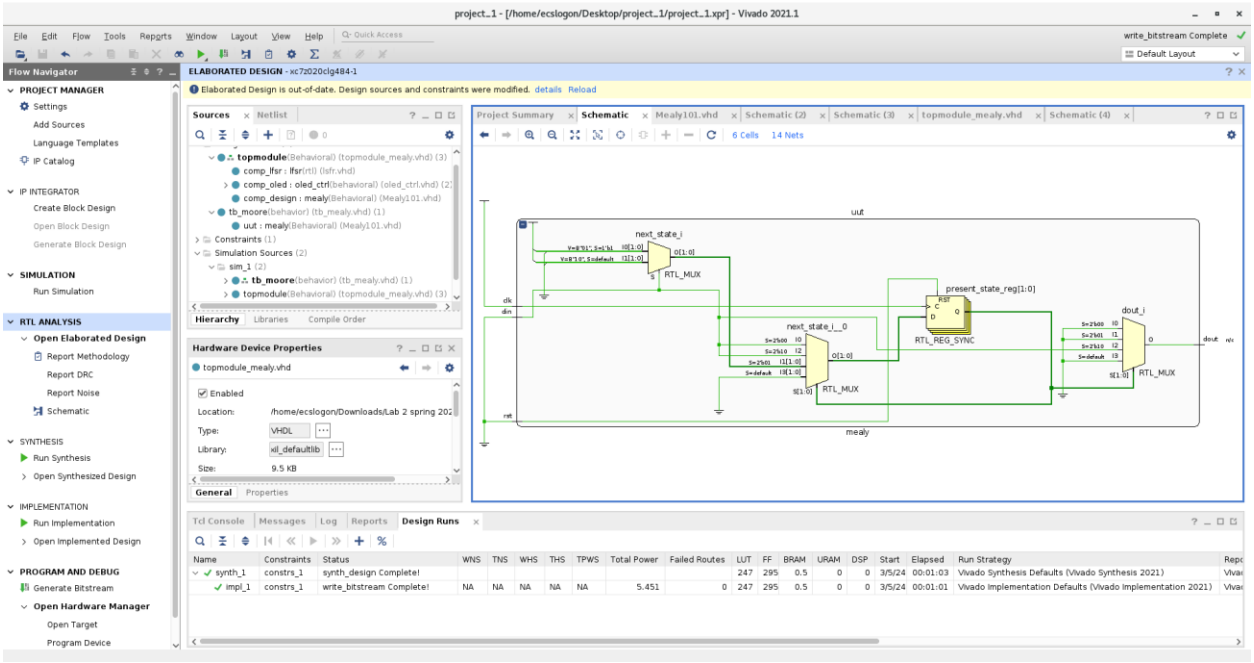
Case 1:

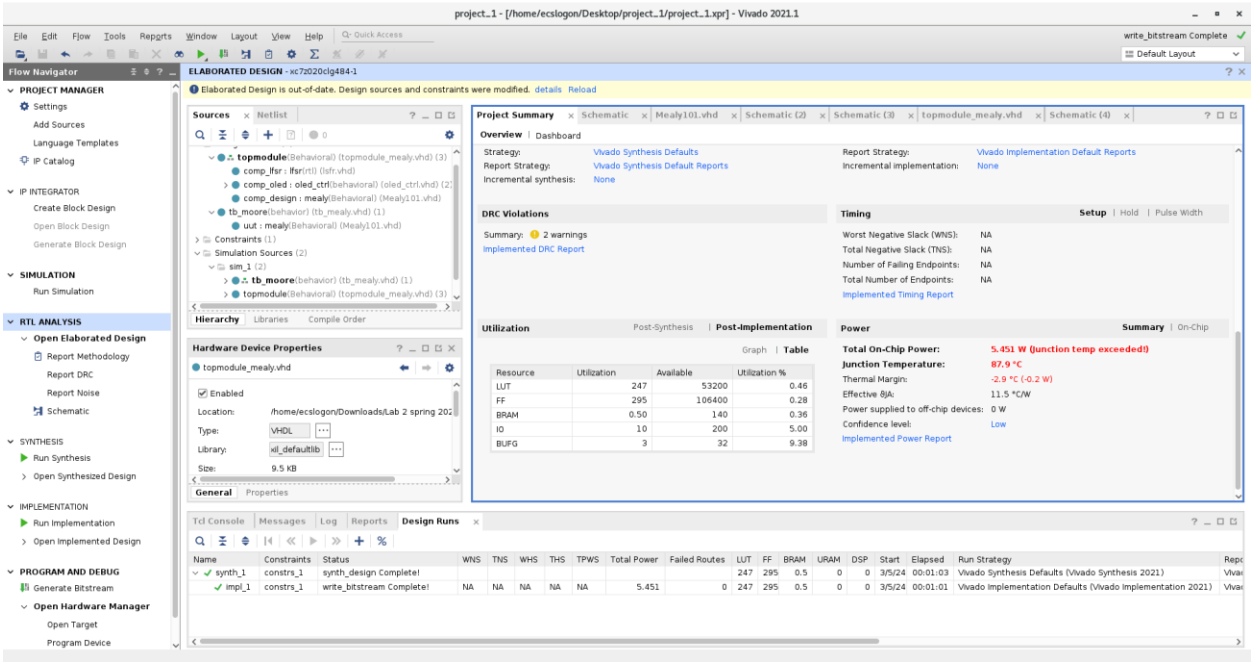





project_1 - [/home/ecslogon/Desktop/project_1/project_1.xpr] - Vivado 2021.1
Flow Navigator
SYNTHESIZED DESIGN - xc7z020clg484-1
Project Summary
DRC Violations
Timing
Utilization
Power
Hardware Device Properties
Tcl Console
Messages
Log
Reports
Design Runs
Power
Summary
Power Budget Margin: N/A
Junction Temperature: 97.6°C
Total On-Chip Power: 5.521 W (Junction temp exceeded!)
Junction Temperature: 88.7 °C

Case 2:


project_1 - [/home/ecslogon/Desktop/project_1/project_1.xpr] - Vivado 2021.1
Flow Navigator
ELABORATED DESIGN - xc7z020clg484-1
Elaborated Design is out-of-date. Design sources and constraints were modified.
Schematic
uut
next_state_i
RTL_MUX
present_state_reg[1:0]
RTL_REG_SYNC
next_state_i__0
dout_i
mealy
Hardware Device Properties
Design Runs


project_1 - [/home/ecslogon/Desktop/project_1/project_1.xpr] - Vivado 2021.1
File Edit Flow Tools Reports Window Layout View Help
write_bitstream Complete
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Flow Navigator
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IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
ELABORATED DESIGN - xc7z020clg484-1
Elaborated Design is out-of-date. Design sources and constraints were modified. details Reload
Sources
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Hierarchy
Libraries
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topmodule_mealy.vhd
Enabled
Location:
Type:
Library:
Size:
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Mealy101.vhd
Schematic (2)
Schematic (3)
topmodule_mealy.vhd
Schematic (4)
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Report Strategy:
Vivado Synthesis Default Reports
Incremental synthesis:
None
Report Strategy:
Vivado Implementation Default Reports
Incremental implementation:
None
DRC Violations
Summary:
2 warnings
Implemented DRC Report
Timing
Setup
Hold
Pulse Width
Worst Negative Slack (WNS):
Total Negative Slack (TNS):
Number of Failing Endpoints:
Total Number of Endpoints:
Implemented Timing Report
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Post-Synthesis
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Resource
Utilization
Available
Utilization %
LUT 247 53200 0.46
FF 295 106400 0.28
BRAM 0.50 140 0.36
IO 10 200 5.00
BUFG 3 32 9.38
Power
Summary
On-Chip
Total On-Chip Power:
5.451 W (junction temp exceeded!)
Junction Temperature:
87.9 °C
Thermal Margin:
-2.9 °C (-0.2 W)
Effective θJA:
11.5 °C/W
Power supplied to off-chip devices:
0 W
Confidence level:
Low
Implemented Power Report
Tcl Console
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Name
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TNS
WHS
THS
TPWS
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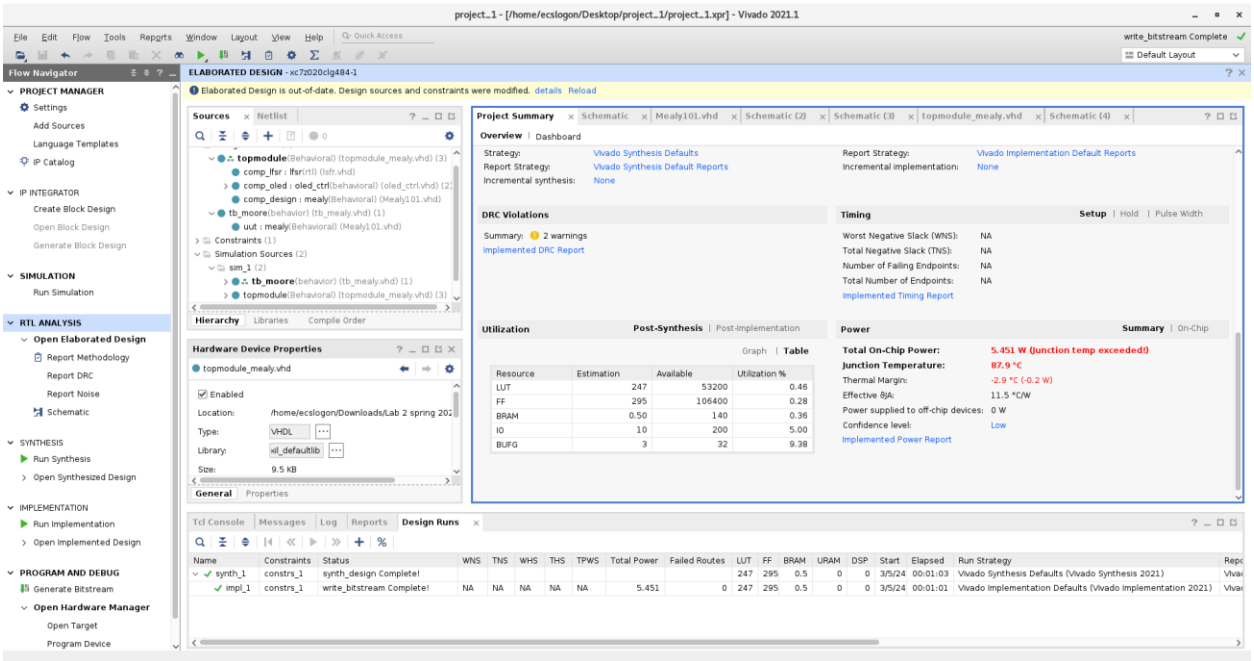
Failed Routes
LUT
FF
BRAM
URAM
DSP
Start
Elapsed
Run Strategy
synth_1 constrs_1 synth_design Complete! 3/5/24 00:01:03 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 write_bitstream Complete! 5.451 3/5/24 00:01:01 Vivado Implementation Defaults (Vivado Implementation 2021)


project_1 - [/home/ecslogon/Desktop/project_1/project_1.xpr] - Vivado 2021.1
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Report Methodology
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Schematic
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Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Open Target
Program Device
ELABORATED DESIGN - xc7z020clg484-1
Elaborated Design is out-of-date. Design sources and constraints were modified. details Reload
Sources
Netlist
Hierarchy
Libraries
Compile Order
Hardware Device Properties
topmodule_mealy.vhd
Enabled
Location:
Type:
Library:
Size:
General
Properties
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Mealy101.vhd
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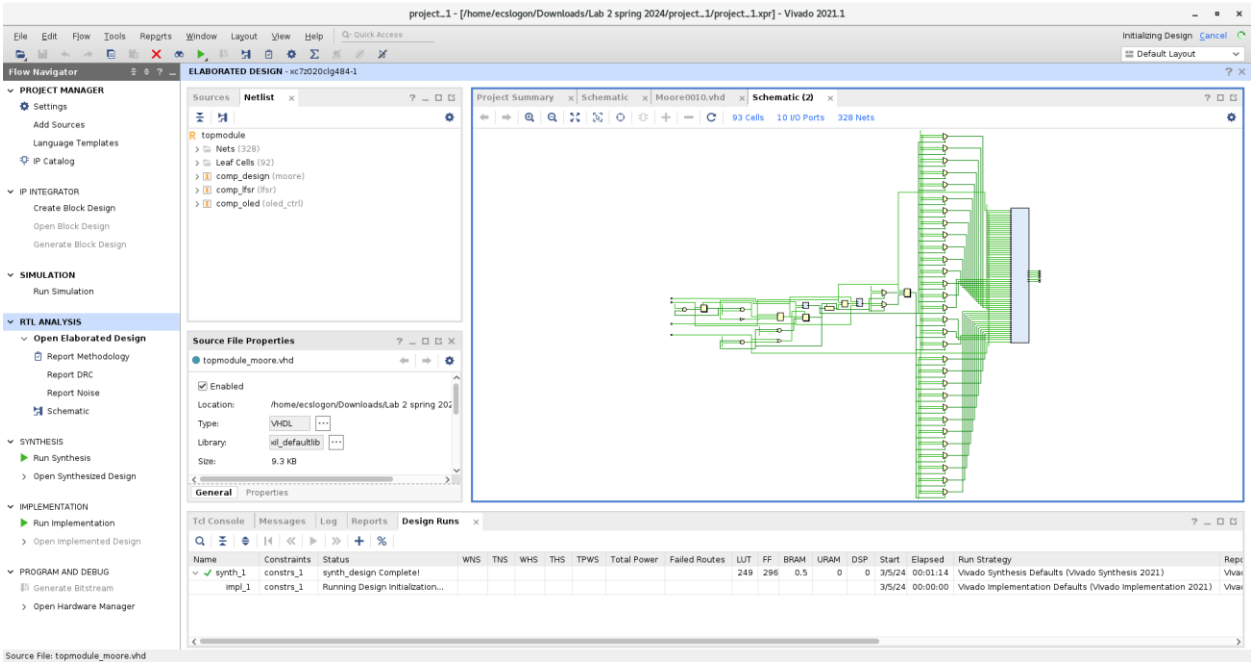
Strategy:
Vivado Synthesis Defaults
Report Strategy:
Vivado Synthesis Default Reports
Incremental synthesis:
None
Report Strategy:
Vivado Implementation Default Reports
Incremental implementation:
None
DRC Violations
Summary:
2 warnings
Implemented DRC Report
Timing
Setup
Hold
Pulse Width
Worst Negative Slack (WNS):
Total Negative Slack (TNS):
Number of Failing Endpoints:
Total Number of Endpoints:
Implemented Timing Report
Utilization
Post-Synthesis
Post-Implementation
Graph
Table
Resource
Estimation
Available
Utilization %
LUT 247 53200 0.46
FF 295 106400 0.28
BRAM 0.50 140 0.36
IO 10 200 5.00
BUFG 3 32 9.38
Power
Summary
On-Chip
Total On-Chip Power:
5.451 W (junction temp exceeded!)
Junction Temperature:
87.9 °C
Thermal Margin:
-2.9 °C (-0.2 W)
Effective θJA:
11.5 °C/W
Power supplied to off-chip devices:
0 W
Confidence level:
Low
Implemented Power Report
Tcl Console
Messages
Log
Reports
Design Runs
Name
Constraints
Status
WNS
TNS
WHS
THS
TPWS
Total Power
Failed Routes
LUT
FF
BRAM
URAM
DSP
Start
Elapsed
Run Strategy
synth_1 constrs_1 synth_design Complete! 3/5/24 00:01:03 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 write_bitstream Complete! 5.451 3/5/24 00:01:01 Vivado Implementation Defaults (Vivado Implementation 2021)

Case 3:


project_1 - [/home/ecslogon/Downloads/Lab 2 spring 2024/project_1/project_1.xpr] - Vivado 2021.1
File Edit Flow Tools Reports Window Layout View Help
Initializing Design Cancel
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7z020clg484-1
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Open Block Design
Generate Block Design
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Open Elaborated Design
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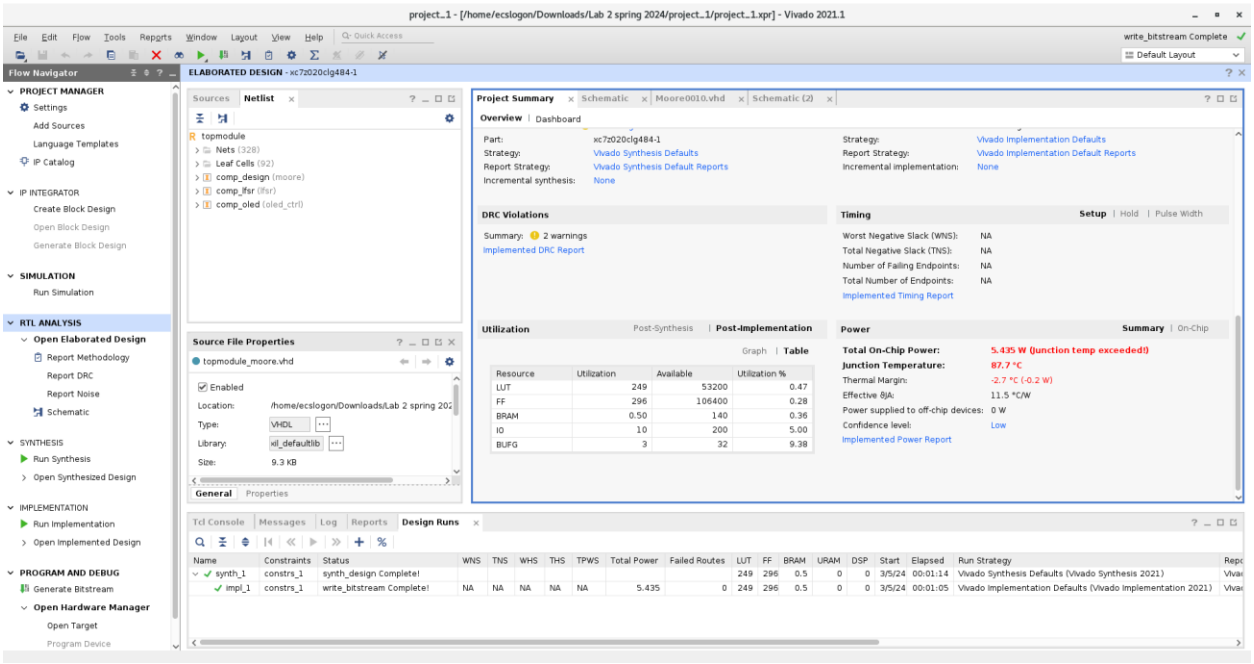
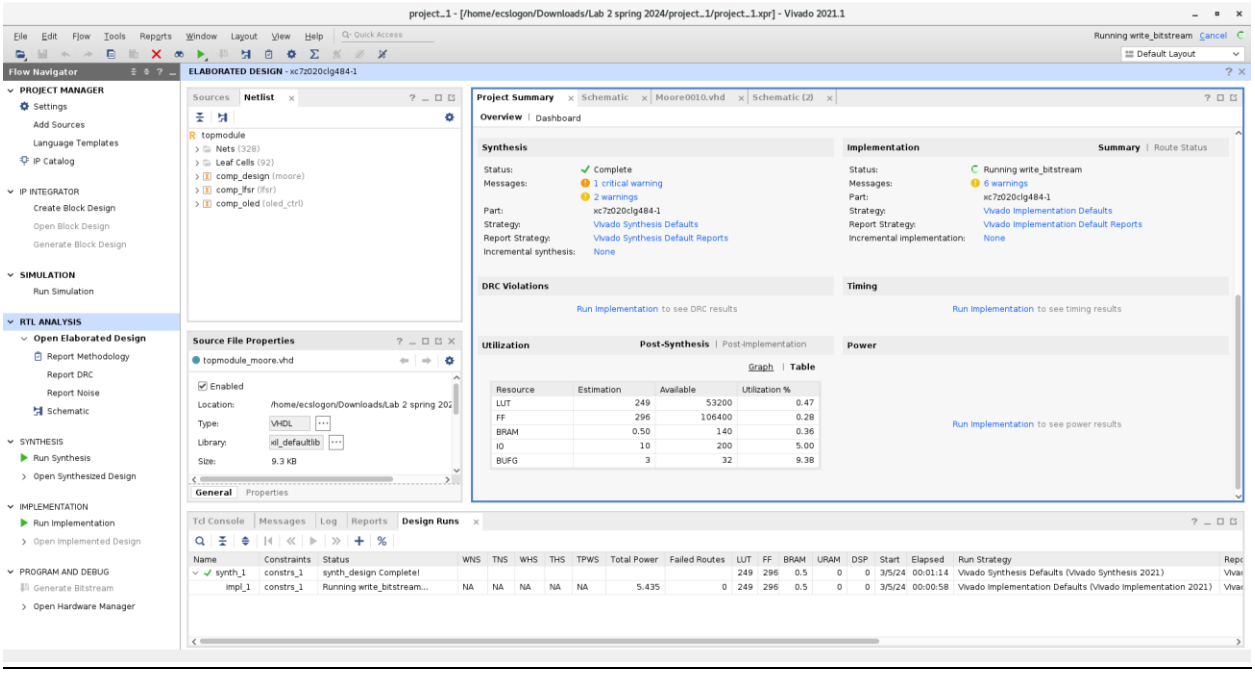
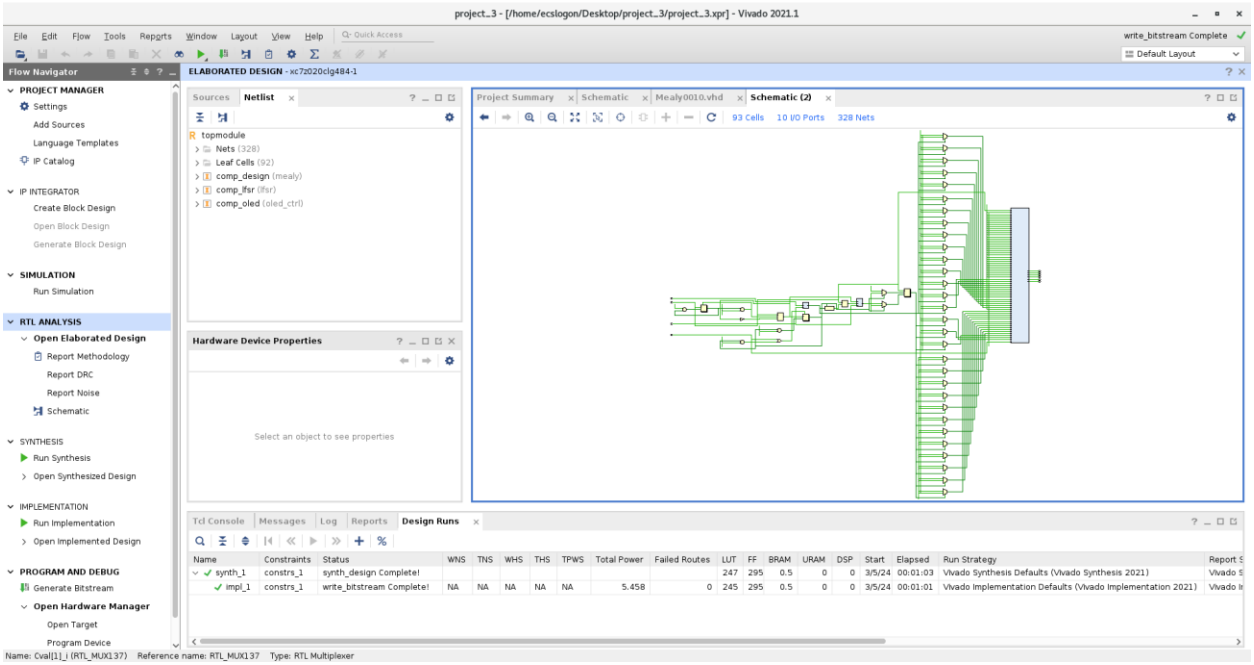
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Netlist
topmodule
Nets (328)
Leaf Cells (92)
comp_design (moore)
comp_lfsr (lfsr)
comp_oled (oled_ctrl)
Source File Properties
topmodule_moore.vhd
Enabled
Location: /home/ecslogon/Downloads/Lab 2 spring 202
Type: VHDL
Library: xil_defaultlib
Size: 9.3 KB
General
Properties
Project Summary
Schematic
Moore0010.vhd
Schematic (2)
93 Cells
10 I/O Ports
328 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 synth_design Complete! 249 296 0.5 0 0 3/5/24 00:01:14 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 Running Design Initialization... 3/5/24 00:00:00 Vivado Implementation Defaults (Vivado Implementation 2021)
Source File: topmodule_moore.vhd


project_1 - [/home/ecslogon/Downloads/Lab 2 spring 2024/project_1/project_1.xpr] - Vivado 2021.1
write_bitstream Complete
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7z020clg484-1
Project Summary
Overview
Dashboard
Part: xc7z020clg484-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 2 warnings
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 249 53200 0.47
FF 296 106400 0.28
BRAM 0.50 140 0.36
IO 10 200 5.00
BUFG 3 32 9.38
Power
Summary | On-Chip
Total On-Chip Power: 5.435 W (Junction temp exceeded!)
Junction Temperature: 87.7 °C
Thermal Margin: -2.7 °C (-0.2 W)
Effective θJA: 11.5 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 synth_design Complete! 249 296 0.5 0 0 3/5/24 00:01:14 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 write_bitstream Complete! NA NA NA NA NA 5.435 0 249 296 0.5 0 0 3/5/24 00:01:05 Vivado Implementation Defaults (Vivado Implementation 2021)


project_1 - [/home/ecslogon/Downloads/Lab 2 spring 2024/project_1/project_1.xpr] - Vivado 2021.1
File Edit Flow Tools Reports Window Layout View Help
Running write_bitstream Cancel
Default Layout
Flow Navigator
ELABORATED DESIGN - xc7z020clg484-1
PROJECT MANAGER
Settings
Add Sources
Language Templates
IP Catalog
IP INTEGRATOR
Create Block Design
Open Block Design
Generate Block Design
SIMULATION
Run Simulation
RTL ANALYSIS
Open Elaborated Design
Report Methodology
Report DRC
Report Noise
Schematic
SYNTHESIS
Run Synthesis
Open Synthesized Design
IMPLEMENTATION
Run Implementation
Open Implemented Design
PROGRAM AND DEBUG
Generate Bitstream
Open Hardware Manager
Sources
Netlist
topmodule
Nets (328)
Leaf Cells (92)
comp_design (moore)
comp_lfsr (lfsr)
comp_oled (oled_ctrl)
Source File Properties
topmodule_moore.vhd
Enabled
Location: /home/ecslogon/Downloads/Lab 2 spring 202
Type: VHDL
Library: xil_defaultlib
Size: 9.3 KB
General
Properties
Project Summary
Schematic
Moore0010.vhd
Schematic (2)
Overview
Dashboard
Synthesis
Status: Complete
Messages: 1 critical warning
2 warnings
Part: xc7z020clg484-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Implementation
Summary
Route Status
Status: Running write_bitstream
Messages: 6 warnings
Part: xc7z020clg484-1
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Run Implementation to see DRC results
Timing
Run Implementation to see timing results
Utilization
Post-Synthesis
Post-Implementation
Graph
Table
Resource Estimation Available Utilization %
LUT 249 53200 0.47
FF 296 106400 0.28
BRAM 0.50 140 0.36
IO 10 200 5.00
BUFG 3 32 9.38
Power
Run Implementation to see power results
Tcl Console
Messages
Log
Reports
Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 synth_design Complete! 249 296 0.5 0 0 3/5/24 00:01:14 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 Running write_bitstream... NA NA NA NA NA 5.435 0 249 296 0.5 0 0 3/5/24 00:00:58 Vivado Implementation Defaults (Vivado Implementation 2021)

Case 4:


project_3 - [/home/ecslogon/Desktop/project_3/project_3.xpr] - Vivado 2021.1
File Edit Flow Tools Reports Window Layout View Help
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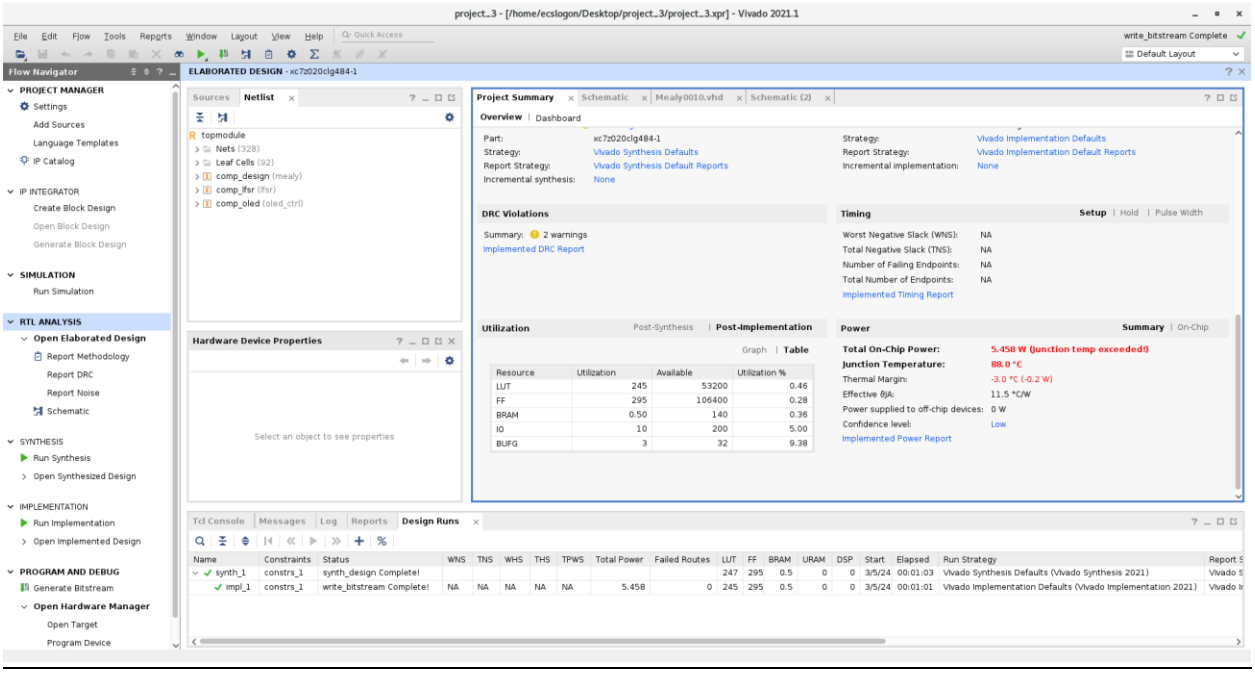
Open Target
Program Device
Sources
Netlist
topmodule
Nets (328)
Leaf Cells (92)
comp_design (mealy)
comp_lfsr (lfsr)
comp_oled (oled_ctrl)
Hardware Device Properties
Select an object to see properties
Project Summary
Schematic
Mealy0010.vhd
Schematic (2)
93 Cells
10 I/O Ports
328 Nets
Tcl Console
Messages
Log
Reports
Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 synth_design Complete! 247 295 0.5 0 0 3/5/24 00:01:03 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 write_bitstream Complete! NA NA NA NA NA 5.458 0 245 295 0.5 0 0 3/5/24 00:01:01 Vivado Implementation Defaults (Vivado Implementation 2021)
Name: Cval[1]_i (RTL_MUX137) Reference name: RTL_MUX137 Type: RTL Multiplexer


project_3 - [/home/ecslogon/Desktop/project_3/project_3.xpr] - Vivado 2021.1
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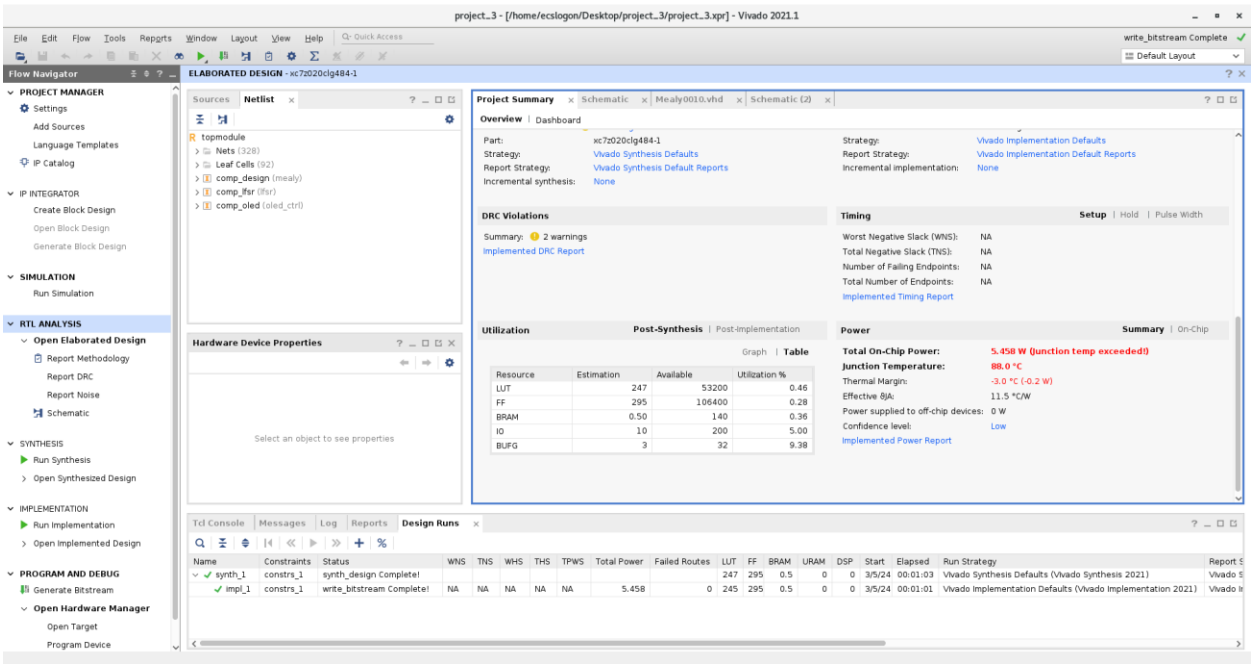
Schematic
Mealy0010.vhd
Schematic (2)
Overview
Dashboard
Part: xc7z020clg484-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 2 warnings
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Utilization Available Utilization %
LUT 245 53200 0.46
FF 295 106400 0.28
BRAM 0.50 140 0.36
IO 10 200 5.00
BUFG 3 32 9.38
Power
Summary | On-Chip
Total On-Chip Power: 5.458 W (Junction temp exceeded!)
Junction Temperature: 88.0 °C
Thermal Margin: -3.0 °C (-0.2 W)
Effective θJA: 11.5 °C/W
Power supplied to off-chip devices: 0 W
Confidence level: Low
Implemented Power Report
Tcl Console
Messages
Log
Reports
Design Runs
Name Constraints Status WNS TNS WHS THS TPWS Total Power Failed Routes LUT FF BRAM URAM DSP Start Elapsed Run Strategy
synth_1 constrs_1 synth_design Complete! 247 295 0.5 0 0 3/5/24 00:01:03 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 write_bitstream Complete! NA NA NA NA NA 5.458 0 245 295 0.5 0 0 3/5/24 00:01:01 Vivado Implementation Defaults (Vivado Implementation 2021)


project_3 - [/home/ecslogon/Desktop/project_3/project_3.xpr] - Vivado 2021.1
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write_bitstream Complete
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Schematic
Mealy0010.vhd
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Part: xc7z020clg484-1
Strategy: Vivado Synthesis Defaults
Report Strategy: Vivado Synthesis Default Reports
Incremental synthesis: None
Strategy: Vivado Implementation Defaults
Report Strategy: Vivado Implementation Default Reports
Incremental implementation: None
DRC Violations
Summary: 2 warnings
Implemented DRC Report
Timing
Setup | Hold | Pulse Width
Worst Negative Slack (WNS): NA
Total Negative Slack (TNS): NA
Number of Failing Endpoints: NA
Total Number of Endpoints: NA
Implemented Timing Report
Utilization
Post-Synthesis | Post-Implementation
Graph | Table
Resource Estimation Available Utilization %
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Summary | On-Chip
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Junction Temperature: 88.0 °C
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Tcl Console
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Design Runs
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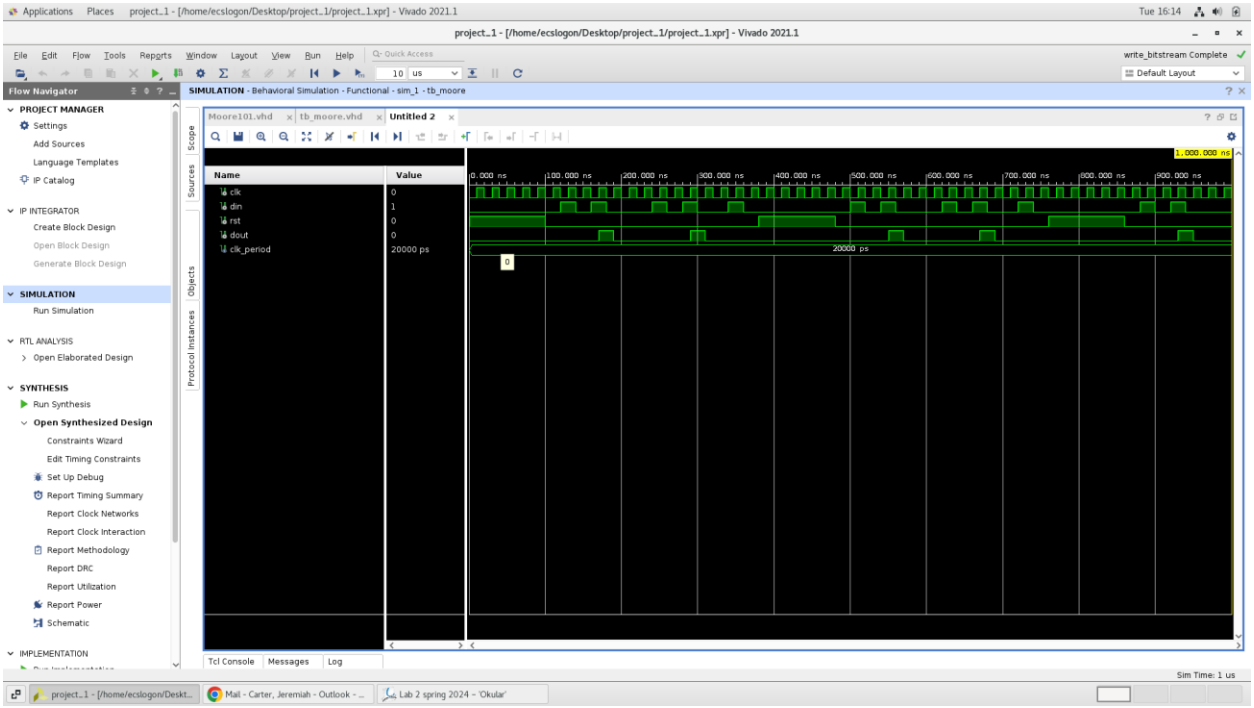
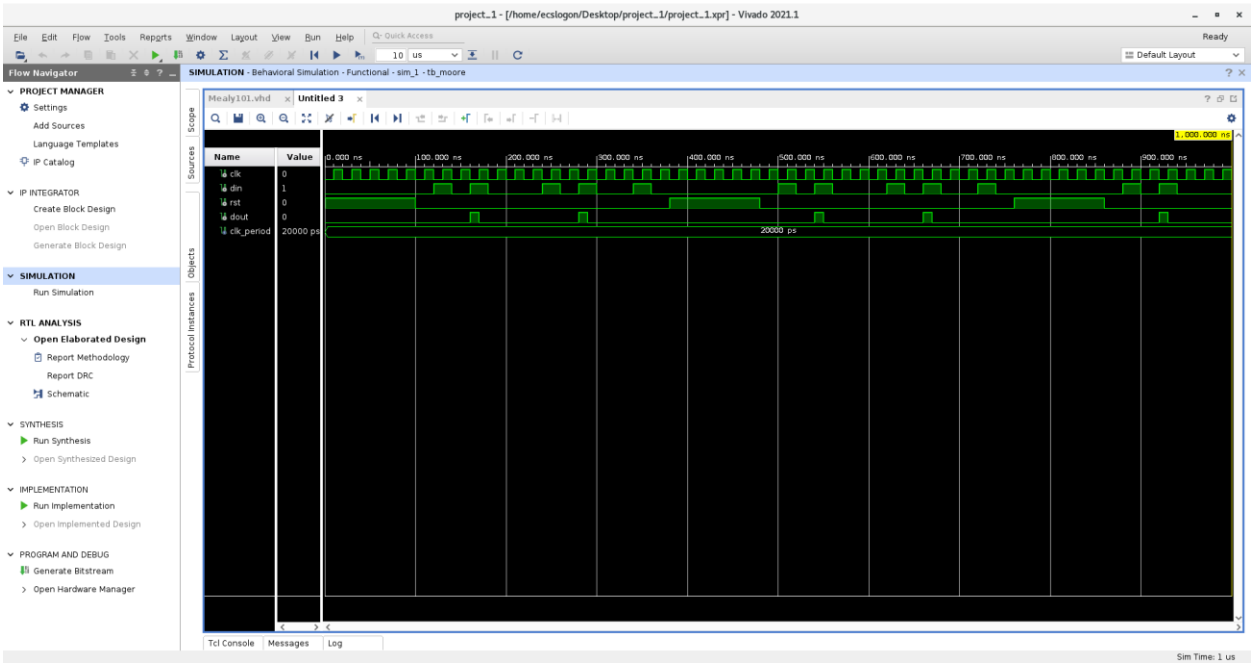
synth_1 constrs_1 synth_design Complete! 247 295 0.5 0 0 3/5/24 00:01:03 Vivado Synthesis Defaults (Vivado Synthesis 2021)
impl_1 constrs_1 write_bitstream Complete! NA NA NA NA NA 5.458 0 245 295 0.5 0 0 3/5/24 00:01:01 Vivado Implementation Defaults (Vivado Implementation 2021)

6. Simulation Waveform for all cases:

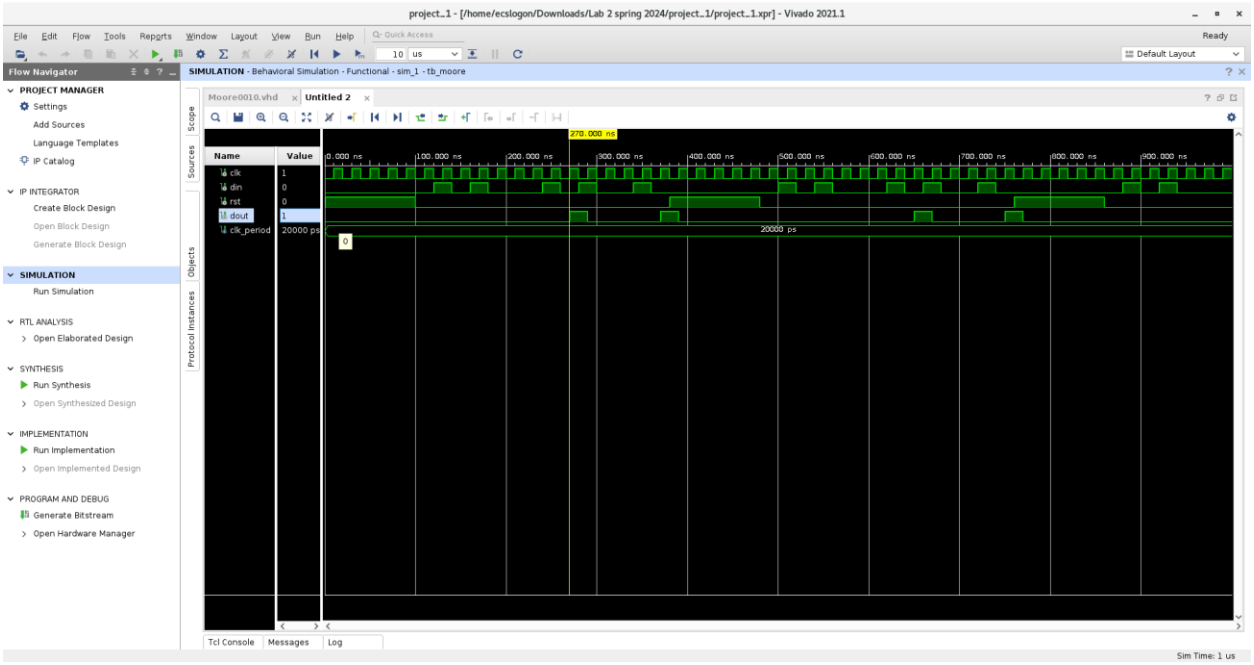
Case 1:



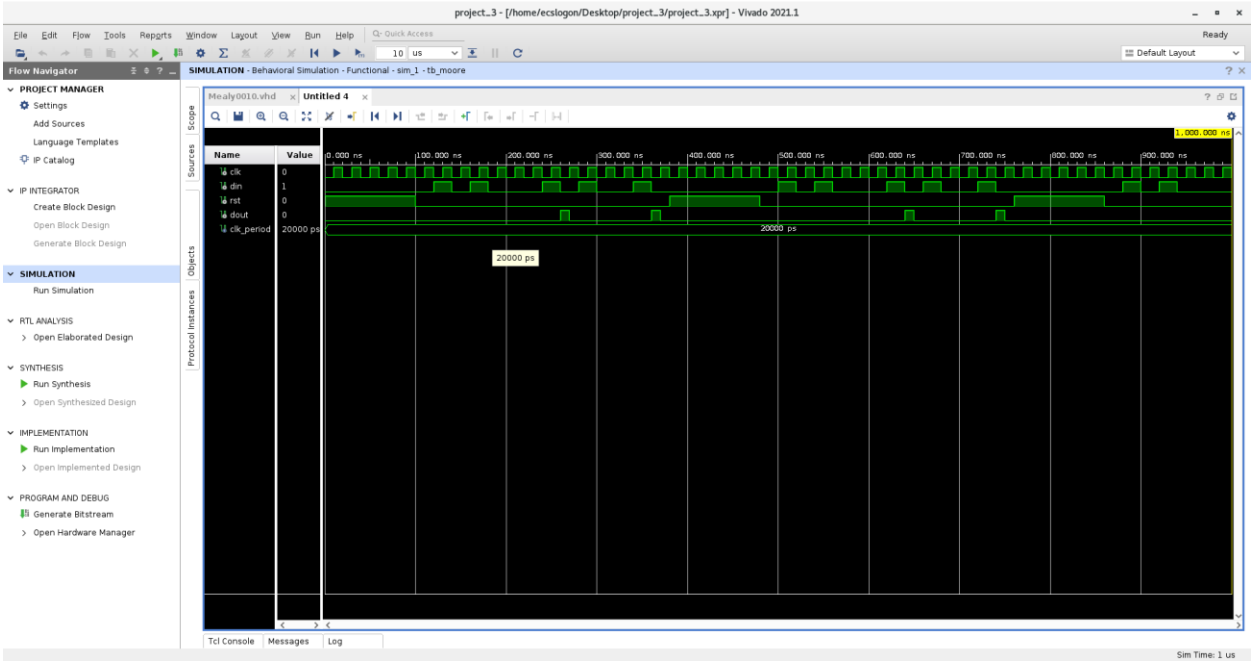
Case 2:



Case 3:


project_1 - [/home/ecslogon/Downloads/Lab 2 spring 2024/project_1/project_1.xpr] - Vivado 2021.1
Flow Navigator
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_moore
Moore0010.vhd
Untitled 2
Name
Value
clk
din
rst
dout
clk_period
20000 ps
270.000 ns
20000 ps
Tcl Console
Messages
Log
Sim Time: 1 us

Case 4:


project_3 - [/home/ecslogon/Desktop/project_3/project_3.xpr] - Vivado 2021.1
Flow Navigator
SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_moore
Mealy0010.vhd
Untitled 4
Name
Value
clk
din
rst
dout
clk_period
20000 ps
1,000.000 ns
20000 ps
20000 ps
Tcl Console
Messages
Log
Sim Time: 1 us