EE4620L/EE6620L/CEG4324L/CEG6324L

DIGITAL INTEGRATED CIRCUIT DESIGN LAB

Lab 3

By

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Submission date: 03/26/2024

"I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code"

Signature : [illegible]

Date : 03/26/2024

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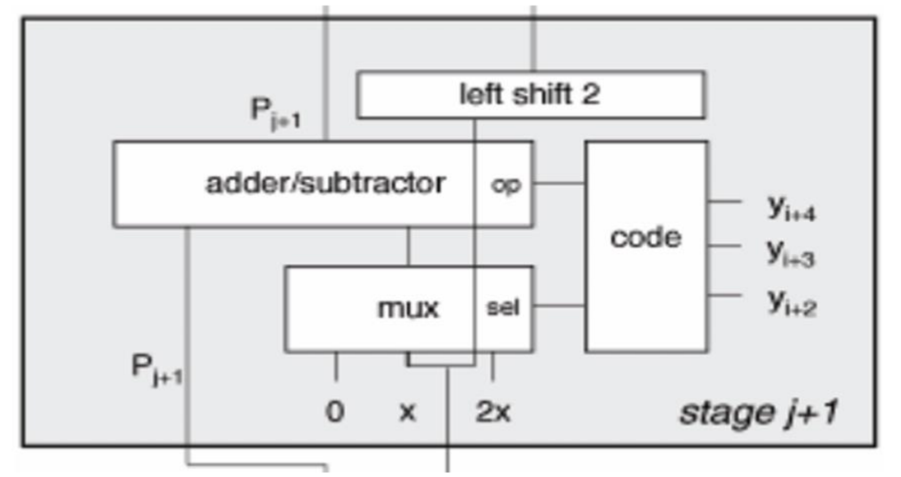
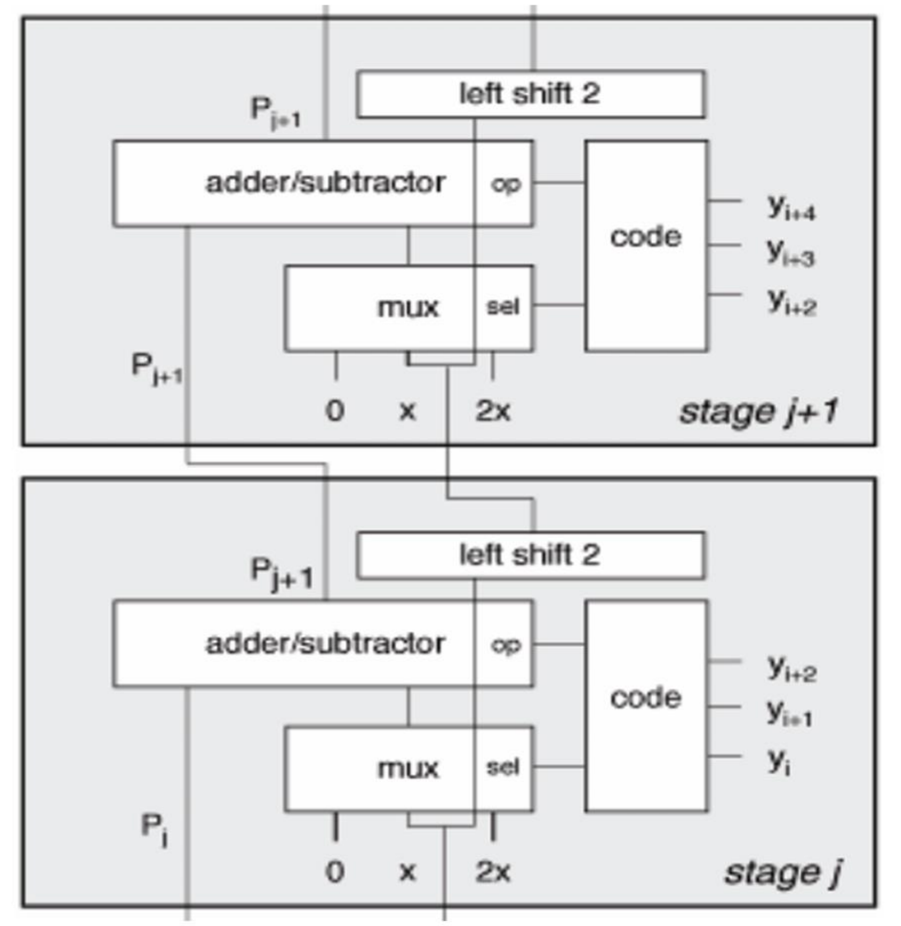
1. <u>AIM / OBJECTIVE:</u>

   The aim of this lab was to explore and design Booth multiplier circuit designs and to become familiar with the Vivado environment.

2. <u>Booth Algorithm:</u>





3. VHDL Code & tb 6x6 Booth :

Booth :

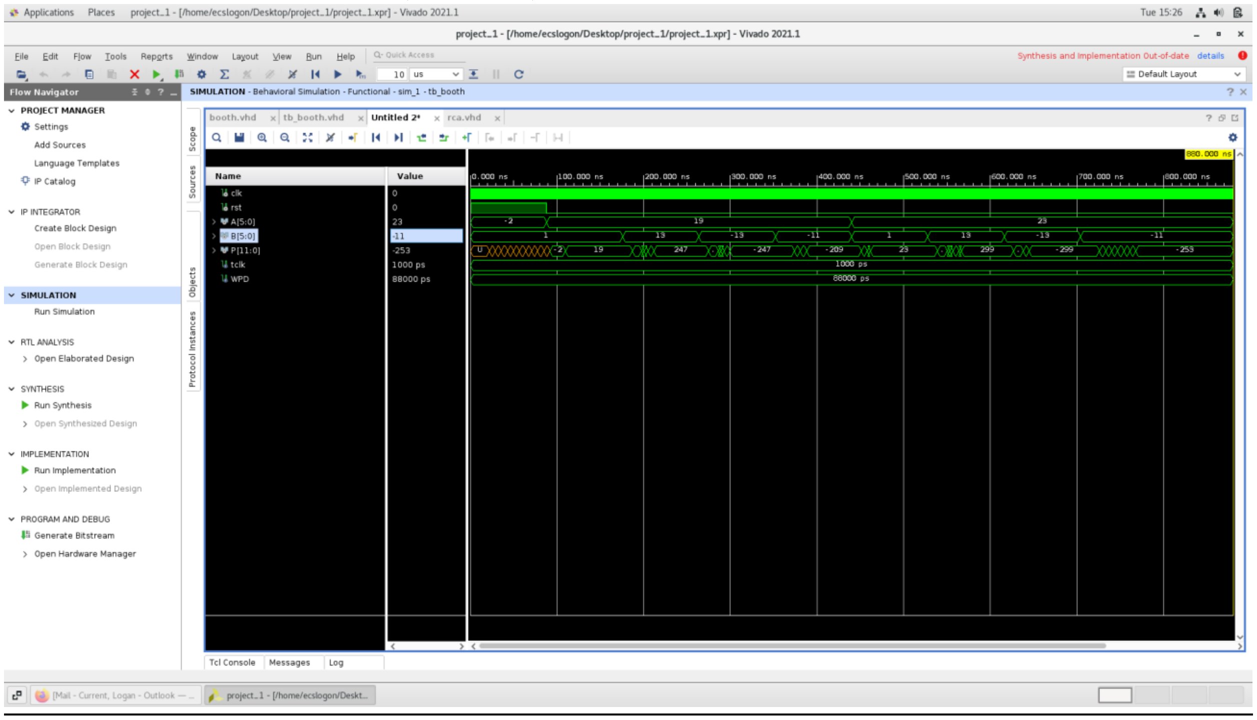
```vhdl
library ieee;
use ieee.std_logic_1164.all;
use ieee.numeric_std.all;
use ieee.std_logic_unsigned.all;

entity booth is
    port (operand_a : in std_logic_vector (5 downto 0);
          operand_b : in std_logic_vector (5 downto 0);
          rst       : in std_logic;
          clk       : in std_logic;
          z         : out std_logic_vector (11 downto 0));
end booth;



architecture rtl of booth is
    component RCA is
        generic(N:integer:=11);
        port(   A,B: in std_logic_vector(N-1 downto 0);
        Ci: in std_logic;
        Co: out std_logic;
                S: out std_logic_vector(N-1 downto 0));
end component;
--Declare  Signals

signal x, y, nx : std_logic_vector (5 downto 0);
signal y1, y2, y3 : std_logic_vector (2 downto 0);
signal x_p1, x_p2, x_p3, p1, p2, p3 : std_logic_vector (10 downto 0);
signal Co1, Co2 : std_logic;
begin
    process(operand_a, operand_b)
    begin
        if(operand_a(5) = '1') then
            x <= operand_b;
            y <= operand_a;
        elsif (operand_b(5) = '1') then
            x <= operand_a;
            y <= operand_b;
        else
            x <= operand_a;
            y <= operand_b;
        end if;
    end process;

    y1 <= y(1 downto 0) & '0';
    y2 <= y(3 downto 1);
    y3 <= y(5 downto 3);

    nx <= not(x) + 1;


--Declare  Components
process(y1, y2, y3)
    begin
        case (y1) is
            when "000" => x_p1 <= "00000000000";
            when "001" => x_p1 <= "00000" & x;
            when "010" => x_p1 <= "00000" & x;
            when "011" => x_p1 <= "0000" & x & '0';
            when "100" => x_p1 <= "1111" & nx & '0';
            when "101" => x_p1 <= "11111" & nx;
            when "110" => x_p1 <= "11111" & nx;
            when "111" => x_p1 <= "00000000000";
            when others => x_p1 <= "00000000000";
        end case;

        case (y2) is
            when "000" => x_p2 <= "00000000000";
            when "001" => x_p2 <= "000" & x & "00";
            when "010" => x_p2 <= "000" & x & "00";
            when "011" => x_p2 <= "00" & x & "000";
            when "100" => x_p2 <= "11" & nx & "000";
            when "101" => x_p2 <= "111" & nx & "00";
            when "110" => x_p2 <= "111" & nx & "00";
            when "111" => x_p2 <= "00000000000";
            when others => x_p2 <= "00000000000";
        end case;

        case (y3) is
            when "000" => x_p3 <= "00000000000";
            when "001" => x_p3 <= "0" & x & "0000";
            when "010" => x_p3 <= "0" & x & "0000";
            when "011" => x_p3 <=  x & "00000";
            when "100" => x_p3 <= nx & "00000";
            when "101" => x_p3 <= "1" & nx & "0000";
            when "110" => x_p3 <= "1" & nx & "0000";
            when "111" => x_p3 <= "00000000000";
            when others => x_p3 <= "00000000000";
        end case;
    end process;

    p1 <= x_p1;

add1: rca generic map(N=>11) port map (A=> p1, B => x_p2, Ci => '0',
Co => Co1, s => p2);
add2: rca generic map(N=>11) port map (A=> p2, B => x_p3, Ci => '0',
Co => Co2, s => p3);

z <= p3(10) & p3;

end;
```

TB :

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;
use std.env.stop;

entity tb_booth is
    generic(tclk:time := 1 ns;  -- clock speed
            WPD: time := 88 ns   -- rate at which the input changes
            );

end tb_booth;

architecture Behavioral of tb_booth is

signal clk : std_logic;
signal rst : std_logic;

signal A : std_logic_vector (5 downto 0);
signal B : std_logic_vector (5 downto 0);
signal P : std_logic_vector (11 downto 0);

component booth is
  port (operand_a : in std_logic_vector (5 downto 0);
        operand_b : in std_logic_vector (5 downto 0);
        rst       : in std_logic;
        clk       : in std_logic;
        z         : out std_logic_vector (11 downto 0));
end component;



begin

clock:process
          begin
            clk <= '1'; wait for tclk / 2;
            clk <= '0'; wait for tclk / 2;
          end process;

DUT: booth port map(clk=>clk,rst=>rst,operand_a=>A,operand_b=>B,z=>P);

test_vectors:process
                begin
                    A<="111110"; --(-2)
                    B<="000001"; --(1)
                    rst<='1';
                    wait for WPD;
                    rst<='0';

                    A<="010011"; --(19)
                    B<="000001"; --(1)
                    wait for WPD;

                    A<="010011"; --(19)
                    B<="001101"; --(13)
                    wait for WPD;

                    A<="010011"; --(19)
                    B<="110011"; --(-13)
                    wait for WPD;

                    A<="010011"; --(19)
                    B<="110101"; --(-11)
                    wait for WPD;

                    A<="010111"; --(23)
                    B<="000001"; --(1)
                    wait for WPD;

                    A<="010111"; --(23)
                    B<="001101"; --(13)
                    wait for WPD;

                    A<="010111"; --(23)
                    B<="110011"; --(-13)
                    wait for WPD;
```

```vhdl
                    A<="010111"; --(23)
                    B<="110101"; --(-11)
                    wait for WPD;

                    wait for WPD;
                    stop;
                end process;


end Behavioral;
```

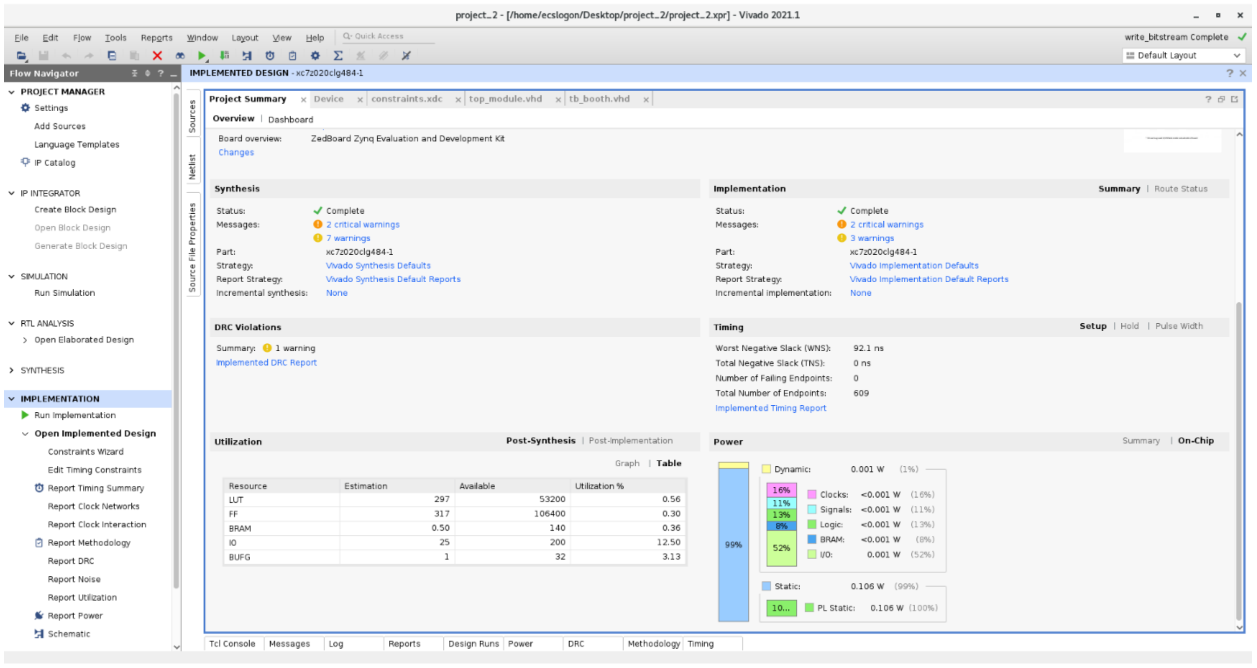
4. Simulation Waveform (8 cases) :


project_1 - [/home/ecslogon/Desktop/project_1/project_1.xpr] - Vivado 2021.1

SIMULATION - Behavioral Simulation - Functional - sim_1 - tb_booth

Name	Value
clk	0
rst	0
A[5:0]	23
B[5:0]	-11
P[11:0]	-253
tclk	1000 ps
WPD	88000 ps

5. Area, Power, Timing & Post-synthesis Timing and Power:



project_2 - [/home/ecslogon/Desktop/project_2/project_2.xpr] - Vivado 2021.1

IMPLEMENTED DESIGN - xc7z020clg484-1

Board overview: ZedBoard Zynq Evaluation and Development Kit
Changes

Synthesis

Status:	✓ Complete
Messages:	2 critical warnings
	7 warnings
Part:	xc7z020clg484-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	None

Implementation — Summary | Route Status

Status:	✓ Complete
Messages:	2 critical warnings
	3 warnings
Part:	xc7z020clg484-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: 1 warning
Implemented DRC Report

Timing — Setup | Hold | Pulse Width

Worst Negative Slack (WNS):	92.1 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	609

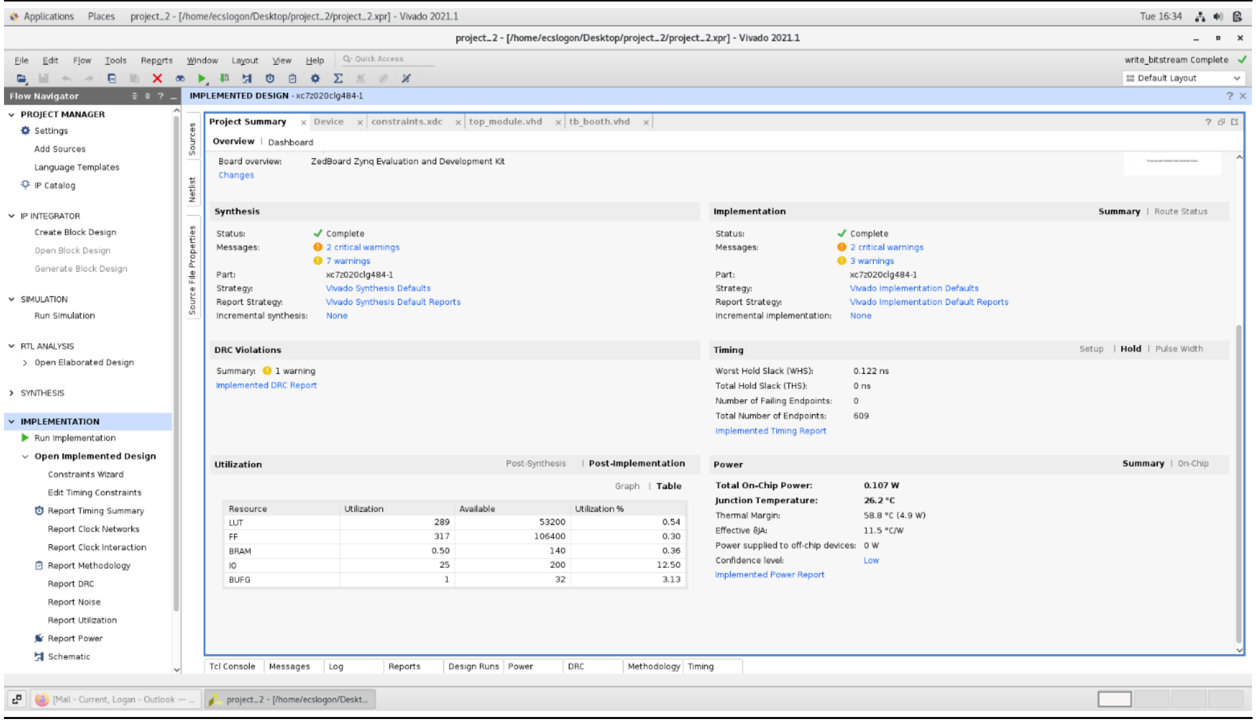
Implemented Timing Report

Utilization — Post-Synthesis | Post-Implementation — Graph | Table

Resource	Estimation	Available	Utilization %
LUT	297	53200	0.56
FF	317	106400	0.30
BRAM	0.50	140	0.36
IO	25	200	12.50
BUFG	1	32	3.13

Power — Summary | On-Chip

Dynamic:	0.001 W	(1%)
Clocks:	<0.001 W	(16%)
Signals:	<0.001 W	(11%)
Logic:	<0.001 W	(13%)
BRAM:	<0.001 W	(8%)
I/O:	0.001 W	(52%)
Static:	0.106 W	(99%)
PL Static:	0.106 W	(100%)



project_2 - [/home/ecslogon/Desktop/project_2/project_2.xpr] - Vivado 2021.1

IMPLEMENTED DESIGN - xc7z020clg484-1

Board overview: ZedBoard Zynq Evaluation and Development Kit
Changes

Synthesis

Status:	✓ Complete
Messages:	2 critical warnings
	7 warnings
Part:	xc7z020clg484-1
Strategy:	Vivado Synthesis Defaults
Report Strategy:	Vivado Synthesis Default Reports
Incremental synthesis:	None

Implementation — Summary | Route Status

Status:	✓ Complete
Messages:	2 critical warnings
	3 warnings
Part:	xc7z020clg484-1
Strategy:	Vivado Implementation Defaults
Report Strategy:	Vivado Implementation Default Reports
Incremental implementation:	None

DRC Violations

Summary: 1 warning
Implemented DRC Report

Timing — Setup | Hold | Pulse Width

Worst Hold Slack (WHS):	0.122 ns
Total Hold Slack (THS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	609

Implemented Timing Report

Utilization — Post-Synthesis | Post-Implementation — Graph | Table

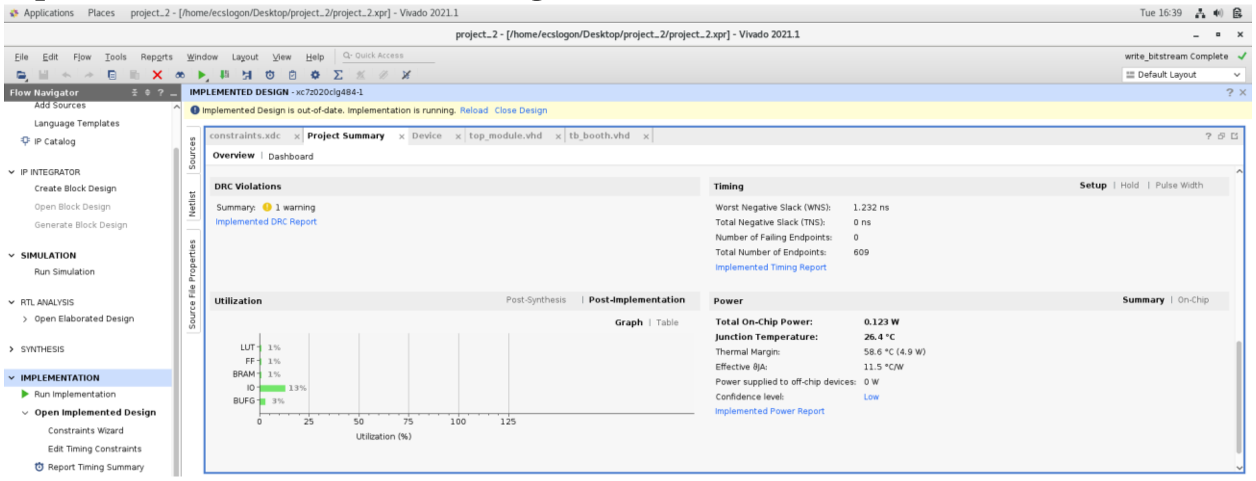
Resource	Utilization	Available	Utilization %
LUT	289	53200	0.54
FF	317	106400	0.30
BRAM	0.50	140	0.36
IO	25	200	12.50
BUFG	1	32	3.13

Power — Summary | On-Chip

Total On-Chip Power:	**0.107 W**
Junction Temperature:	**26.2 °C**
Thermal Margin:	58.8 °C (4.9 W)
Effective θJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

Updated Constraints.xdc timing:



IMPLEMENTED DESIGN - xc7z020clg484-1

Implemented Design is out-of-date. Implementation is running. Reload Close Design

DRC Violations

Summary: 1 warning

Implemented DRC Report

Timing

Worst Negative Slack (WNS):	1.232 ns
Total Negative Slack (TNS):	0 ns
Number of Failing Endpoints:	0
Total Number of Endpoints:	609

Implemented Timing Report

Utilization

Power

Total On-Chip Power:	**0.123 W**
Junction Temperature:	**26.4 °C**
Thermal Margin:	58.6 °C (4.9 W)
Effective θJA:	11.5 °C/W
Power supplied to off-chip devices:	0 W
Confidence level:	Low

Implemented Power Report

6. Conclusion:

This Lab I learned how to do booth multiplication, it’s a pretty simple concept luckily.