WRIGHT STATE UNIVERSITY

EE 4550L IC Hardware Security and Trust

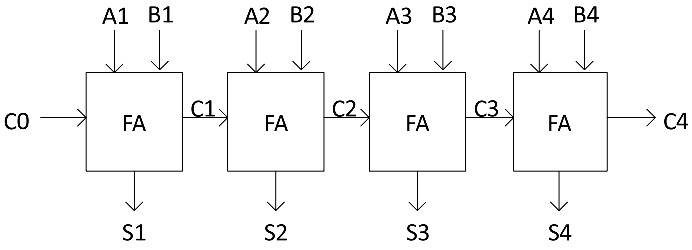
Lab 1 – Test 4-bit adder/subtractor in Xilinx Vivado

(Note: Write your TA's name and your login on the report)

Objective

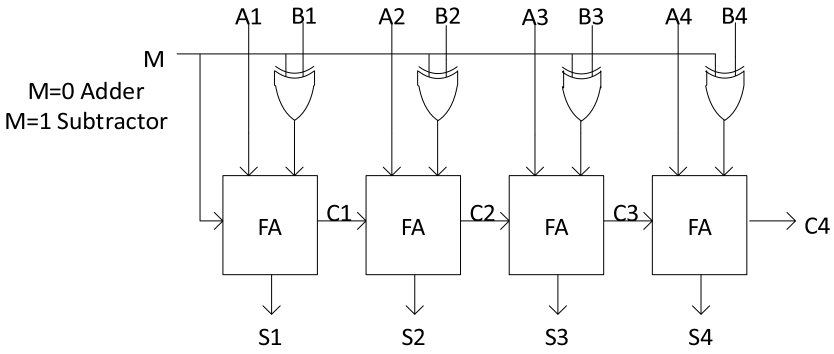
The objective of this lab is to practice writing VHDL code and testbench. Xilinx Vivado is used to simulate VHDL code and testbench.

A. 4-bit Binary Ripple Carry Adder



1. Create truth table for 1-bit full adder.
2. Create basic logic gates in VHDL code for 1-bit full adder.
3. Create 1-bit full adder in VHDL code.
4. Simulate testbench and 1-bit full adder in Vivado. Verify the simulation waveform with truth table.
5. Create 4-bit binary ripple carry adder in VHDL code.
6. Create a testbench for 4-bit binary ripple carry adder with the following testing cases.
   case 1: C0=0, A=0110, B=0011 case 2: C0=0, A=1010, B=0011
   case 3: C0=1, A=0100, B=0101 case 4: C0=1, A=0101, B=0110
7. Simulate testbench and circuit 4-bit binary adder in Vivado.

B. 4-bit Binary Adder/Subtractor



1. Create 4-bit binary adder/subtractor in VHDL code.
2. Create a testbench for 4-bit binary adder/subtractor with the following testing cases.
   case 1: M=0, A=0110, B=0011 case 2: M=0, A=1010, B=0011
   case 3: M=1, A=0100, B=0101 case 4: M=1, A=0101, B=0110
3. Simulate testbench and circuit 4-bit binary adder/subtractor in Vivado.

Lab Report (30 points)

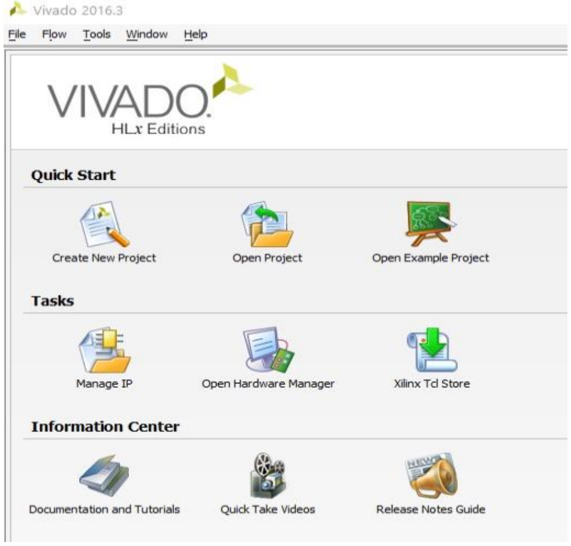
A LAB REPORT SHOULD BE SUBMITTED INDIVIDUALLY. This should include:

Truth table of 1-bit full adder.
All related VHDL code (including testbench).
Simulation waveform of 1-bit full adder, 4-bit adder, and 4-bit adder/subtractor. Label binary value of waveforms.
Question: How many input patterns are required for exhaustive testing on 4-bit adder and adder/subtractor? Why?

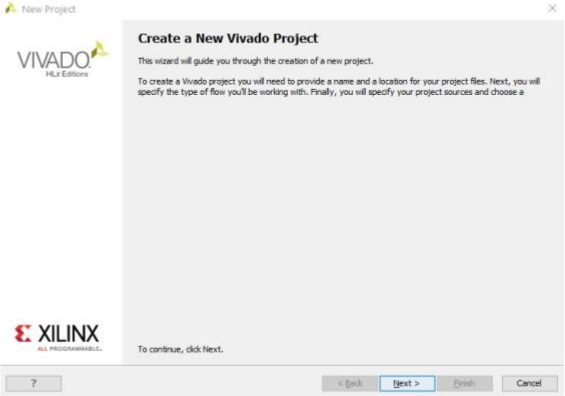
Appendix

Xilinx Vivado tutorial:

Start Xilinx Vivado by typing “`vivado &`” in terminal. Click “Create New Project”.



Click “Next”.



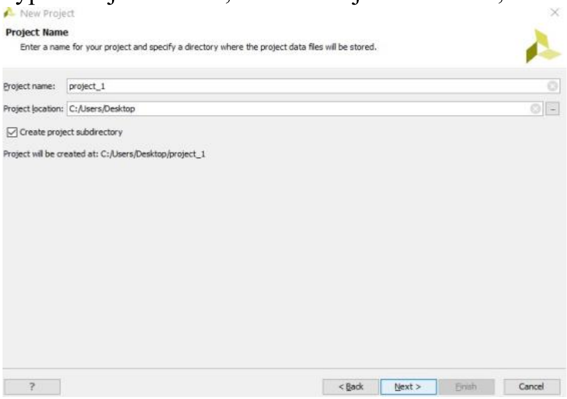
Create a New Vivado Project

This wizard will guide you through the creation of a new project.

To create a Vivado project you will need to provide a name and a location for your project files. Next, you will specify the type of flow you'll be working with. Finally, you will specify your project sources and choose a

To continue, click Next.

Type “Project name”, select “Project location”, hit “Next”.



Project Name

Enter a name for your project and specify a directory where the project data files will be stored.

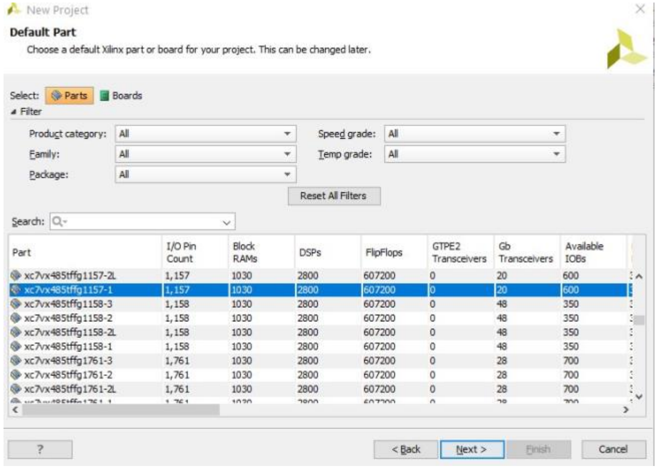
Project name: project_1

Project location: C:/Users/Desktop

☑ Create project subdirectory

Project will be created at: C:/Users/Desktop/project_1

Click “Next” until the following window, select “xc7vx485tffg1157-1”, click “Next”.



New Project

Default Part

Choose a default Xilinx part or board for your project. This can be changed later.

Product category: All

Family: All

Package: All

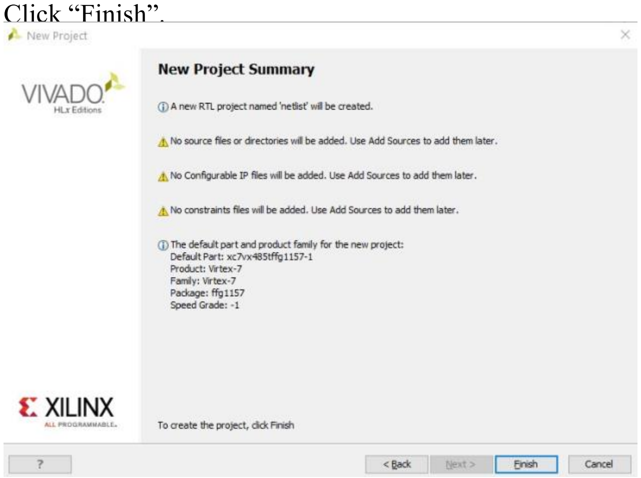
Speed grade: All

Temp grade: All

Search:

Part	I/O Pin Count	Block RAMs	DSPs	FlipFlops	GTPE2 Transceivers	Gb Transceivers	Available IOBs
xc7vx485tffg1157-2L	1,157	1030	2800	607200	0	20	600
xc7vx485tffg1157-1	1,157	1030	2800	607200	0	20	600
xc7vx485tffg1158-3	1,158	1030	2800	607200	0	48	350
xc7vx485tffg1158-2	1,158	1030	2800	607200	0	48	350
xc7vx485tffg1158-2L	1,158	1030	2800	607200	0	48	350
xc7vx485tffg1158-1	1,158	1030	2800	607200	0	48	350
xc7vx485tffg1761-3	1,761	1030	2800	607200	0	28	700
xc7vx485tffg1761-2	1,761	1030	2800	607200	0	28	700
xc7vx485tffg1761-2L	1,761	1030	2800	607200	0	28	700

Click “Finish”.



New Project

New Project Summary

ⓘ A new RTL project named 'netlist' will be created.

⚠ No source files or directories will be added. Use Add Sources to add them later.

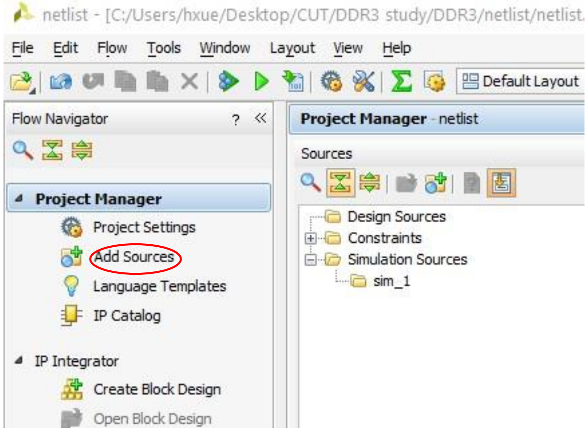
⚠ No Configurable IP files will be added. Use Add Sources to add them later.

⚠ No constraints files will be added. Use Add Sources to add them later.

ⓘ The default part and product family for the new project:
Default Part: xc7vx485tffg1157-1
Product: Virtex-7
Family: Virtex-7
Package: ffg1157
Speed Grade: -1

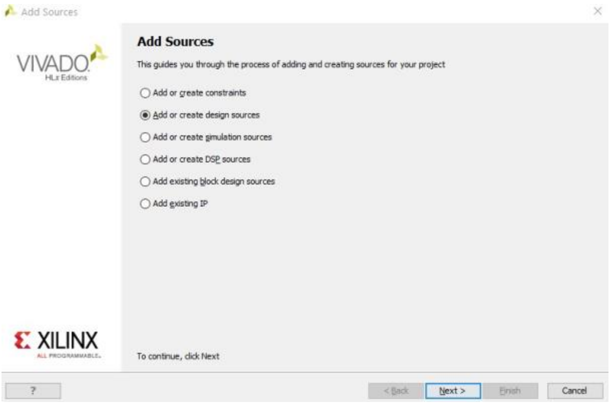
To create the project, click Finish

Click “Add Sources” in Project Manager.



netlist - [C:/Users/hxue/Desktop/CUT/DDR3 study/DDR3/netlist/netlist.

Select “Add or create design sources”, click “Next”, add or create RTL code and testbench.



Add Sources

This guides you through the process of adding and creating sources for your project

○ Add or create constraints
● Add or create design sources
○ Add or create simulation sources
○ Add or create DSP sources
○ Add existing block design sources
○ Add existing IP

To continue, click Next

Click “Run Simulation” in Simulation.

```
-- 2 inputs AND gate library
IEEE;
use IEEE.STD_LOGIC_1164.ALL;


entity AND2 is
    Port ( A : in  STD_LOGIC; -- AND gate input
B      : in  STD_LOGIC; -- AND gate input
C : out STD_LOGIC); -- AND gate output end
AND2;


architecture Behavioral of AND2 is begin
C      <= A and B; -- 2 input AND gate end
Behavioral;
```

```
-- Testbench for AND gate
library IEEE;
use
IEEE.STD_LOGIC_1164.ALL;
entity AND2TestBench is end
AND2TestBench;


architecture Behavioral of AND2TestBench is
component AND2 is   Port (A,B:in std_logic;
            C: out std_logic );
end component; --inputs
signal a: std_logic:= '0';
signal b: std_logic:= '0';
--outputs
signal c : std_logic;
constant period : time := 1ns;


begin
uut: AND2 PORT MAP(a=>A,b=>B,c=>C);
a<=not a after period; b<=not b
after period*2;


end Behavioral;
```