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**EE 4540L/6540L/CEG4322L/CEG6322L**

**FALL 2024**

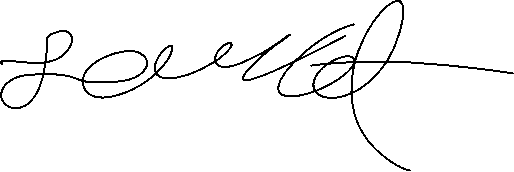
**TA: Kanchan Vissamsetty**

**Lab section: 01**

**Name: Logan Current**

**“I have neither given nor received aid on this assignment, nor have I observed any violation of the Honor code”**

**Signature: Date: 10/18/2024**



**Report due date: 10/18/2024**

1. **OBJECTIVE**

The Objective of this lab is to learn how to design the NAND3, NAND2, and NOR3 in Cadence Virtuoso. We can also design and simulate an XOR2 as an optional bonus.

1. **PROCEDURE**

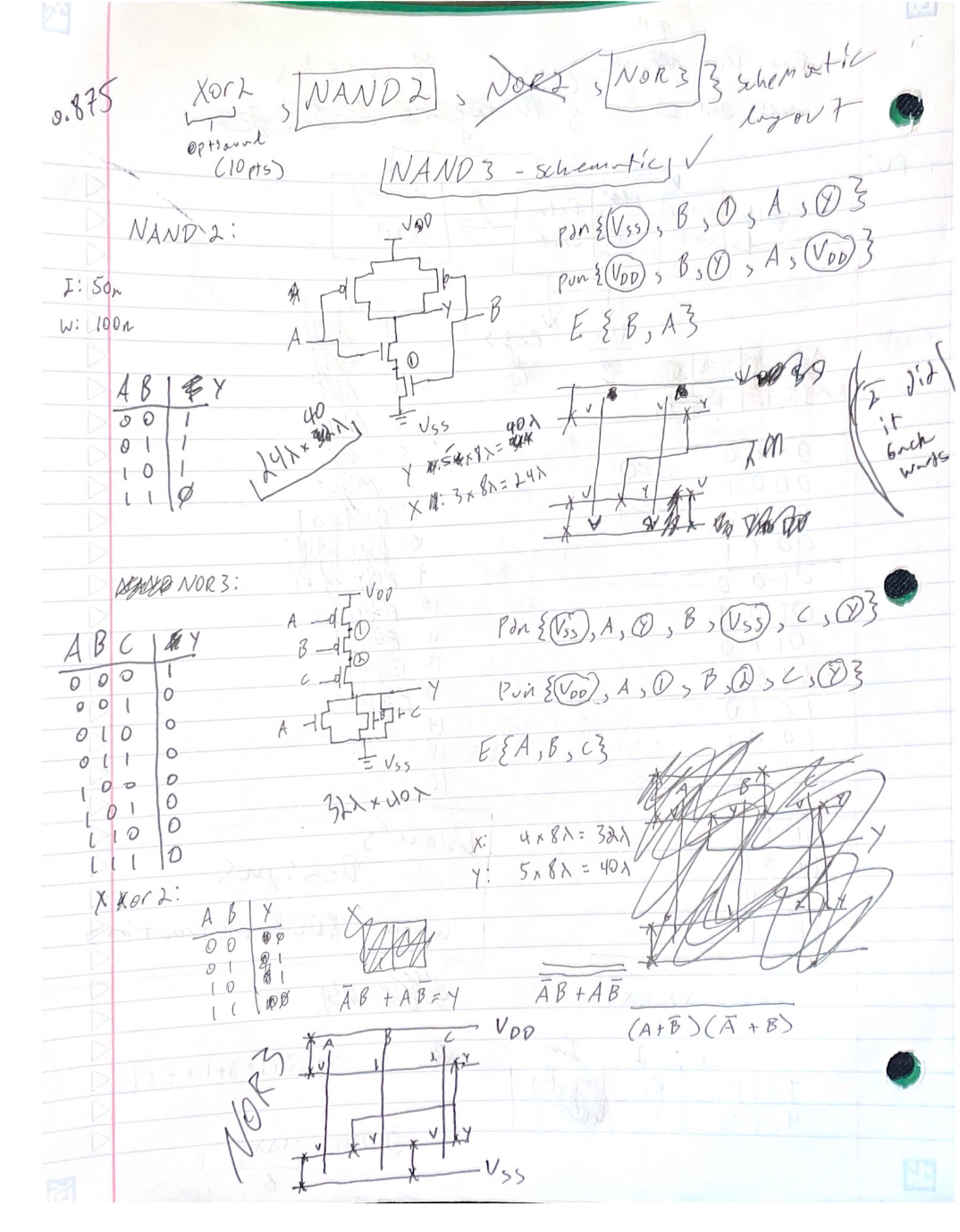
First, I started by finishing the NAND3 gate since I already made the layout and schematic for a previous lab and so I ran a check to make sure that there were no errors with either one. So, I started to make the test bench for this gate but ran into many problems when running my test benches for all of my gates that I will disclose details to in the conclusion portion of the report.

Next, I designed the NAND2 gate by drawing the schematic and stick diagram first then implementing it in cadence. After I had made the schematic in cadence, I found the average power consumption and propagation delay of the gate. Then I made the layout for the gate and ran a DRC check for it to make sure there were no errors before starting my testbench.

I continued the same process for the NOR3 gate as I did with the NAND2 gate. Finally, I designed the XOR2 schematic and stick diagram. I implemented it into cadence and made sure there were no errors before finding the average power for it and propagation delay. Finally, I had started working on implementing the layout but ran into issues and ran out of time to work on it.

1. **RESULT**

The order for the screenshots will be my written work first, then the gates. For each gate, the first screenshot will be schematic, then waveform, and then layout with DRC check.

A paper with drawings on it

Description automatically generated

NAND3:

A computer screen shot of a computer program

Description automatically generated

A computer screen shot of a computer screen

Description automatically generatedA computer screen shot of a computer program

Description automatically generated

NAND2***A computer screen shot of a computer program

Description automatically generatedA computer screen shot of a graph

Description automatically generatedA computer screen shot of a computer program

Description automatically generated***

NOR3: ***A computer screen shot of a computer program

Description automatically generated***

***A computer screen shot of a black screen

Description automatically generated***

***A computer screen shot of a computer program

Description automatically generated***

XOR2: ***A computer screen shot of a computer program

Description automatically generated***

***A screenshot of a computer

Description automatically generated***

1. **CONCLUSION**

Overall, I was able to complete most of the lab. The main issues I had run into were running the test benches the graphing my points in MATLAB and comparing the propagation delay. I couldn’t run a LVS check but instead a PEX check which was fine, but my MATLAB was running on my computer or letting me run it. After many attempts and trying different commands, I couldn’t get it to run for me, I was able to get hspice running and make the files needed for if I got into MATLAB, but I had run out of time to continue trying. Other than those issues this lab was a fun lab to design and implement! I wish I had gotten the XOR2 layout working but I can continue to work on that in my free time.