9, 10, 15

9: 1001 $n_3 = 1$ AND1 =

10: 1010 $n_2 = 0$

$n_1 = 0$ AND2 =

15: 1111 $n_0 = 1$ AND3 =

AND4 =

Lab 2

45 nm tech

feature size $2\lambda = 50\,nm$ (L)

$0.025\,\mu m = 25\,nm = 1\lambda$

$2 \cdot \lambda = 50\,nm$

PDN - NMOS

$8\lambda = 200\,nm$

1.) transistor level schematic } Hand written

2.) Stick diagram

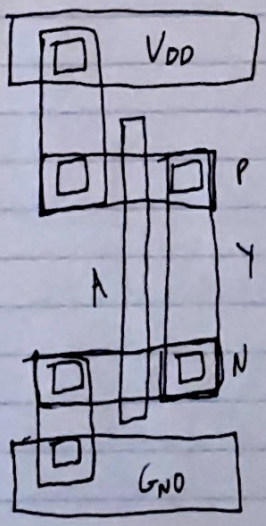
3.) Layout } Cadence

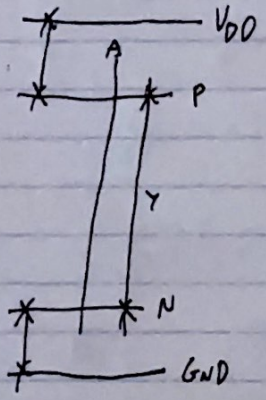
4.) NO DRC Errors }

(-0.1625, -0.2)

0.1625, -0.3

INV



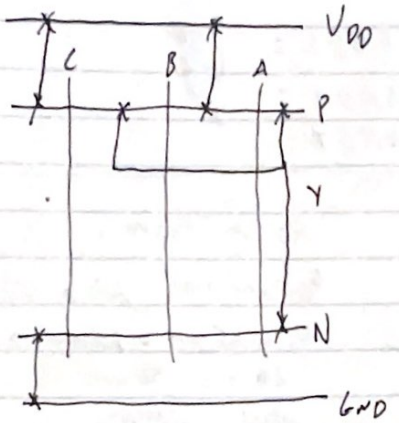


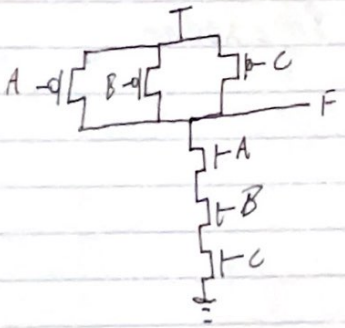
0.0625

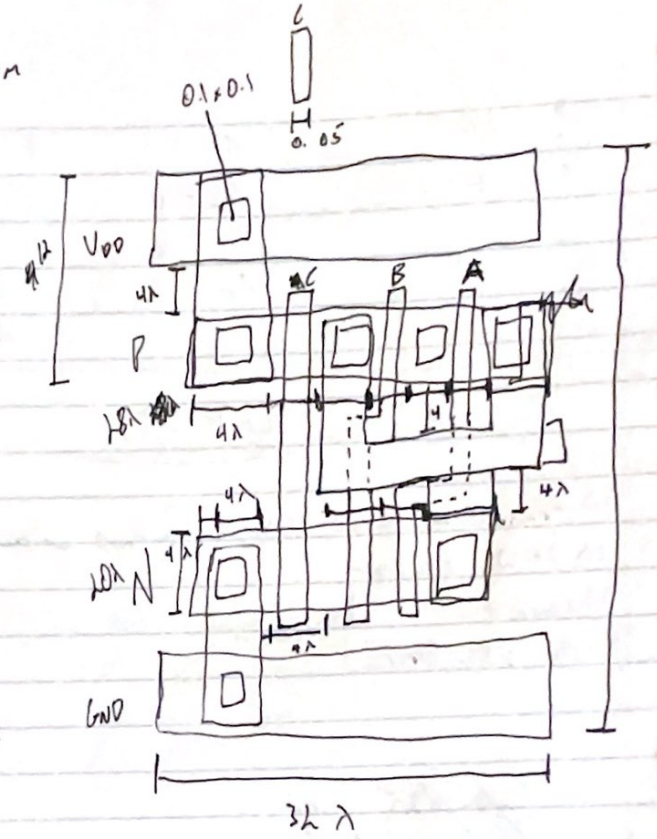
$\lambda = 25nm$

$0.025\,\mu m$

NAND 3







$5\frac{1}{2} \times 2 = 11$

$2 \times 3 = 6$

$7 \times 2 = 14$

31λ